RICHTEK®

RTQ9128DL-QA

45W, Ultra-Low Noise, High-Efficiency, Digital Input 4-Channel Automotive Audio Amplifier with I²C Diagnostics

1 General Description

The RTQ9128DL-QA is an ultra-low output noise, high-efficiency, four-channel class-D audio power amplifier. It delivers 4x27W into 4Ω at 10% THD+N from a 14.4V supply in automotive applications. It can achieve over 87% power efficiency with an output switching frequency of up to 2.1MHz for clarity, which enables a cost-optimized solution in a very small PCB size. Additionally, the RTQ9128DL-QA can be set either above the AM band, which eliminates the AM-band interference and reduces output filter size and cost, or below the AM band to optimize efficiency.

The RTQ9128DL-QA is fully configurable through the I²C bus interface and features comprehensive diagnostics array specially designed for automotive applications.

The built-in anti-pop functions can reduce the speaker's pop noise under all kinds of scenarios. Its built-in protection circuits provide thermal fold-back, over-temperature, overcurrent, overvoltage, and undervoltage protections and report error status.

The RTQ9128DL-QA is a 3-wire device that receives all clocks from external sources with standard I²S and TDM (Time-Division Multiplexing) formats. It supports a wide range of input sampling rates from 32kHz to 96kHz. The device is offered in a 64-pin RLQFP package with the exposed thermal pad facing up.

The recommended junction temperature range is −40°C to 150°C, and the ambient temperature range is −40°C to 125°C.

2 Features

- **AEC-Q100 Grade 1 Qualified**
- **I²S and TDM Input**
- **4x22W, THD + N = 1%, 4Ω, 14.4V**
- **4x27W, THD + N = 10%, 4Ω, 14.4V**
- **4x45W, THD + N = 10%, 2Ω, 14.4V**
- **THD + N is 0.03%**
- **SNR up to 115dB**
- **Ultra-Low Quiescent Current Mode**
- **Ultra-Low Noise = 18μV**
- **Low R_{DS_ON} (80mΩ)**
- **Switching Frequency up to 2.1MHz**
- **Sampling Frequency from 32kHz to 96kHz**
- **I²C Control with 16 Address Options**
- **Built-In Anti-Pop Function**
- **Built-In Thermal Fold-Back and Clip Detection**
- **Load Diagnostics**
  - **Output Open Load and Short Load**
  - **Output Short to Ground or Power**
  - **DC and AC Coupled Load Detection**
- **Protection Features**
  - **Output Short-Circuit**
  - **Overvoltage and Undervoltage**
  - **Output Current Limit and Protection**
  - **Over-Temperature**
  - **DC Offset Detection**
  - **40V Load Dump**
- **Ambient Temperature Range: –40°C to 125°C**
- **Junction Temperature Range: –40°C to 150°C**

3 Applications

- Automotive Head Units
- In-Vehicle Infotainment
- Automotive External Amplifier Modules

4 Ordering Information

RTQ9128DL □ - QA □

Packing

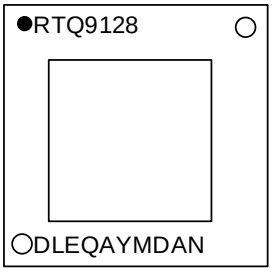
Grade
QA: AEC-Q100 Qualified
Screened by High Temperature

Package Type(1)
E: RLQFP-64L 10x10 (PP)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5 Marking Information

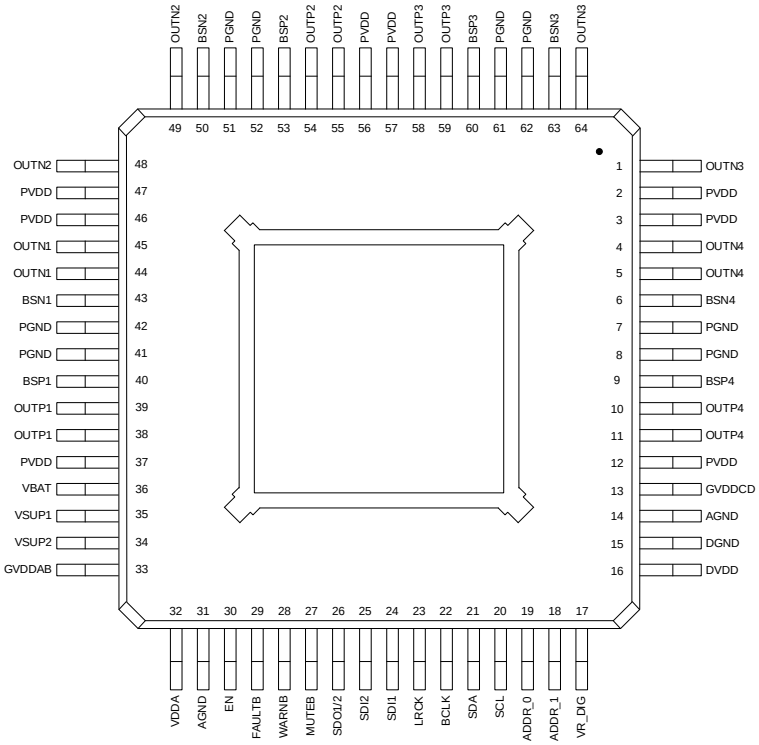


RTQ9128DLE: Product Code
QA: Automotive Product Grade
YMDAN: Date Code

Table of Contents

6 Pin Configuration

(TOP VIEW)



RLQFP-64L 10x10 (PP)

7 Functional Pin Description

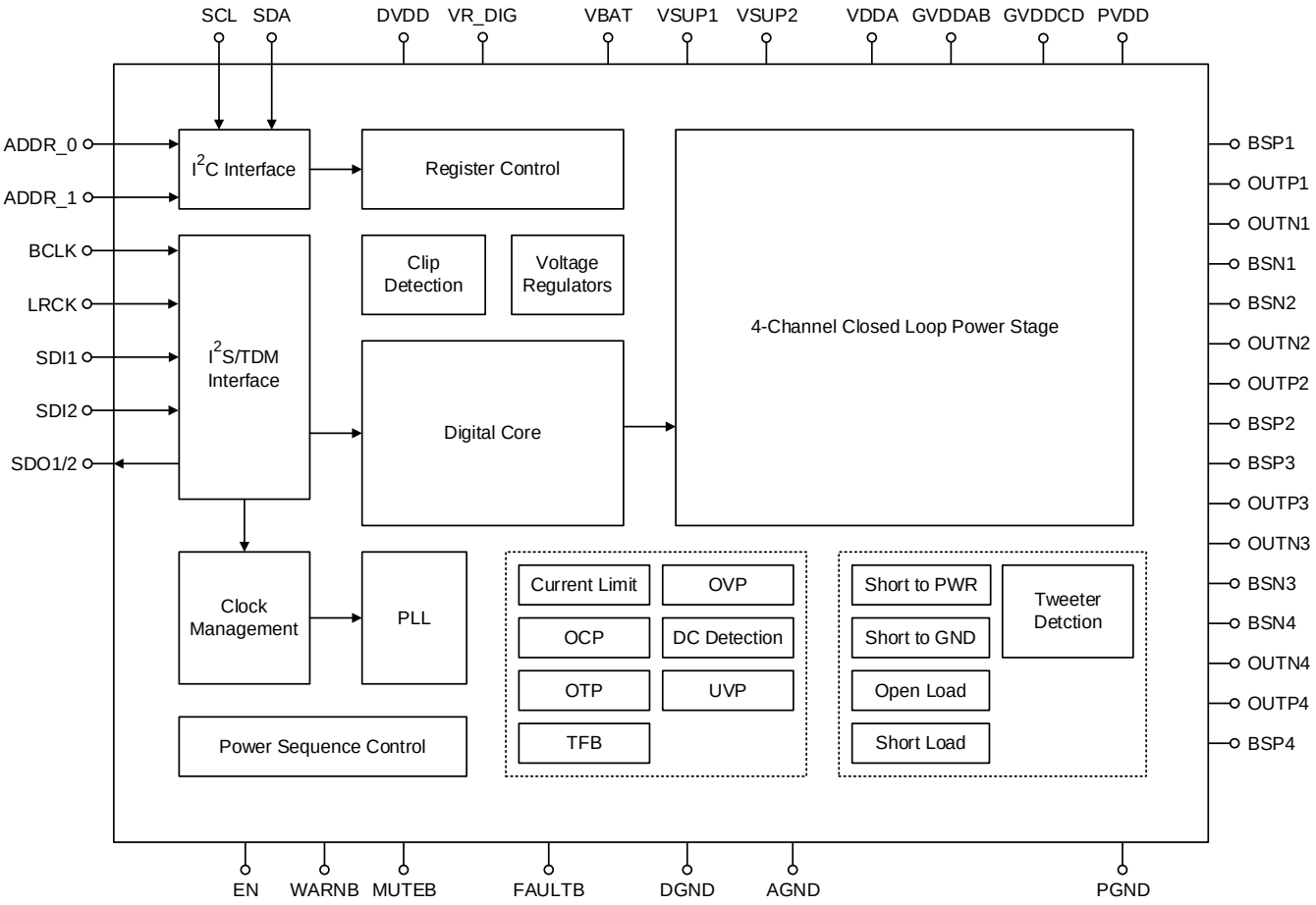
Pin No.	Pin Name	IO	Pin Function
1, 64	OUTN3	NO	Negative PWM output of CH3.
2, 3, 12, 37, 46, 47, 56, 57	PVDD	PWR	Supply voltage for power stage.
4, 5	OUTN4	NO	Negative PWM output of CH4.
6	BSN4	PWR	Bootstrap for CH4 negative output.
7, 8, 41, 42, 51, 52	PGND	GND	Ground for power stage.
9	BSP4	PWR	Bootstrap for CH4 positive output.
10, 11	OUTP4	PO	Positive PWM output of CH4.
13	GVDDCD	PWR	Gate drive voltage for CH3/CH4.
14, 31	AGND	GND	Ground for analog circuit.
15	DGND	GND	Ground for digital circuit.
16	DVDD	PWR	Power supply, 3.3V or 1.8V.
17	VR_DIG	PWR	Voltage regulator output is 1.8V; tie to DVDD when DVDD = 1.8V.
18	ADDR_1	DI	I^2C address pins_1.
19	ADDR_0	DI	I^2C address pins_0.
20	SCL	DI	I^2C reference clock.

Pin No.	Pin Name	IO	Pin Function
21	SDA	DI/DO	I^2C data.
22	BCLK	DI	I^2S bit clock.
23	LRCK	DI	I^2S frame clock.
24	SDI1	DI	I^2S data in for CH1/CH2.
25	SDI2	DI	I^2S data in for CH3/CH4.
26	SDO1/2	DO	I^2S data out.
27	MUTEB	DI	Mute control. Pull low for mute; pull high for unmute.
28	WARNB	DO	Warning flag. When a warning occurs, the level goes low; normal operation is indicated by a high level.
29	FAULTB	DO	Fault flag. When a fault occurs, the level goes low; normal operation is indicated by a high level.
30	EN	DI	Enable control. Pull low for shutdown; pull high to enable the chip.
32	VDDA	PWR	Voltage regulator output, 5V.
33	GVDDAB	PWR	Gate drive voltage for CH1/CH2.
34	VSUP2	PWR	Supply voltage2, tie to VBAT.
35	VSUP1	PWR	Supply voltage1, tie to VBAT.
36	VBAT	PWR	Battery voltage input.
38, 39	OUTP1	PO	Positive PWM output of CH1.
40	BSP1	PWR	Bootstrap for CH1 positive output.
43	BSN1	PWR	Bootstrap for CH1 negative output.
44, 45	OUTN1	NO	Negative PWM output of CH1.
48, 49	OUTN2	NO	Negative PWM output of CH2.
50	BSN2	PWR	Bootstrap for CH2 negative output.
53	BSP2	PWR	Bootstrap for CH2 positive output.
54, 55	OUTP2	PO	Positive PWM output of CH2.
58, 59	OUTP3	PO	Positive PWM output of CH3.
60	BSP3	PWR	Bootstrap for CH3 positive output.
61, 62	PGND	GND	Ground.
63	BSN3	PWR	Bootstrap for CH3 negative output.

7.1 IO Type Definition

- GND: Ground
- PWR: Power
- PO: Positive Output
- NO: Negative Output
- DI: Digital Input
- DO: Digital Output
- DI/DO: Digital Input and Output
- AO: Analog Output

8 Functional Block Diagram



9 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, PVDD, VBAT, VSUP1, VSUP2 ---------- –0.3V to 32V
- Vpeak, Transient Supply Voltage, PVDD, VBAT, VSUP1, VSUP2
  (t ≤ 400ms Exposure) ---------- –1V to 40V
- Supply Voltage, DVDD ---------- –0.3V to 6V
- Speaker Amplifier Output Voltage, OUTXX ---------- –10V to 32V
- Vpeak, Speaker Amplifier Output Voltage, OUTXX (Note 3) ---------- –10V to 37V
- BSXX to PGND DC ---------- –0.3V to 36V
- SCL, SDA, FAULTB, EN, WARNB, MUTEB, ADDR_0, ADDR_1 ---------- –0.3V to 6V
- LRCK, BCLK, SDI1, SDI2, SDO1/2 ---------- –0.3V to DVDD + 0.5V
- GND to DGND, PGND, AGND ---------- –0.3V to 0.3V
- VDDA, GVDDAB, GVDDCD ---------- –0.3V to 6V
- VR_DIG ---------- –0.3V to 4V
- Power Dissipation, P_D @ T_A = 25°C
  RLQFP-64L 10x10 (PP) ---------- 2.18W
- Package Thermal Resistance (Note 4)
  RLQFP-64L 10x10 (PP), θ_{JA} ---------- 57.45°C/W
  RLQFP-64L 10x10 (PP), $\theta_{JC(Top)}$ ---------- 0.37°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)
  HBM (Human Body Model) ---------- ±2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. The switching terminal should be used within AC peak limits. Overshoot and undershoot must be less than 100ns.

Note 4. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. $\theta_{JC(Top)}$ is simulated at the case top of the package. Refer to the EVB user guide for thermal information, which includes the heat sink.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

10 Recommended Operating Conditions

(Note 6)

- Supply Input Voltage Range, DVDD ---------- 1.62V to 3.63V
- Supply Input Voltage Range, PVDD, VBAT, VSUP1, VSUP2 ---------- 4.5V to 18V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 150°C

Note 6. The device is not guaranteed to function outside its operating conditions.

11 Electrical Characteristics

(PVDD = VBAT = 14.4V, DVDD = 3.3V, RL = 4Ω, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
EN, ADDR_0, ADDR_1, MUTEB	VIH: High-Level Input Voltage	V_{IH}			DVDD x 0.7	--	--	V
	VIL: Low-Level Input Voltage	V_{IL}			--	--	DVDD x 0.3	
FAULTB, WARNB	VOL: Low-Level Output Voltage	V_{OL}	I_{PULLUP} = 3mA		--	--	0.4	V
DVDD Quiescent Current		I_{Q_DVDD}	EN = 3.3V, 0dB FS input		--	15	18	mA
DVDD Shutdown Current		I_{SD_DVDD}	EN = 0V, for DVDD, no load		--	--	0.2	mA
PVDD Quiescent Current (BD Mode)		$I_{Q\_PVDD\_BD}$	EN = 3.3V, switch 50% duty for PVDD = 14.4V no load		--	40	--	mA
PVDD Quiescent Current (CMH Mode)		$I_{Q\_PVDD\_CMH}$	EN = 3.3V, switch 25% duty for PVDD = 14.4V no load		--	20	--	mA
PVDD Quiescent Current (ULQM)		$I_{Q\_PVDD\_ULQM}$	ULQM, no load		--	0.3	1	mA
VBAT Quiescent Current (BD Mode)		$I_{Q\_VBAT\_BD}$	EN = 3.3V, switch 50% duty for VBAT = 14.4V no load		--	65	--	mA
VBAT Quiescent Current (CMH Mode)		$I_{Q\_VBAT\_CMH}$	EN = 3.3V, switch 25% duty for PVDD = 14.4V no load		--	75	--	mA
VBAT Quiescent Current (ULQM)		$I_{Q\_VBAT\_ULQM}$	ULQM, no load		--	2	5	mA
PVDD Shutdown Current		I_{SD_PVDD}	EN = 0V, no load for PVDD		--	5	10	uA
VBAT Shutdown Current		I_{SD_VBAT}	EN = 0V, no load for VBAT		--	13	20	uA
Drain-Source On-State Resistance		$R_{DS(ON)}$	PVDD = 14.4V, I_{OUT} = 500mA, T_J = 25°C	High-Side	--	80	--	mΩ
				Low-Side	--	80	--	
GVDDAB, GVDDCD		V_{GVDDAB}, V_{GVDDCD}	All channels playing, 0dB input		4.8	5.1	5.5	V
VDDA		V_{VDDA}	All channels playing, 0dB input		4.8	5.1	5.5	V
VR_DIG		V_{VR_DIG}	All channels playing, 0dB input		--	1.8	--	V
Speaker Gain Variation		ΔGain	Channel-to-channel gain variation		–0.5	--	0.5	dB
PWM Switching Frequency		f_{SW}	384kHz mode		--	384	--	kHz
			2112kHz mode		--	2112	--	

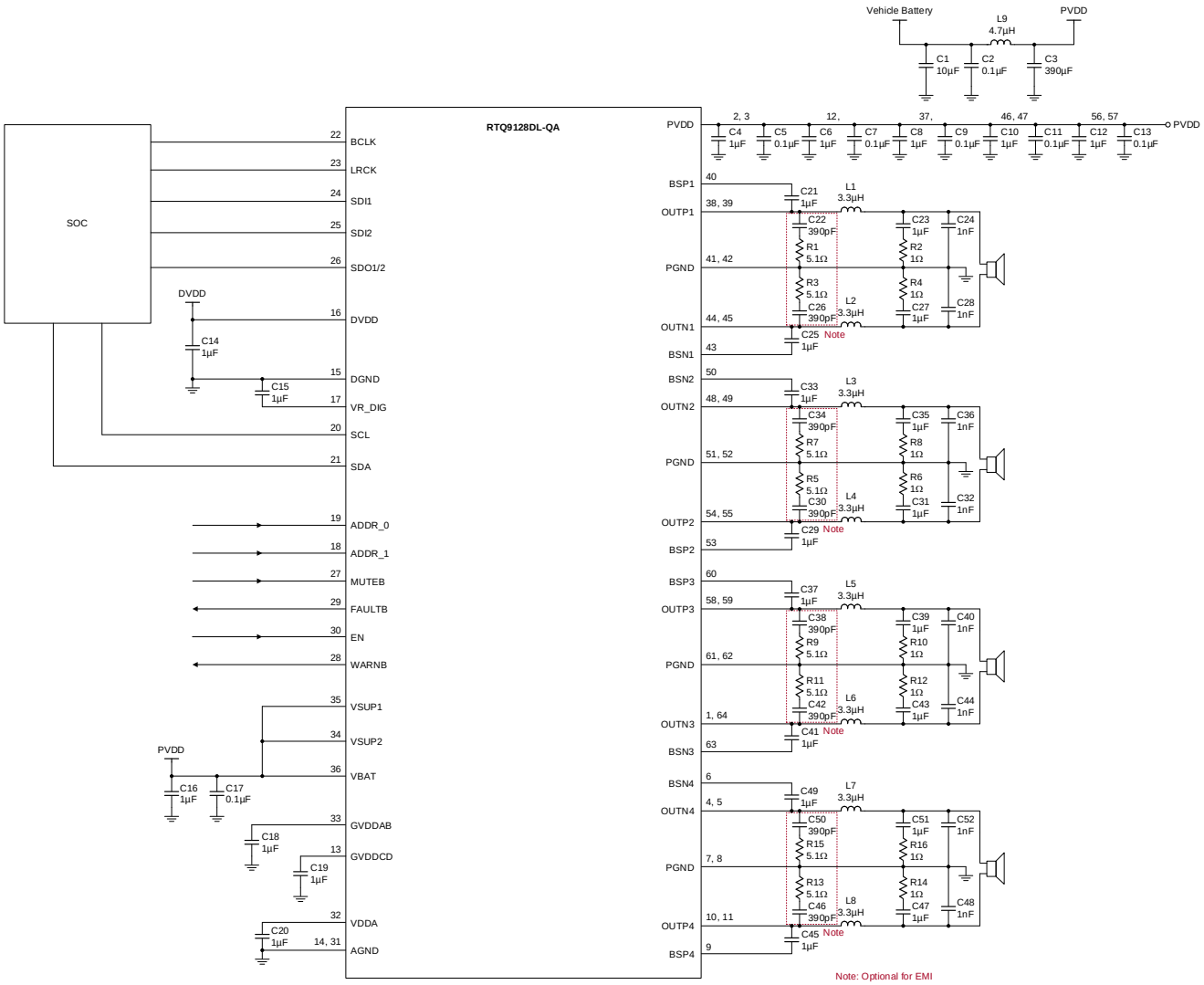
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RMS Output Power Per Channel, BTL	P_{O_BTL}	4Ω, PVDD = 14.4V, THD + N = 1%, T_A = 75°C	20	22	--	W
		4Ω, PVDD = 14.4V, THD + N = 10%, T_A = 75°C	25	27	--	
		2Ω, PVDD = 14.4V, THD + N = 1%, T_A = 75°C	38	40	--	
		2Ω, PVDD = 14.4V, THD + N = 10%, T_A = 75°C	43	45	--	
		4Ω, PVDD = 18V, THD + N = 1%, T_A = 75°C	34	36	--	
		4Ω, PVDD = 18V, THD + N = 10%, T_A = 75°C	45	48	--	
RMS Output Power Per Channel, PBTL	P_{O_PBTL}	2Ω, PVDD = 14.4V, THD + N = 1%, T_A = 75°C	35	40	--	W
		2Ω, PVDD = 14.4V, THD + N = 10%, T_A = 75°C	45	50	--	
		2Ω, PVDD = 18V, THD + N = 1%, T_A = 75°C	60	65	--	
		2Ω, PVDD = 18V, THD + N = 10%, T_A = 75°C	75	80	--	
Total Harmonic Distortion + Noise	THD+N	1kHz, P_O =1W (BTL)	--	0.03	0.08	%
Output Integrated Noise	Vn	20Hz to 20kHz, A-weighted	--	18	25	μV
Output Offset Voltage	V_{OS}		–6.5	--	6.5	mV
Crosstalk	X_{TALK}	1kHz, P_O = 1W	--	–90	--	dB
Signal-to-Noise Ratio	SNR	PVDD = 14.4V, THD + N = 10%	--	115	--	dB
Power Supply Rejection Ratio	PSRR	Frequency @1kHz	–70	–80	--	dB
Dynamic Range	DR	Input level –60dBFS	--	115	--	dB
Output Attenuation		MUTEB = 0V	--	100	--	dB
Efficiency	η	4-channel operating, 25W output/CH 4Ω load, PVDD = 14.4V, including inductor loss (L = 3.3μH, C = 1μF)	87	--	--	%
Click and POP		High-Z/MUTE to Play, Play to MUTE/High-Z	--	7	14	mV
Global Junction Over-Temperature Warning	T_{OTW}		--	130	--	°C
Global Junction Over-Temperature Protection	T_{OTP}		--	160	--	°C
Over-Temperature Hysteresis	T_{OTP_HYS}		--	30	--	°C
Overcurrent Limit	I_{LIM}	OCLIM = 01	4	5.8	--	A
		OCLIM = 10	5.5	7.3	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Overcurrent Protection	I_{OCP}	Any short to supply, ground or channels	5.6	8	--	A
PVDD Overvoltage Protection	V_{OVP_PVDD}		--	21.5	--	V
PVDD Overvoltage Hysteresis	$V_{OVP\_HYS\_PVDD}$		--	0.6	--	V
VBAT Overvoltage Protection	V_{OVP_VBAT}		--	21.5	--	V
VBAT Overvoltage Hysteresis	$V_{OVP\_HYS\_VBAT}$		--	0.6	--	V
PVDD Undervoltage	V_{UVP_PVDD}		--	4	4.5	V
PVDD Undervoltage Hysteresis	$V_{UVP\_HYS\_PVDD}$		--	0.3	--	V
VBAT Undervoltage	V_{UVP_VBAT}		--	4	4.5	V
VBAT Undervoltage Hysteresis	$V_{UVP\_HYS\_VBAT}$		--	0.3	--	V
DC Offset Detection	DC_{FAULT}	Output DC fault protection	--	0.9	--	V
Maximum Resistance to Detect a Short from the OUT Pins to PVDD	R_{S2P}		--	--	1200	Ω
Maximum Resistance to Detect a Short from the OUT Pins to Ground	R_{S2G}		--	--	400	Ω
Short Load Detection Tolerance	R_{SL}	Other channels in Hi-Z	--	--	±0.5	Ω
Open Load	R_{OL}	Other channels in Hi-Z	40	70	--	Ω
DC Diagnostic Time	t_{DC_DIAG}	All 4 channels	--	--	100	ms
AC Impedance Accuracy	$R_{AC\_IMP\_ACC}$	Gain linearity, f = 19kHz, R_L = 2Ω to 16Ω	--	--	0.25	Ω
		Offset	--	--	±0.5	
AC Diagnostic Time	t_{AC_DIAG}	All 4 channels	--	100	--	ms
I^2C Interface Electrical Characteristics						
High-Level Input Voltage	V_{IH}		DVDD x 0.7	--	--	V
Low- Level Input Voltage	V_{IL}		--	--	DVDD x 0.3	V
Digital Output Low (SDA)	V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency	f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3	--	--	µs
Hold Time After (Repeated) Start Condition	$t_{HD;STA}$		0.6	--	--	µs

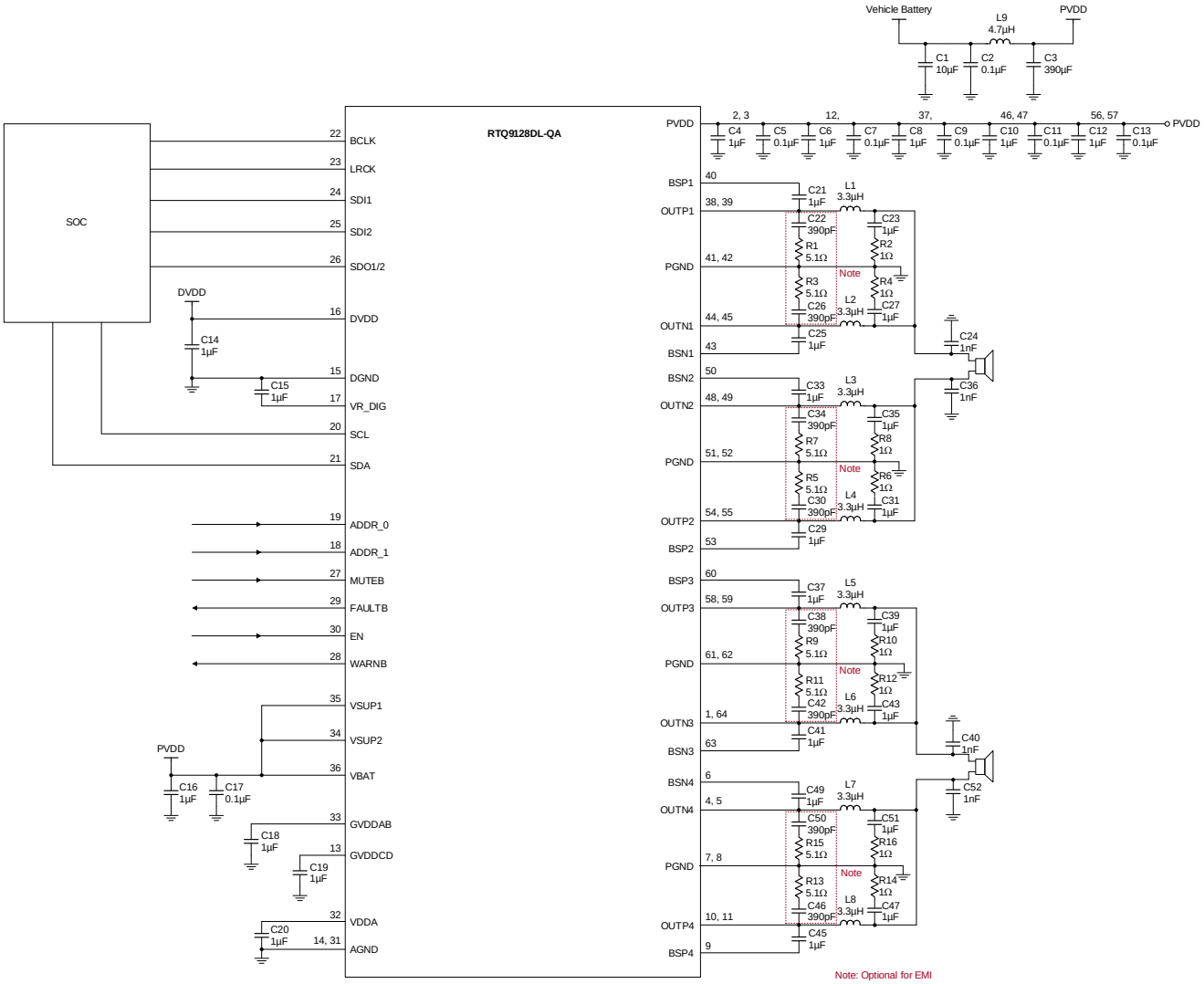
Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Repeated Start Condition Setup Time		$t_{SU;STA}$		0.6	--	--	µs
Stop Condition Time		$t_{SU;STD}$		0.6	--	--	µs
Data Hold Time		$t_{HD;DAT}$ (OUT)		225	--	--	ns
Input Data Hold Time		$t_{HD;DAT}$ (IN)		0	--	900	ns
Data Setup Time		$t_{SU;DAT}$		100	--	--	ns
Clock Low Period		t_{LOW}		1.3	--	--	µs
Clock High Period		t_{HIGH}		0.6	--	--	µs
Clock Data Fall Time		t_F		20	--	300	ns
Clock Data Rise Time		t_R		20	--	300	ns
Spike Suppression Time		t_{SP}		--	--	20	ns
Slave Mode I^2S Interface Electrical Characteristics							
High-Level Input Voltage		V_{IH}		DVDD x 0.7	--	--	V
Low-Level Input Voltage		V_{IL}		--	--	DVDD x 0.3	V
SDO1/2	VOH: High-Level Output Voltage	V_{OH}		--	--	3.3	V
	VOL: Low-Level Output Voltage	V_{OL}		--	--	0.4	
Frequency		f_{BCLKIN}		1.024	--	24.576	MHz
Setup Time, LRCK to BCLK Rising Edge		t_{SU1}		10	--	--	ns
Hold Time, LRCK from BCLK Rising Edge		t_{H1}		10	--	--	ns
Setup Time, SDIN to BCLK Rising Edge		t_{SU2}		10	--	--	ns
Hold Time, SDIN from BCLK Rising Edge		t_{H2}		10	--	--	ns
Rise/Fall Time for BCLK/LRCK		t_R/t_F		--	--	8	ns
I^2S Duty Cycle for Rising		%		40	--	60	%

12 Typical Application Circuit

12.1 4-Channel Bridge-Tied Load (BTL)Configuration



12.2 2-Channel Parallel Bridge-Tied Load (PBTL) Configuration



13 Timing Diagram

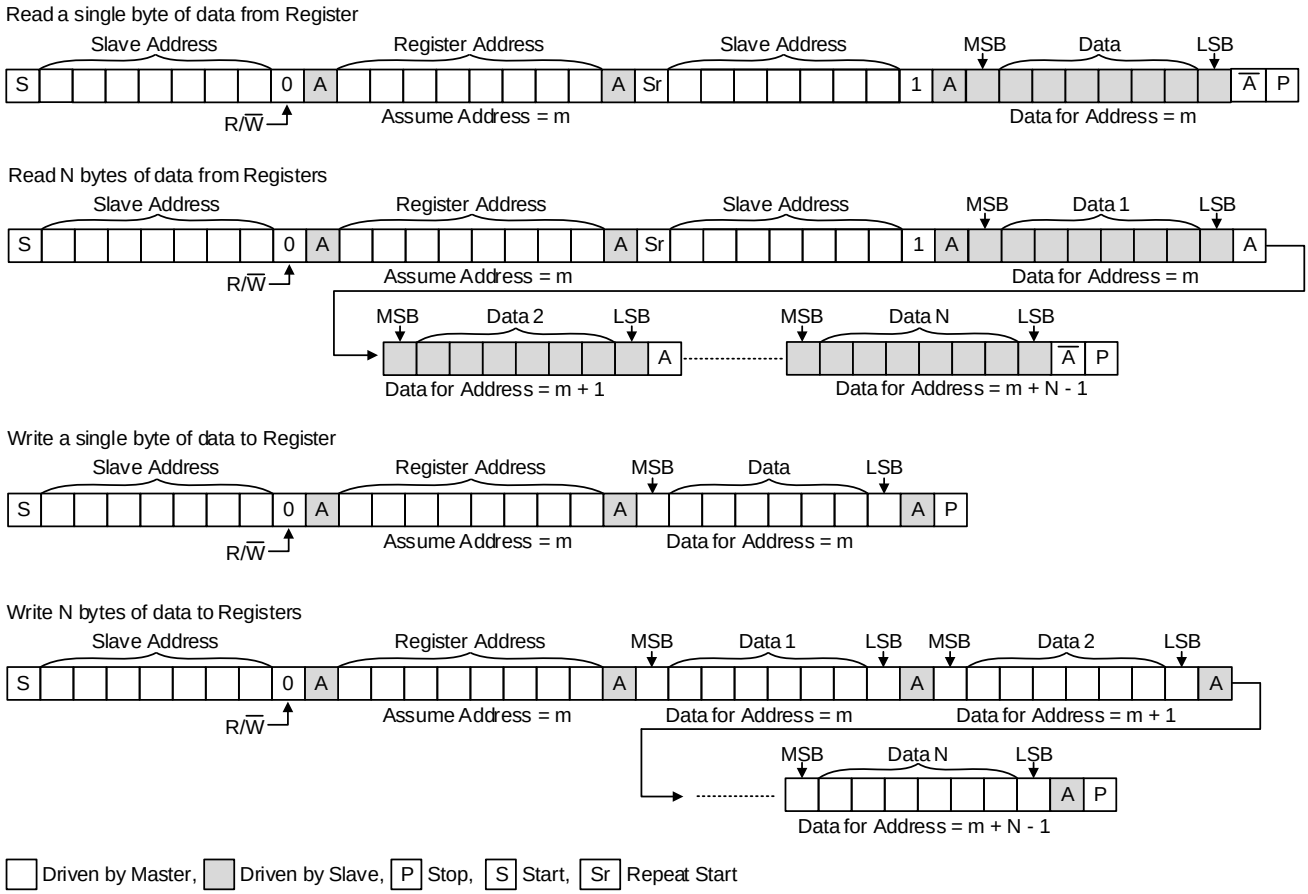


Figure 1. Read and Write Function

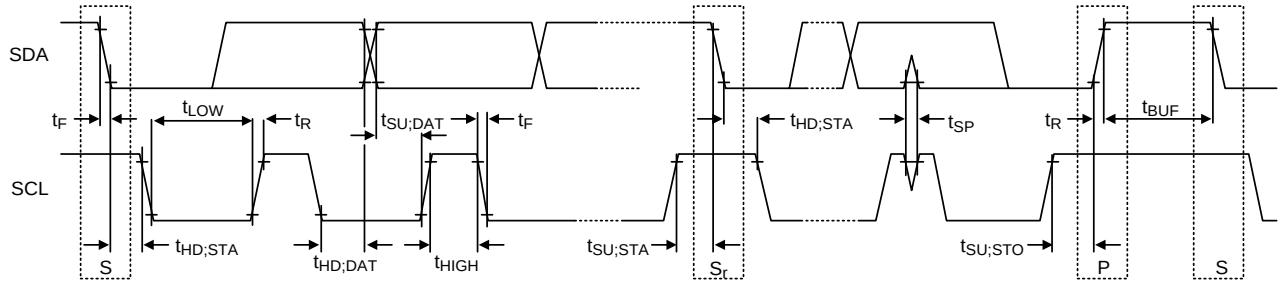


Figure 2. I²C Waveform Information

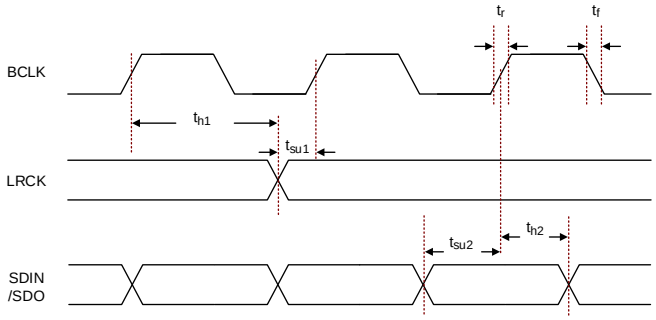


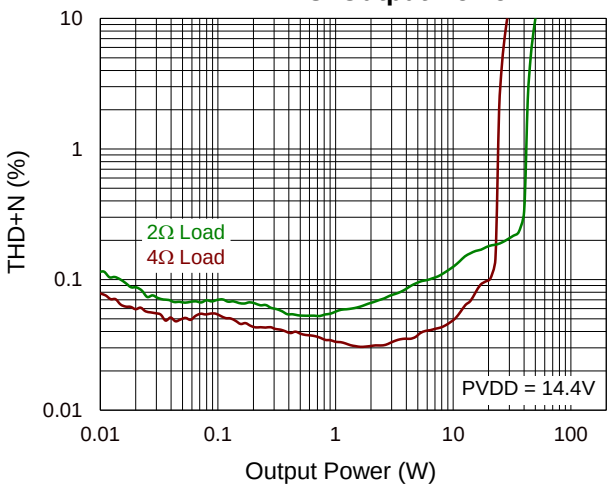
Figure 3. Timing Diagram of Slave Mode I²S Interface

14 Typical Operating Characteristics

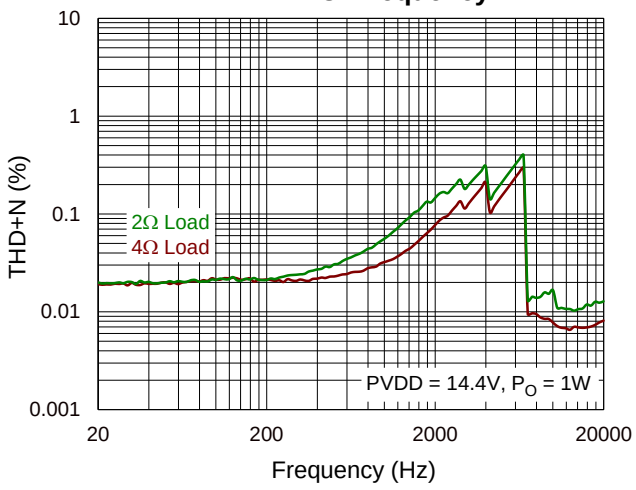
14.1 Bridge-Tied Load (BTL)

T_A = 25°C, DVDD = 3.3V, VBAT = PVDD = 14.4V, R_L = 4Ω, fin = 1kHz, f_S = 48kHz, f_{SW} = 2.1MHz, AES17 filter, LC filter: 3.3μF – HCM1A0703V2-3R3-R, 1μF + 1Ω

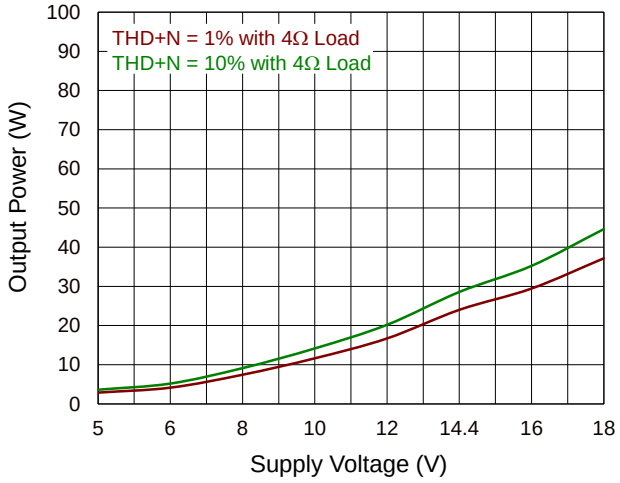
THD+N vs. Output Power



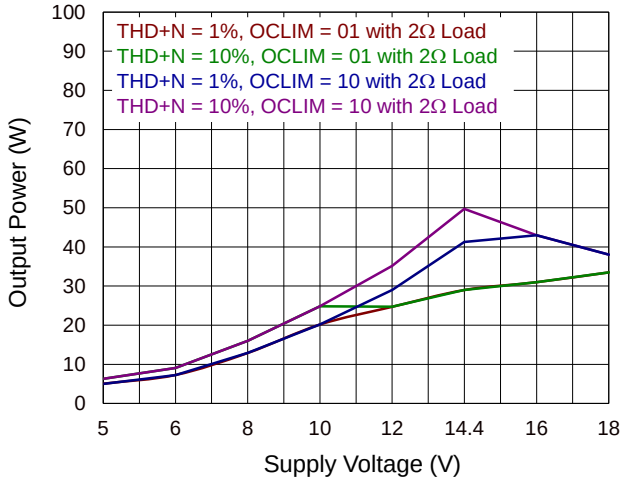
THD+N vs. Frequency



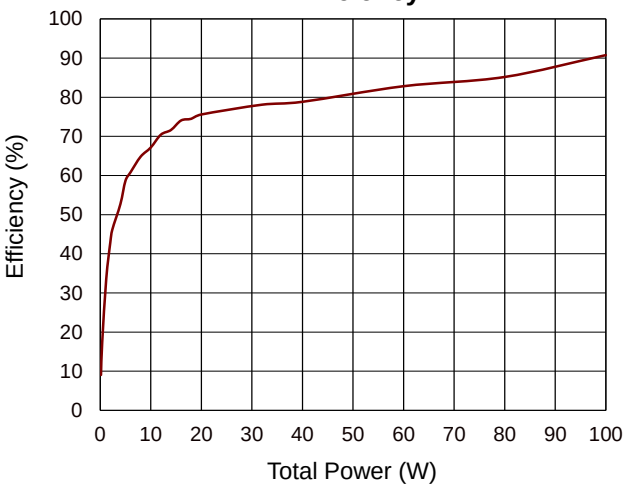
Output Power vs. Supply Voltage



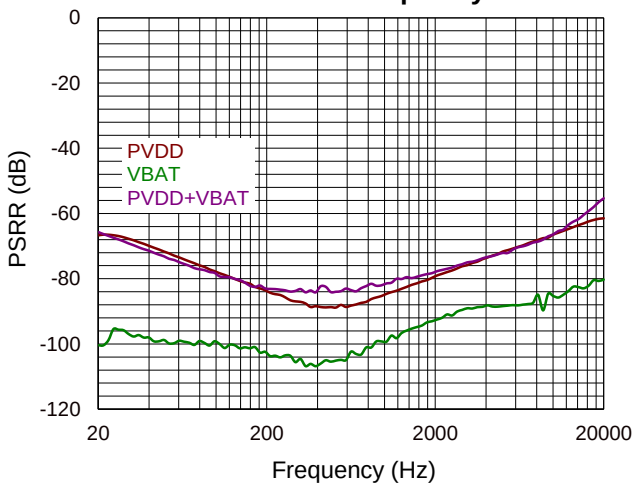
Output Power vs. Supply Voltage



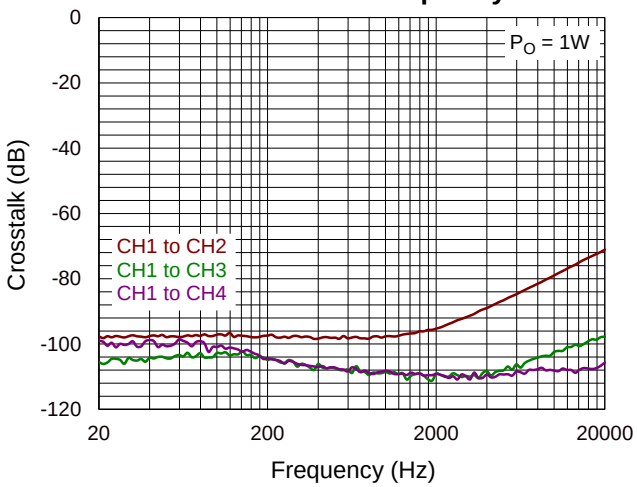
Efficiency



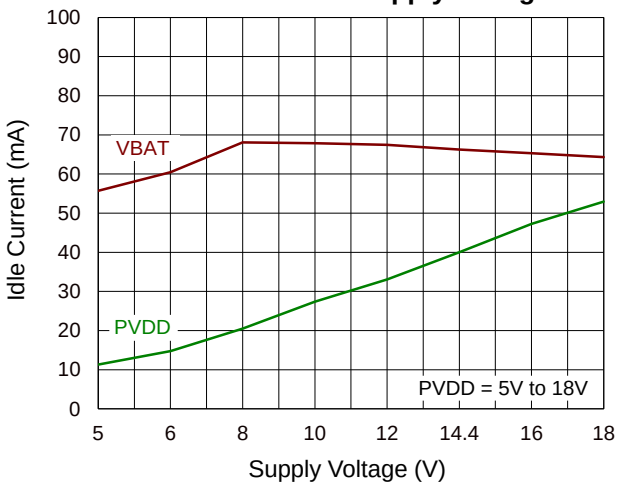
PSRR vs. Frequency



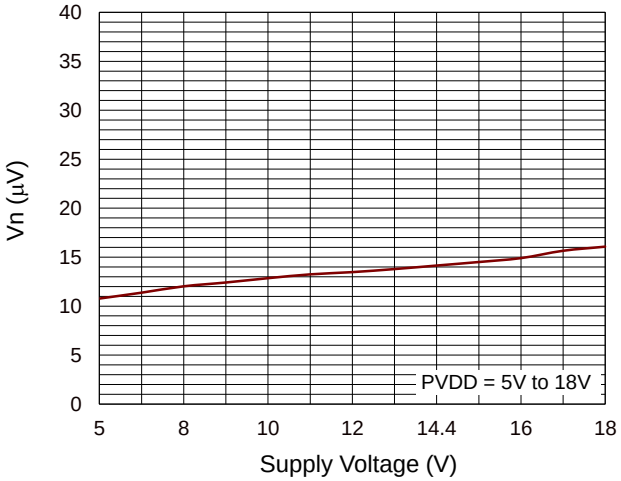
Crosstalk vs. Frequency



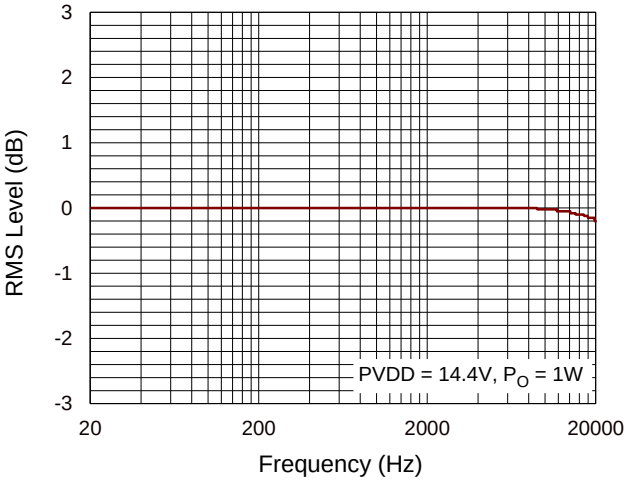
Idle Current vs. Supply Voltage



Vn vs. Supply Voltage



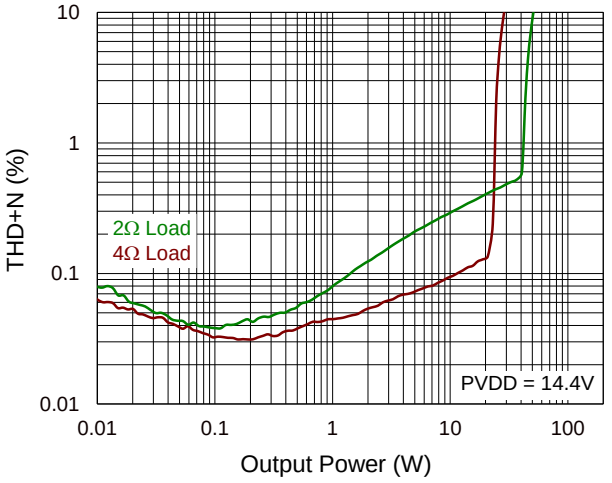
Frequency Response



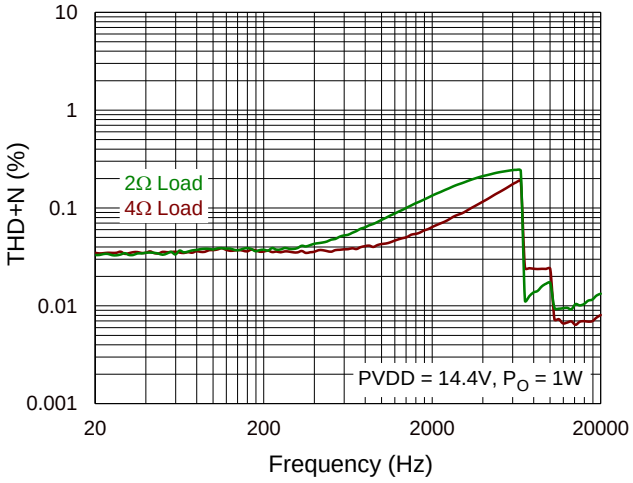
14.2 Bridge-Tied Load (BTL)

T_A = 25°C, DVDD = 3.3V, VBAT = PVDD = 14.4V, R_L = 4Ω, fin = 1kHz, f_S = 48kHz, f_{SW} = 384kHz, AES17 filter, LC filter: 10μH – HCM1A1307V2-100-R, 1μF + 1Ω (Note 7)

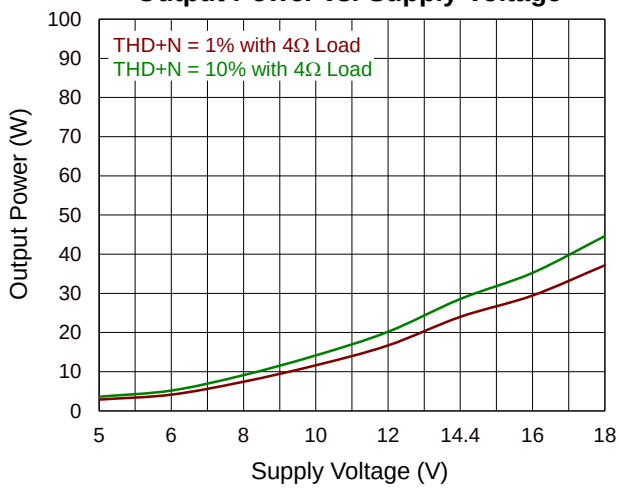
THD+N vs. Output Power



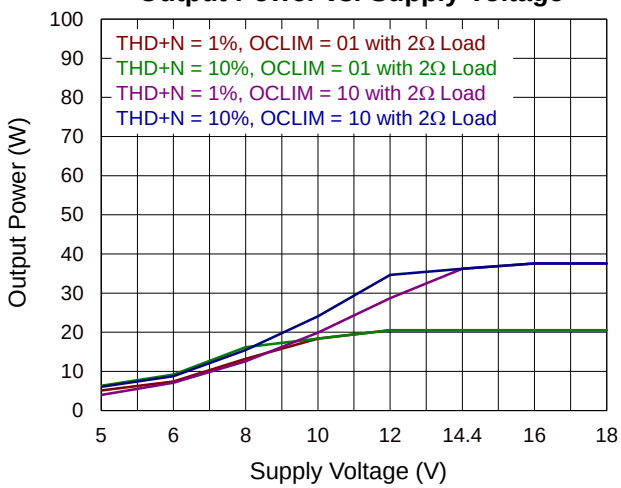
THD+N vs. Frequency



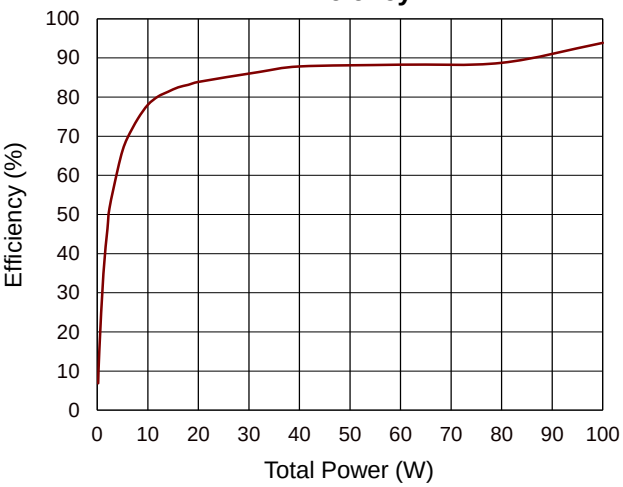
Output Power vs. Supply Voltage



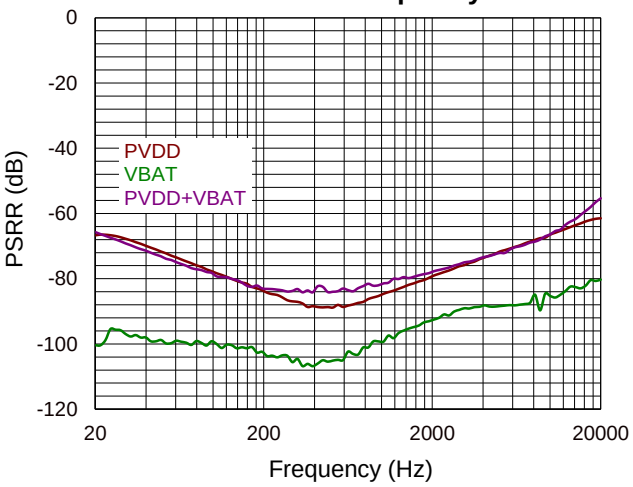
Output Power vs. Supply Voltage

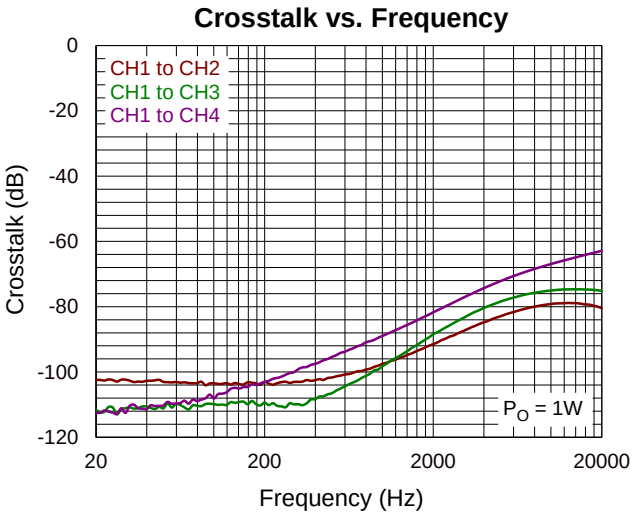


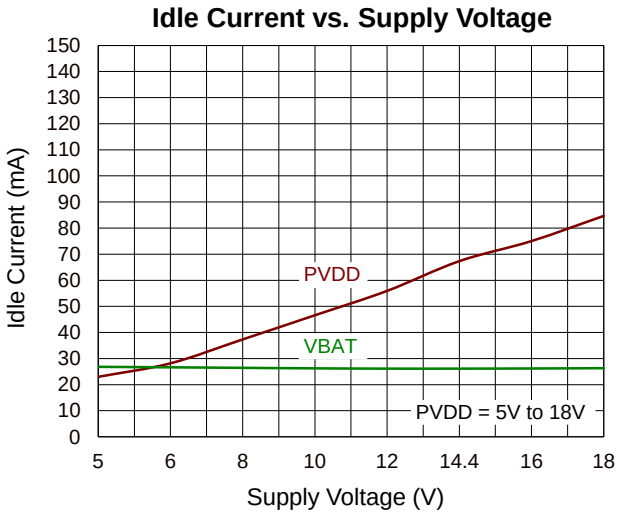
Efficiency

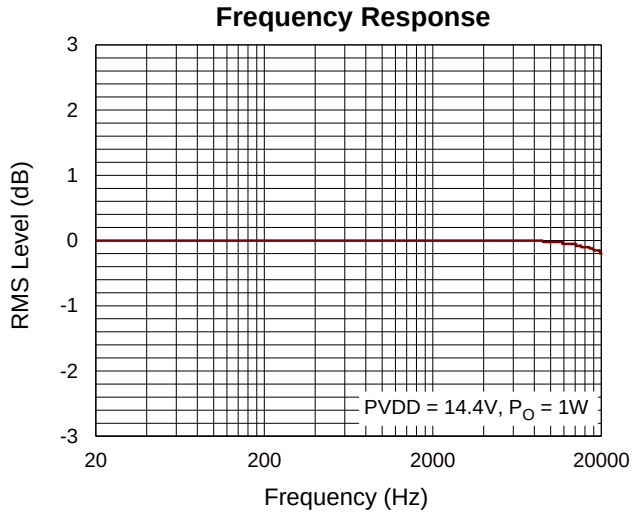


PSRR vs. Frequency







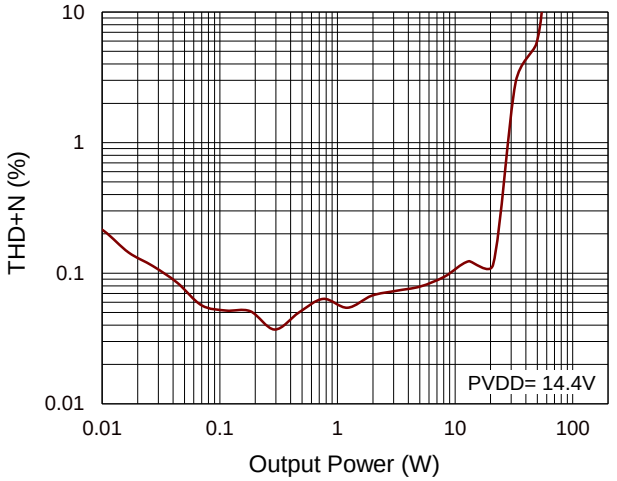


Note 7. All measurements were conducted using the RTQ9128DL-QA_EVM evaluation board in conjunction with an audio precision system equipped with an AUX-0025 low-pass filter. The tests were performed with a 1kHz test signal.

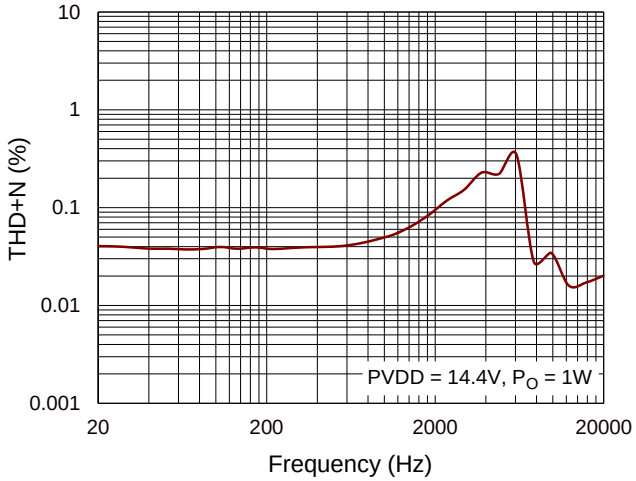
14.3 Parallel Bridge-Tied Load (PBTL)

T_A = 25°C, DVDD = 3.3V, VBAT = PVDD = 14.4V, R_L = 2Ω, fin = 1kHz, f_S = 48kHz, f_{SW} = 2.1MHz, AES17 filter, LC filter: 3.3μF – HCM1A1104V2-3R3-R, 1μF + 1Ω

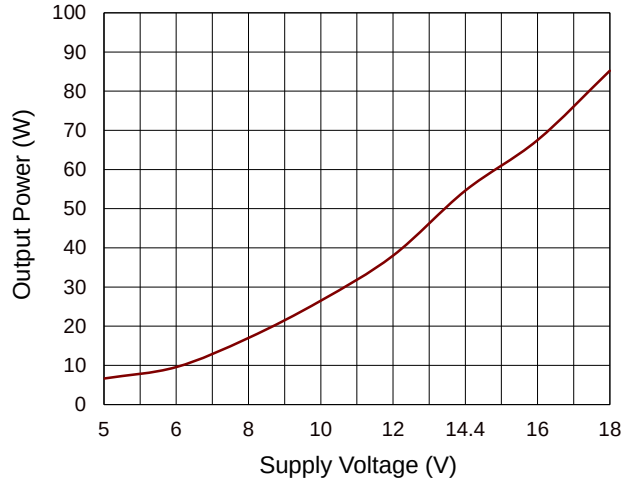
THD+N vs. Output Power



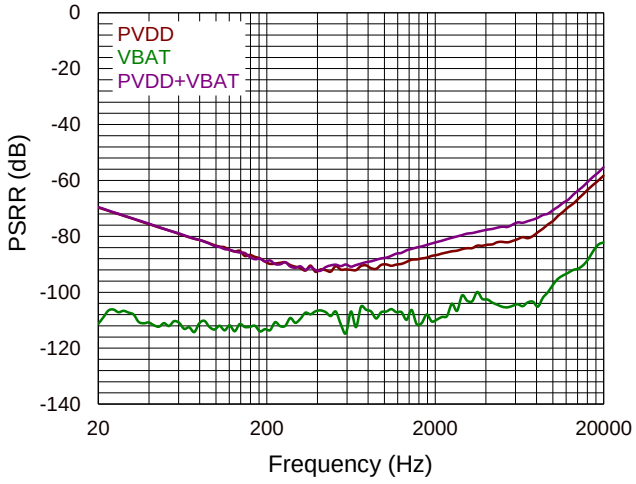
THD+N vs. Frequency



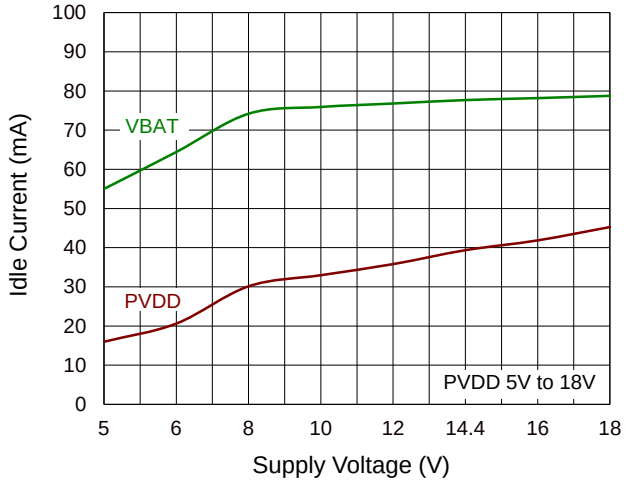
Output Power vs. Supply Voltage



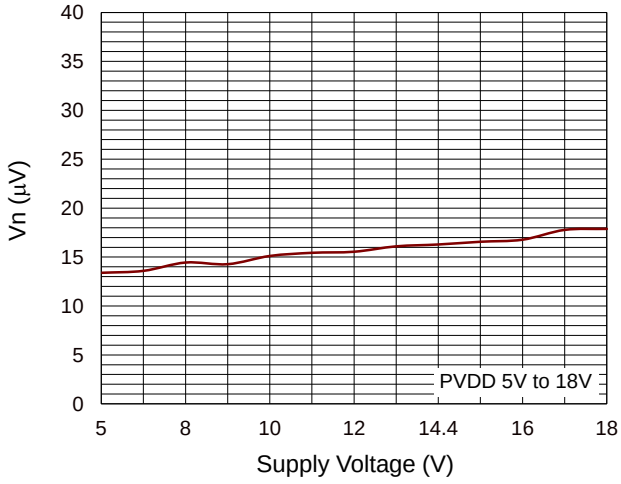
PSRR vs. Frequency

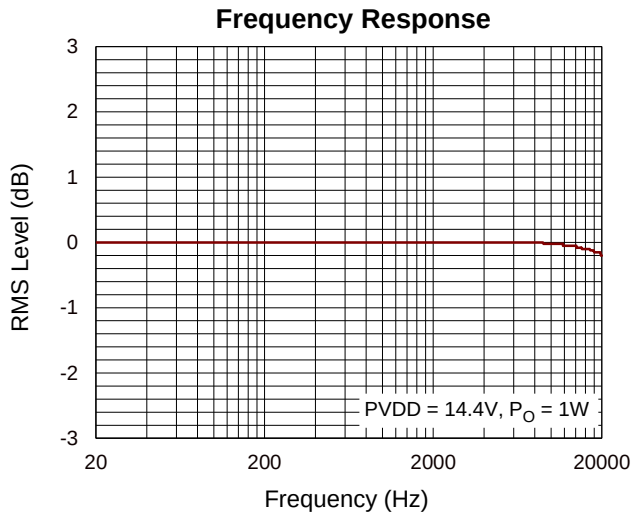


Idle Current vs. Supply Voltage



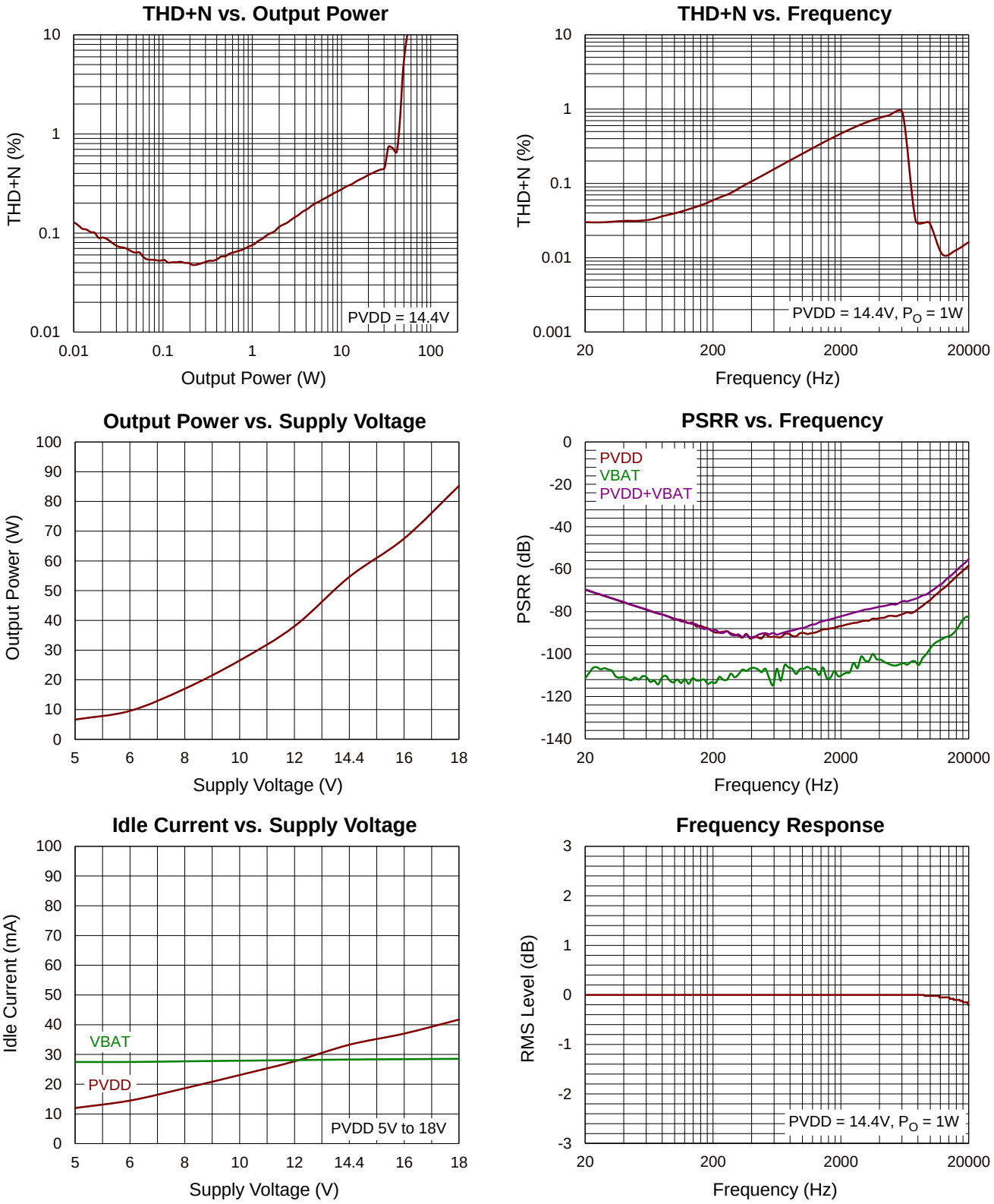
Vn vs. Supply Voltage





14.4 Parallel Bridge-Tied Load (PBTL)

T_A = 25°C, DVDD = 3.3V, VBAT = PVDD = 14.4V, R_L = 2Ω, fin = 1kHz, f_S = 48kHz, f_{SW} = 384kHz, AES17 filter, LC filter: 10μH – HCM1A1307V2-100-R, 1μF + 1Ω (Note 8)

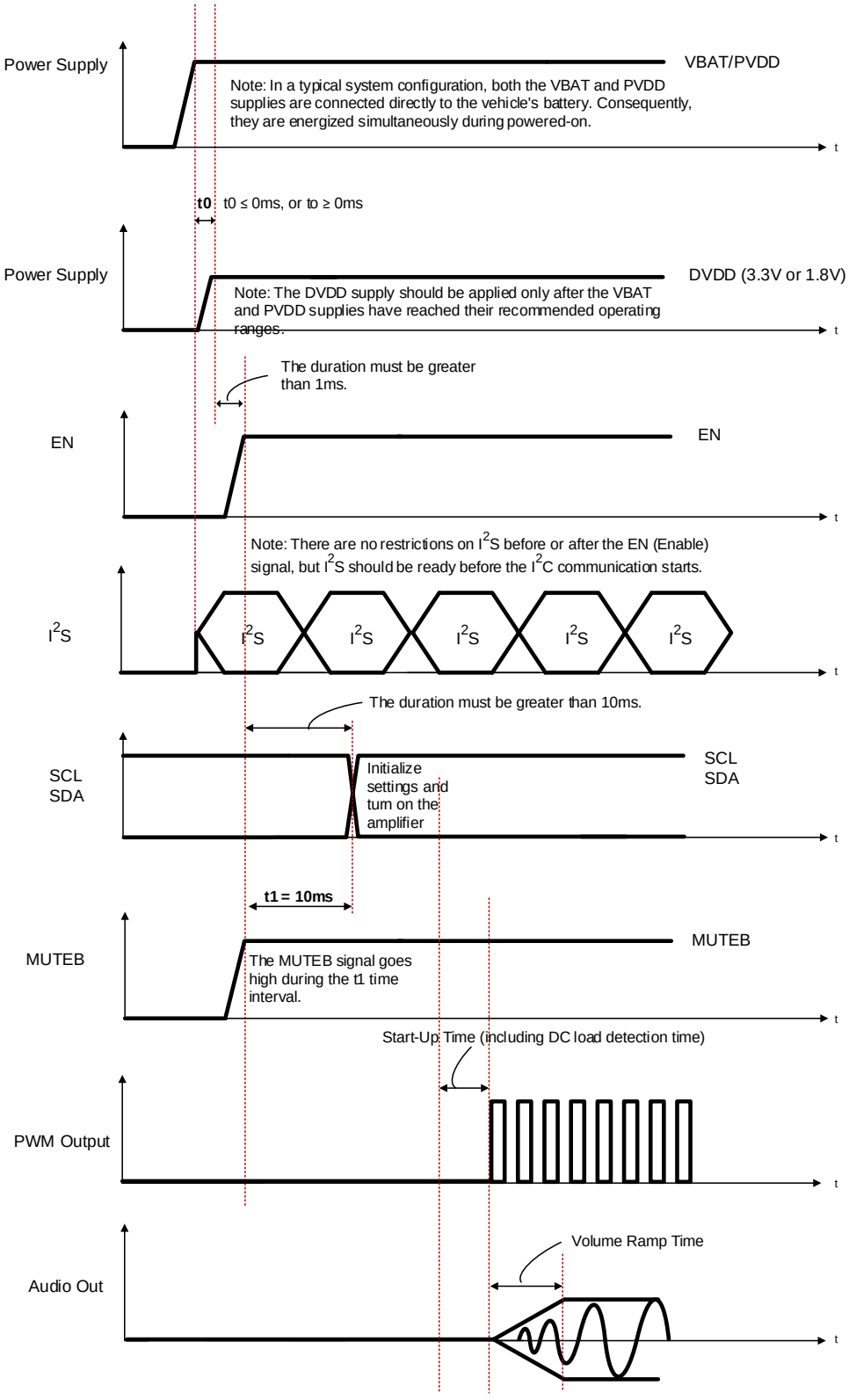


Note 8. Measurements were made using the RTQ9128DL-QA_EVM board and Audio Precision with AUX-0025 low-pass filter. All measurements taken with 1kHz.

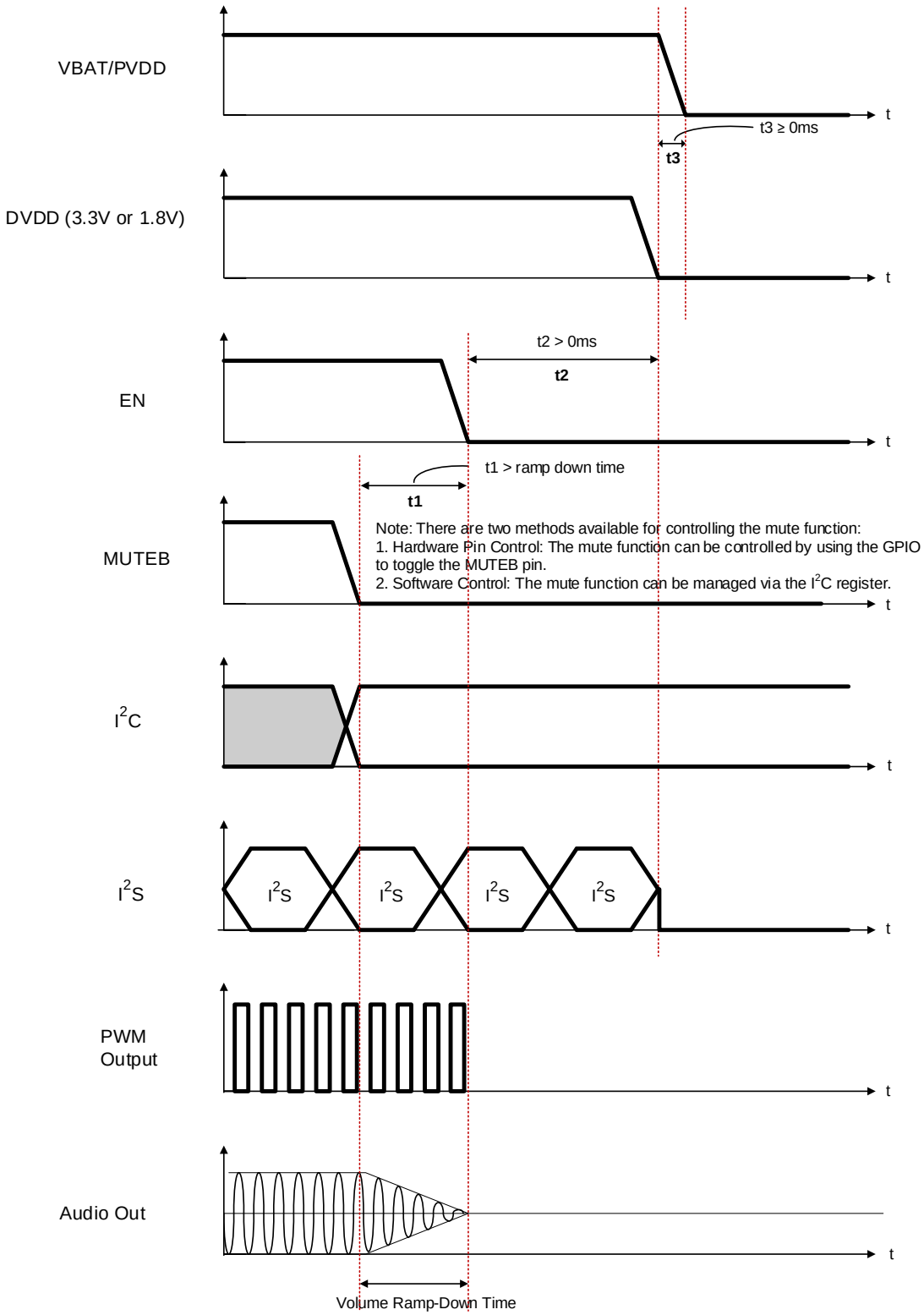
15 Application Information

(Note 9)

15.1 Power-On Sequence



15.2 Power-Off Sequence



15.3 Initial Sequence (BTL Mode, PWM = 2.1MHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x03	1	0x4D	Internal setting (SPK gain selection)	Initial setting
2	0x0F	1	0x00	Clear error flag	
3	0x30	2	0x01, 0x80	Set the volume 0dB	
4	0x04	1	0x00	Amp turn on	Amp turn on

15.4 Initial Sequence (BTL Mode, PWM = 384kHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x03	1	0x4D	Internal setting (SPK gain selection)	Initial setting
2	0x05	1	0x01	PWM is 384kHz	
3	0x0F	1	0x00	Clear error flag	
4	0x30	2	0x01, 0x80	Set the volume 0dB	
5	0x04	1	0x00	Amp turn on	Amp turn on

15.5 Initial Sequence (PBTL Mode, PWM = 2.1MHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x03	1	0x7D	Internal setting (SPK gain selection)	Initial setting
2	0x0F	1	0x00	Clear error flag	
3	0x30	2	0x01, 0x80	Set the volume 0dB	
4	0x04	1	0x00	Amp turn on	Amp turn on

15.6 Initial Sequence (PBTL Mode, PWM = 384kHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x03	1	0x7D	Internal setting (SPK gain selection)	Initial setting
2	0x05	1	0x01	PWM is 384kHz	
3	0x0F	1	0x00	Clear error flag	
4	0x30	2	0x01, 0x80	Set the volume 0dB	
5	0x04	1	0x00	Amp turn on	Amp turn on

15.7 I²C Serial Communication Bus

The RTQ9128DL-QA supports 16 sets of slave addresses, configurable through combinations of the ADDR_0 and ADDR_1 pins. These pins can be set using different resistors, each with a tolerance of 20%. Refer to the table below for specific address configurations.

ADDR_1 Pin	ADDR_0 Pin	Slave Address	Write	Read
Pull low	Pull low	0x10 (0010000x)	0x20	0x21
Pull low	Pull high	0x11 (0010001x)	0x22	0x23
Pull low	Pull low with 600kΩ	0x12 (0010010x)	0x24	0x25
Pull low	Pull high with 600kΩ	0x13 (0010011x)	0x26	0x27
Pull high	Pull low	0x14 (0010100x)	0x28	0x29
Pull high	Pull high	0x15 (0010101x)	0x2A	0x2B
Pull high	Pull low with 600kΩ	0x16 (0010110x)	0x2C	0x2D
Pull high	Pull high with 600kΩ	0x17 (0010111x)	0x2E	0x2F
Pull low with 600kΩ	Pull low	0x18 (0011000x)	0x30	0x31
Pull low with 600kΩ	Pull high	0x19 (0011001x)	0x32	0x33
Pull low with 600kΩ	Pull low with 600kΩ	0x1A (0011010x)	0x34	0x35
Pull low with 600kΩ	Pull high with 600kΩ	0x1B (0011011x)	0x36	0x37
Pull high with 600kΩ	Pull low	0x1C (0011100x)	0x38	0x39
Pull high with 600kΩ	Pull high	0x1D (0011101x)	0x3A	0x3B
Pull high with 600kΩ	Pull low with 600kΩ	0x1E (0011110x)	0x3C	0x3D
Pull high with 600kΩ	Pull high with 600kΩ	0x1F (0011111x)	0x3E	0x3F

The RTQ9128DL-QA is equipped with I²C communication capabilities, utilizing the SCL and SDA input ports. In the I²C protocol, devices transmitting data are designated as transmitters, while those reading the data are receivers. The master device initiates and controls the data transfer, supplying the serial clock to ensure synchronization. The RTQ9128DL-QA functions exclusively as a slave device in all communications and is capable of operating at speeds of up to 400 kB/s. Its I²C interface is designed to be slave-only.

15.8 I²C Bus Protocol

Data transitions on the SDA line are only permitted when the SCL clock signal is low. Transitions on the SDA line while the SCL signal is high indicate a START or STOP condition. A START condition is signaled by a high-to-low transition on the SDA line while the SCL line remains high and stable. This condition must be established before any data transfer command is issued. Conversely, a STOP condition is signaled by a low-to-high transition on the SDA line while the SCL line remains high and stable, marking the end of communication between the RTQ9128DL-QA and the bus master. During data reception, the RTQ9128DL-QA samples the SDA line at the rising edge of the SCL signal. To ensure proper operation of the device, the SDA signal must remain stable during the rising edge of the SCL signal, and data changes on the SDA line should only occur when the SCL signal is low.

15.9 Audio Interface

The RTQ9128DL-QA supports four types of audio interfaces: I^{2}S, Left-Justified, Right-Justified, and TDM. Each interface is capable of handling audio data formats of 32-bit, 24-bit, 20-bit, and 16-bit. The corresponding timing diagrams are provided below.

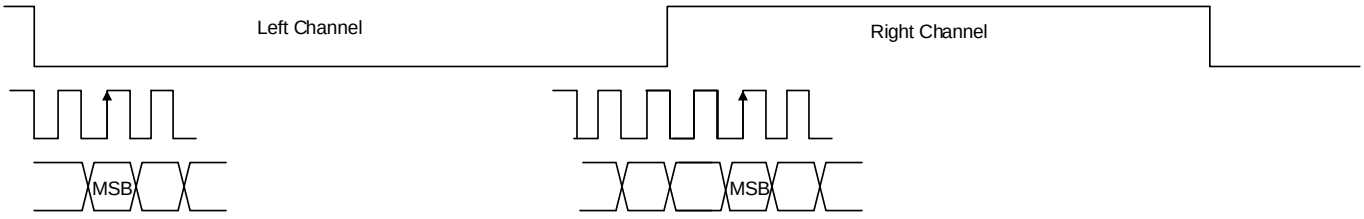


Figure 4. I^{2}S Format

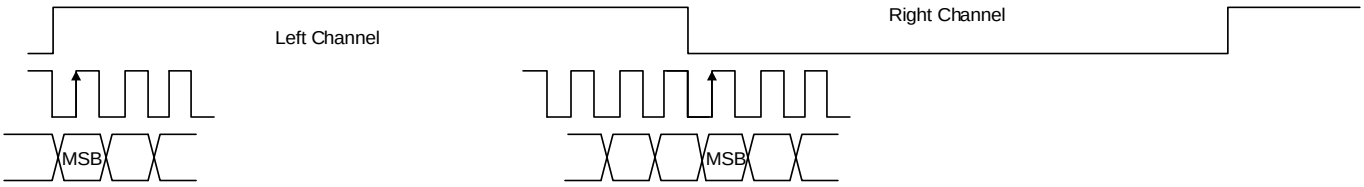


Figure 5. Left-Justified

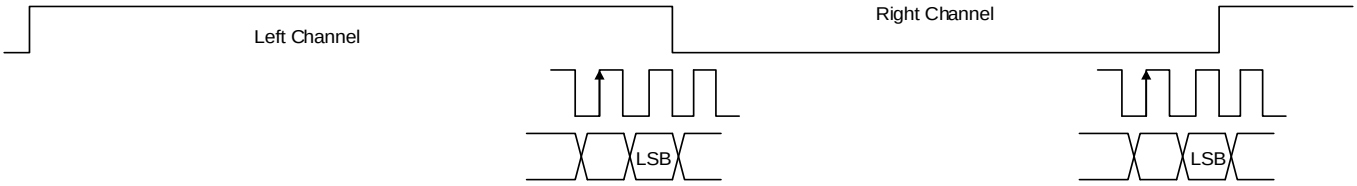


Figure 6. Right-Justified

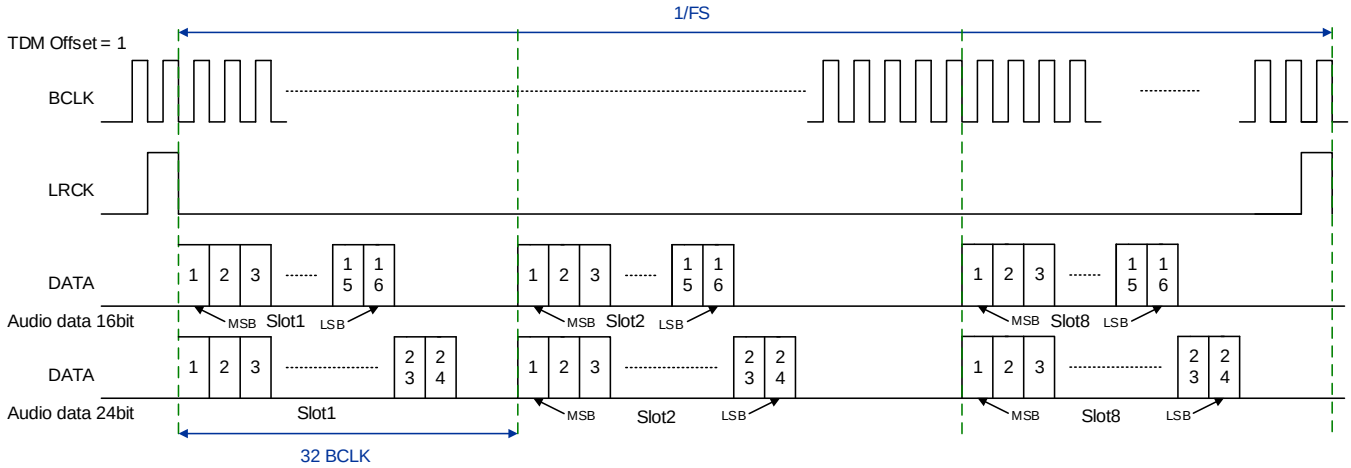


Figure 7. TDM (Offset = 1)

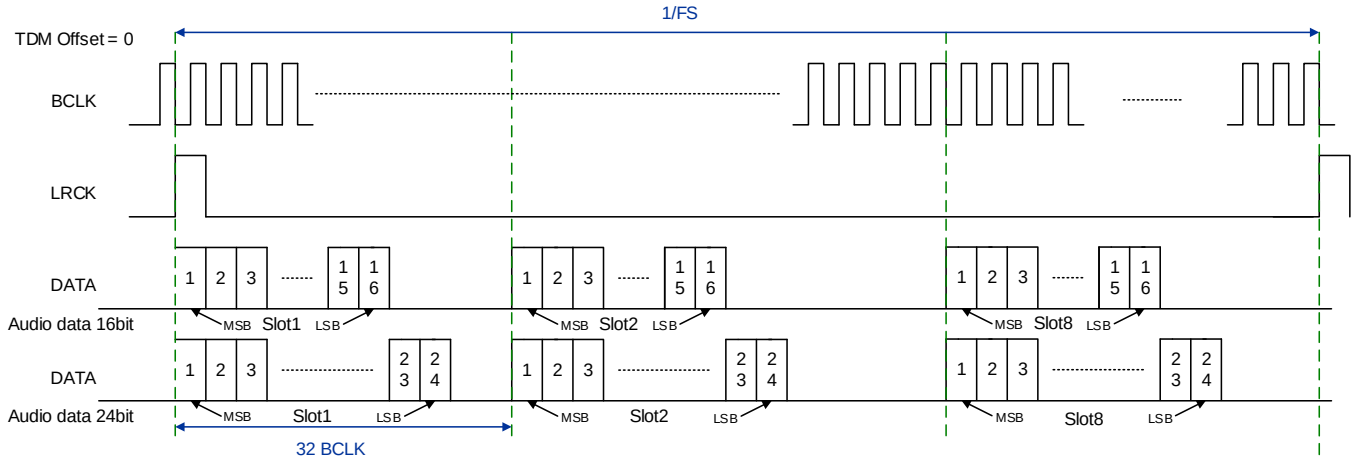


Figure 8. TDM (Offset = 0)

15.10 Time-Division Multiplexing (TDM) Mode

The TDM mode supports a maximum of 16 audio channels. The device can be configured via I^2C to select different stereo pairs within the TDM data stream.

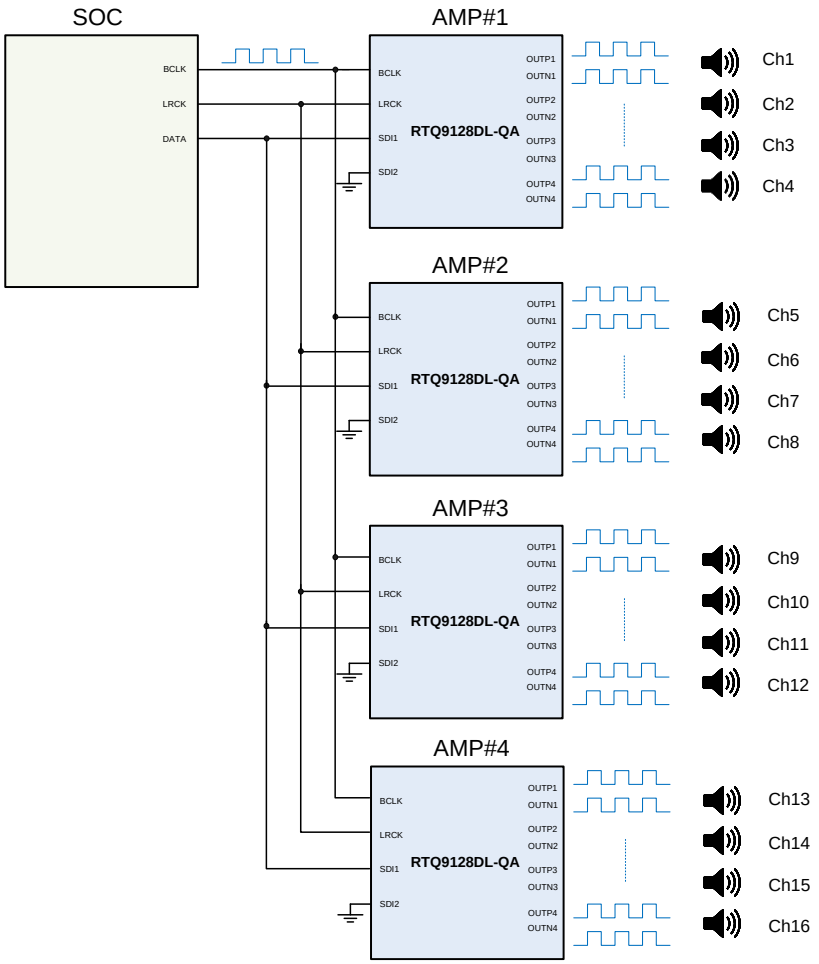


Figure 9. TDM16

15.11 Digital Signal Processor

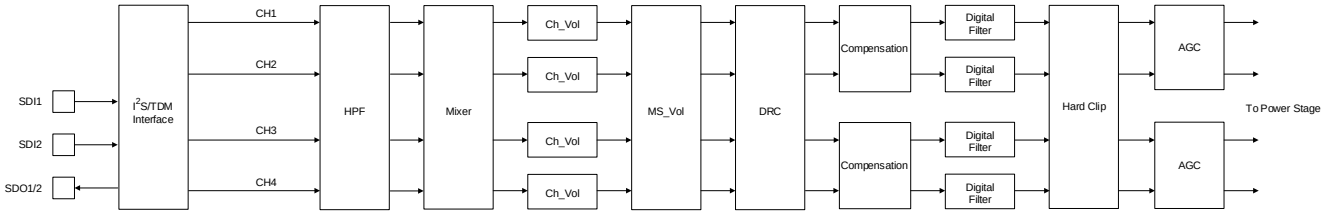


Figure 10. Digital Signal Processor

15.12 High-Pass Filter (HPF)

The RTQ9128DL-QA supports an input high-pass filter (HPF) for each channel, designed to act as a DC-cut filter with a cutoff frequency of 1.5Hz.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x08	1	7	RW	HPF_EN	High-Pass filter enable 0: Disable 1: Enable (default)	1

15.13 Mixer

The RTQ9128DL-QA supports an input channel mixer that can route to any output channel.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x00	1	7:6	RW	Ch1_SI	00: CH1 to CH1 (default) 01: CH2 to CH1 10: CH3 to CH1 11: CH4 to CH1	00
		5:4	RW	Ch2_SI	00: CH1 to CH2 01: CH2 to CH2 (default) 10: CH3 to CH2 11: CH4 to CH2	01
		3:2	RW	Ch3_SI	00: CH1 to CH3 01: CH2 to CH3 10: CH3 to CH3 (default) 11: CH4 to CH3	10
		1:0	RW	Ch4_SI	00: CH1 to CH4 01: CH2 to CH4 10: CH3 to CH4 11: CH4 to CH4 (default)	11

15.14 Volume

The RTQ9128DL-QA features a master volume control (MS_VOL) and individual channel volume controls (CH1_VOL, CH2_VOL, CH3_VOL, and CH4_VOL). The volume adjustment step size is 0.0625dB, ranging from 24dB to mute. Each channel also includes a mute control (CH1_MUTE, CH2_MUTE, CH3_MUTE, and CH4_MUTE).

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x30	2	10:0	RW	MS_Vol	Master volume control 11'h000: 24dB 11'h180: 0dB 11'h7FF: Mute (default) 0.0625dB per step	11'h7FF

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x31	2	10:0	RW	CH1_VOL	CH1 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180

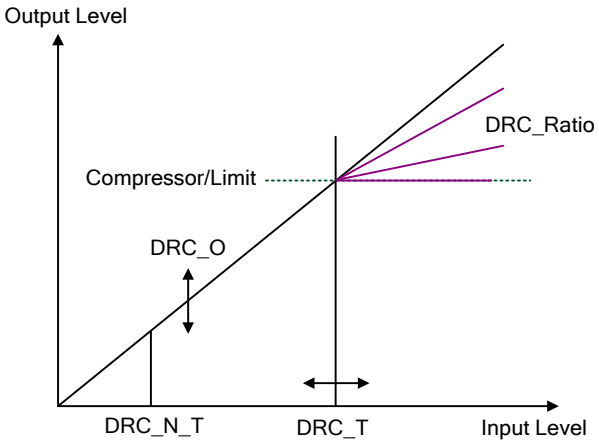
ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x32	2	10:0	RW	CH2_VOL	CH2 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x33	2	10:0	RW	CH3_VOL	CH3 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x34	2	10:0	RW	CH4_VOL	CH4 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180

15.15 Dynamic Range Control (DRC)

The RTQ9128DL-QA features Dynamic Range Control (DRC), which provides compression capabilities to adjust audio signals, making them sound softer or louder based on the input level.

DRC Description	Address	Description
DRC_T: Threshold	0x40	
DRC_O: Make up gain	0x41	
DRC_Ratio: Compress ratio	0x42	
DRC_N_T: Noise gate threshold	0x43	
Noise gate enable	0x2A	

15.15.1 DRC Threshold

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x40	3	10:0	RW	DRC_TH	DRC threshold 11'h000: 0dB (default) 11'h180: –24dB 11'h67E: –103.875dB 11'h67F ~ 11'h7FF: Not available 0.0625dB per step	11'h000

15.15.2 DRC Offset

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x41	3	10:0	RW	DRC_ OFFSET	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: –103.9375dB 0.0625dB per step	11'h180

15.15.3 DRC_RATIO

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x42	3	7:0	RW	DRC_ RATIO	DRC compress ratio 8'h00: No compression 8'h80 (default) ~ 8'hFF: Full compression 1/128 per step	8'h80

15.15.4 Noise Gate Threshold

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x43	3	10:0	RW	DRC_NG_TH	Noise gate threshold 11'h000: 0dB 11'h180: −24dB 11'h640: −100dB (default) 11'h67E: −103.875dB 11'h67F ~ 11'h7FF: Not available 0.0625dB per step	11'h640

15.15.5 DRC_EN

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x2A	1	7:4	RW	DRC_EN_CH	Dynamic range control (DRC) enabled {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable	0000
		3:0	RW	DRC_N_EN_CH	DRC Noise gate enabled {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable	0000

15.16 Compensation Filter

The compensation filter is used to adjust the internal gain from the DAC. This filter can also correct the frequency response affected by the LC filter. The recommended settings will vary based on different application circuits to achieve the desired response curve.

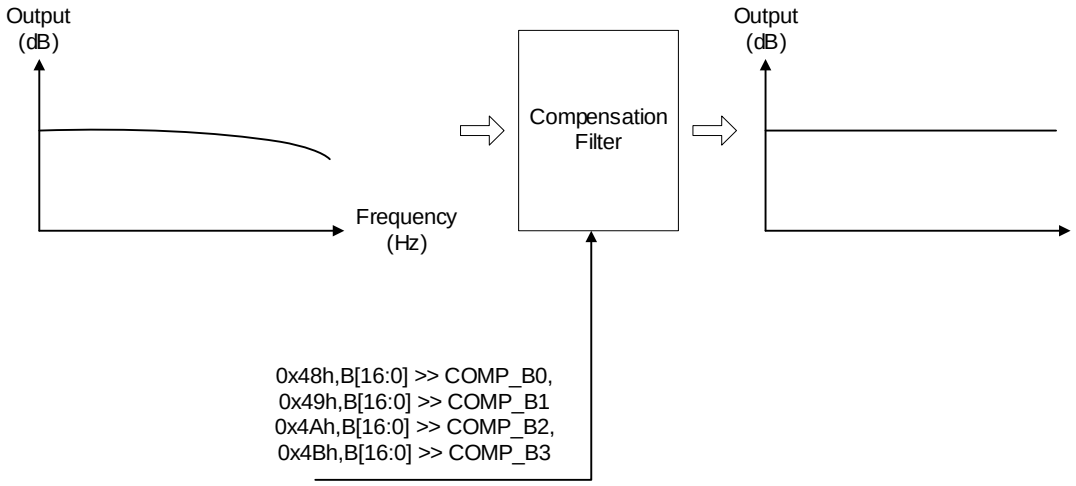


Figure 11. Compensation Filter

Table 1. Compensation Table

	−1.0	−0.9	−0.8	−0.7	−0.6	−0.5	−0.4	−0.3	−0.2	−0.1	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
B3 0x4B	1FFE6	1FFE8	1FFEA	1FFED	1FFF0	1FFF2	1FFF5	1FFF8	1FFFA	1FFFE	0000	2	6	9	C	F	12	16	19	1D	21
B2 0x4A	1FFBD	1FFC3	1FFCA	1FFD2	1FFD7	1FFDE	1FFE5	1FFEC	1FFF2	1FFF9	0000	7	E	14	1B	22	29	30	37	3B	43
B1 0x49	3D7	37A	31B	2B6	255	1F4	193	130	CC	62	0000	1FF9D	1FF2F	1FEC5	1FE5A	1FDED	1FD7F	1FD10	1FC9F	1FC2C	1FBB0
B0 0x48	790E	79B6	7A60	7B17	7BC9	7C77	7D27	7DDA	7E8F	7F50	8000	80B3	817A	823B	82FE	83C3	848B	8555	8622	86F6	87D9

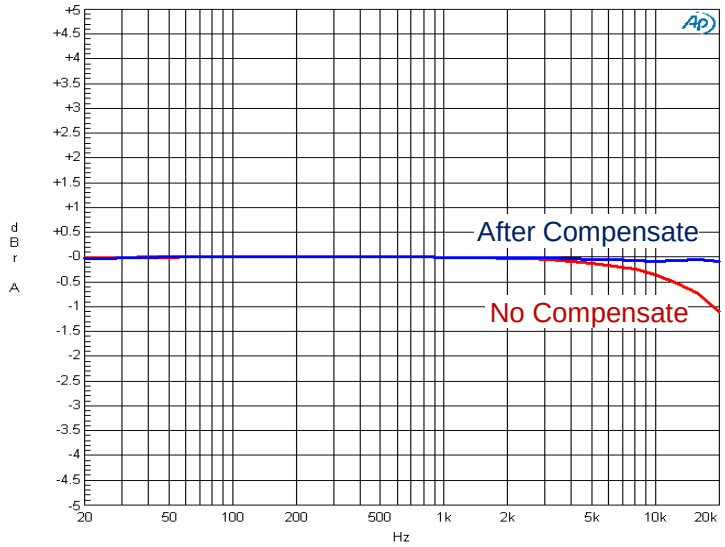


Figure 12. Compensation Filter Measured Result

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x48	3	16:0	RW	COMP_B0	Compensation filter coefficient B0, COEF_PAGE_SEL (0x09) select CH12 or CH34	17'h0_8000
0x49	3	16:0	RW	COMP_B1	Compensation filter coefficient B1, COEF_PAGE_SEL (0x09) select CH12 or CH34	17'h0_0000
0x4A	3	16:0	RW	COMP_B2	Compensation filter coefficient B2, COEF_PAGE_SEL (0x09) select CH12 or CH34	17'h0_0000
0x4B	3	16:0	RW	COMP_B3	Compensation filter coefficient B3, COEF_PAGE_SEL (0x09) select CH12 or CH34	17'h0_0000

15.17 Hard Clip Function

A hard clip can be employed to digitally maintain specified THD levels without resorting to voltage clipping. This feature enables users to consistently achieve the same THD (for example, 10% THD) across various power levels (15W, 10W, and 5W) while using the same PVDD level.

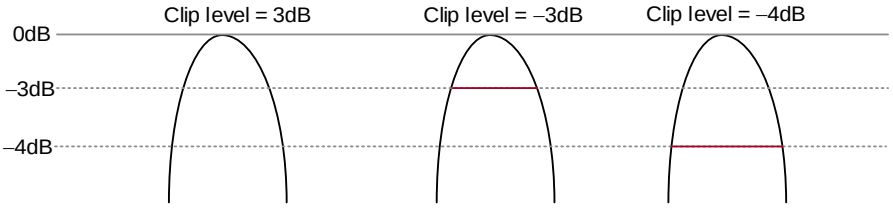


Figure 13. Hard Clip

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x35	2	10:0	RW	HC_TH	Hard clip threshold when HARD_CLIP_EN = 1 >0dB is not allowable for hard clip threshold setting 11'h180: 0dB (default) 0.0625db per step	11'h180

15.18 Auto-Gain Control (AGC)

The RTQ9128DL-QA supports AGC (Auto-Gain Control) for current limiting and clip detection functions. The AGC enable is independently controlled by the register at address 0x71 for both current limiting and clip detection.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x71	1	1	RW	EN_ILIMIT_AGC	Enable auto gain control for current limit detection 0: Disable 1: Enable (default)	1
		0	RW	EN_CLIP_AGC	Enable auto gain control for CLIP detection 0: Disable (default) 1: Enable	0

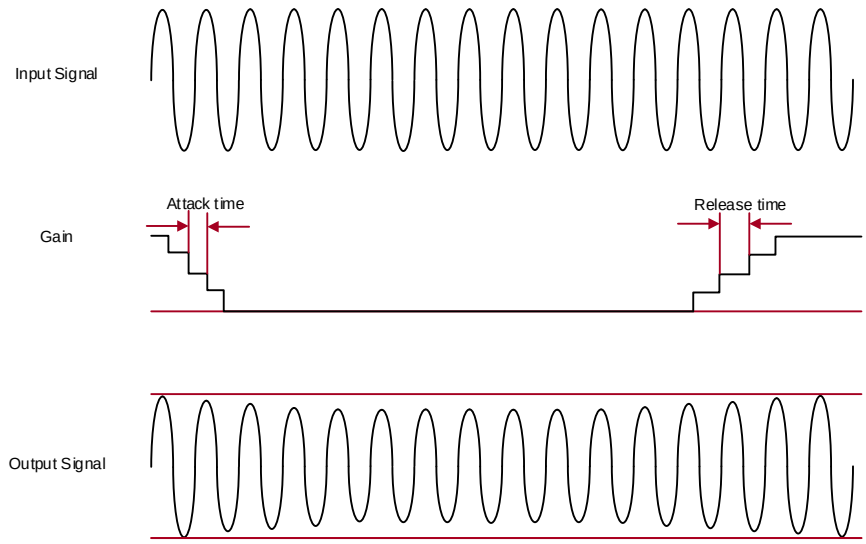


Figure 14. AGC Attack and Release

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x74	1	3:2	RW	AGC_ ATTACK_ RATE	AGC attack time selection for AGC and IAGC 00: 0.25dB/20μs 01: 0.25dB/40μs (default) 10: 0.25dB/80μs 11: 0.25dB/160μs	01
		1:0	RW	AGC_ RELEASE_ RATE	AGC release time selection for AGC and IAGC 00: 0.25dB/200ms 01: 0.25dB/400ms (default) 10: 0.25dB/800ms 11: 0.25dB/1600ms	01

15.19 SDO Output Configure

The I^{2}S/TDM digital input signal path from the input pin to the power stage is illustrated in Figure 15. There are several nodes along the digital signal transmission path where the signal can be measured to verify proper functionality. The settings in register 0x01 Bit[3:0] can be output through the SDO1/2 pin.

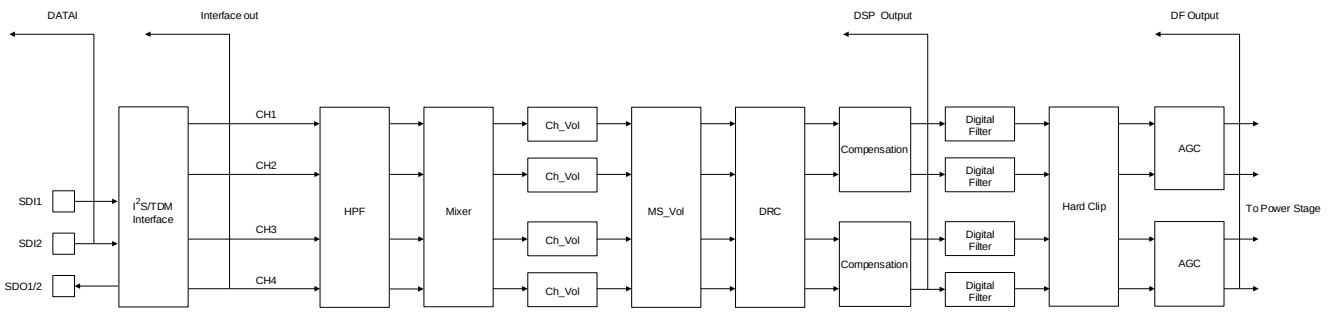


Figure 15. SDO Output Configure

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x01	1	3:0	RW	SDO_SEL	I²S/LJ/RJ/DSPM 0000: No output (default) 0001: I2S_DATAI_1 0010: I2S_DATAI_2 0100: Interface output CH1, CH2 0101: Interface output CH3, CH4 0110: DSP output CH1, CH2 0111: DSP output CH3, CH4 1000: DF output CH1, CH2 1001: DF output CH3, CH4 Others: No output TDM 0000: No output (default) 0001: I2S_DATAI_1 0010: I2S_DATAI_2 010X: Interface output CH1, CH2, CH3, CH4 011X: DSP output CH1, CH2, CH3, CH4 100X: DF output CH1, CH2, CH3, CH4 Others: No output	0000

Under specific conditions, the Serial Data Output (SDO) supports a maximum frequency of 18.8MHz. Considering the variable stray capacitance of external wiring, the internal drive current of the SDO can be adjusted as needed through register settings. For scenarios where the stray capacitance is 30pF, increasing the drive current to 16mA ensures reliable operation of the application at 18.8MHz.

0xF3, D_DRV bit[7:6]	Io at DVDD = 3.3V
D_DRV bit[7:6] = 00	4mA
D_DRV bit[7:6] = 01	8mA
D_DRV bit[7:6] = 10	12mA
D_DRV bit[7:6] = 11	16mA

15.20 Hardware Control Pins

The device features four pins for control and status indication: FAULTB, MUTEB, WARNB, and EN. The FAULTB pin reports faults and is active low under any of the following conditions:

- Any channel faults (overcurrent or DC offset detection)
- Over-temperature protection
- Overvoltage or undervoltage conditions on the VBAT or PVDD pins
- Clock errors

For all listed faults, the FAULTB pin remains asserted even after the fault condition is rectified. The register reports for all faults remain asserted until the CLEAR FAULT method is executed by writing to address 0x0F=00. At that point, all fault register reports in ERR_INT_INDEX will be cleared to their default values, and the FAULTB pin will no longer remain asserted.

Register bits are available to mask fault categories from being reported to the FAULTB pin. These bits only mask the pin's status and do not affect the register reporting or the device's protection mechanisms. By default, all faults are reported to the pin. Refer to the Register Maps section for a description of the mask settings.

The active-low output WARNB pin reports audio clipping, over-temperature warnings, and overcurrent limit warnings. Clipping is reported when any channel reaches maximum modulation for 20 consecutive PWM clocks (default value), resulting in a 10μs delay in reporting the onset of clipping. The Clip Detect Warning bit, which is sticky in latching mode, can be cleared by accessing the ERR_INT_INDEX in the register at address 0x0F and writing to address 0x0F = 00. An over-temperature warning (OTW) is triggered if the general temperature or any channel-specific temperature warnings are activated. Register bits are available to selectively mask the reporting of clipping, OTW, or ILIMIT to the pin. These bits solely affect the pin's setting and do not influence the register reporting. By default, clipping, ILIMIT, and OTW are reported at addresses 0x14 and 0x15.

The active-low input MUTEB pin controls the mute and unmute functions for all channels.

When the EN pin is at a low level, the device enters shutdown mode, the I^2C function is disabled, and the current consumption is minimized. This pin allows for rapid shutdown of the device and resets the registers to their default values. When the EN pin is at a high level, the device enters standby mode and the I^2C function is enabled. In this mode, the RTQ9128DL-QA can be commanded via I^2C to enter other modes.

15.21 Operating Modes and Faults

STATE_CTRL	Power MOSFETS	OSCILLATOR	I^2C
Normal	Switching with input signal	Active	Active
Shutdown	Hi-Z	Stopped	Inactive
Standby	Hi-Z	Stopped	Active
Hi-Z	Hi-Z	Active	Active
MUTE	25% (CMH) or 50% (BD) switching	Active	Active
ULQM	Hi-Z	Stopped	Active

Fault Event	Reporting	Result	Monitor State	Protection Active	Behavior
CLK Error	I^2C+FAULTB pin	Hi-Z	All	4 Channel	Auto-recovery (default)
DVDD UV	I^2C+FAULTB pin	Hi-Z	All	4 Channel	Auto-recovery (default)
VDDA/GVDD UV	I^2C+FAULTB pin	Hi-Z	All	4 Channel	Auto-recovery (default)
VBAT/PVDD UV	I^2C+FAULTB pin	Hi-Z	All	4 Channel	Auto-recovery (default)
VBAT/PVDD OV	I^2C+FAULTB pin	Hi-Z	All	4 Channel	Auto-recovery (default)
OTPG	I^2C+FAULTB pin	Hi-Z	All	4 Channel	Auto-recovery (default)
OTPC	I^2C+FAULTB pin	Hi-Z	All	1 Channel (individual)	Auto-recovery (default)
S2P/S2G/OL/SL	I^2C+FAULTB pin	Hi-Z	Load detection	1 Channel (individual)	Latch (default)
Overcurrent	I^2C+FAULTB pin	Hi-Z	Normal, Mute	1 Channel (individual)	Auto-recovery (default)

Fault Event	Reporting	Result	Monitor State	Protection Active	Behavior
DC	I²C+FAULTB pin	Hi-Z	Normal, Mute	1 Channel (individual)	Latch (default)
POR	I²C+WARNB pin	Shutdown	All	N/A	N/A
OTWG	I²C+WARNB pin	N/A	All	N/A	N/A
OTWC	I²C+WARNB pin	TFB (optional)	Normal, Mute	1 Channel (individual TFB)	N/A
Current Limit	I²C+WARNB pin	AGC (optional)	Normal, Mute	1 Channel (individual AGC)	N/A
Clip	I²C+WARNB pin	AGC (optional)	Normal, Mute	1 Channel (individual AGC)	N/A

15.22 Common Mode Hopping (CMH) Mode

The RTQ9128DL-QA incorporates CMH (Common Mode Hopping) mode to reduce pulse width at small signal levels. This reduction in pulse width decreases inductor current ripple, thereby improving light load efficiency. The CMH Mode can be configured by registers 0xA5[3:2] and 0xA5[1:0].

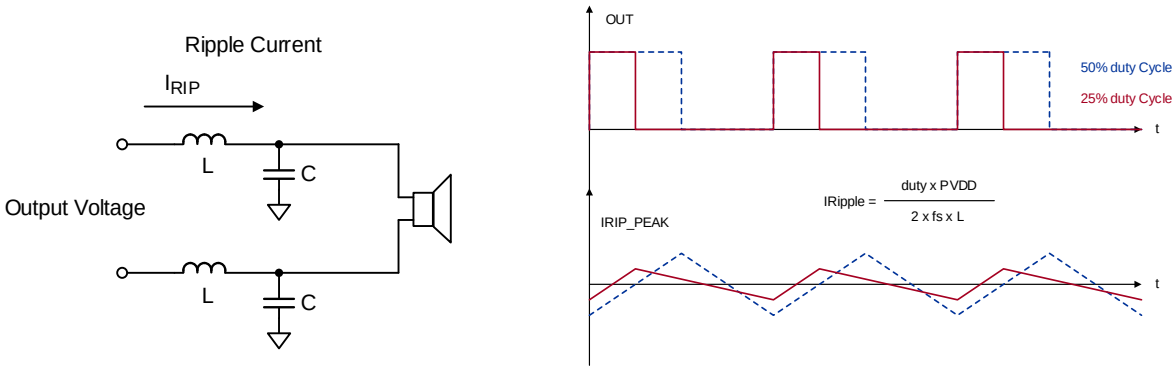


Figure 16. Current Ripple with CMH

15.23 Ultra-Low Quiescent Mode (ULQM)

In ULQM, the RTQ9128DL-QA powers the FETs in Hi-Z status with low standby current, and the transition time from ULQM to normal mode is approximately 4ms. After the initial power-on, it is recommended to use ULQM to save energy.

15.24 Pulse-Width-Modulator (PWM) Frequency

The output switching rate is synchronous to the serial audio clock input and is programmed through I²C to match the input sample rate in the register (address 0x05[6:4]). The option to switch at a high frequency allows the use of smaller and lower-cost external filtering components.

Sample Rate	Reg 0x05h, BITS 6:4 Setting				
	000	001	010	011	100
32kHz	Not support	Not support	1.28MHz	1.41MHz	1.53MHz
44.1kHz	352kHz	441kHz	1.76MHz	1.94MHz	2.1MHz
48kHz	384kHz	480kHz	1.92MHz	2.1MHz	2.3MHz
88.2kHz	352kHz	441kHz	1.76MHz	1.94MHz	Not support
96kHz	384kHz	480kHz	1.92MHz	2.1MHz	Not support

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x05	1	6:4	RW	PWM_FREQ	PWM frequency selection 000: 8*fs 001: 10*fs 010: 40*fs 011: 44*fs (default) 100: 48*fs Others: Reserved	011

15.25 AM-Radio Band Avoidance

By setting the switching frequency of the device above the AM frequency band, interference with AM radio frequencies can be avoided. The available switching frequency options include 38fs, 44fs, and 48fs. If the switching frequency cannot be set above the AM frequency band, the alternatives of 8fs and 10fs should be used. These settings should be adjusted to avoid active AM channels.

15.26 EMI Management Features

The RTQ9128DL-QA features a spread-spectrum function and output phase control to address EMI issues.

15.26.1 Spread-Spectrum Function

There are two methods: varying the spread-spectrum frequency and adding noise to the triangular modulation.

The spread-spectrum frequency variation amplitude is controlled via the register at address 0x07[1:0], and noise can be added to the triangular modulation through the register at address 0x07[6:2].

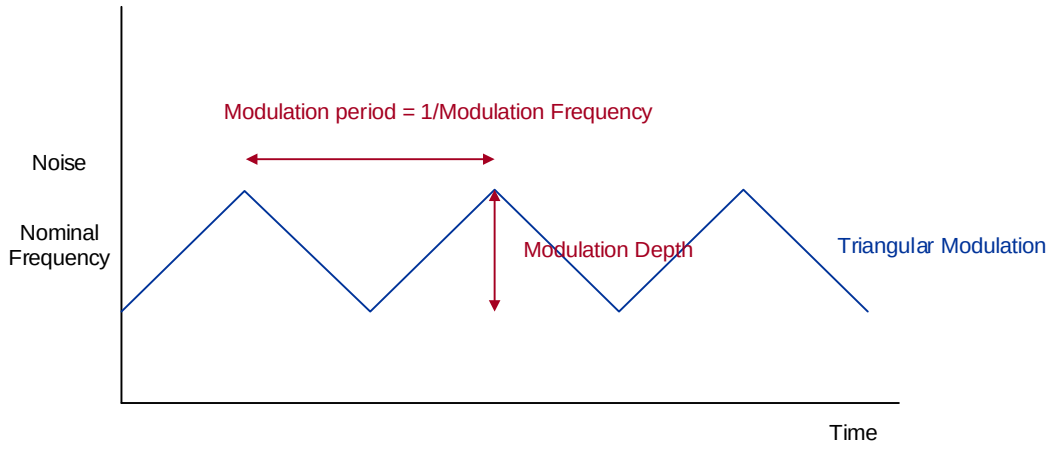


Figure 17. Spread-Spectrum Algorithm

15.27 Channel-to-Channel Output Phase Control

The RTQ9128DL-QA features a channel-to-channel phase control function. Channel 1 is used as a reference for other channels, and the PWM phase of channels 2, 3, and 4 can be shifted from 0 to 315 degrees in 45-degree increments.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x05	1	2:0	RW	OUT_ PHASE_2	CH2 output phase offset 000: 0 degree 001: 45 degree (default) 010: 90 degree 011: 135 degree 100: 180 degree 101: 225 degree 110: 270 degree 111: 315 degree	001
0x06	1	6:4	RW	OUT_ PHASE_3	CH3 output phase offset 000: 0 degree 001: 45 degree 010: 90 degree (default) 011: 135 degree 100: 180 degree 101: 225 degree 110: 270 degree 111: 315 degree	010
		2:0	RW	OUT_ PHASE_4	CH4 output phase offset 000: 0 degree 001: 45 degree 010: 90 degree 011: 135 degree (default) 100: 180 degree 101: 225 degree 110: 270 degree 111: 315 degree	011

15.28 Load Diagnostics

The device features both DC and AC load diagnostics to assess the status of the load. DC diagnostics are enabled by default via the register at address 0x03[6]. However, for a fast start-up that bypasses diagnostics, DC diagnostics can be disabled through I^2C. DC diagnostics activate when any channel transitions from the Hi-Z state to either the MUTE or PLAY state. Additionally, DC diagnostics can be manually activated for any or all channels. They can commence under any operating condition; however, if a channel is in the PLAY state, the diagnostic process takes longer. This delay occurs because the device must decrease the audio signal of that channel before it can switch to the Hi-Z state. DC diagnostics become available as soon as the device's power supply is within the recommended operating range. These diagnostics do not depend on the availability of audio input clocks. Results from the DC diagnostics are reported individually for each channel via the I^2C registers.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x03	1	6	RW	EN_DC_LOAD_DET	Execute DC load diagnostics before amp on sequence 0: Disable 1: Enable (default)	1

15.29 DC Load Detection

DC load detection assesses the status of the speaker side to prevent speaker damage. During this process, the device remains in a high-impedance state while playing a detection pattern. There are five types of DC load detection results: S2G (short to ground), SL (short load), normal, OL (open load), and S2P (short to power). The DC load detection method involves playing a pattern between the output channels OUTP and OUTN to diagnose the load (RL) status. The diagnostic results are obtained through an internal ADC and stored in registers 0x8C to 0x8F after offset subtraction. Converting these register values to decimal and dividing by 740 provides the diagnostic results. For load resistances below 5Ω, the tolerance is within ±0.5Ω. DC load detection can be automatically initiated when the amplifier is powered on, as configured by bit 6 of register 0x03. It can also be manually triggered by setting bits [7:4] of register 0x53. The thresholds for short load detection are controlled by registers at addresses 0x51 and 0x52, while the typical threshold for an open load is 70Ω. Thus, a normal status falls between the short and open load thresholds.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x51	1	7:4	RW	SL_TH_CH1	CH1 SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω Others: Reserved	0001
		3:0	RW	SL_TH_CH2	CH2 SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω Others: Reserved	0001
0x52	1	7:4	RW	SL_TH_CH3	CH3 SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω Others: Reserved	0001
		3:0	RW	SL_TH_CH4	CH4 SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω Others: Reserved	0001

When the DC load detection result indicates an abnormal output channel, the device will pull the FAULTB voltage low. Registers 0x16 and 0x17 can be read to confirm the diagnostic result and identify the abnormal output channel.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x16	1	7:4	RWC	S2P	Output short to power {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
		3:0	RWC	S2G	Output short to ground {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
0x17	1	7:4	RWC	OL	Output open load {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
		3:0	RWC	SL	Positive output shorting to negative output {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000

15.30 AC Load Detection

AC load detection can help distinguish speaker types such as woofers and tweeters. For AC load detection, the device must be in the Hi-Z state. When detection finishes, users can obtain the magnitude and phase. The method of AC diagnosis involves playing a signal frequency pattern between the output channels OUTP and OUTN to diagnose the speaker status. The diagnostic result is obtained through an internal ADC, and the parameter values can be compensated and converted internally to obtain the magnitude and phase. AC load detection can be manually executed by setting bits [7:4] of register 0x55. The RTQ9128DL-QA GUI provides a load diagnostics function, which allows the load detection results to be displayed through the GUI without the need for manual calculation.

15.31 Output Voltage

There are three types of gain in the RTQ9128DL-QA: digital volume gain, analog DAC gain, and speaker gain. The output voltage calculation formula is: Output Voltage (Vp) = 10^ ((D + Volume Gain) / 20) x 3.74 x Output Gain.

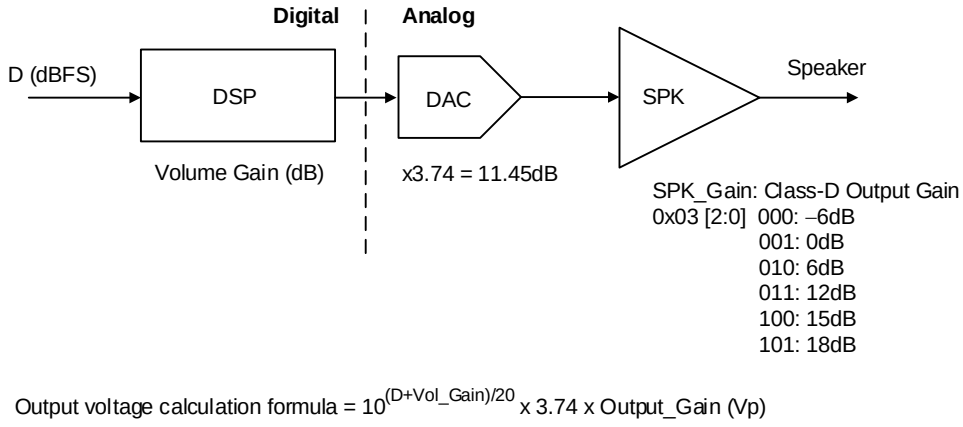


Figure 18. Output Voltage Calculation

15.32 Overcurrent Limit (ILIMIT)

When the current limit (ILIMIT) is exceeded, the overcurrent protection terminates each PWM pulse to limit the output current. Although power is restricted, the operation continues uninterrupted, preventing accidental protection during brief musical events. ILIMIT is not reported as a fault condition to registers or the FAULTB pin; instead, it is indicated as a warning condition on the WARNB pin and in the ILIMIT status register (address 0x15). Each channel is monitored and limited independently. Four programmable levels can be configured using two bits in the register at address 0xB4.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x15	1	3	RWC	ILIMIT_Flag_4	Current limit flag CH4 0: Normal (default) 1: Warning (write 0 to clear)	0
		2	RWC	ILIMIT_Flag_3	Current limit flag CH3 0: Normal (default) 1: Warning (write 0 to clear)	0
		1	RWC	ILIMIT_Flag_2	Current limit flag CH2 0: Normal (default) 1: Warning (write 0 to clear)	0
		0	RWC	ILIMIT_Flag_1	Current limit flag CH1 0: Normal (default) 1: Warning (write 0 to clear)	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0xB4	1	7:6	RW	ILIMIT_SEL_1	CH1 current limit threshold selection 00: 4.8A 01: 5.8A (default) 10: 7.3A 11: Reserved	01
		5:4	RW	ILIMIT_SEL_4	CH4 current limit threshold selection 00: 4.8A 01: 5.8A (default) 10: 7.3A 11: Reserved	01
		3:2	RW	ILIMIT_SEL_3	CH3 current limit threshold selection 00: 4.8A 01: 5.8A (default) 10: 7.3A 11: Reserved	01
		1:0	RW	ILIMIT_SEL_2	CH2 current limit threshold selection 00: 4.8A 01: 5.8A (default) 10: 7.3A 11: Reserved	01

15.33 Overcurrent Protection (OCP)

The RTQ9128DL-QA features an Overcurrent Protection (OCP) function to prevent damage to the device under overload or short-circuit conditions. This function is monitored by an internal sensing circuit. If the output current reaches the OC threshold, such as in case of an output short to GND, a peak current limit is triggered, which by default shuts down the channel in latch mode. Users can also select an auto-recovery mode for different applications. The RTQ9128DL-QA supports four programmable levels, which can be configured using two bits in the registers at addresses 0xB2 and 0xB3.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0xB2	1	7:6	RW	HS_OC_SEL_1	CH1 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		5:4	RW	HS_OC_SEL_4	CH4 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		3:2	RW	HS_OC_SEL_3	CH3 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		1:0	RW	HS_OC_SEL_2	CH2 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0xB3	1	7:6	RW	LS_OC_SEL_1	CH1 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		5:4	RW	LS_OC_SEL_4	CH4 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		3:2	RW	LS_OC_SEL_3	CH3 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		1:0	RW	LS_OC_SEL_2	CH2 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01

15.34 DC Offset Detection

During normal operation, the amplifier circuit continuously monitors the DC offset. If the DC offset exceeds a specified threshold, the channel is placed in the Hi-Z state, a fault is reported to the I^2C register, and the FAULTB pin is activated. Optionally, register bits can be configured to mask this fault report to the FAULTB pin. This monitoring is crucial for protecting the loudspeaker from DC at the output. The detection method involves analyzing the DC at the final PWM stage, calculating the difference between the PWM output and a sinc filter to determine the DC level. The IC will automatically shut down upon detecting excessive DC.

15.35 Global Over-Temperature Warning (OTWG) and Over-Temperature Protection (OTPG)

The device offers four over-temperature warning levels (see the Register Map section for threshold values). When the junction temperature surpasses a warning level, the WARNB pin is activated unless the mask bit in the pin control register (address 0x19) is configured to disable this alert. The device operates normally until it reaches the OTSD threshold, at which point it places all channels in Hi-Z state and activates the FAULTB pin. By default, the device remains deactivated until the temperature normalizes. However, this behavior can be modified to automatic recovery by setting bits 2 and 0 in the miscellaneous control register (address 0x0D). Upon normalization of the junction temperature, the device automatically resumes operation and restores the channels to the configurations specified in the state control register. It is important to note that, even with automatic recovery enabled, the FAULTB pin stays active until the CLEAR FAULT bit (bit 1) in the register (address 0x11) is activated.

15.36 Channel Over-Temperature Warning (OTWC) and Over-Temperature Protection (OTPC)

In addition to the Global Over-Temperature Warning (OTWG) and Over-Temperature Protection (OTPG), each output channel has individual over-temperature warning and protection functions. If any channel exceeds the OTW threshold, the corresponding bit in the warning register (address 0x14) will be set, and the WARNB pin will be activated unless the mask bit is configured to disable reporting. If the channel temperature exceeds the OTSD threshold, the channel enters Hi-Z state and remains in that state. Alternatively, it can automatically return to the state indicated by the status

control register when the temperature drops below the OTW threshold, depending on the setting of bit 0 in the miscellaneous control register (address 0x0D).

15.37 Undervoltage (UV) and Power-On-Reset (POR)

The RTQ9128DL-QA monitors the PVDD voltage threshold. When the voltage at the PVDDL/R pin drops below the programmable undervoltage threshold of 4V, the Undervoltage Protection (UVP) circuit immediately shuts down the output. This device can also be configured to operate in latch mode instead.

When the DVDD voltage is set to 3.3V, the DVDD UVP is configured to 2.3V. If the DVDD operating voltage is 1.8V, then the VR_DIG pin must also be supplied with 1.8V, and the register must be configured to lower the DVDD UVP to 1.4V.

15.38 Overvoltage (OV) and Load Dump

The RTQ9128DL-QA monitors the voltage thresholds of the PVDD and VBAT pins. When the voltage on the PVDDL/R pin or the VBAT pin rises above the overvoltage threshold of 21.5V, the OVP circuit immediately shuts down the output. The device can then operate in auto-recovery mode or be configured to use latch mode.

15.39 Clip Detection

Clip detection is reported on the WARNB pin if a 100% duty-cycle PWM is sustained for a minimum number of PWM cycles as set by the Clip Window Register (address 0x73). The default setting is 20 PWM cycles.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x73	1	3:0	RW	CLIP_DET_SEL	Clipping detect threshold, release threshold (unit: PWM cycle) 4'b0000: 1, 0 4'b0001: 5, 3 4'b0010: 10, 5 4'b0011: 20, 5 (default) 4'b0100: 50, 30 4'b0101: 100, 80 4'b0110: 150, 130 Others: 250, 230	0011

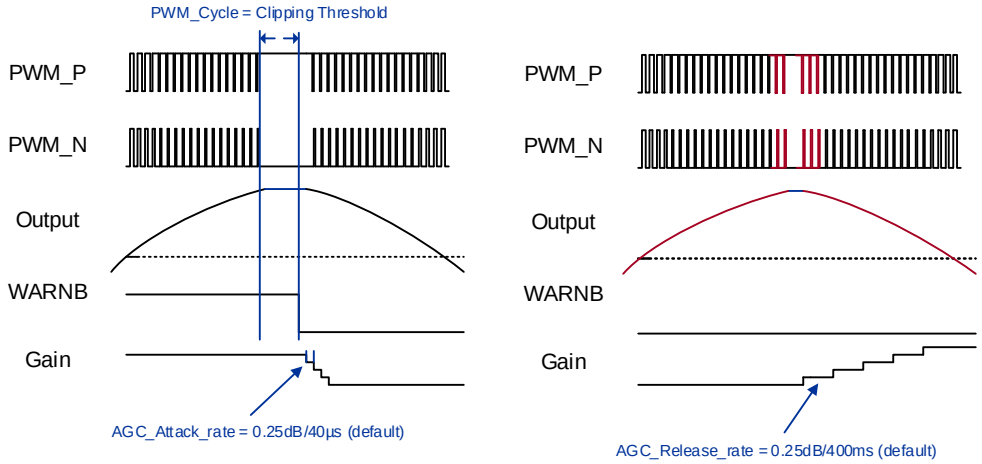


Figure 19. Clip Detection

15.40 Thermal Fold-Back (TFB)

The RTQ9128DL-QA features built-in Thermal Fold-Back Protection (TFP), which is activated when the average junction temperature exceeds a specified threshold. TFP decreases the amplifier gain to reduce power dissipation, maintaining the junction temperature around the threshold level. The device will not completely switch off but will remain operational at lower output power levels. If the average junction temperature continues to rise, a second built-in temperature protection threshold will shut down the amplifier completely.

15.41 Parallel BTL Operation (PBTL)

The RTQ9128DL-QA can drive more current to the load side of the LC output filter by paralleling the BTL channels. For parallel operation, the Parallel BTL (PBTL) mode must be used, and both parallel channels must have the same status in the status control register. If the statuses are inconsistent, the device will report a fault condition. To set a channel to PBTL mode, the device must be in standby mode for the command to take effect. PBTL channels support load diagnosis but cannot be paralleled on the load side of the LC output filter.

15.42 Recommended Operating Conditions

The RTQ9128DL-QA is designed for specific application conditions. It supports speakers with a typical impedance of 4Ω and a minimum impedance of 2Ω.

Minimum Speaker Load Impedance		
Min	**Typ**	**Max**
2Ω	4Ω	--

Based on the internal settings of the RTQ9128DL-QA and the LDMOS parameters, recommended application ranges are provided for the corresponding loaded speaker impedance and PVDD voltage.

Speaker Load	**PVDD Range**		
R_L (Ω)	**Min**	**Typ**	**Max**
2	4.5V	--	14.5V
≥3	4.5V	--	18V

It is recommended that the inductance value of the loaded speaker not exceed 10mH.

Minimum Speaker Load Impedance		
Min	**Typ**	**Max**
--	--	10mH

15.43 Line Driver

The RTQ9128DL-QA output supports a wide range of impedances, from a few ohms for speakers to several kiloohms, making it ideal for external amplifier inputs. The external amplifier input configuration must have a differential impedance ranging from 600Ω to 4.7kΩ.

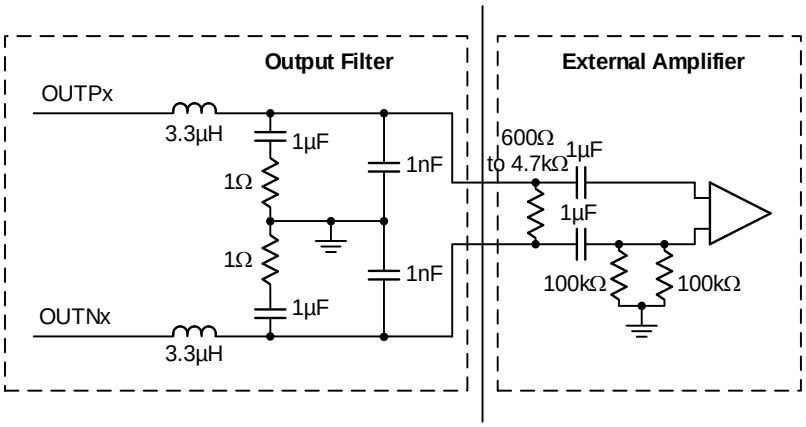


Figure 20. Output Filter

15.44 Demodulation Filter Design

The amplifier output is driven by high-current LDMOS transistors in an H-bridge configuration. These transistors are either fully cut off or fully conducting. As a result, the output signal is a square wave with a duty cycle proportional to the amplitude of the audio signal. An LC demodulation filter is used to recover the audio signal, attenuating the high-frequency components of the output signal outside the audio band. The design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, the choice of inductors used in the output filter should be carefully considered to meet the system's THD+N requirements. The RTQ9128DL-QA requires an additional damping filter to avoid LC filter resonance and ensure low idle current consumption. The schematic for the typical recommended LC output filters is shown in Figure 21.

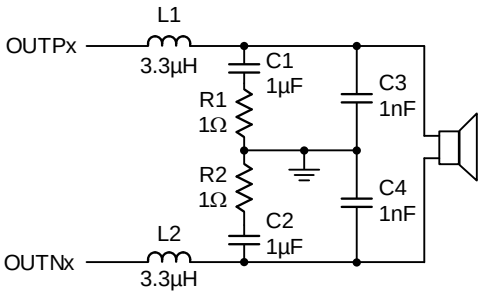


Figure 21. Output Filter

Additional EMI improvements can be achieved by adding snubber networks from each of the Class-D outputs to ground. Suggested values for a simple RC series snubber network are 5.1Ω in series with a 390pF capacitor. However, the design of the snubber network is specific to each application and must consider the parasitic reactance of the printed circuit board and the audio amplifier. Be cautious to evaluate the stress on the components in the snubber network, especially if the amplifier is operating at high PVDD. Additionally, ensure the layout of the snubber network is tight and returns directly to the GND pins on the IC.

15.45 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a RLQFP-64L 10x10 (PP) package, the thermal resistance, θ_{JA}, is 57.45°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (150°C - 25°C) / (57.45°C/W) = 2.18W for a RLQFP-64L 10x10 (PP) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 22 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

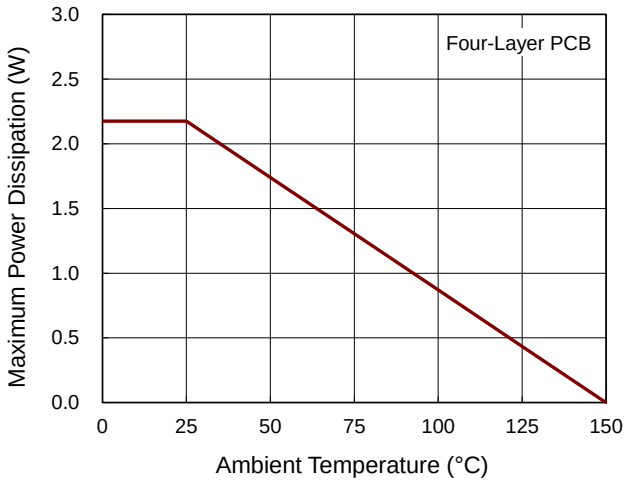
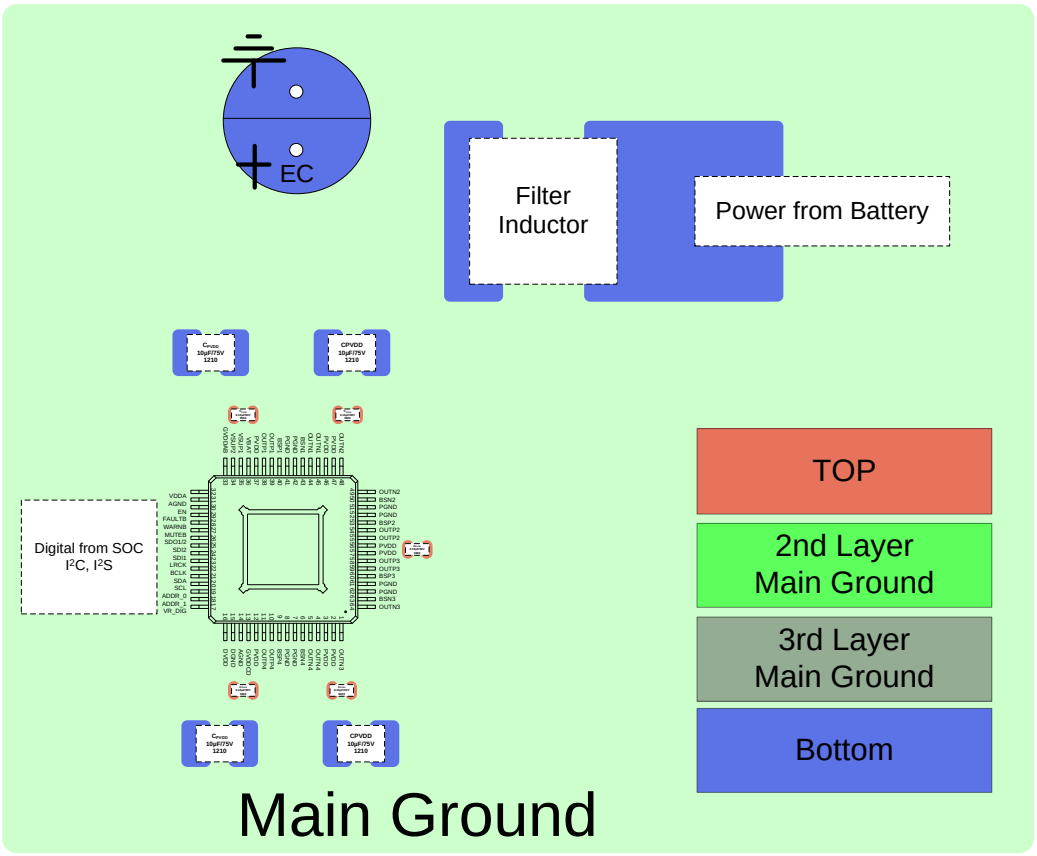


Figure 22. Derating Curve of Maximum Power Dissipation

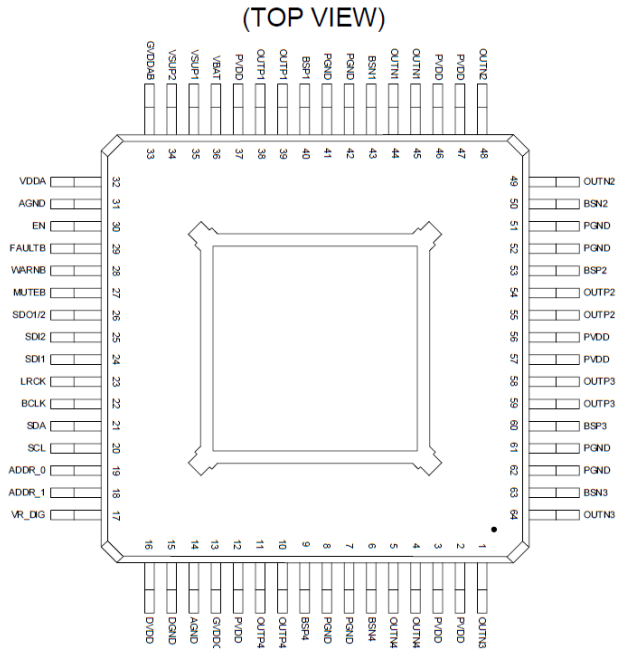
15.46 Layout Considerations

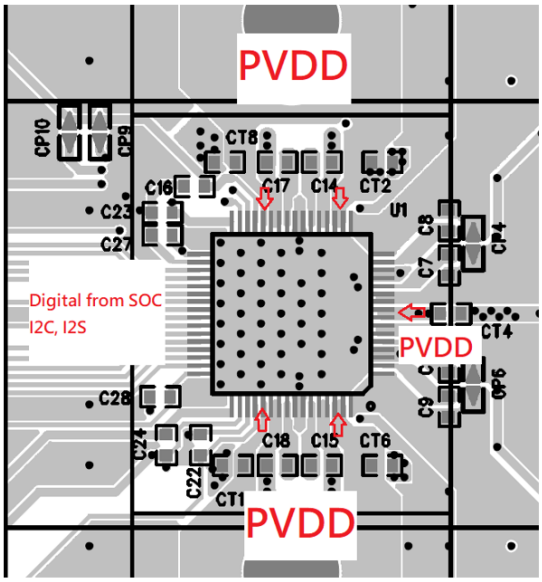
For the best performance of the RTQ9128DL-QA, the following PCB layout guidelines must be strictly followed.

1. The application of RTQ9128DL-QA will require the heat sink. Therefore, the height limit of the mechanism must be considered. For example, the height of MLCC, electrolytic capacitors, and filter inductors may prevent the heat sink from fitting the IC package. It is recommended that these components be placed on the bottom layer of the EVB.

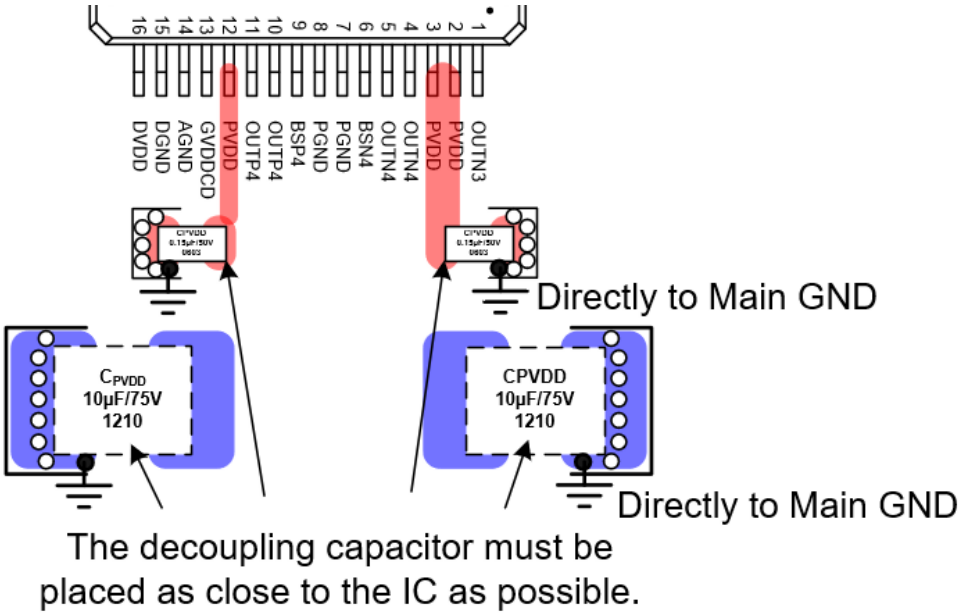


2. In the RTQ9128DL-QA pin configuration, the digital signal pin and the power pin have been separated. Digital signal traces and power traces must be separated, and layout traces should not cross. The trace from VSYS or battery to the PVDD pin must be wide enough to meet the current demand.

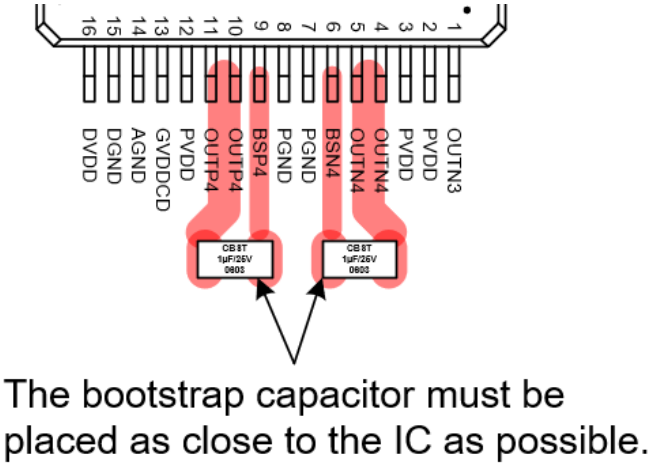




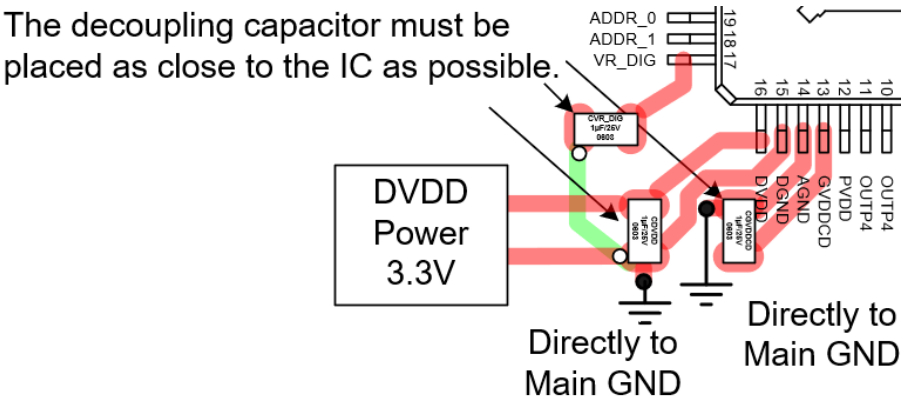
3. Pins 2, 3, 12, 37, 46, 47, 56, and 57 are PVDD power pins for the 4-CH Class-D structure application. Place the filter capacitors as close as possible to the PVDD pins and use the shortest possible traces to connect these capacitors. Capacitors with smaller capacitance should be placed near the PVDD pins. To reduce parasitic inductance and resistance, use multiple vias to connect to the main ground. The optimal approach is to use vias that are directly connected to the Main GND. Before making this connection, ensure that the vias are isolated to prevent unintended connections with other grounds.



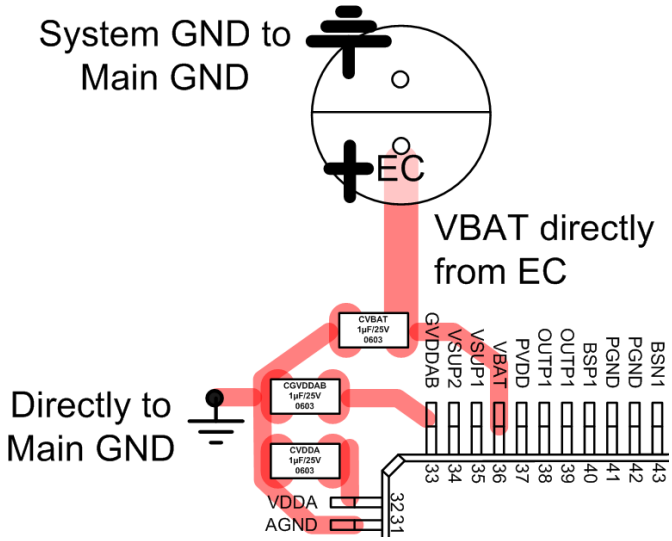
4. To ensure the upper MOSFET turns on normally, place a bootstrap capacitor between the OUT and BSP pins. Position this capacitor as close as possible to the pins for optimal performance. The application circuit requires a total of eight capacitors. Refer to the placement diagram below for details.



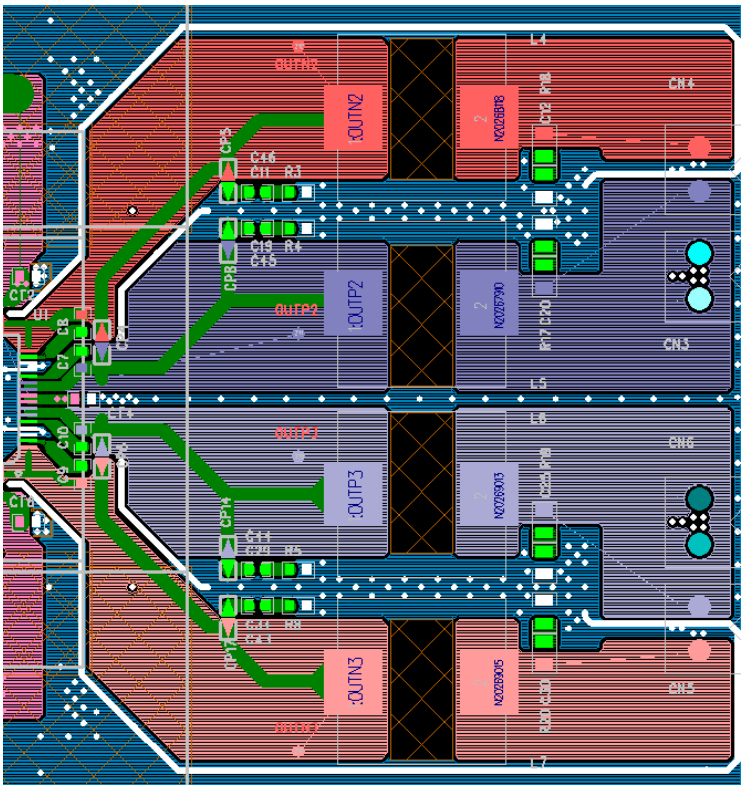
5. The ground defined by the GVDDCD pin is AGND, and the placement of the capacitor is shown in the figure below. The AGND pin trace should first connect to the ground terminal of the capacitor, and then use a via (a conductive hole that connects different layers of the PCB) to connect to the Main GND. To achieve good audio quality, the ground connection of decoupling capacitors (VDDD caps) should be linked to DGND first before connecting to the main ground. Similarly, the VR_DIG decoupling capacitor ground connection should be linked to DGND, and then use a via to connect to the Main GND.



6. The ground defined by the VBAT, GVDDAB, and VDDA pins is AGND, and the placement of the capacitor is shown in the figure below. The AGND pin trace should first connect to the ground terminal of the capacitor, and then use a via to connect to the Main GND. The VBAT pin must be separated from PVDD using a star connection and routed separately from the electrolytic capacitor on the battery path to CVBAT.



7. The traces for OUTP and OUTN should have equal widths and lengths to ensure balanced performance. When using a ferrite bead filter, place it close to the chip for optimal EMI performance. It is recommended to position ground vias around the output traces to enhance grounding effectiveness.



8. Due to the many external traces, the ground of the RTQ9128DL-QA is connected to the Main GND using vias. Copper can be placed under the IC, and additional GND vias can be used to better connect the PGND pin on the top layer to the Main GND. This approach can also increase the heat dissipation area.

Note 9. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

16 Functional Register Description

16.1 Register Map

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x00	1	7:6	RW	CH1_SI	00: CH1 to CH1 (default) 01: CH2 to CH1 10: Ch3 to CH1 11: CH4 to CH1	00
		5:4	RW	CH2_SI	00: CH1 to CH2 01: CH2 to CH2 (default) 10: Ch3 to CH2 11: CH4 to CH2	01
		3:2	RW	CH3_SI	00: CH1 to CH3 01: CH2 to CH3 10: Ch3 to CH3 (default) 11: CH4 to CH3	10
		1:0	RW	CH4_SI	00: CH1 to CH4 01: CH2 to CH4 10: Ch3 to CH4 11: CH4 to CH4 (default)	11

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x01	1	7:6	RW	I2S_DO_LEN	I²S data out length 00: 16bits 01: 24bits 10: 32bits (default) 11: Reserved	10
		5	RW	TDM_CH12_SEL	TDM CH12 receive data select 0: Receive from I²S data 1 (default) 1: Receive from I²S data 2	0
		4	RW	TDM_CH34_SEL	TDM CH34 receive data select 0: Receive from I²S data 1 1: Receive from I²S data 2 (default)	1
		3:0	RW	SDO_SEL	I²S/LJ/RJ/DSPM 0000: No output (default) 0001: I2S_DATAI_1 0010: I2S_DATAI_2 0100: Interface output CH1, CH2 0101: Interface output CH3, CH4 0110: DSP output CH1, CH2 0111: DSP output CH3, CH4 1000: DF output CH1, CH2 1001: DF output CH3, CH4 Others: No output TDM 0000: No output (default) 0001: I2S_DATAI_1 0010: I2S_DATAI_2 010X: Interface output CH1, CH2, CH3, CH4 011X: DSP output CH1, CH2, CH3, CH4 100X: DF output CH1, CH2, CH3, CH4 Others: No output	0000
0x02	1	7	RW	BCLK_EDGE_SEL	0: LRCK transition align with BCLK falling (default) 1: LRCK transition align with BCLK rising	0
		6	RW	SDO_EDGE_SEL	I²S data out launch edge selection 0: BCLK_EDGE_SEL = 0, launch with falling edge (default) 1: BCLK EDGE_SEL = 0, launch with rising edge	0
		5:4	RW	AUD_BITS	00: 16 bits 01: 18 bits 10: 20 bits 11: 24 bits (default)	11
		3	RW	TDM_DSP_OFFSET	TDM or DSPM offset selection 0: Without offset (DSPMB) 1: 1 bit clock offset (DSPMA) (default)	1
		2:0	RW	AUD_FMT	000: I²S (default) 001: Left-Justified 010: Right-Justified 011: DSP mode 1xx: TDM mode	000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x03	1	7	RW	Reserved	Reserved	0
		6	RW	EN_DC_LOAD_DET	Execute DC load diagnostics before amp on sequence 0: Disable 1: Enable (default)	1
		5	RW	PBTL12	CH1, CH2 operation mode 0: BTL (default) 1: PBTL	0
		4	RW	PBTL34	CH3, CH4 operation mode 0: BTL (default) 1: PBTL	0
		3	RW	I2S_DEG_EN	I^2S data deglitch time selection 0: No deglitch 1: 2T deglitch (default)	1
		2:0	RW	SPK_GAIN_SEL	Speaker gain selection 000: −6dB (0.5x) 001: 0dB (1x) 010: 6dB (2x) 011: 12dB (4x) (default) 100: 15dB (5.5x) 101: 18dB (8x) Others: Reserved	011
0x04	1	7:6	RW	CH1_STATE	CH1 mode 00: Normal 01: Hi-Z (default) 10: MUTE 11: ULQM mode	01
		5:4	RW	CH2_STATE	CH2 mode 00: Normal 01: Hi-Z (default) 10: MUTE 11: ULQM mode	01
		3:2	RW	CH3_STATE	CH3 mode 00: Normal 01: Hi-Z (default) 10: MUTE 11: ULQM mode	01
		1:0	RW	CH4_STATE	CH4 mode 00: Normal 01: Hi-Z (default) 10: MUTE 11: ULQM mode	01

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x05	1	7	RW	Reserved	Reserved	0
		6:4	RW	PWM_FREQ	PWM frequency selection 000: 8*fs 001: 10*fs 010: 40*fs 011: 44*fs (default) 100: 48*fs Others: Reserved	011
		3	RW	Reserved	Reserved	0
		2:0	RW	OUT_PHASE_2	CH2 output phase offset 000: 0 degree 001: 45 degree (default) 010: 90 degree 011: 135 degree 100: 180 degree 101: 225 degree 110: 270 degree 111: 315 degree	001
0x06	1	7	RW	Reserved	Reserved	0
		6:4	RW	OUT_PHASE_3	CH3 output phase offset 000: 0 degree 001: 45 degree 010: 90 degree (default) 011: 135 degree 100: 180 degree 101: 225 degree 110: 270 degree 111: 315 degree	010
		3	RW	Reserved	Reserved	0
		2:0	RW	OUT_PHASE_4	CH4 output phase offset 000: 0 degree 001: 45 degree 010: 90 degree 011: 135 degree (default) 100: 180 degree 101: 225 degree 110: 270 degree 111: 315 degree	011

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x07	1	7	R/W	FSS_EN	Spread spectrum enable 0: Disable (default) 1: Enable	0
		6	R/W	PWM_ MODEWHITE	Noise select 0: Pink noise (default) 1: White noise	0
		5	R/W	PWM_ SELCOEF	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal. It is not recommended to modify it. 0: 1/2 (default) 1: 1/4	0
		4	R/W	PWM_NOISE _EN	Add noise to TRI_GEN 0: Disable (default) 1: Enable	0
		3:2	R/W	NOISE_AMP	Nosie amplitude for SSC 00: 6.3% (default) 01: 11.7% 10: 17.1% 11: 35.1%	00
		1:0	R/W	FSS_AMP	Spread spectrum frequency variation amplitude 00: 14.73% 01: 22.5% (default) 10: 22.5% 11: 30.35%	01
0x08	1	7	RW	HPF_EN	High-Pass filter enabled 0: Disable 1: Enable (default)	1
		6	RW	COMP_EN	Compensation filter enable 0: Disable (default) 1: Enable	0
		5	RW	DRC_EN	DRC enabled 0: Disable (default) 1: Enable	0
		4	RW	DRC_N_EN	DRC Noise Gate enabled 0: Disable (default) 1: Enable	0
		3	RW	HARD_CLIP_ EN	Hard clip enabled 0: Disable (default) 1: Enable	0
		2	RW	DRE_EN	DRE enabled 0: Disable 1: Enable (default)	1
		1	RW	DRC_PEAK	DRC mode selection 0: RMS mode 1: Peak mode (default)	1
		0	RW	MS_MUTE	1: Master soft mute	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x09	1	7:3	RW	Reserved	Reserved	0000
		2	RW	DRC_GAIN_HYS_EN	0: DRC gain hysteresis disable 1: DRC gain hysteresis enable (default) Gain release condition is gain difference ≥ 0.125dB	1
		1	RW	COMP_SHARE	Compensation filter common coefficients selection 0: CH1/CH2 share CH1 coefficients, CH3/CH4 share CH3 coefficients 1: All channel share CH1 coefficients (default)	1
		0	RW	COEF_PAGE_SEL	DSP Coefficient page selection for mixer (0x40 to 0x43)/compensation (0x4C to 0x4F) 0: Setting for CH1/CH2 (default) 1: Setting for CH3/CH4	0
0x0A	1	7	RW	SKIP_RAMP	Skip volume ramp 0: Disable (default) 1: Enable	0
		6	RW	FAST_RAMP_MUTE	Mute pin fast mute, mute time < 1ms 0: Normal ramp time (default) 1: Fast mute time	0
		5	RW	MUTE_MODE	Mute pin behavior 0: Mute only (default) 1: Enter ULQM	0
		4:2	RW	Reserved	Reserved	000
		1:0	RW	VOL_RAMP_MODE	Volume Slew step control 00: 1 step in every sample 01: mute → −40dB, every sample with1 step. −40dB → 24dB, 2 samples with 1 step. (default) 10: mute → −40dB, 2 samples with 1 step. −40dB → 24dB, 4 samples with 1 step. Others: Mute → −40dB, 4 samples with 1 step. −40dB → 24dB, 8 samples with 1 step.	01
0x0B	1	7:5	RW	Reserved	Reserved	000
		4	RW	FAULT_B_TYPE	0: Recovery type 1: Latch type (default)	1
		3:0	RW	RCVRY_TIME	Power stage auto-recovery time 0000: 100ms 0001: 150ms 0010: 300ms (default) 0011: 450ms 0100: 600ms 0101: 750ms 0110: 900ms 0111: 1050ms 1000: 1200ms 1001: 1350ms Others: 1500ms	0010

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x0C	1	7:3	RW	Reserved	Reserved	00000
		2	RW	I2S_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
		1	RW	UVP_DVDD_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
		0	RW	UVP_VBAT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
0x0D	1	7	RW	OVP_VBAT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
		6	RW	UVP_VDDA_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
		5	RW	UVP_PVDD_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
		4	RW	OVP_PVDD_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
		3	RW	UVP_GVDD_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
		2	RW	OTPG_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
		1	RW	OCPC_TYPE	Fault behavior type select. 0: Auto-recovery 1: Latch (default)	1
		0	RW	OTPC_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x0E	1	7:4	RW	Reserved	Reserved	0000
		3	RW	I2C_TIMEOUT_TIME_SEL	I^2C timeout timing selection 0: 100ms (default) 1: 150ms	0
		2	RW	I2C_TIMEOUT_TYPE_SEL	I^2C timeout check pin type 0: SCL & SDAO both keep low start timeout counting 1: SDAO keep low start timeout counting (default)	1
		1	RW	I2C_TIME_OUT_SEL	I^2C timeout reset selection 0: Reset I^2C IP only (default) 1: Reset whole chip	0
		0	RW	I2C_TIME_OUT_EN	I^2C timeout function: If SDA & SCL remain low for 100ms, an I^2C timeout reset will occur. Bit 0 of register 0x05 is a reset option to select the reset block. Bit 1 of register 0x05 is used to enable the I^2C timeout function. 0: Disable 1: Enable (default)	1
0x0F	1	7:0	R	ERR_INT_INDEX	Report ERR_INT summary from ERR_INT0 (0x10) to ERR_INT7 (0x17)	00000001
0x10	1	7:6	RW	Reserved	Reserved	00
		5	RWC	PWM_ERR	PWM frequency setting error under sampling rate (0x06, 0x20) 0: PWM is supported (default) 1: PWM is not supported (write 0 to clear)	0
		4:3	RWC	ADS_ERR	Address R detection error {ADDR_1, ADDR_0} 0: R detect correct (default) 1: R detect error (write 0 to clear flag)	00
		2	RWC	POR	Power-on reset 0: Normal 1: Warning (write 0 to clear) (default)	1
		1	RWC	BCLK_ERR	0: No BCLK error (default) 1: BCLK error, write 0 to clear flag	0
		0	RWC	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write0 to clear flag	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x11	1	7	RWC	VDDA_UV	VDDA UVP 0: Normal (default) 1: Fault (write 0 to clear)	0
		6	RWC	GVDDAB_UV	GVDDAB UVP 0: Normal (default) 1: Fault (write 0 to clear)	0
		5	RWC	GVDDCD_UV	GVDDCD UVP 0: Normal (default) 1: Fault (write 0 to clear)	0
		4	RWC	DVDD_UV	DVDD UVP 0: Normal (default) 1: Fault (write 0 to clear)	0
		3	RWC	VBAT_UV	VBAT UVP 0: Normal (default) 1: Fault (write 0 to clear)	0
		2	RWC	VBAT_OV	VBAT OVP 0: Normal (default) 1: Fault (write 0 to clear)	0
		1	RWC	OTPG	Global OTP 0: Normal (default) 1: Fault (write 0 to clear)	0
		0	RWC	OTWG	Global OT warning 0: Normal (default) 1: Warning (write 0 to clear)	0
0x12	1	7:6	RWC	PVDD_UV	PVDD UVP {AB, CD} 0: Normal (default) 1: Fault (write 0 to clear)	00
		5:4	RWC	PVDD_OV	PVDD OVP {AB, CD} 0: Normal (default) 1: Fault (write 0 to clear)	00
		3:0	RWC	DCP	Output DC detected flag {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
0x13	1	7:4	RWC	OTPC	Channel OTP {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
		3:0	RWC	OCPC	Channel OCP {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
0x14	1	7:4	RWC	OTWC	Channel OT Warning {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Warning (write 0 to clear)	0000
		3:0	RWC	BS_LOW	Channel boost low {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Warning (write 0 to clear)	0000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x15	1	7:4	RWC	CLIP	Clip detection {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Warning (write 0 to clear)	0000
		3	RWC	ILIMIT_Flag_4	Current limit flag CH4 0: Normal (default) 1: Warning (write 0 to clear)	0
		2	RWC	ILIMIT_Flag_3	Current limit flag CH3 0: Normal (default) 1: Warning (write 0 to clear)	0
		1	RWC	ILIMIT_Flag_2	Current limit flag CH2 0: Normal (default) 1: Warning (write 0 to clear)	0
		0	RWC	ILIMIT_Flag_1	Current limit flag CH1 0: Normal (default) 1: Warning (write 0 to clear)	0
0x16	1	7:4	RWC	S2P	Output short to power {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
		3:0	RWC	S2G	Output short to ground {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
0x17	1	7:4	RWC	OL	Output open load {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
		3:0	RWC	SL	Positive output shorting to negative output {CH4, CH3, CH2, CH1} 0: Normal (default) 1: Fault (write 0 to clear)	0000
0x18	1	7:6	RW	Reserved	Reserved	00
		5	RW	MASK_PWM_ERR	Fault mask for PWM setting error 0: Not mask (default) 1: Mask	0
		4:1	R	Reserved		0000
		0	RW	MASK_I2S_FAULT	Fault mask for BCLK and LRCK error 0: Not mask (default) 1: Mask	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x19	1	7	RW	MASK_UV_VDDA	Fault mask for VDDA UV 0: Not mask (default) 1: Mask	0
		6	RW	MASK_UV_GVAB	Fault mask for GVAB UV 0: Not mask (default) 1: Mask	0
		5	RW	MASK_UV_GVCD	Fault mask for GVCD UV 0: Not mask (default) 1: Mask	0
		4	RW	MASK_UV_DVDD	Fault mask for DVDD UV 0: Not mask (default) 1: Mask	0
		3	RW	MASK_UV_VBAT	Fault mask for VBAT UV 0: Not mask (default) 1: Mask	0
		2	RW	MASK_OV_VBAT	Fault mask for VBAT OV 0: Not mask (default) 1: Mask	0
		1	RW	MASK_OTPG	Fault mask for OTPG 0: Not mask (default) 1: Mask	0
		0	RW	MASK_OTWG	Fault mask for OTWG 0: Not mask (default) 1: Mask	0
0x1A	1	7:6	RW	MASK_UV_PVDD	Fault mask for PVDD UV {AB, CD} 0: Not mask (default) 1: Mask	00
		5:4	RW	MASK_OV_PVDD	Fault mask for PVDD OV {AB, CD} 0: Not mask (default) 1: Mask	00
		3:0	RW	MASK_DCP	Fault mask for DCP {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
0x1B	1	7:4	RW	MASK_OTPC	Fault mask for OTPC {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
		3:0	RW	MASK_OCPC	Fault mask for OCPC {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
0x1C	1	7:4	RW	MASK_OTWC	Fault mask for OTWC {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
		3:0	RW	MASK_BS_LOW	Fault mask for BST_LOW {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x1D	1	7:4	RW	MASK_CLIP	Fault mask for chip detection {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
		3:0	RW	MASK_ILIMIT	Fault mask for current limit {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
0x1E	1	7:4	RW	MASK_S2P	Fault mask for S2P {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
		3:0	RW	MASK_S2G	Fault mask for S2G {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
0x1F	1	7:4	RW	MASK_OL	Fault mask for OL {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
		3:0	RW	MASK_SL	Fault mask for SL {CH4, CH3, CH2, CH1} 0: Not mask (default) 1: Mask	0000
0x20	1	7	R	PWM_ STATUS	PWM status 0: Sampling rate vs. PWM frequency is supported (default) 1: Sampling rate vs. PWM frequency is not supported	0
		6:4	R/RW	SR_MODE	Sampling rate: manual or auto-detected. SR_AUTO_DET enabled: SR_MODE reports result. SR_AUTO_DET disabled: Set SR_MODE manually. 100: 32kHz 101: 44.1/48kHz (default) 110: 88.2/96kHz Others: Reserved	101
		3:0	R/RW	BCLK_MODE	BCLK mode: manual or auto-detected. SR_AUTO_DET enabled: BCLK_MODE reports result. SR_AUTO_DET disabled: Set BCLK_MODE manually. 0000: BCLK = 32fs 0001: BCLK = 48fs 0010: BCLK = 64fs (default) 0011: BCLK = 96fs 0100: BCLK = 128fs Others: Reserved	0010

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x21	1	7:6	RW	Reserved	Reserved	00
		5:0	RW	TDM_TX_LOC_CH1	TDM start transmitting location select for CH1 000000: Start from 0+offset (default) 000001: Start from 8+offset … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000000
0x22	1	7:6	RW	Reserved	Reserved	00
		5:0	RW	TDM_TX_LOC_CH2	TDM start transmitting location select for CH2 000000: Start from 0+offset 000001: Start from 8+offset … 000011: Start from 24+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000011
0x23	1	7:6	RW	Reserved	Reserved	00
		5:0	RW	TDM_TX_LOC_CH3	TDM start transmitting location select for CH3 000000: Start from 0+offset 000001: Start from 8+offset … 000110: Start from 48+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000110
0x24	1	7:6	RW	Reserved	Reserved	00
		5:0	RW	TDM_TX_LOC_CH4	TDM start transmitting location select for CH4 000000: Start from 0+offset 000001: Start from 8+offset … 001001: Start from 72+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	001001
0x25	1	7:6	RW	Reserved	Reserved	00
		5:0	RW	TDM_RX_LOC_CH1	TDM start receiving location select for CH1 000000: Start from 0+offset (default) 000001: Start from 8+offset … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x26	1	7:6	RW	Reserved	Reserved	00
		5:0	RW	TDM_RX_LOC_CH2	TDM start receiving location select for CH2 000000: Start from 0+offset 000001: Start from 8+offset … 000011: Start from 24+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000011
0x27	1	7:6	RW	Reserved	Reserved	00
		5:0	RW	TDM_RX_LOC_CH3	TDM start receiving location select for CH3 000000: Start from 0+offset 000001: Start from 8+offset … 000110: Start from 48+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000110
0x28	1	7:6	RW	Reserved	Reserved	00
		5:0	RW	TDM_RX_LOC_CH4	TDM start receiving location select for CH4 000000: Start from 0+offset 000001: Start from 8+offset … 001001: Start from 72+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	001001
0x29	1	7:4	RW	HPF_EN_CH	High-pass filter enabled {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable	0000
		3:0	RW	COMP_EN_CH	Compensation filter enabled {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable	0000
0x2A	1	7:4	RW	DRC_EN_CH	Dynamic range control (DRC) enabled {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable	0000
		3:0	RW	DRC_N_EN_CH	DRC Noise Gate enabled {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable	0000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x2B	1	7:4	RW	HARD_CLIP_EN_CH	Hard clip enabled {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable	0000
		3:0	RW	DRE_EN_CH	DRE enabled {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable	0000
0x30	2	15:11	RW	Reserved	Reserved	00000
		10:0	RW	MS_VOL	Master Volume control 11'h000: 24dB 11'h180: 0dB 11'h7FF: Mute (default) 0.0625dB per step	11'h7FF
0x31	2	15:11	RW	Reserved	Reserved	00000
		10:0	RW	CH1_VOL	CH1 Volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180
0x32	2	15:11	RW	Reserved	Reserved	00000
		10:0	RW	CH2_VOL	CH2 Volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180
0x33	2	15:11	RW	Reserved	Reserved	00000
		10:0	RW	CH3_VOL	CH3 Volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180
0x34	2	15:11	RW	Reserved	Reserved	00000
		10:0	RW	CH4_VOL	CH4 Volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180
0x35	2	15:11	RW	Reserved	Reserved	00000
		10:0	RW	HC_TH	Hard clip threshold when HARD_CLIP_EN = 1 > 0dB is not allowable for hard clip threshold setting 11'h180: 0dB (default) 0.0625db per step	11'h180

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x40	3	23:11	RW	Reserved	Reserved	13'h0000
		10:0	RW	DRC_TH	DRC threshold 11'h000: 0dB (default) 11'h180: −24dB 11'h67E: −103.875dB 11'h67F to 11'h7FF: not available 0.0625dB per step	11'h000
0x41	3	23:11	RW	Reserved	Reserved	13'h0000
		10:0	RW	DRC_ OFFSET	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: −103.9375dB 0.0625dB per step	11'h180
0x42	3	23:8	RW	Reserved	Reserved	16'h0000
		7:0	RW	DRC_RATIO	DRC compress ratio 8'h00: No compression 8'h80 (default) ~ 8'hFF: Full compression 1/128 per step	8'h80
0x43	3	23:11	RW	Reserved	Reserved	13'h0000
		10:0	RW	DRC_NG_TH	Noise gate threshold 11'h000: 0dB 11'h180: -24dB 11'h640: −100dB (default) 11'h67E: −103.875dB 11'h67F to 11'h7FF: Not available 0.0625dB per step	11'h640
0x44	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	DRC_AE	DRC_AE	17'h0_8000
0x45	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	DRC_1_AE	DRC_1_AE	17'h0_0000
0x46	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	DRC_AD	DRC_AD	17'h0_8000
0x47	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	DRC_AA	DRC_AA	17'h0_8000
0x48	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	COMP_B0	Compensation filter coefficient B0, COEF_PAGE_SEL (0x09) select CH12 or CH34	17'h0_8000
0x49	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	COMP_B1	Compensation filter coefficient B1, COEF_PAGE_SEL (0x09) select CH12 or CH34	17'h0_0000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x4A	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	COMP_B2	Compensation filter coefficient B2, COEF_PAGE_SEL (0x09) select CH12 or CH34	17'h0_0000
0x4B	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	COMP_B3	Compensation filter coefficient B3, COEF_PAGE_SEL (0x09) select CH12 or CH34	17'h0_0000
0x4C	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	CH13_MIX_0	Channel input mixer coefficient 0, COEF_PAGE_SEL (0x09) select CH1 or CH3	17'h0_8000
0x4D	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	CH13_MIX_1	Channel input mixer coefficient 1, COEF_PAGE_SEL (0x09) select CH1 or CH3	17'h0_0000
0x4E	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	CH24_MIX_0	Channel input mixer coefficient 0, COEF_PAGE_SEL (0x09) select CH2 or CH4	17'h0_0000
0x4F	3	23:17	RW	Reserved	Reserved	0000000
		16:0	RW	CH24_MIX_1	Channel input mixer coefficient 1, COEF_PAGE_SEL (0x09) select CH2 or CH4	17'h0_8000
0x51	1	7:4	RW	SL_TH_CH1	CH1 SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω Others: Reserved	0001
		3:0	RW	SL_TH_CH2	CH2 SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω Others: Reserved	0001
0x52	1	7:4	RW	SL_TH_CH3	CH3 SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω Others: Reserved	0001
		3:0	RW	SL_TH_CH4	CH4 SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω Others: Reserved	0001

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x53	1	7:4	RW	EN_DC_DET	DC load detection enable {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable After the command is executed, the value is returned to 0, and the command is set to 1 to enable DC load detection.	0000
		3:0	R	DC_DET_DONE	DC load detection done flag after enabling DC load detection {CH4, CH3, CH2, CH1} 0: DC load detection do not executed or do not finished 1: DC load detection finishes (default)	1111
0x54	1	7:5	RW	Reserved	Reserved	000
		4:0	RW	AC_PHI	Generated signal frequency: 00: No signal 01: Set 1 = 1kHz, 02: set 2 = 2kHz, …, set 17 = 23kHz 13: Set 19kHz (default) 18~1F: Reserved	5'h13
0x55	1	7:4	RW	EN_AC_DET	AC load detection enable {CH4, CH3, CH2, CH1} 0: Disable (default) 1: Enable	0000
		3:0	R	AC_DET_DONE	AC detection done flag after enabling AC load detection {CH4, CH3, CH2, CH1} 0: AC_PHASE_R and AC_PHASE_I keep the last result if ever enabling detection 1: AC_PHASE_R and AC_PHASE_I is valid (default)	1111
0x5C	4	31:16	R	AC_MAG_1	Report CH1 magnitude	16'd0
		15:0	R	AC_PHA_1	Report CH1 phase	16'd0
0x5D	4	31:16	R	AC_MAG_2	Report CH2 magnitude	16'd0
		15:0	R	AC_PHA_2	Report CH2 phase	16'd0
0x5E	4	31:16	R	AC_MAG_3	Report CH3 magnitude	16'd0
		15:0	R	AC_PHA_3	Report CH3 phase	16'd0
0x5F	4	31:16	R	AC_MAG_4	Report CH4 magnitude	16'd0
		15:0	R	AC_PHA_4	Report CH4 phase	16'd0
0x60	4	31:0	R	AC_INT_R_1	Report the real part of CH1 internal phase	32'd0
0x61	4	31:0	R	AC_INT_I_1	Report the imaginary part of CH1 internal phase	32'd0
0x62	4	31:0	R	AC_SPK_R_1	Report the real part of CH1 speaker phase	32'd0
0x63	4	31:0	R	AC_SPK_I_1	Report the imaginary part of CH1 speaker phase	32'd0
0x64	4	31:0	R	AC_INT_R_2	Report the real part of CH2 internal phase	32'd0
0x65	4	31:0	R	AC_INT_I_2	Report the imaginary part of CH2 internal phase	32'd0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x66	4	31:0	R	AC_SPK_R_2	Report the real part of CH2 speaker phase	32'd0
0x67	4	31:0	R	AC_SPK_I_2	Report the imaginary part of CH2 speaker phase	32'd0
0x68	4	31:0	R	AC_INT_R_3	Report the real part of CH3 internal phase	32'd0
0x69	4	31:0	R	AC_INT_I_3	Report the imaginary part of CH3 internal phase	32'd0
0x6A	4	31:0	R	AC_SPK_R_3	Report the real part of CH3 speaker phase	32'd0
0x6B	4	31:0	R	AC_SPK_I_3	Report the imaginary part of CH3 speaker phase	32'd0
0x6C	4	31:0	R	AC_INT_R_4	Report the real part of CH4 internal phase	32'd0
0x6D	4	31:0	R	AC_INT_I_4	Report the imaginary part of CH4 internal phase	32'd0
0x6E	4	31:0	R	AC_SPK_R_4	Report the real part of CH4 speaker phase	32'd0
0x6F	4	31:0	R	AC_SPK_I_4	Report the imaginary part of CH4 speaker phase	32'd0
0x70	1	7	RW	Reserved	Reserved	0
		6	RW	EN_OTPC	Channel OT protection enabled 0: Disable 1: Enable (default)	1
		5	RW	EN_OTWC	Channel OT warning enabled 0: Disable 1: Enable (default)	1
		4	RW	EN_UVOVOT	Enable UV/OV/OT 0: Disable 1: Enable (default)	1
		3	RW	EN_ILIMIT	Enable current limit function 0: Disable 1: Enable (default)	1
		2	RW	EN_DC_PROT	DC protection enabled 0: Disable 1: Enable (default)	1
		1	RW	EN_CLIP_DET	Clip detection enabled 0: Disable 1: Enable (default)	1
		0	RW	EN_BS_PROT	Boot low protection enabled 0: Disable 1: Enable (default)	1

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x71	1	7:6	RW	UV_DV_SEL	DVDD UV threshold selection 00: 1.4V 01: 1.5V 10: 2.1V 11: 2.3V (default)	11
		5	RW	DC_UVP_CAL_EN	PVDD UVP re-calibration dc offset enabled 0: Disable (default) 1: Enable	0
		4	RW	UV_RAMP_DOWN	PVDD UV protection behavior 0: HZ_PROT directly (default) 1: Power-off sequence	0
		3	RW	GAIN_CTRL_SEL	Gain control selection for TFC/AGC/IAGC 0: Channel 12 is separated from Channel 34 Channel 12 will be active at the same time. Channel 34 will be active at the same time. 1: 4 channel active at the same time (default)	1
		2	RW	EN_OTW_TFC	Enable thermal fold-back 0: Disable (default) 1: Enable	0
		1	RW	EN_ILIMIT_AGC	Enable auto gain control for current limit detection 0: Disable 1: Enable (default)	1
		0	RW	EN_CLIP_AGC	Enable auto gain control for CLIP detection 0: Disable (default) 1: Enable	0
0x72	1	7	RW	BS_LOW_SEL	Boot low protection threshold selection 0: 3V (default) 1: 3.5V	0
		6:4	RW	UV_VBAT_SEL	Battery UV threshold selection 000: 4V (default) 001: 6.12V 010: 8.88V 011: 11.1V 100: 12.67V 101: 15.26V 110: 19.71V 111: 21.5V	000
		3	RW	Reserved	Reserved	0
		2:0	RW	UV_PVDD_SEL	PVDD UV threshold selection 000: 4V (default) 001: 6.12V 010: 8.88V 011: 11.1V 100: 12.67V 101: 15.26V 110: 19.71V 111: 21.5V	000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x73	1	7:6	RW	OTPG_SEL	Global OTP threshold selection 00: 160°C (default) 01: 170°C 10: Reserved 11: Reserved	00
		5:4	RW	OTPC_SEL	Channel OTP threshold selection 00: 160°C 01: 170°C (default) 10: Reserved 11: Reserved	01
		3:0	RW	CLIP_DET_SEL	Clip detect threshold, release threshold (unit: PWM cycle) 0000: 1, 0 0001: 5, 3 0010: 10, 5 0011: 20, 5 (default) 0100: 50, 30 0101: 100, 80 0110: 150, 130 Others: 250, 230	0011
0x74	1	7:6	RW	TFC_ATTACK_RATE	Thermal Fold-Back attack rate 00: 0.0625dB/25ms (default) 01: 0.0625dB/50ms 10: 0.0625dB/100ms 11: 0.0625dB/200ms	00
		5:4	RW	TFC_RELEASE_RATE	Thermal Fold-Back release rate 00: 0.0625dB/50ms (default) 01: 0.0625dB/100ms 10: 0.0625dB/200ms 11: 0.0625dB/400ms	00
		3:2	RW	AGC_ATTACK_RATE	AGC attack time selection for AGC and IAGC 00: 0.25dB/20μs 01: 0.25dB/40μs (default) 10: 0.25dB/80μs 11: 0.25dB/160μs	01
		1:0	RW	AGC_RELEASE_RATE	AGC release time selection for AGC and IAGC 00: 0.25dB/200ms 01: 0.25dB/400ms (default) 10: 0.25dB/800ms 11: 0.25dB/1600ms	01
0x75	1	7:6	RW	Reserved	Reserved	00
		5:4	RW	OC_HZ_DELAY_SEL	HZ delay time after OCP is triggered. 00: 1.5ms 01: 3.4ms (default) 10: 8.8ms 11: 21.5ms	01
		3:0	RO	Reserved	Reserved	1111

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x76	1	7:5	RW	Reserved	Reserved	000
		4	RW	DC_DET_REF_TIME	DC offset detection reference time strobe 0: Follow sampling rate (default) 1: PLL divide down to 16kHz	0
		3	RW	DC_DET_MODE	DC offset detection mode 0: Detect DC every (detection time) 1: Consecutively 8 times of (detection time/8) (default)	1
		2	RW	DC_TIME_SEL	DC offset detection time 0: 342ms (default) 1: 684ms	0
		1:0	RW	DC_TH	DC offset detection threshold at PWM frequency = 384kHz 00: No available 01: 12.5% (default) 10: 18.75% 11: 25% For example, DC offset = PVDD x DC offset detection threshold → DC offset = 14.4V x 12.5% = 1.8V	01
0x80	1	7:6	RW	Reserved	Reserved	00
		5	RW	ADC_CKSEL	ADC clock selection when VT sense & DC load detection 0: 192kHz 1: 384kHz (default)	1
		4	RW	ADC_AVG_SEL	VT sense & DC load detection average method, only support ADC_CKSEL = 1 0: Average 2 samples 1: Average 8 samples (default)	1
		3:2	RW	ADC_CHP_FREQ	ADC chopper frequency selection 00: div 64 01: div 32 10: div 16 11: div 8 (default)	11
		1	RW	ADC_DITH_EN	ADC dither enabled 0: Disable (default) 1: Enable	0
		0	RW	ADC_CHP_EN	ADC chopper enable 0: Disable (default) 1: Enable	0
0x81	1	7:4	RW	ADC_G_PVDD	The median value offset of ADC gain at PVDD sense	1101
		3:0	RW	ADC_G_TEMP	The median value offset of ADC gain at temperature sense	0000
0x82	1	7	RW	Reserved	Reserved	0
		6:0	RW	ADC_G_DC	The median value offset of ADC gain at DC load detection	0000000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x83	1	7:5	RW	Reserved	Reserved	000
		4:0	RW	ADC_G_AC	The median value offset of ADC gain at AC load detection	00000
0x84	1	7:6	RW	Reserved	Reserved	00
		5:4	RW	R_SPSG_GAIN_ADC_SEL	ADC PGA gain for DC load short to power/ground 00: 1x (default) 01: 4x 1x: 8x	00
		3:2	RW	R_OLSLAC_GAIN_ADC_SEL	ADC PGA gain for DC load open/short load and AC load 00: 1x (default) 01: 4x 1x: 8x	00
		1	RW	IDAC_IMAX_SEL	0: 1.5mA (−6dB) (default) 1: 3mA (0dB)	0
		0	RW	LDET_GAIN_MANUAL	Load detection manual mode 0: Gain select from IDAC_IMAX_SEL (default) 1: AC gain select from MS_VOL; DC gain select from IDAC_VEC_MSB/IDAC_VEC_SSB	0
0x85	1	7:1	RW	Reserved	Reserved	0000000
		0	RW	DC_RAMP_TIME	DC load detection ramp time 0: 1.28ms (default) 1: 2.56ms (ramp from 0.9V to 1.2V)	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x86	1	7	RW	AC_BIT	Phase resolution within computation stage 0: 16-bit 1: 32-bit (default)	1
		6	RW	AC_SETTLE_TIME	AC load detection settle time 0: 1ms (default) 1: 2ms	0
		5:4	RW	AC_DFT_DELAY	Delay to start computing AC phase 00: Delay 1ms (48*1 samples) (default) 01: Delay 2ms (48*2 samples) 10: Delay 5ms (48*5 samples) 11: Delay 10ms (48*10 samples)	00
		3:2	RW	AC_LOOP_MODE	AC load detection loop-back mode 00: ADC output: analog loop-back and then speaker detection (default) 01: ADC output: analog loop-back and then still analog loop-back 10: Generated sine (0x51), ignore analog path 11: Down-sampled digital filter output, ignore analog path	00
		1	RW	AC_INT_PHASE	Digital internal built-in phase enabled 0: Disable, phase 90 (generated sine) (default) 1: Enable, phase 0 (generated cosine)	0
		0	RW	AC_OFS_GAIN_EN	AC load detection ADC offset-gain function 0: Disable 1: Enable (default)	1
0x87	1	7	RW	EN_VDDA5	Enable VDDA5 0: Disable 1: Enable (default)	1
		6	RW	EN_GVAB	Enable GVDDAB 0: Disable 1: Enable (default)	1
		5	RW	EN_GVCD	Enable GVDDCD 0: Disable 1: Enable (default)	1
		4	RW	EN_UV_DV	Enable DVDD UV detection 0: Disable 1: Enable (default)	1
		3:0	RW	EN_PWR	Enable power stage {CH4, CH3, CH2, CH1} 0: Disable 1: Enable (default)	1111
0x88	1	7:4	RW	EN_SCDAC	Enable DAC for Channel {CH4, CH3, CH2, CH1} 0: Disable 1: Enable (default)	1111
		3:0	RW	EN_TRI	Enable triangle generator {CH4, CH3, CH2, CH1} 0: Disable 1: Enable (default)	1111

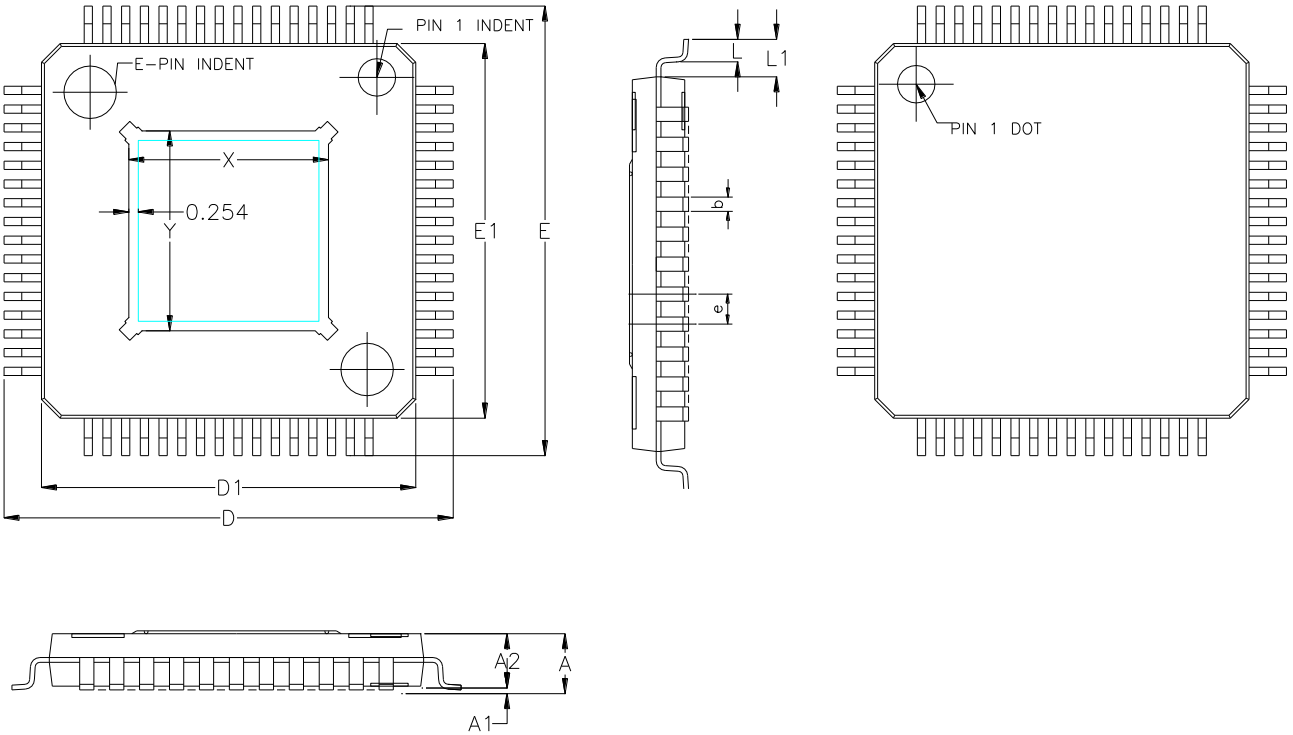
ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x89	1	7:4	RW	EN_SPK	Enable SPK for Channel {CH4, CH3, CH2, CH1} 0: Disable 1: Enable (default)	1111
		3	RW	Reserved	Reserved	0
		2	RW	VDDA5_SEL	VDDA5 voltage selection 0: 5V (default) 1: 5.5V	0
		1	RW	GVDD_SEL	GVDD_AB/CD voltage selection 0: 5V (default) 1: 5.5V	0
		0	RW	SEQ_TIME_SEL	Power down to Disable LDO time select 0: 10ms (default) 1: 20ms	0
0x8A	1	7:6	RW	D_KDC_QC_TIME	KDC unity-gain time option 00: 25µs 01: 50µs (default) 10: 200µs 11: 1ms	01
		5	RW	Reserved	Reserved	0
		4	RW	PVDD_SET_TIME	0: 2ms 1: 16ms (default)	1
		3:2	RW	SPK_SST	SPK start-up time 00: 2.5ms 01: 5ms (default) 10: 10ms 11: 20ms	01
		1:0	RW	D_KDC_CMP_TIME	KDC compare time option 00: 25µs 01: 50µs (default) 10: 200µs 11: 1ms	01
0x8B	1	7:3	RW	Reserved	Reserved	00000
		2:0	RW	R_DC_LOAD_ADC_SEL	DC load ADC report selection 000: 0 (default) 001: S2PG channel P 010: S2PG channel N 011: OLSL channel offset 100: OLSL channel data 101: OLSL channel data - offset	000
0x8C	2	15:00	R	RDC_LOAD_ADC_RPT_CH1	DC load ADC report data	16'd0
0x8D	2	15:00	R	RDC_LOAD_ADC_RPT_CH2	DC load ADC report data	16'd0
0x8E	2	15:00	R	RDC_LOAD_ADC_RPT_CH3	DC load ADC report data	16'd0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x8F	2	15:00	R	RDC_LOAD_ADC_RPT_CH4	DC load ADC report data	16'd0
0x90	2	16	R	SENSE_PVDDAB	PVDDAB sense code	16'd0
0x91	2	15:0	R	SENSE_PVDDCD	PVDDCD sense code	16'd0
0x92	2	15:0	R	SENSE_VBAT	VBAT sense code	16'd0
0x93	2	15:0	R	SENSE_TEMP_G	Global temperature sense code	16'd0
0x94	2	15:0	R	SENSE_TEMP_1	CH1 Temperature sense code	16'd0
0x95	2	15:0	R	SENSE_TEMP_2	CH2 Temperature sense code	16'd0
0x96	2	15:0	R	SENSE_TEMP_3	CH3 Temperature sense code	16'd0
0x97	2	15:0	R	SENSE_TEMP_4	CH4 Temperature sense code	16'd0
0x98	4	31:16	R	AC_INT_MAG_1	Report CH1 internal magnitude	16'd0
		15:0	R	AC_INT_PHA_1	Report CH1 internal phase	16'd0
0x99	4	31:16	R	AC_SPK_MAG_1	Report CH1 speaker magnitude	16'd0
		15:0	R	AC_SPK_PHA_1	Report CH1 speaker phase	16'd0
0x9A	4	31:16	R	AC_INT_MAG_2	Report CH2 internal magnitude	16'd0
		15:0	R	AC_INT_PHA_2	Report CH2 internal phase	16'd0
0x9B	4	31:16	R	AC_SPK_MAG_2	Report CH2 speaker magnitude	16'd0
		15:0	R	AC_SPK_PHA_2	Report CH2 speaker phase	16'd0
0x9C	4	31:16	R	AC_INT_MAG_3	Report CH3 internal magnitude	16'd0
		15:0	R	AC_INT_PHA_3	Report CH3 internal phase	16'd0
0x9D	4	31:16	R	AC_SPK_MAG_3	Report CH3 speaker magnitude	16'd0
		15:0	R	AC_SPK_PHA_3	Report CH3 speaker phase	16'd0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x9E	4	31:16	R	AC_INT_MAG_4	Report CH4 internal magnitude	16'd0
		15:0	R	AC_INT_PHA_4	Report CH4 internal phase	16'd0
0x9F	4	31:16	R	AC_SPK_MAG_4	Report CH4 speaker magnitude	16'd0
		15:0	R	AC_SPK_PHA_4	Report CH4 speaker phase	16'd0
0xA5	1	7:4	RW	Reserved	Reserved	0001
		3:2	RW	SPK_CMH_MODE	At heavy load, SPK SW mode: 00: BD mode (default) 10: CMH mode Others: Reserved	00
		1:0	RW	SPK_CMH_DUTY	At 0dBFS input amplitude, SPK SW duty cycle: 00: 50% (default) 10: 25% Others: Reserved	00
0xB2	1	7:6	RW	HS_OC_SEL_1	CH1 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		5:4	RW	HS_OC_SEL_4	CH4 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		3:2	RW	HS_OC_SEL_3	CH3 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		1:0	RW	HS_OC_SEL_2	CH2 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0xB3	1	7:6	RW	LS_OC_SEL_1	CH1 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		5:4	RW	LS_OC_SEL_4	CH4 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		3:2	RW	LS_OC_SEL_3	CH3 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
		1:0	RW	LS_OC_SEL_2	CH2 OC protection threshold selection 00: 6.5A 01: 8A (default) 10: 10A 11: Reserved	01
0xB4	1	7:6	RW	ILIMIT_SEL_1	CH1 current limit threshold selection 00: 4.8A 01: 5.8A (default) 10: 7.3A 11: Reserved	01
		5:4	RW	ILIMIT_SEL_4	CH4 current limit threshold selection 00: 4.8A 01: 5.8A (default) 10: 7.3A 11: Reserved	01
		3:2	RW	ILIMIT_SEL_3	CH3 current limit threshold selection 00: 4.8A 01: 5.8A (default) 10: 7.3A 11: Reserved	01
		1:0	RW	ILIMIT_SEL_2	CH2 current limit threshold selection 00: 4.8A 01: 5.8A (default) 10: 7.3A 11: Reserved	01
0xF7	1	7	RW	SR_AUTO_DET	Sampling rate detection enable bit detect sampling rate and BCLK mode 0: Disable, manual set 0x01 SR mode and BCLK mode 1: Enable (default)	1

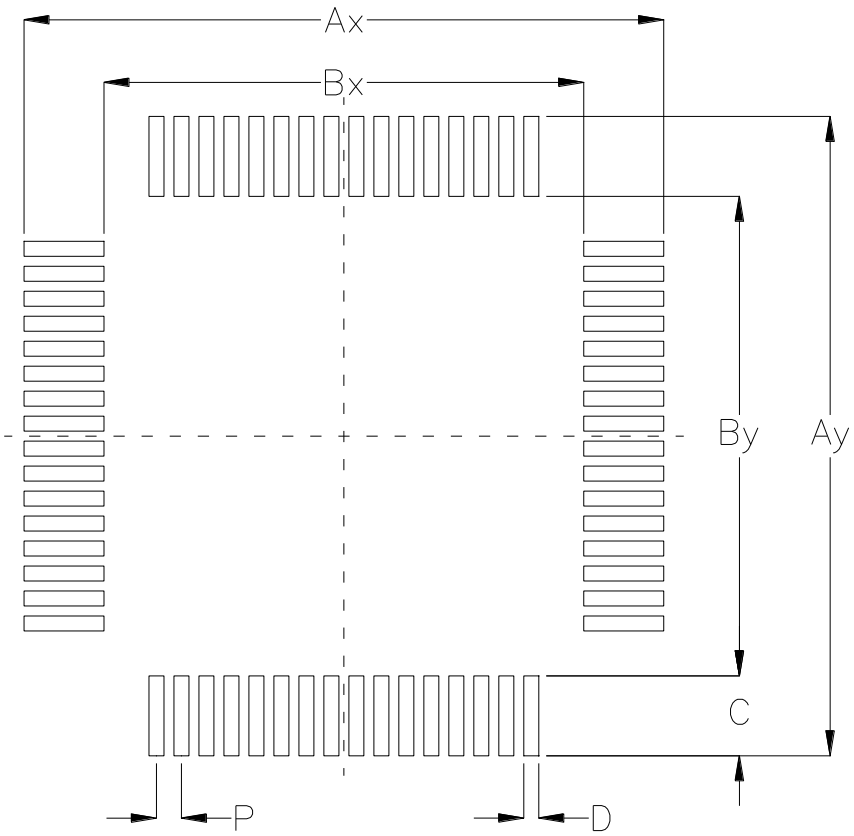
17 Outline Dimension



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	normal	Max	Min	normal	Max
A	1.400	1.500	1.600	0.055	0.059	0.063
A1	0.050	0.100	0.150	0.002	0.004	0.006
A2	1.350	1.400	1.450	0.053	0.055	0.057
b	0.170	0.220	0.270	0.007	0.009	0.011
C	0.090	0.150	0.200	0.004	0.006	0.008
D	11.800	12.000	12.200	0.465	0.472	0.480
E	11.800	12.000	12.200	0.465	0.472	0.480
D1	9.900	10.000	10.100	0.390	0.394	0.398
E1	9.900	10.000	10.100	0.390	0.394	0.398
X	4.675	5.334	5.434	0.184	0.210	0.214
Y	4.675	5.334	5.434	0.184	0.210	0.214
e	0.500			0.020		
L	0.450	0.600	0.750	0.018	0.024	0.030
L1	0.800	1.000	1.200	0.031	0.039	0.047

RLQFP-64L 10x10 (Exposed Pad) Plastic Package

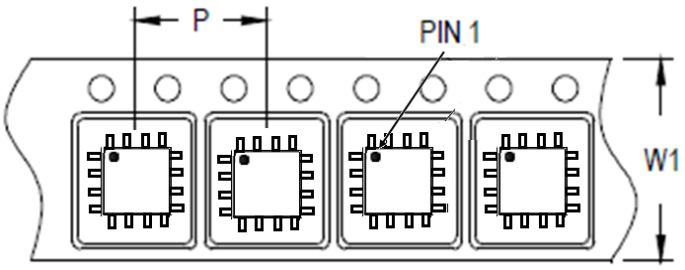
18 Footprint Information

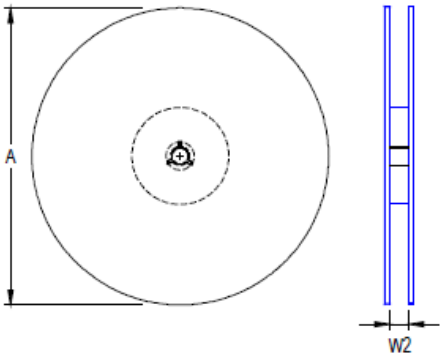


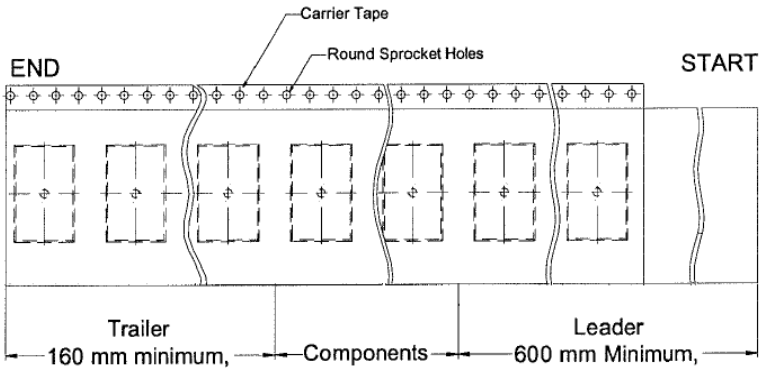
Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P	Ax	Ay	Bx	By	C	D	
RLQFP10x10-64(PP)	64	0.50	12.80	12.80	9.60	9.60	1.60	0.30	±0.05

19 Packing Information

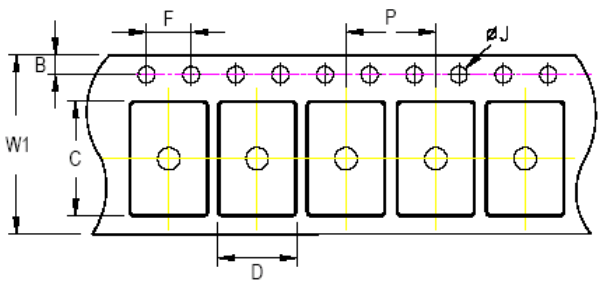
19.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
LQFP10x10	24	16	330	13	1,500	160	600	24.4/26.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 24mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
24mm	24.3mm	15.9mm	16.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	2.1mm	2.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
LQFP10x10	13”	1,500	Box G	1	1,500	Carton A	6	9,000

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

20 Datasheet Revision History

Version	Date	Description	Item
00	2024/7/10	Final	General Description on P1 Ordering Information on P2 Electrical Characteristics on P10 Typical Operating Characteristics on P16, 17, 20 Application Information on P23, 33 Packing Information on P83, 84
01	2025/1/21	Modify	*Feature on page 1* - Changed Clipping Detection to **Clip Detection** - Changed the description of **Load Diagnostics** - Changed the description of **Protection Features** *Absolute Maximum Ratings on page 7* - Added “Refer to the EVB user guide for thermal information, which includes the heat sink.” in Note 4 *Electrical Characteristics on page 8 to 11* - Changed DVDD Shutdown Current EN voltage **Changed from EN = 0.8V to EN = 0V** - Changed PVDD Shutdown Current EN voltage **Changed from EN = 0.8V to EN = 0V** - Changed VBAT Shutdown Current EN voltage **Changed from EN = 0.8V to EN = 0V** - Change Output Attenuation MUTEN voltage **Changed from MUTEB = 0.8V to MUTEB = 0V** - Changed the description of the test conditions for the Overcurrent Limit **Changed Level 1 to OCLIM = 01** **Changed Level 2 to OCLIM = 10** - Changed **PVDD Overvoltage Hysteresis to 0.6** - Changed **VBAT Overvoltage Hysteresis to 0.6** - Updated the output DC fault protection by changing it to **DC Offset Detection** with a new threshold of **0.9V** - Changed the parameter to **Short Load Detection Tolerance** - Removed RMS Output Power Per Channel, PBTL **1Ω, PVDD = 14.4V, THD + N = 1%, T_A = 75°C** **1Ω, PVDD = 14.4V, THD + N = 10%, T_A = 75°C** *Typical Application Circuit on page 13* - Changed the Picture of 2-Channel Parallel Bridge-Tied Load (PBTL) Configuration *Typical Operating Characteristics on page 15 to 21* - Changed all the figures *Application Information on page 35, 37, 42, 44* - Changed the description of 15.20 Hardware Control Pins description from **DC detection to DC offset detection**. - Changed the description of **15.23 Ultra Low Quiescent Mode (ULQM) Mode to Ultra-Low Quiescent Mode (ULQM)** - Changed 15.32 Overcurrent Limit (ILIMIT) table **0xB4 table ILIMIT_SEL_1, changed the description 11 as reserved** **0xB4 table ILIMIT_SEL_4, changed the description 11 as**

Version	Date	Description	Item
			reserved **0xB4 table ILIMIT_SEL_3, change the description 11 as reserved** **0xB4 table ILIMIT_SEL_2, change the description 11 as reserved** - Changed the title of **15.34 DC Offset Detection** *Functional Register Description on page 55, 56, 58, 59, 60, 62, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 76, 77, 78, 80, 81* - Changed 0x03 the R/W, Reg name, Description of BIT 7, Change to Reserved. - Changed 0x05 the R/W, Reg name, Description of BIT 7, BIT 3, changed to Reserved. - Changed 0x06 the R/W, Reg name, Description of BIT 7, BIT 3, changed to Reserved. - Changed 0x09 the R/W, Reg name, Description of BIT 7:3, changed to Reserved. - Changed 0x0A the R/W, Reg name, Description of BIT 4:2, changed to Reserved. - Changed 0x0B the R/W, Reg name, Description of BIT 5:7, change to Reserved. - Changed 0x0C the R/W, Reg name, Description of BIT 7:3, change to Reserved. - Changed 0x0E the R/W, Reg name, Description of BIT 7:4, change to Reserved. - Changed 0x10 the R/W, Reg name, Description of BIT 7:6, change to Reserved. - Changed 0x18 the R/W, Reg name, Description of BIT 7:6, change to Reserved. - Changed 0x21 the R/W, Reg name, Description of BIT 7:6, change to Reserved. - Changed 0x22 the R/W, Reg name, Description of BIT 7:6, change to Reserved. - Changed 0x23 the R/W, Reg name, Description of BIT 7:6, change to Reserved. - Changed 0x24 the R/W, Reg name, Description of BIT 7:6, change to Reserved. - Changed 0x25 the R/W, Reg name, Description of BIT 7:6, change to Reserved. - Changed 0x26 the R/W, Reg name, Description of BIT 7:6, change to Reserved. - Change 0x27 the R/W, Reg name, Description of BIT 7:6, Change to Reserved. - Changed 0x28 the R/W, Reg name, Description of BIT 7:6, change to Reserved. - Changed 0x30 the R/W, Reg name, Description of BIT 15:11, changed to Reserved. - Changed 0x31 the R/W, Reg name, Description of BIT 15:11, changed to Reserved. - Changed 0x32 the R/W, Reg name, Description of BIT 15:11, changed to Reserved. - Changed 0x33 the R/W, Reg name, Description of BIT 15:11, changed to Reserved. - Changed 0x34 the R/W, Reg name, Description of BIT 15:11, changed to Reserved. - Change 0x35 the R/W, Reg name, Description of BIT 15:11,

Version	Date	Description	Item
			changed to Reserved. - Changed 0x40 the R/W, Reg name, Description of BIT 23:11, changed to Reserved. - Changed 0x41 the R/W, Reg name, Description of BIT 23:11, changed to Reserved. - Changed 0x42 the R/W, Reg name, Description of BIT 23:8, changed to Reserved. - Changed 0x43 the R/W, Reg name, Description of BIT 23:11, changed to Reserved. - Changed 0x44 the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x45 the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x46 the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x47 the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x48 the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x49 the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x4A the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x4B the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x4C the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x4D the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x4E the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Changed 0x4F the R/W, Reg name, Description of BIT 23:17, changed to Reserved. - Change the description of 0x53[3:0] - Changed 0x54 the R/W, Reg name, Description of BIT 7:5, changed to Reserved. - Changed 0x70 the R/W, Reg name, Description of BIT 7, changed to Reserved. - Changed 0x72 the R/W, Reg name, Description of BIT 3, changed to Reserved. - Changed 0x73 the R/W, Reg name, Description of BIT 7:6, changed to Reserved. - Changed 0x80 the R/W, Reg name, Description of BIT 7:6, changed to Reserved. - Changed 0x82 the R/W, Reg name, Description of BIT 7, changed to Reserved. - Changed 0x83 the R/W, Reg name, Description of BIT 7:5, changed to Reserved. - Changed 0x76 the R/W, Reg name, Description of BIT 7:5, changed to Reserved. - Changed the description of 0x76[4], 0x76[3], 0x76[2], 0x76[1] - Changed 0x84 the R/W, Reg name, Description of BIT 7:5, changed to Reserved. - Changed 0x85 the R/W, Reg name, Description of BIT 7:1, changed to Reserved. - Changed 0x89 the R/W, Reg name, Description of BIT 3, changed

Version	Date	Description	Item
			to Reserved. - Changed 0x8A the R/W, Reg name, Description of BIT 5, changed to Reserved. - Changed 0x8B the R/W, Reg name, Description of BIT 7:3, changed to Reserved. - Changed 0XA5 the R/W, Reg name, Description of BIT 7:4, changed to Reserved. - Changed 0XB4[7:6], 0XB4[5:4], 0XB4[3:2], 0XB4[1:0], changed to 11: Reserved.