RICHTEK®

RTQ2533E

3A, 6.5V, Low-Noise, Low-Dropout Linear Regulator

1 General Description

The RTQ2533E is a high-current (3A), low-noise (6.8μV_{RMS}), high accuracy (1% over line, load, and temperature), low-dropout linear regulator (LDO) capable of sourcing 3A with an extremely low dropout (maximum 180mV). The device supports a single input supply voltage as low to 1.1V, which makes it easy to use.

The low-noise, high PSRR, and high output current capability make the RTQ2533E ideal to power noise-sensitive devices such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. With very high accuracy, remote sensing, and soft-start capabilities to reduce inrush current, the RTQ2533E is ideal for powering digital loads such as FPGAs, DSPs, and ASICs.

The external enable control and power good indicator function make the control sequence easier. The output noise immunity is enhanced by adding an external bypass capacitor on the NR/SS pin. The device is fully specified over the temperature range of T_J = –40°C to 125°C and is offered in the VQFN-20L 3.5x3.5 package.

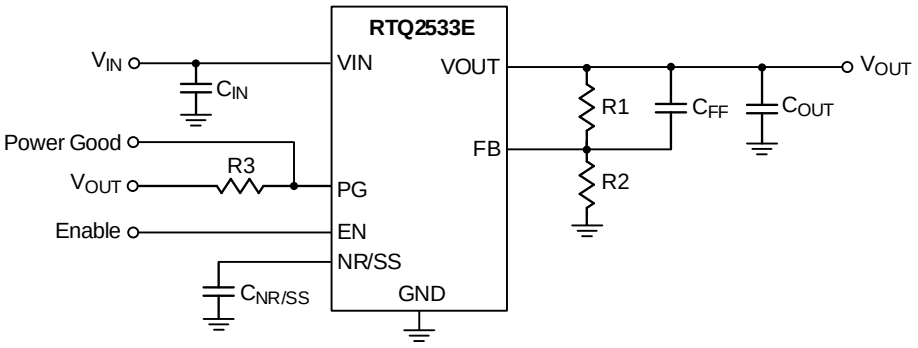
2 Features

- **Input Voltage Range: 1.1V to 6.5V**
- **Two Output Voltage Modes**
  - **0.5 V to 5.5V (Set by a Resistive Divider)**
  - **0.5V to 2.075V (Set via PCB Layout, No External Resistor Required)**
- **Accurate Output Voltage Accuracy (1%) Over Line, Load, and Temperature**
- **PSRR: 44dB at 500kHz**
- **Noise Immunity**
  - **6.8μV_{RMS} at 0.5V Output**
  - **16μV_{RMS} at 5V Output**
- **Dropout Voltage: 180mV Maximum at 3A**
- **Enable Control**
- **Programmable Soft-Start Output**
- **Stable with a 47μF or Larger Ceramic Output Capacitor**
- **Support Power-Good Indicator Function**
- **Junction Temperature Range: –40°C to 125°C**

3 Applications

- Portable Electronic Devices
- Wireless Infrastructures: SerDes, FPGA, DSP
- RF, IF, Components: VCO, ADC, DAC, LVDS

4 Simplified Application Circuit



5 Ordering Information

RTQ2533□□-□□

Packing
B: Pin 1 Orientation
(Quadrant 2, Follow EIA-481)

Product Grade
T: Industrial Grade

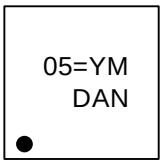
Package Type(1)
N: VQFN-20L 3.5x3.5 (V-Type)

V_{REF}
E: 0.5V_{REF}

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

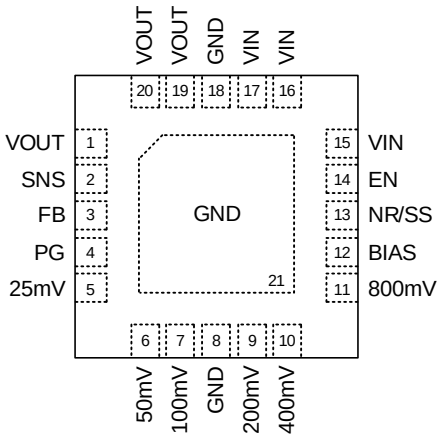


05=: Product Code
YMDAN: Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)



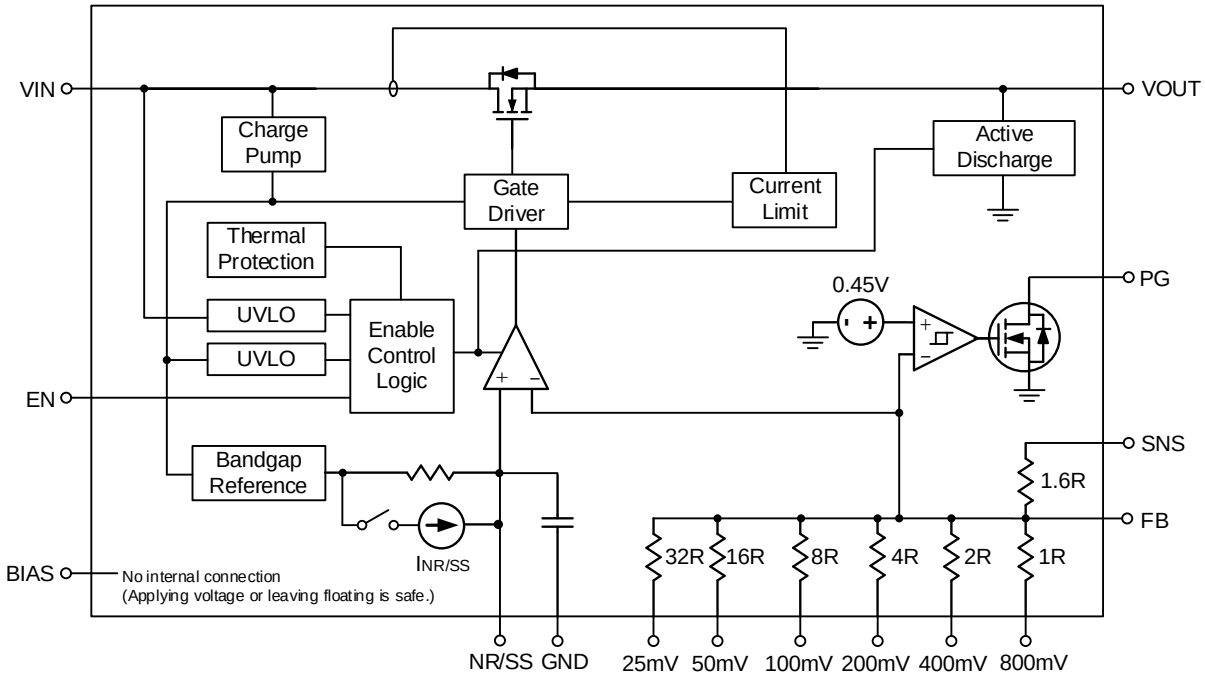
VQFN-20L 3.5x3.5

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 19, 20	VOUT	LDO output pins. A 47µF or larger ceramic capacitor (22µF or greater effective capacitance) is required for stability. Place the output capacitor as close to the device as possible and minimize the impedance between the VOUT pin and the load.
2	SNS	Output voltage sense input pin. Connect this pin only if using the configuration without external resistors. Keep the SNS pin floating if the VOUT voltage is set by an external resistor.
3	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.5V typically.
4	PG	Power good indicator output. This is an open-drain output that is active high when the output voltage reaches 88% of the target. The pin is pulled low when the output voltage is lower than its specified thresholds, including EN shutdown, OCP, and OTP.
5, 6, 7, 9, 10, 11	25mV, 50mV, 100mV, 200mV, 400mV, 800mV	Output voltage setting pins. Connect these pins to the ground or leave floating. Connecting these pins to the ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) if the VOUT voltage is set by an external resistor.
8, 18, 21 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
12	BIAS	This pin has no internal IC connection. A BIAS input voltage below 6.5V can be applied to this pin (for compatibility with other vendors), or this pin can be left open (floating). Either option is safe and will not affect IC's operation.
13	NR/SS	Noise-reduction and soft-start pin. Decoupling this pin to GND with an external capacitor $C_{NR/SS}$ can reduce output noise to very low levels and also slow down the rising of VOUT, providing a soft-start behavior. For low-noise applications, a 10nF to 1µF $C_{NR/SS}$ is suggested.

Pin No.	Pin Name	Pin Function
14	EN	Enable control input. Connecting this pin to a logic high enables the regulator, and driving this pin low puts it into shutdown mode. The device can have V_{IN} and V_{EN} sequenced in any order without causing damage to the device. However, to ensure the soft-start function works as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} is present is preferred.
15, 16, 17	VIN	Supply input. A general 47μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN, PG, EN ---------- –0.3V to 7V
- VOUT ---------- –0.3V to 7V
- NR/SS, FB ---------- –0.3V to 3.6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ---------- 1.1V to 6.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		VQFN-20L 3.5x3.5	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	38.5	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	50.57	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	2.47	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	39.33	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	5.79	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.06	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), (1.1V ≤ V_{IN} ≤ 6.5V and V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.5V, VOUT connected to 50Ω to GND, V_{EN} = 1.1 V, C_{IN} = 10µF, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and the PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.) (Note 7)

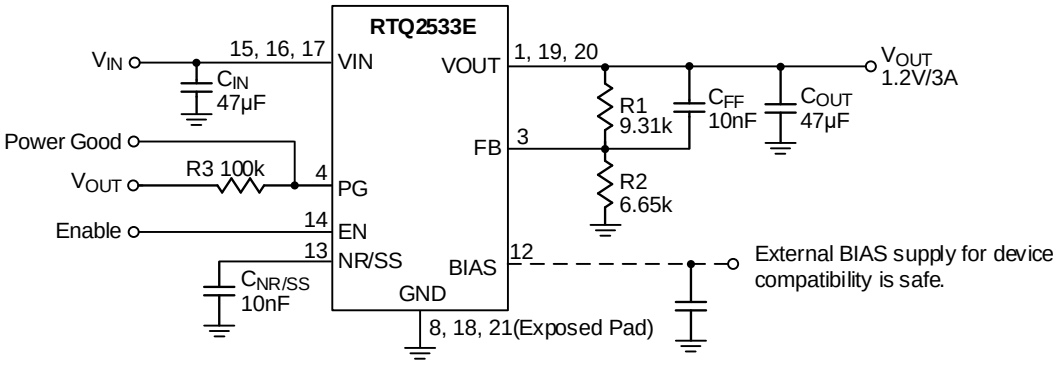
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Supply Input Voltage	V_{IN}		1.1	--	6.5	V
Reference Voltage	V_{REF}		--	0.5	--	V
NR/SS Pin Voltage	$V_{NR/SS}$		--	0.5	--	V
Undervoltage Lockout Rising Threshold	V_{UVLO_R}	V_{IN} increasing	--	1.02	1.085	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	Hysteresis	--	100	--	mV
Output Voltage	V_{OUT}	Using external resistors	0.5	--	5.5	V
		Using voltage setting pins (25mV, 50mV, 100mV, 200mV, 400mV, 800mV)	0.5	--	2.075	
Output Voltage Accuracy (Note 8)	V_{OUT_ACC}	V_{IN} = V_{OUT} + 0.3V, 0.5V ≤ V_{OUT} ≤ 5.5V, 1mA ≤ I_{OUT} ≤ 3A	–1	--	1	%
Line Regulation	V_{LINE_REG}	I_{OUT} = 1mA, 1.1V ≤ V_{IN} ≤ 6.5V	--	0.05	--	%/V
Load Regulation	V_{LOAD_REG}	1mA ≤ I_{OUT} ≤ 3A	--	0.08	--	%/A
Dropout Voltage	V_{DROP}	V_{IN} = 1.1V to 6.5V, I_{OUT} = 3A, V_{FB} = 0.5V – 3%	--	86	180	mV
Current Limit	I_{LIM}	V_{OUT} = 90%$V_{OUT(TARGET)}$, V_{IN} = $V_{OUT(TARGET)}$ + 400mV	3.5	4.2	4.8	A
Short-Circuit Current Limit	I_{SC}	R_{LOAD} = 20mΩ, under foldback operation	--	1	--	A
Ground Pin Current	I_{GND}	Minimum load, V_{IN} = 6.5V, I_{OUT} = 5mA	--	3	4	mA
		Maximum load, V_{IN} = 1.4V, I_{OUT} = 3A	--	4.3	5.5	
Shutdown Current	I_{SHDN}	PG = Open, V_{IN} = 6.5V, V_{EN} = 0.5V	--	1.2	25	µA
EN Pin Current	I_{EN}	V_{IN} = 6.5V, V_{EN} = 0V and 6.5V	–0.1	--	0.1	µA
EN Input Voltage Rising Threshold	V_{EN_R}	Enable device	1.1	--	6.5	V
EN Input Voltage Falling Threshold	V_{EN_F}	Disable device	0	--	0.5	V
Power-Good Voltage Threshold	V_{PG}	For the direction PG signal falling with decreasing VOUT	0.82 x V_{OUT}	0.883 x V_{OUT}	0.93 x V_{OUT}	V
Power-Good Voltage Hysteresis	V_{PG_HYS}	For PG signal rising	--	2% x V_{OUT}	--	V
PG Pin Low- Level Output Voltage	V_{PG_L}	V_{OUT} < V_{PG}, I_{PG} = –1mA (current into device)	--	--	0.4	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
PG Pin Leakage Current	I_{PG_LK}	V_{OUT} > V_{PG}, V_{PG} = 6.5V		--	--	1	μA
NR/SS Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 6.5V		4	--	9	μA
FB Pin Current	I_{FB}	V_{IN} = 6.5V		−100	--	100	nA
Power Supply Rejection Ratio	PSRR	V_{IN} = 1.2V, I_{OUT} = 3A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 47μF//10μF//10μF	f = 10kHz, V_{OUT} = 0.5V	--	48	--	dB
			f = 500kHz, V_{OUT} = 0.5V	--	44	--	
		V_{IN} − V_{OUT} = 0.4V, I_{OUT} = 3A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 47μF//10μF//10μF	f = 10kHz, V_{OUT} = 5V	--	40	--	
			f = 500kHz, V_{OUT} = 5V	--	35	--	
Output Noise	V_N	BW = 10Hz to 100kHz I_{OUT} = 3A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 47μF//10μF//10μF	V_{IN} = 1.1V V_{OUT} = 0.5V	--	6.8	--	μV_{RMS}
			V_{IN} = 3.6V V_{OUT} = 3.3V	--	10	--	
			V_{OUT} = 5V	--	16	--	
Over-Temperature Protection Threshold	T_{OTP}			--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}			--	20	--	

Note 7. $V_{OUT(TARGET)}$ is the expected V_{OUT} value set by the external feedback resistors. The 50Ω load is disconnected when the test conditions specify an I_{OUT} value.

Note 8. External resistor tolerance is not taken into account.

15 Typical Application Circuit



$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) = 0.5V \times \left(1 + \frac{9.31k}{6.65k}\right) = 1.2V$$

Figure 1. Configuration Circuit for V_{OUT} Adjusted by a Resistor Divider.

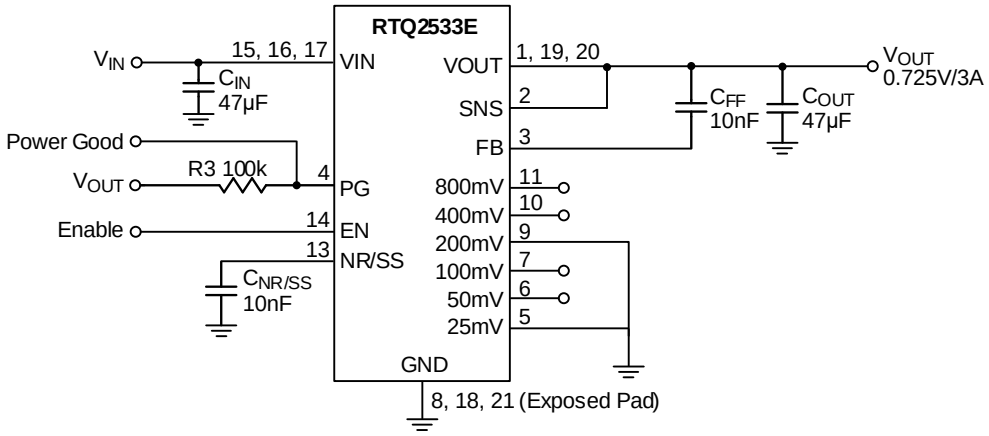
Table 1. Recommended Feedback-Resistor Values

Targeted Output Voltage (V)	Feedback Resistor Values	
	R1 (kΩ)	R2 (kΩ)
0.6	11	54.9
0.7	10.2	25.5
0.75	10	20
0.8	10.7	17.8
0.9	11	13.7
1	9.09	9.09
1.05	11	10
1.1	10.7	8.87
1.2	9.31	6.65
1.5	11	5.49
1.8	10.2	3.92
3.3	10.7	1.91
5	10.2	1.13
5.5	10.2	1.02

Table 2. Recommended External Components

Component	Description	Vendor P/N
C_{FF}, $C_{NR/SS}$	10nF, 50V, X7R, 0603	GRM033R71E103KE14 (Murata)
C_{IN}, C_{OUT} (Note 9)	47µF, 16V, X6S, 1210	GRT32EC81C476KE13L (Murata)

Note 9. Considering the effective capacitance derated with the biased voltage level, the C_{OUT} component needs to satisfy the effective capacitance at least 22µF or above at targeted output level for stable and normal operation.



$V_{OUT} = V_{REF} + 25mv + 200mV = 0.5V + 25mV + 200mV = 0.725V$

(Table 3 provides a full list for different V_{OUT} targets and the corresponding pin settings.)

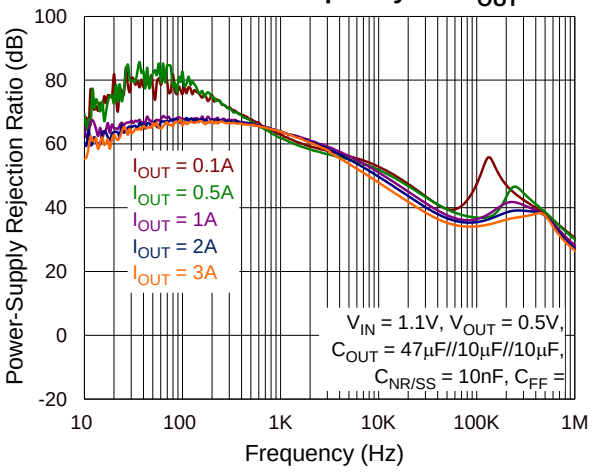
Figure 2. Configuration Circuit for Adjusted V_{OUT} via PCB Layout

Table 3. V_{OUT} Select Pin Settings for Different Targets

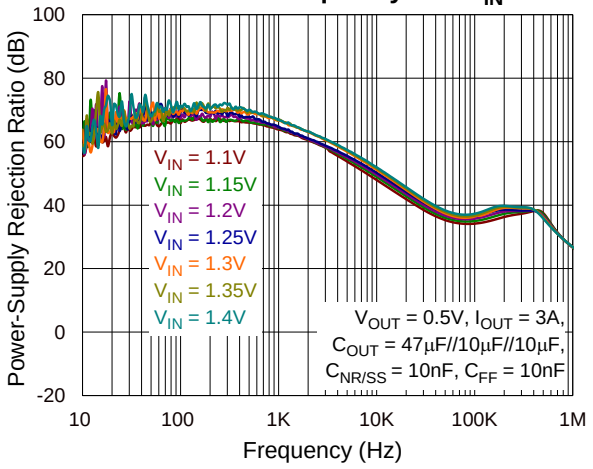
V_{OUT} (V)	25mV	50mV	100mV	200mV	400mV	800mV	V_{OUT} (V)	25mV	50mV	100mV	200mV	400mV	800mV
0.5	Open	Open	Open	Open	Open	Open	1.3	Open	Open	Open	Open	Open	GND
0.525	GND	Open	Open	Open	Open	Open	1.325	GND	Open	Open	Open	Open	GND
0.55	Open	GND	Open	Open	Open	Open	1.35	Open	GND	Open	Open	Open	GND
0.575	GND	GND	Open	Open	Open	Open	1.375	GND	GND	Open	Open	Open	GND
0.6	Open	Open	GND	Open	Open	Open	1.4	Open	Open	GND	Open	Open	GND
0.625	GND	Open	GND	Open	Open	Open	1.425	GND	Open	GND	Open	Open	GND
0.65	Open	GND	GND	Open	Open	Open	1.45	Open	GND	GND	Open	Open	GND
0.675	GND	GND	GND	Open	Open	Open	1.475	GND	GND	GND	Open	Open	GND
0.7	Open	Open	Open	GND	Open	Open	1.5	Open	Open	Open	GND	Open	GND
0.725	GND	Open	Open	GND	Open	Open	1.525	GND	Open	Open	GND	Open	GND
0.75	Open	GND	Open	GND	Open	Open	1.55	Open	GND	Open	GND	Open	GND
0.775	GND	GND	Open	GND	Open	Open	1.575	GND	GND	Open	GND	Open	GND
0.8	Open	Open	GND	GND	Open	Open	1.6	Open	Open	GND	GND	Open	GND
0.825	GND	Open	GND	GND	Open	Open	1.625	GND	Open	GND	GND	Open	GND
0.85	Open	GND	GND	GND	Open	Open	1.65	Open	GND	GND	GND	Open	GND
0.875	GND	GND	GND	GND	Open	Open	1.675	GND	GND	GND	GND	Open	GND
0.9	Open	Open	Open	Open	GND	Open	1.7	Open	Open	Open	Open	GND	GND
0.925	GND	Open	Open	Open	GND	Open	1.725	GND	Open	Open	Open	GND	GND
0.95	Open	GND	Open	Open	GND	Open	1.75	Open	GND	Open	Open	GND	GND
0.975	GND	GND	Open	Open	GND	Open	1.775	GND	GND	Open	Open	GND	GND
1	Open	Open	GND	Open	GND	Open	1.8	Open	Open	GND	Open	GND	GND
1.025	GND	Open	GND	Open	GND	Open	1.825	GND	Open	GND	Open	GND	GND
1.05	Open	GND	GND	Open	GND	Open	1.85	Open	GND	GND	Open	GND	GND
1.075	GND	GND	GND	Open	GND	Open	1.875	GND	GND	GND	Open	GND	GND
1.1	Open	Open	Open	GND	GND	Open	1.9	Open	Open	Open	GND	GND	GND
1.125	GND	Open	Open	GND	GND	Open	1.925	GND	Open	Open	GND	GND	GND
1.15	Open	GND	Open	GND	GND	Open	1.95	Open	GND	Open	GND	GND	GND
1.175	GND	GND	Open	GND	GND	Open	1.975	GND	GND	Open	GND	GND	GND
1.2	Open	Open	GND	GND	GND	Open	2	Open	Open	GND	GND	GND	GND
1.225	GND	Open	GND	GND	GND	Open	2.025	GND	Open	GND	GND	GND	GND
1.25	Open	GND	GND	GND	GND	Open	2.05	Open	GND	GND	GND	GND	GND
1.275	GND	GND	GND	GND	GND	Open	2.075	GND	GND	GND	GND	GND	GND

16 Typical Operating Characteristics

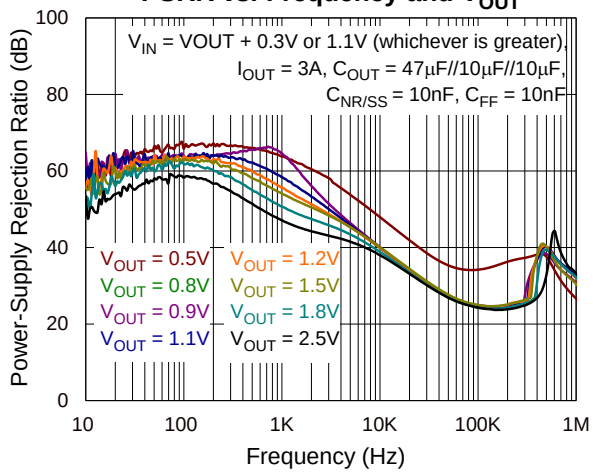
PSRR vs. Frequency and I_{OUT}



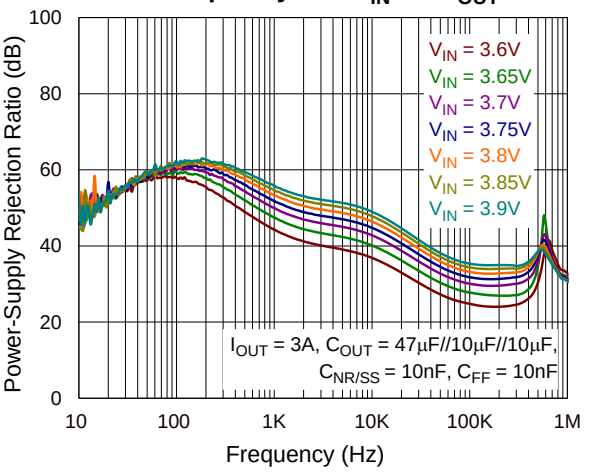
PSRR vs. Frequency and V_{IN}



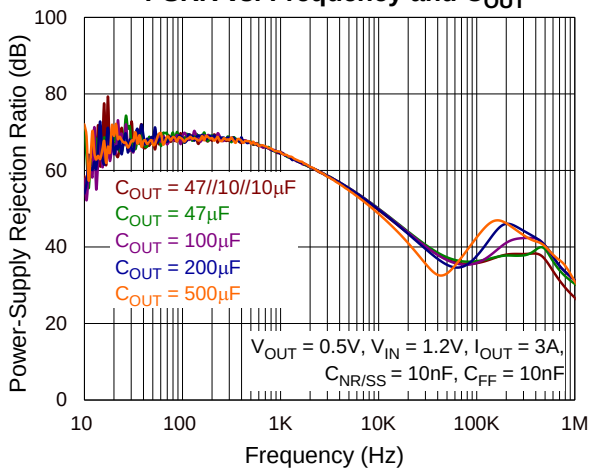
PSRR vs. Frequency and V_{OUT}



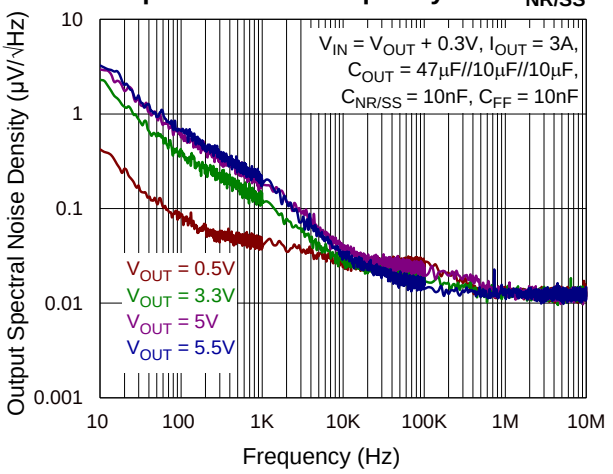
PSRR vs. Frequency and V_{IN} for V_{OUT} = 3.3V

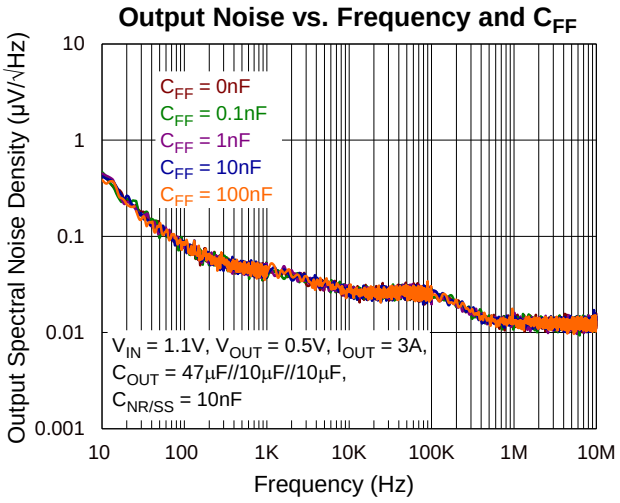


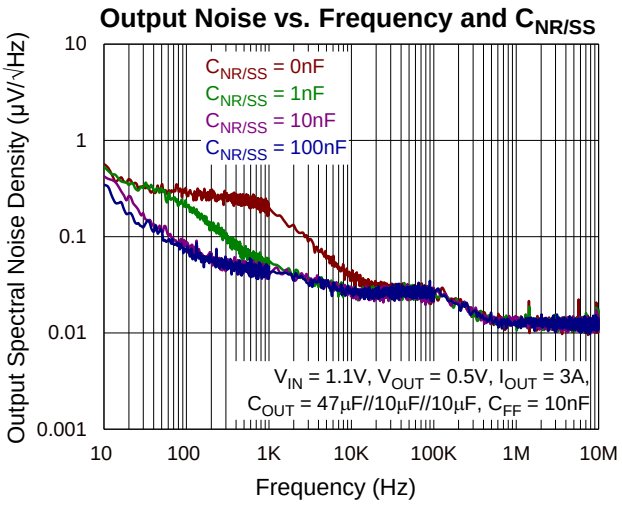
PSRR vs. Frequency and C_{OUT}

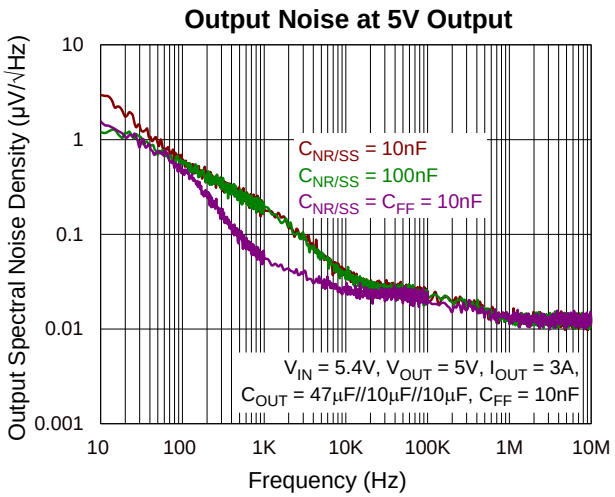


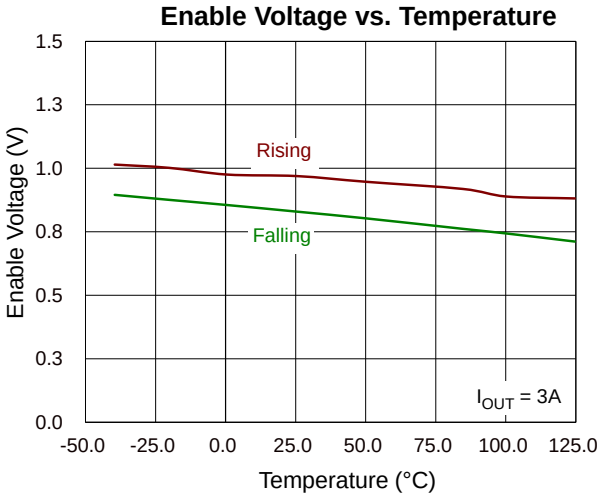
Output Noise vs. Frequency and $C_{NR/SS}$

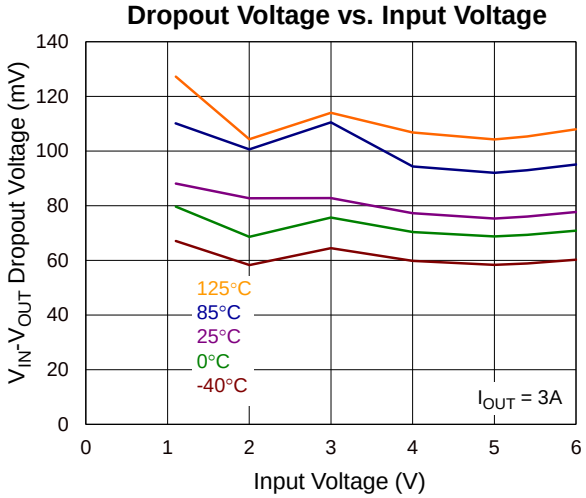


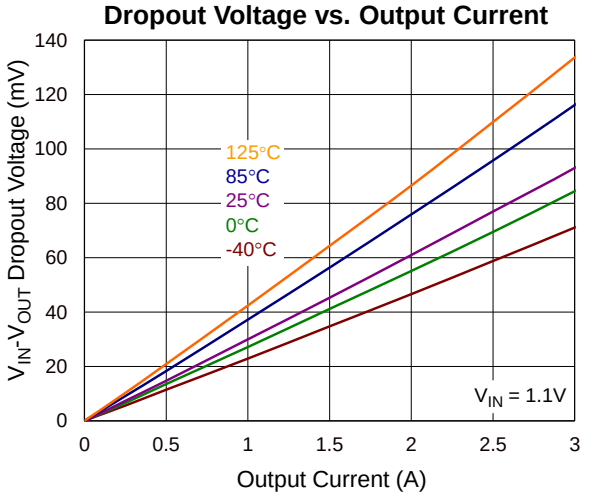




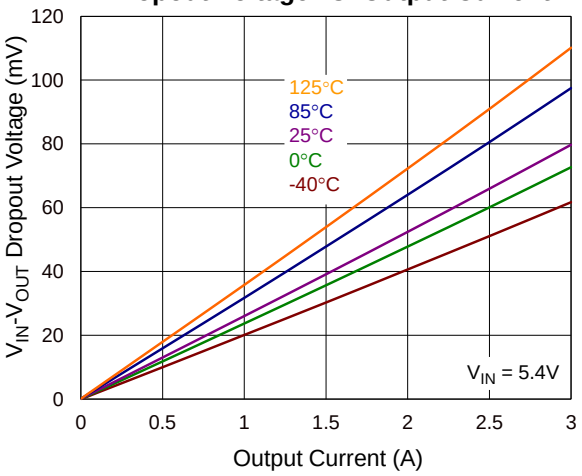




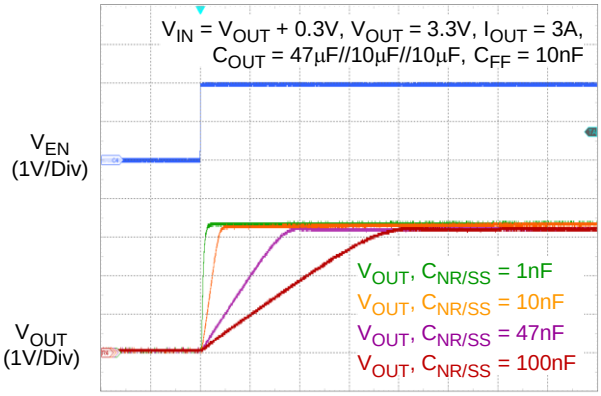




Dropout Voltage vs. Output Current

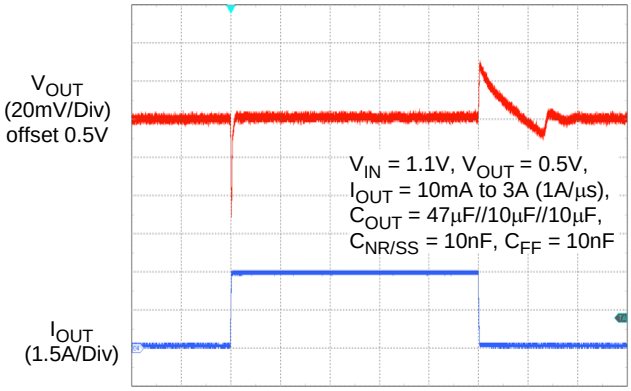


Power-On Response



Time (4ms/Div)

Load Transient Response



Time (100µs/Div)

17 Operation

The RTQ2533E operates with a single supply input ranging from 1.1V to 6.5V and it can deliver a maximum current of 3A. The device features a high PSRR and low noise characteristics to provide a clean power supply to the application.

For further reduce device noise, a low-noise reference and an error amplifier are included. The NR/SS capacitor is employed to filter noise originating from the reference, while the feed-forward capacitor is used to mitigate noise from the error amplifier. With its high power-supply rejection ratio (PSRR), the RTQ2533E effectively minimizes the coupling of input supply noise to the output.

17.1 Enable and Shutdown

The RTQ2533E features an EN pin for external enable control, allowing the user to enable or disable the device. A V_{EN} below 0.5V disables the regulator and enters shutdown mode, while a V_{EN} above 1.1V enables the regulator. When the regulator is disabled, the ground current is reduced to a maximum of 25μA. The enable circuitry includes hysteresis (typically 120mV) to accommodate relatively slowly-ramping analog signals.

If the EN pin is not utilized, it should be connected as close as possible to the largest capacitance on the input to prevent voltage drops on the VIN line from triggering the enable circuit.

17.2 VOUT Programming Pins

The RTQ2533E features a built-in matched feedback resistor network that allows for setting the output voltage. The output voltage can be programmed from 0.8V to 2.075V in increments of 25mV. This is achieved by connecting these programming pins 5, 6, 7, 9, 10, and 11 to ground. Additionally, connecting any of the VOUT programming pins to SNS will reduce the resistance of the upper portion of the resistor divider. As a result, the resolution of the VOUT programming is enhanced.

17.3 Programmable Soft-Start

The noise-reduction capacitor ($C_{NR/SS}$) serves to reduce noise and to program the soft-start ramp-up duration upon activation. When both EN and UVLO exceed their respective threshold voltages, the RTQ2533E initiates a quick-start sequence that charges the noise reduction capacitor ($C_{NR/SS}$); subsequently, the output voltage ramps up.

17.4 Power Good

The power-good circuit monitors the feedback pin voltage to indicate the status of the output voltage. The open-drain PG pin requires an external pull-up resistor to an external supply, and any downstream device can receive the power-good signal as a logic input that can be used for sequencing. A pull-up resistor from 10kΩ to 100kΩ is recommended. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices.

After start-up, the PG pin becomes high impedance when the feedback voltage exceeds V_{PG_HYS} (typically 90% of the 0.5V reference voltage level). The PG pin is pulled to GND when the feedback pin voltage falls below V_{PG}. Additionally, this pin is pulled low under protection conditions, during an enable (EN) shutdown, or throughout the soft-start process.

17.5 Undervoltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from activating before V_{IN} rises above the V_{UVLO} threshold. The UVLO circuit also deactivates the output of the device when V_{IN} falls below the lockout voltage ($V_{UVLO\_R} - V_{UVLO\_HYS}$). The UVLO circuit is designed to respond quickly to glitches on V_{IN} and attempts to disable the output of the device if V_{IN} collapses.

17.6 Internal Current Limit (I_{LIM})

The RTQ2533E continuously monitors the output current to protect the device against high load current faults or short-circuit events. The current limiting feature is not designed to allow operation above the rated current of the device. Operating the RTQ2533E continuously above its rated current can degrade the reliability of the device.

During a current limit event, the output voltage drops as the load impedance decreases. If the output voltage becomes too low, excessive power dissipation may cause the thermal shutdown.

To further protect the RTQ2533E, a foldback feature reduces the short-circuit current. This ensures the regulator is safeguarded from damage under all load conditions. If the load current demand surpasses the foldback current threshold before EN goes high, the device will remain disabled.

17.7 Over-Temperature Protection (OTP)

The RTQ2533E implements over-temperature protection. The device is disabled when the junction temperature (T_J) exceeds 160°C (typical). The LDO automatically reactivates when the temperature falls below 140°C (typical).

Note that the over-temperature protection feature is designed to protect the device under temporary overload conditions. The protection is activated outside of the absolute maximum ratings of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

17.8 Output Active Discharge

When the RTQ2533E is disabled, it discharges the LDO output (via VOUT pins) to ground through an internal current sink. The active discharge circuit is not designed for discharging a significant amount of output capacitance after the input supply has failed. Under such conditions, reverse current may flow from the output back to the input. It is recommended to implement external current protection when the device operates in a reverse voltage condition.

18 Application Information

(Note 10)

The RTQ2533E is a high-current, low-noise, high-accuracy, low-dropout linear regulator capable of sourcing up to 3A with a 180mV maximum dropout. The input voltage operating range is from 1.1V to 6.5V. Additionally, the output voltage can be adjusted from 0.5V to 5.5V using external resistors. For output voltages between 0.5V and 2.075V, specific pins can be shorted via PCB layout to achieve the desired output voltage.

18.1 Output Voltage Setting

The output voltage of the RTQ2533E can be set using external resistors to achieve different output targets.

The output voltage is determined by the resistance values of R1 and R2, as shown in Figure 3, when external resistors are utilized. The values of R1 and R2 can be calculated for any voltage value using the following formula:

$$V_{OUT} = 0.5 \times \frac{R1 + R2}{R2}$$

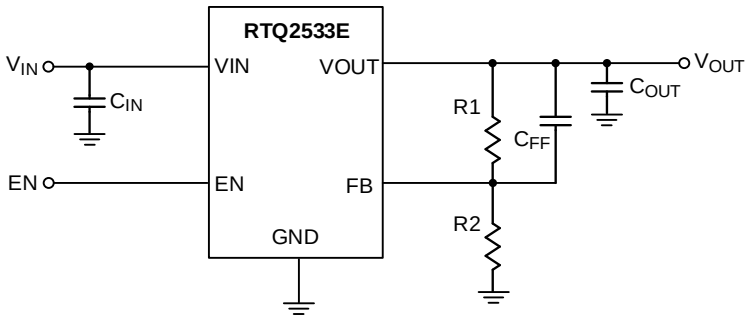


Figure 3. Output Voltage Set by External Resistors

Alternatively, the RTQ2533E allows for the programming of the regulated output voltage level without external resistors by shorting pins 5, 6, 7, 9, 10, and 11 to ground. This method requires the SNS pin to be connected to VOUT. Pins 5, 6, 7, 9, 10, and 11 interface with internal resistor pairs, where each pin can be either grounded (active) or left unconnected (floating) to influence the output voltage.

Voltage programming is achieved by adding the internal reference voltage (V_{REF} = 0.5V) to the cumulative voltages corresponding to each activated pin, as illustrated in Figure 4.

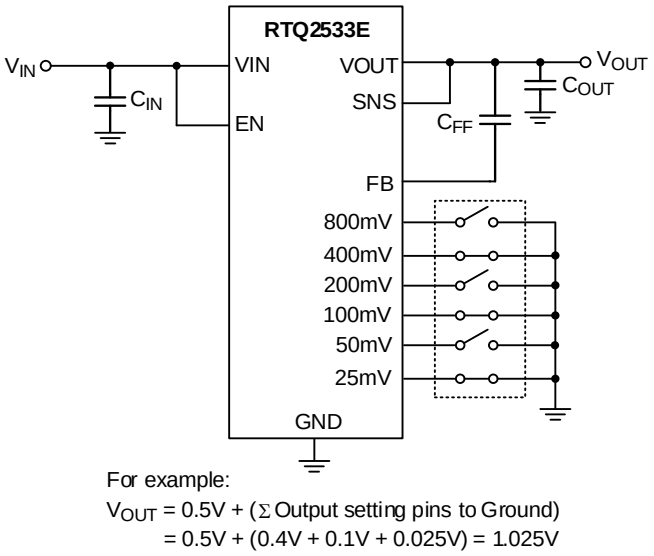


Figure 4. Output Setting without External Resistors

Table 3 provides a summary of the voltage values corresponding to each active pin configuration for reference. By leaving all programming pins open, or floating, the output is programmed to the minimum possible output voltage, equal to V_{REF} (0.5V). The maximum achievable output voltage is 2.075V when pins 5, 6, 7, 9, 10, and 11 are simultaneously shorted to ground.

18.2 Dropout Voltage

The dropout voltage, denoted as V_{DROP}, is the voltage difference between the VIN and VOUT pins while operating at a specific output current (I_{RATED}). The dropout voltage, V_{DROP}, can also be described as the voltage drop across the pass-FET at a specific output current (I_{RATED}) while the pass-FET is fully operating in the ohmic region and can be characterized by a resistance $R_{DS(ON)}$. Thus, the dropout voltage can be defined as $V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$. For normal operation, it is recommended that the LDO operates within the range $V_{IN} > (V_{OUT} + V_{DROP})$ to ensure optimal transient response and PSRR performance. However, operation in the ohmic region will degrade the performance severely.

18.3 C_{IN} and C_{OUT} Selection

The RTQ2533E is designed to support low series resistance (ESR) ceramic capacitors. X7R, X5R, and COG rated ceramic capacitors are recommended for their stable capacitance across different temperatures. In contrast, Y5V-rated capacitors are not recommended due to their significant capacitance variations with temperature.

However, the capacitance of ceramic capacitors varies with operating voltage and temperature. Design engineers must be aware of these characteristics. It is usually recommended to derate ceramic capacitors by 50% to account for their capacitance variance under different conditions. A 47μF or greater output ceramic capacitor (or 22μF effective capacitance) is suggested to ensure stability. Input capacitance is selected to minimize transient input drop during load current steps. For general applications, an input capacitor of at least 47μF is highly recommended for minimal input impedance. If the trace inductance between the RTQ2533E input pin and power supply is high, a fast load transient can cause VIN voltage level ringing above the absolute maximum voltage rating which damages the device. Adding more input capacitors can restrict the ringing and keep it below the device's absolute maximum ratings.

Generally, using a 47μF 1210-sized ceramic capacitor in parallel with two 10μF 0805-sized ceramic capacitors ensures the required minimum effective capacitance for high input voltage and high output voltage conditions. Place these capacitors as close to the pins as possible for optimum performance and to ensure stability.

18.4 Feed-Forward Capacitor (C_{FF})

The RTQ2533E is designed to be stable without the external feed-forward capacitor (C_{FF}). However, adding a 10nF external feed-forward capacitor optimizes the transient response, noise suppression, and PSRR performance. Utilizing a higher capacitance value for C_{FF} is possible, but it will result in a prolonged start-up time, and the power-good signal may mistakenly indicate that the output voltage has stabilized.

18.5 Soft-Start and Noise Reduction ($C_{NR/SS}$)

The RTQ2533E is designed for a programmable, monotonic soft-start time during the output voltage rise, achieved by connecting an external capacitor ($C_{NR/SS}$) to the NR/SS pin. For general applications, using an external $C_{NR/SS}$ is recommended to minimize in-rush current and reduce noise from the internal reference.

During the monotonic start-up procedure, the error amplifier of the RTQ2533E regulates the output by tracking the voltage ramp of the external soft-start capacitor ($C_{NR/SS}$), until it reaches the internal reference of 0.5V. The soft-start ramp time can be calculated using Equation a1, which is a function of the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference (V_{REF}).

$$t_{SS} = \frac{(V_{REF} \times C_{NR/SS})}{I_{NR/SS}} \quad (a1)$$

For noise-reduction, $C_{NR/SS}$ works with an internal noise-reduction resistor to form a low-pass filter (LPF), filtering out noise from the internal bandgap reference before it is amplified by the error amplifier, thus reducing the total device noise floor.

18.6 Input Inrush Current

During start-up, the input Inrush current into the VIN pin consists of the sum of load current and the charging current of the output capacitor. Measuring the inrush current is challenging as it requires removal of the input capacitor, which is not recommended. Generally, the soft-start inrush current can be estimated using Equation b1, where $V_{OUT}(t)$ represents the instantaneous output voltage of the power-on ramp, $dV_{OUT}(t)/dt$ is the slope of the V_{OUT} ramp, and R_{LOAD} is the resistive load impedance.

$$I_{OUT}(t) = \frac{\left(C_{OUT} \times dV_{OUT}(t)\right)}{dt} + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right) \quad (b1)$$

18.7 Undervoltage Lockout (UVLO)

The Undervoltage Lockout (UVLO) threshold is the minimum input operational voltage range that ensures the device stays disabled. Figure 5 illustrates that the UVLO circuits are triggered during three different input voltage events (durations a, b, and c), assuming $V_{EN} \geq V_{EN\_R}$ all the time. During duration “a”, the input voltage starts rising. When V_{IN} is over the UVLO rising threshold, V_{OUT} starts the power-on process. Then when V_{OUT} reaches the target level, it is under regulation. During duration “b”, although the power line has a voltage drop, it does not drop below the UVLO low threshold (falling threshold). As a result, the device maintains normal operation, and V_{OUT} is still regulated. During duration “c”, V_{IN} drops below the UVLO falling threshold, so the control loop is disabled and there is no regulation. Meanwhile, V_{OUT} drops. For general applications, an instant power line transient with a long power trace at the VIN pin may have V_{IN} level unstable and force a trap, as shown in the duration “c”, which makes V_{OUT} collapse. In this case, adding additional input capacitance or optimizing the input trace layout on the PCB can effectively to enhance the stabilization of the input power.

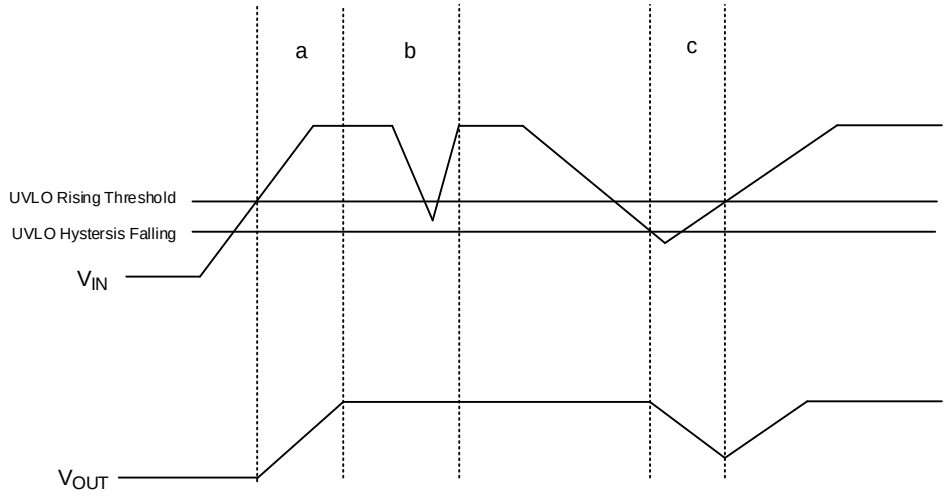


Figure 5. Under Voltage Lockout Trigging Conditions and Output Variation

18.8 Power-Good (PG) Function

The power-good function monitors the voltage level at the feedback pin to determine if the output voltage status is within normal parameters. This function allows other devices to utilize the RTQ2533E's power-good signal as a logic signal that can be used for sequencing system applications. The PG pin has an open-drain configuration, requiring an external pull-up resistor connected to an external supply for proper functionality. A pull-up resistor with a value ranging from 10kΩ to 100kΩ is recommended. The minimum value of 10kΩ is based on the maximum pull-down capability of the power-good transistor, while the maximum value of 100kΩ takes into account the highest leakage current that can occur at the power-good node.

Figure 6 demonstrates some PG scenarios in the relation to VIN, EN, and the protection status. During duration a, V_{EN} exceeds the V_{EN_H} threshold, indicating that the device is under operation. In this phase, V_{OUT} starts to increase (the rise time is related to the soft-start capacitor $C_{NR/SS}$). When V_{OUT} surpasses the PG hysteresis threshold, the reflected feedback voltage V_{FB} exceeds the V_{PG_HYS} threshold causing the PG pin to enter a high-impedance state. The duration b indicates fault conditions such as OTP, OCP, or a significant output voltage drop due to rapid load changes. If V_{FB} falls below the V_{PG} threshold, V_{PG} is pulled to GND, which indicates that the output voltage is not within the acceptable range. During duration c, V_{OUT} has a minor drop, which is not lower than the PG falling threshold; the PG pin remains in a high-impedance. Finally, in duration d, when V_{EN} transitions to a low logic level, V_{PG} is pulled to GND.

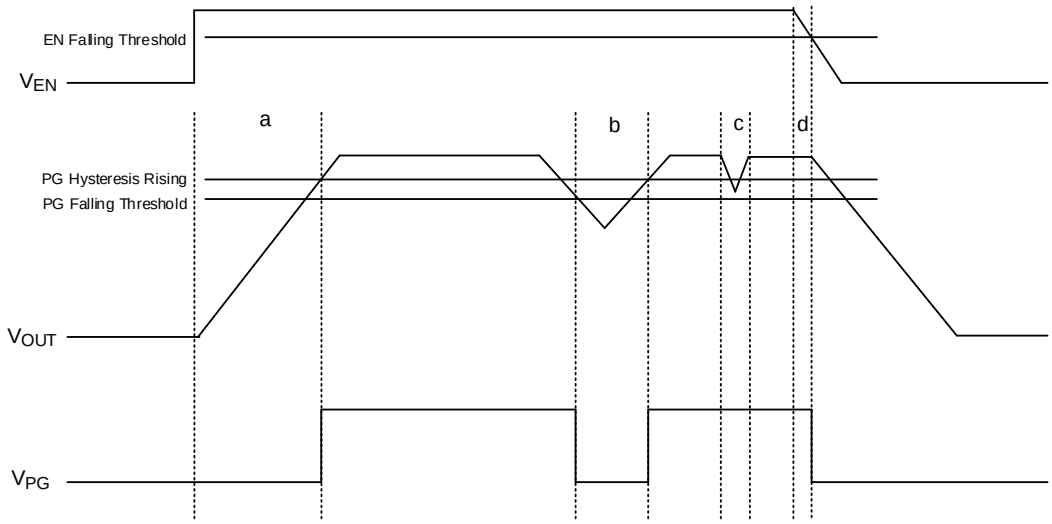


Figure 6. PG Trigger Scenario with Different Operating Status

18.9 Reverse Current Protection

Reverse current flows from V_{OUT} to V_{IN} through the body diode of the pass element, instead of the normal conduction channel, if the maximum V_{OUT} exceeds V_{IN} + 0.3V; in this case, the pass element may be damaged.

For example, if the output is biased above the input supply voltage level or the input supply has an instant drop at light load operation that makes V_{IN} < V_{OUT}. As shown in Figure 7, an external Schottky diode can be added to prevent the pass element from being damaged by the reverse current.

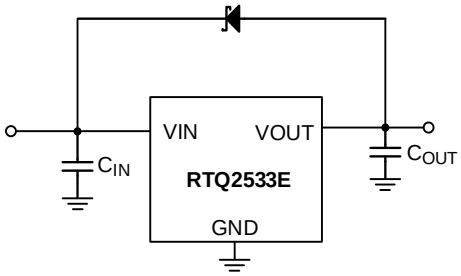


Figure 7. Application Circuit for Reverse Current Protection

18.10 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a VQFN-20L 3.5x3.5 package, the thermal resistance, $\theta_{JA\ (EVB)}$, is 39.33°C/W on a standard high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (39.33°C/W) = 2.54W for a VQFN-20L 3.5x3.5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA\ EVB)}$. The derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

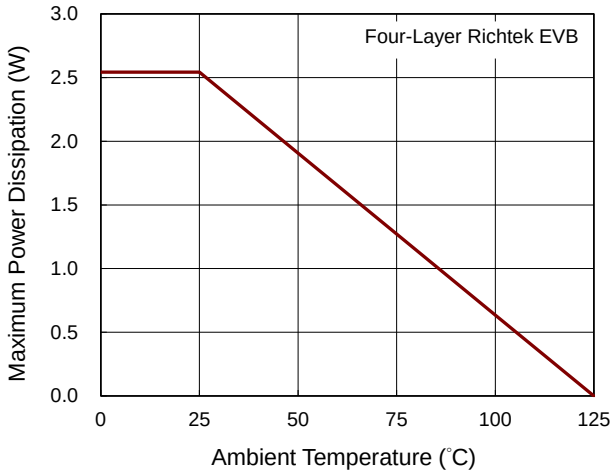


Figure 8. Derating Curve of Maximum Power Dissipation

18.11 Layout Considerations

For optimal of the RTQ2533E, the PCB layout suggestions below are recommended.

1. All circuit components should be placed on the same side and as close to the respective LDO pins as possible.
2. Place the ground return path in close proximity to the input and output capacitors.
3. Ensure the ground plane is connected with a wide copper surface to enhance thermal dissipation.
4. Avoid using vias and long power traces for the input and output capacitors connections, as they can negatively affect performance.
5. Figure 9 show a layout example that reduces conduction trace loops, helping to minimize inductive parasitic and load transient effects, while improving circuit stability.

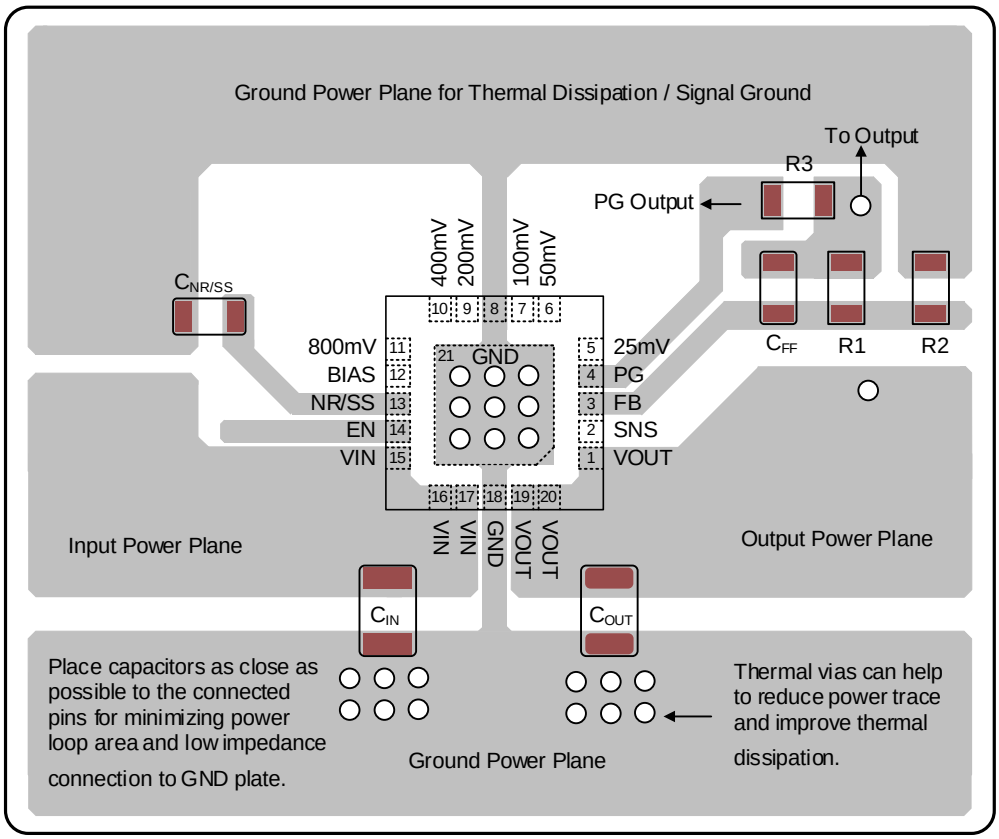
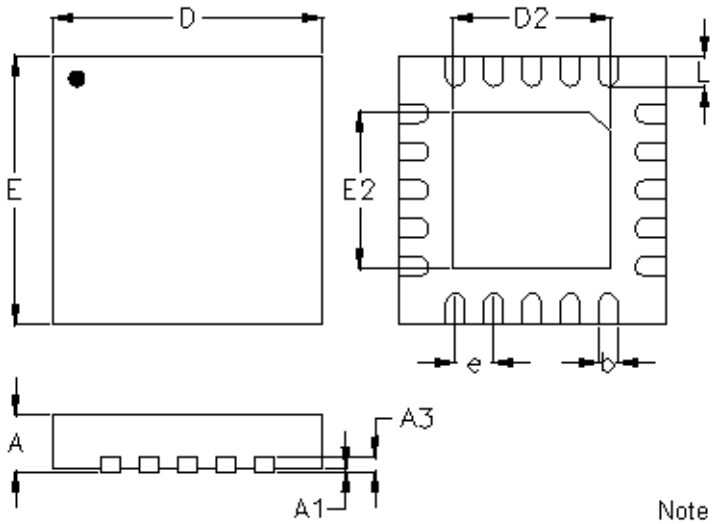
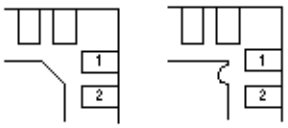


Figure 9. PCB Layout Guide for VQFN-20L 3.5x3.5 package

Note 10. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Outline Dimension





DETAIL A

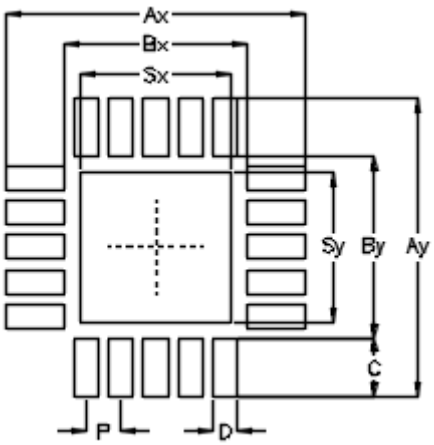
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	3.400	3.600	0.134	0.142
D2	2.000	2.100	0.079	0.083
E	3.400	3.600	0.134	0.142
E2	2.000	2.100	0.079	0.083
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 20L QFN 3.5x3.5 Package

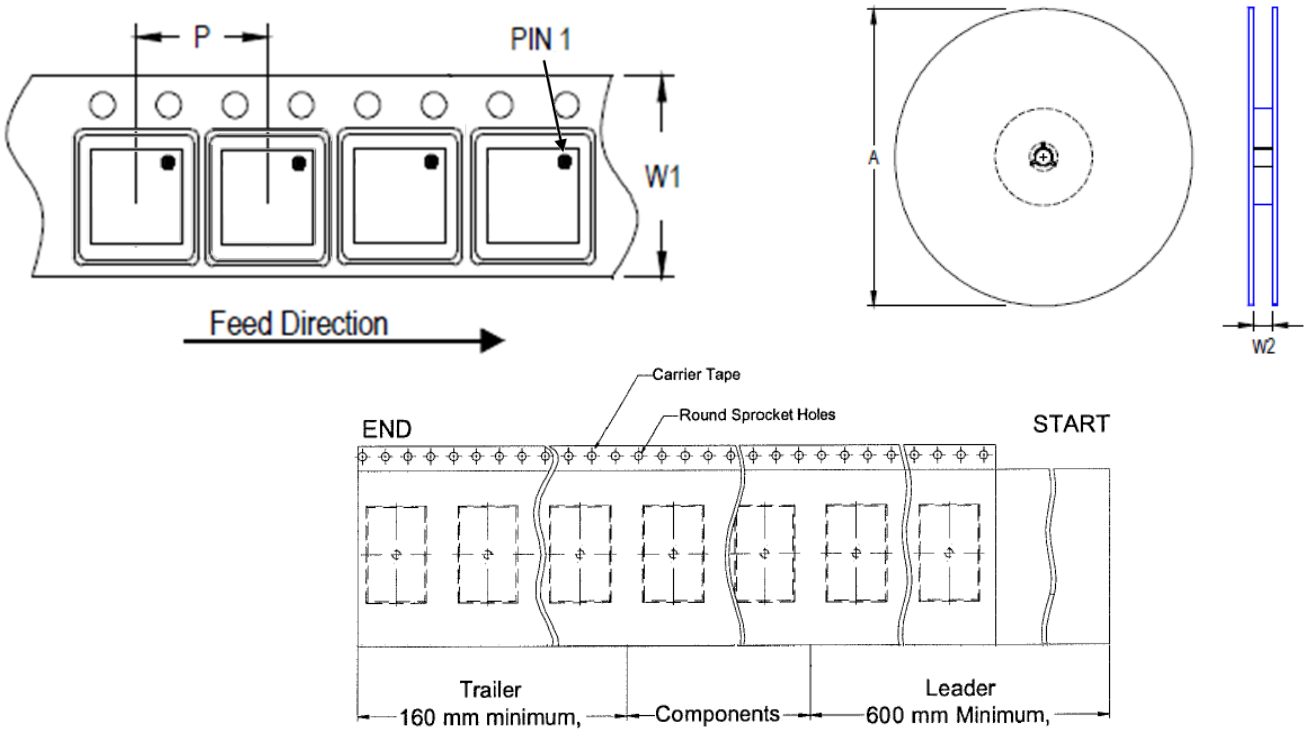
20 Footprint Information



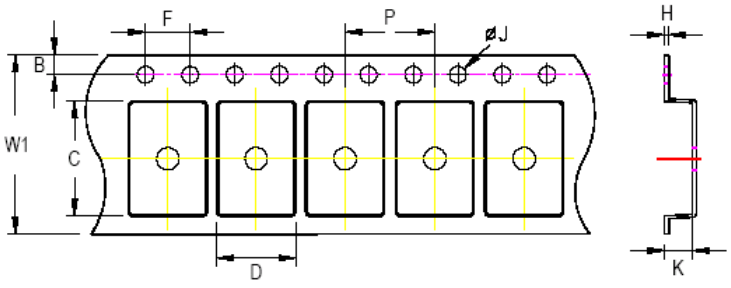
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3.5*3.5-20	20	0.50	4.30	4.30	2.60	2.60	0.85	0.35	2.15	2.15	±0.05

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3.5x3.5	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3.5x3.5	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
00	2024/5/14	Final	*Ordering Information on page 2* *Application Information on page 24* *Packing Information on page 28*
01	2024/12/6	Modify	*Changed the names PGOOD to PG.* *Applications on page 1* *Typical Application Circuit on page 10* *Packing Information on page 26, 27*