# 1A, Low Noise, High PSRR, Low-Dropout Linear Regulator

## 1 General Description

The RTQ2510 is a high performance positive low dropout (LDO) regulator designed for applications requiring very low dropout voltage and high Power Supply Ripple Rejection (PSRR) at up to 1A. The input voltage range is from 2.2V to 6V and the output voltage is programmable as low as 0.8V. The P-MOSFET switch provides excellent transient response with only a 4.7μF ceramic output capacitor. The external enable control effectively reduces power dissipation while shutdown and further output noise immunity is achieved through bypass capacitor on NR pin. Additionally, the RTQ2510 features a precise 3% output regulation over line, load, and temperature variations. The device is available in the VDFN-8L 3x3 package and is specified from –40°C to 125°C.

## 2 Ordering Information

RTQ2510 □ -QT □

- Packing
  B: Pin 1 Orientation
  (Quadrant 2, Follow EIA-481)
- Grade
  QT: AEC-Q100 Qualified and Screened by High Temperature
- Package Type
  N: VDFN-8L 3x3 (V-Type)
  Richtek Green Policy Compliant

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020

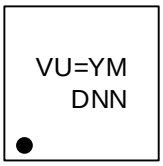
## 3 Features

- **AEC-Q100 Grade 1 Qualified**
- **Dropout : 170mV Typical at 1A**
- **PSRR : 63dB @ 1kHz, 38dB @ 1MHz**
- **Input Voltage Range : 2.2V to 6V**
- **Adjustable Output Voltage : 0.8V to 5.5V**
- **–40°C to 125°C Operating Junction Temperature Range**
- **Excellent Noise Immunity**
- **Fast Response Over Load and Line Transient**
- **Stable with a 4.7μF Output Ceramic Capacitor**
- **Accurate Output Voltage 3% Over Load, Line, Process, and Temperature Variations**
- **Enable Control**
- **Over-Current Protection**
- **Over-Temperature Protection**

## 4 Applications

- In-Vehicle Infotainment Systems
- Telematics Control Units
- Instrument Clusters
- Automotive Head Units
- ADAS Camera and Radar
- Navigation Systems

## 5 Marking Information




VU= : Product Code
YMDNN : Date Code

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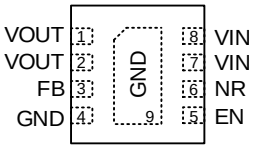
## 6 Pin Configuration

(TOP VIEW)

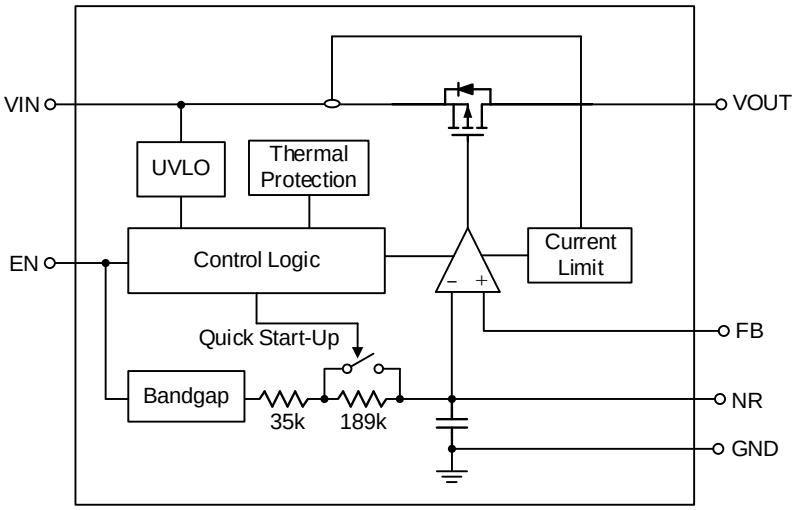



VDFN-8L 3x3

## 7 Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1, 2 | VOUT | Output of the regulator. Decouple this pin to GND with at least 4.7μF for stability. |
| 3 | FB | Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.8V typically. |
| 4, 9 (Exposed Pad) | GND | System ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |
| 5 | EN | Enable control input. Connecting this pin to logic high enables the regulator or driving this pin low puts it into shutdown mode. EN can be connected to IN if not used. (EN pin is not allowed to be left floating.) |
| 6 | NR | Noise reduction input. Decouple this pin to GND with an external capacitor can not only reduce output noise to very low levels but also slow down the VOUT rise like a soft-start behavior. |
| 7, 8 | VIN | Supply input. A minimum of 1μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection. |

## 8 Functional Block Diagram



## 9 Absolute Maximum Ratings

(Note 1)

- All Pins ---------- –0.3V to 7V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

## 10 ESD Ratings

(Note 2)

- ESD Susceptibility
- HBM (Human Body Model)---------- 2kV

**Note 2**. Devices are ESD sensitive. Handling precautions are recommended.

## 11 Recommended Operating Conditions

(Note 3)

- Supply Input Voltage, VIN ---------- 2.2V to 6V
- Junction Temperature Range---------- –40°C to 125°C

**Note 3**. The device is not guaranteed to function outside its operating conditions.

## 12 Thermal Information

(Note 4 and Note 5)

| Thermal Parameter | | VDFN-8L 3x3 | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance (JEDEC standard) | 60.82 | °C/W |
| $\theta_{JC(Top)}$ | Junction-to-case (top) thermal resistance | 83.76 | °C/W |
| $\theta_{JC(Bottom)}$ | Junction-to-case (bottom) thermal resistance | 10.48 | °C/W |
| $\theta_{JA(EVB)}$ | Junction-to-ambient thermal resistance (specific EVB) | 45.06 | °C/W |
| $\Psi_{JC(Top)}$ | Junction-to-top characterization parameter | 5.42 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 26.17 | °C/W |

**Note 4.** For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

**Note 5.** $\theta_{JA\ (EVB)}$, $\Psi_{JC(Top)}$ and $\Psi_{JB}$ are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

## 13 Electrical Characteristics

($V_{IN}$ = $V_{OUT}$ + 0.5V or 2.2V, $V_{OUT}$ = 0.8V and 5.5V, $I_{OUT}$ = 1mA, $V_{EN}$ = 2.2V, $C_{NR}$ = 10nF, $C_{OUT}$ = 4.7µF, $T_J$ = -40°C to 125°C, unless otherwise specified)

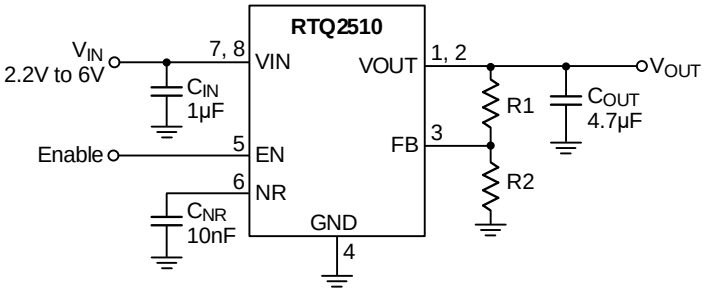
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage** | | | | | | |
| VIN Supply Input Voltage | $V_{IN}$ | | 2.2 | -- | 6 | V |
| Undervoltage Lockout Rising Threshold | $V_{UVLO}$ | $R_{OUT}$ = 1kΩ | 1.86 | 2 | 2.1 | V |
| Undervoltage Lockout Hysteresis | $V_{UVLO\_HYS}$ | $R_{OUT}$ = 1kΩ | -- | 200 | -- | mV |
| Shutdown Current | $I_{SHDN}$ | $V_{EN}$ ≤ 0.4V, $V_{IN}$ ≥ 2.2V, $R_{OUT}$ = 1kΩ, 0°C ≤ $T_J$ ≤ 85°C | -- | 0.2 | 2 | µA |
| | | $V_{EN}$ ≤ 0.4V, $V_{IN}$ ≥ 2.2V, $R_{OUT}$ = 1kΩ, –40°C ≤ $T_J$ ≤ 125°C | -- | 0.2 | 5 | |
| Quiescent Current | $I_Q$ | | -- | 190 | 350 | µA |
| **Output Voltage** | | | | | | |
| Output Voltage | $V_{OUT}$ | | 0.8 | -- | 5.5 | V |
| Output Voltage Accuracy (Note 6) | $V_{OUT\_ACC}$ | $V_{OUT}$ + 0.5V ≤ $V_{IN}$ ≤ 6V, $V_{IN}$ ≥ 2.5V, 100mA ≤ $I_{OUT}$ ≤ 500mA, 0°C ≤ $T_J$ ≤ 85°C | –2 | -- | +2 | % |
| | | $V_{OUT}$ + 0.5V ≤ $V_{IN}$ ≤ 6V, $V_{IN}$ ≥ 2.2V, 100mA ≤ $I_{OUT}$ ≤ 1A | –3 | ±0.3 | +3 | |
| Line Regulation | $V_{LINE\_REG}$ | $V_{OUT}$ + 0.5V ≤ $V_{IN}$ ≤ 6V, $V_{IN}$ ≥ 2.2V, $I_{OUT}$ = 100mA | -- | 0.2 | -- | % |
| Load Regulation | $V_{LOAD\_REG}$ | 100mA ≤ $I_{OUT}$ ≤ 1A | -- | 0.3 | -- | % |
| **Enable Voltage** | | | | | | |
| EN Input Voltage Rising threshold | $V_{EN\_R}$ | $V_{EN}$ rising, 2.2V ≤ $V_{IN}$ ≤ 6V, $R_{OUT}$ = 1kΩ | 1.2 | -- | -- | V |
| EN Input Voltage Falling threshold | $V_{EN\_F}$ | $V_{EN}$ falling, $R_{OUT}$ = 1kΩ | -- | -- | 0.4 | |
| EN Input Current | $I_{EN}$ | $V_{IN}$ = 6V, $V_{EN}$ = 6V | -- | 0.02 | 1 | µA |
| FB Input Current | $I_{FB}$ | $V_{IN}$ = 5.5V, $V_{FB}$ = 0.8V | -- | 0.02 | 1 | µA |
| **Current Limit** | | | | | | |
| Current Limit | $I_{LIM}$ | $V_{IN}$ = 3.3V, $V_{OUT}$ = 0.85 x $V_{OUT}$ | 1.1 | 1.4 | 2 | A |
| **Power-Up Time** | | | | | | |
| Soft-Start Time | $t_{SS}$ | $V_{OUT}$ = 3.3V, $R_{OUT}$ = 3.3kΩ, $C_{OUT}$ = 4.7µF, $C_{NR}$ = 1nF | -- | 0.16 | -- | ms |
| | | $V_{OUT}$ = 3.3V, $R_{OUT}$ = 3.3kΩ, $C_{OUT}$ = 4.7µF, $C_{NR}$ = 10nF | -- | 1.6 | -- | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Dropout Voltage** | | | | | | | |
| Dropout Voltage | $V_{DROP}$ | $V_{OUT}$ + 0.5V ≤ $V_{IN}$ ≤ 6V, $V_{FB}$ = 0V | $V_{IN}$ ≥ 2.2V, $I_{OUT}$ = 500mA | -- | -- | 160 | mV |
| | | | $V_{IN}$ ≥ 2.5V, $I_{OUT}$ = 750mA | -- | -- | 210 | |
| | | | $V_{IN}$ ≥ 2.5V, $I_{OUT}$ = 1A | -- | -- | 370 | |
| **Power Supply Ripple Rejection and Noise** | | | | | | | |
| Power Supply Ripple Rejection | PSRR | $V_{IN}$ = 4.3V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 750mA (Note 7) | f = 100Hz | -- | 48 | -- | dB |
| | | | f = 1kHz | -- | 63 | -- | |
| | | | f = 10kHz | -- | 63 | -- | |
| | | | f = 1MHz | -- | 38 | -- | |
| Output Noise | $V_n$ | BW = 100Hz to 100kHz, $V_{IN}$ = 4.3V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 100mA (Note 7) | $C_{NR}$ = 1nF | -- | 15.6 x $V_{OUT}$ | -- | μVRMS |
| | | | $C_{NR}$ = 10nF | -- | 15.6 x $V_{OUT}$ | -- | |
| | | | $C_{NR}$ = 0.1μF | -- | 15.1 x $V_{OUT}$ | -- | |
| **Over-Temperature Protection** | | | | | | | |
| Over-Temperature Protection Threshold | $T_{OTP}$ | (Note 7) | | -- | 160 | -- | °C |
| Over-Temperature Protection Hysteresis | $T_{OTP\_HYS}$ | (Note 7) | | -- | 20 | -- | |

**Note 6.** The spec doesn't cover the tolerances from external resistors, and which is not tested at condition of $V_{OUT}$ = 0.8V, 4.5V ≤ $V_{IN}$ ≤ 6V, and 750mA ≤ $I_{OUT}$ ≤ 1A since the power dissipation of the device is totally higher than the maximum rating of the package to lead a thermal shutdown issue.

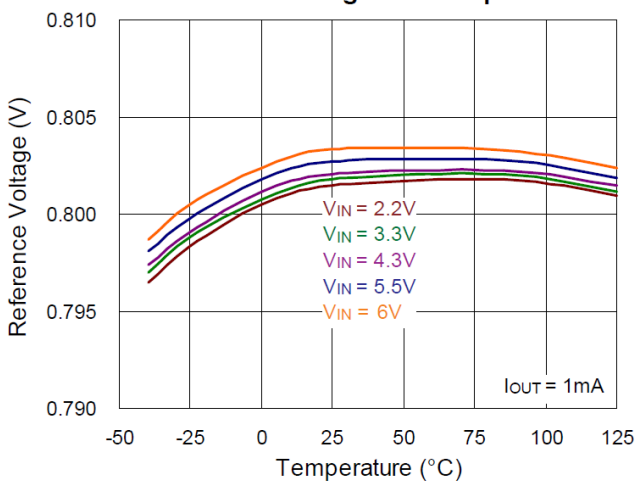
**Note 7.** Guarantee by design.

## 14 Typical Application Circuit

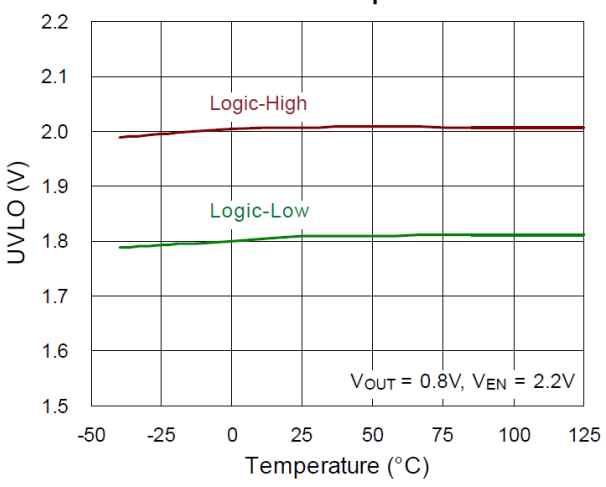


## 15 Typical Operating Characteristics

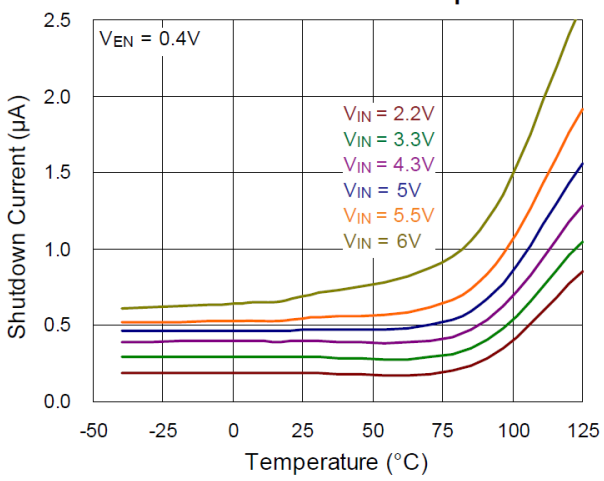
**Reference Voltage vs. Temperature**



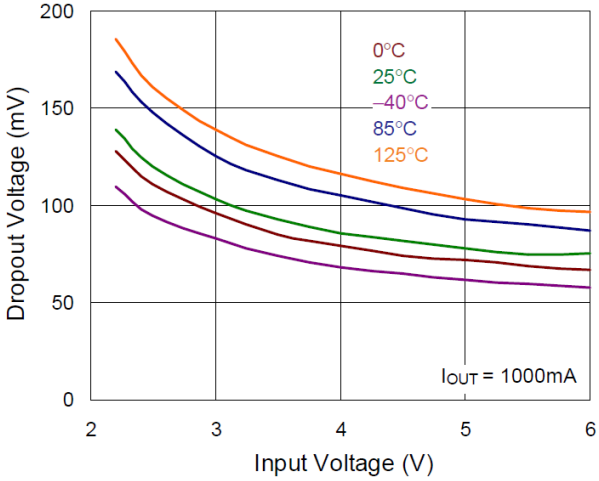

**UVLO vs. Temperature**



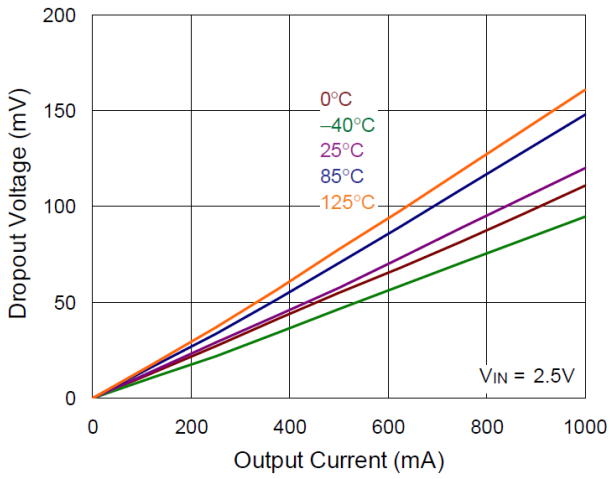

**Shutdown Current vs. Temperature**



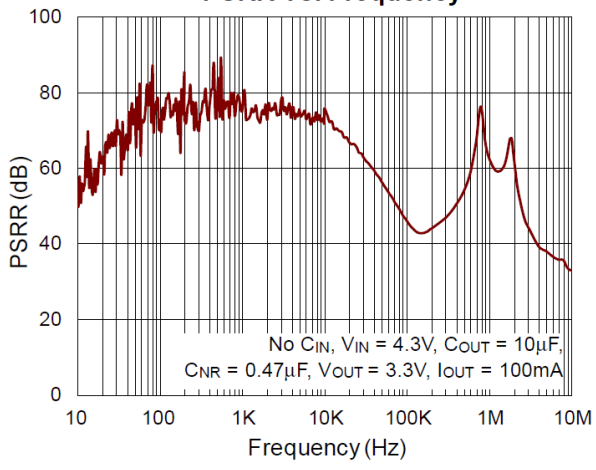

**Dropout Voltage vs. Input Voltage**



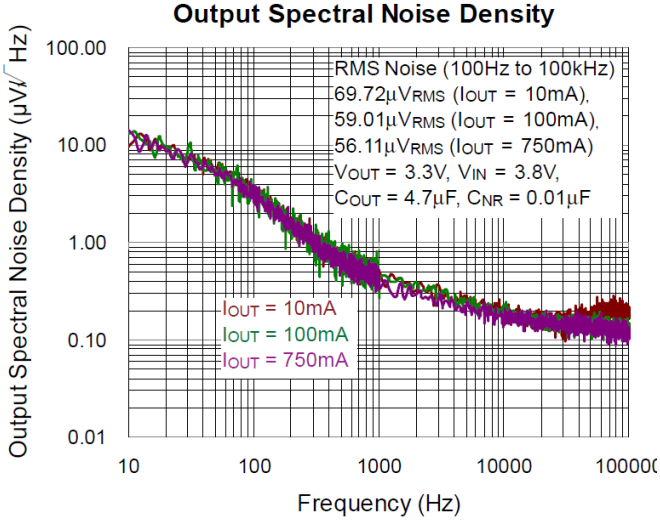

**Dropout Voltage vs. Output Current**



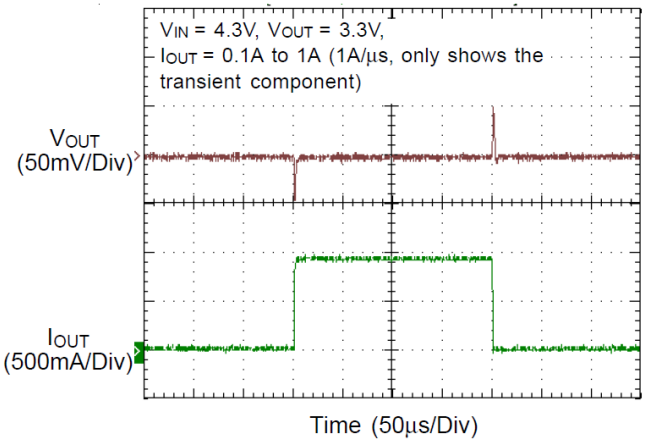

**PSRR vs. Frequency**



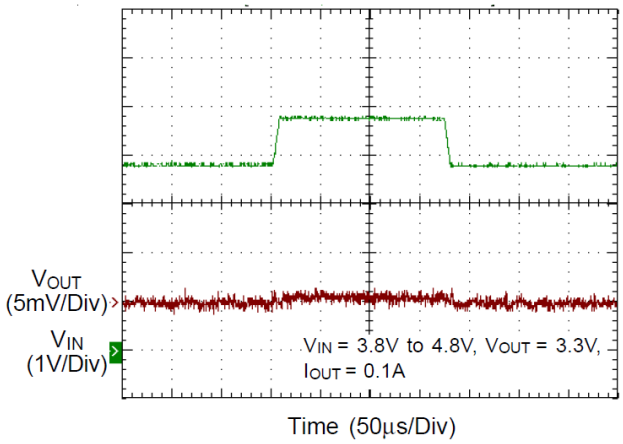
### Output Spectral Noise Density



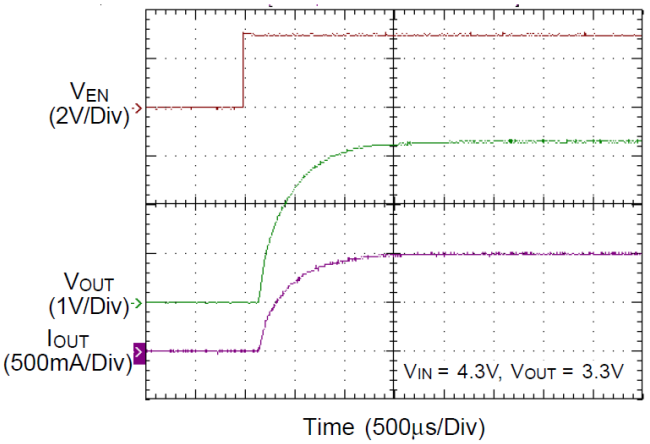

### Load Transient Response



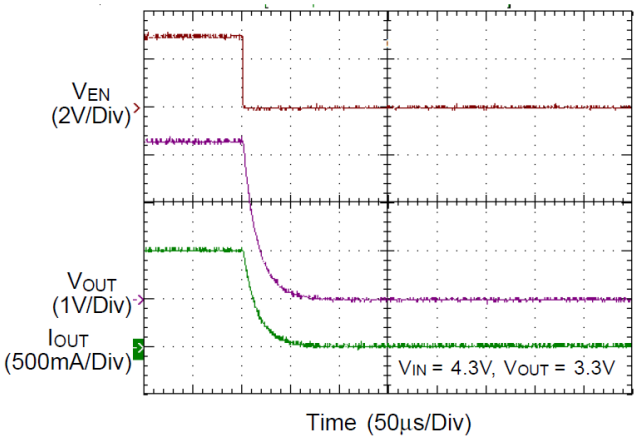

### Line Transient Response



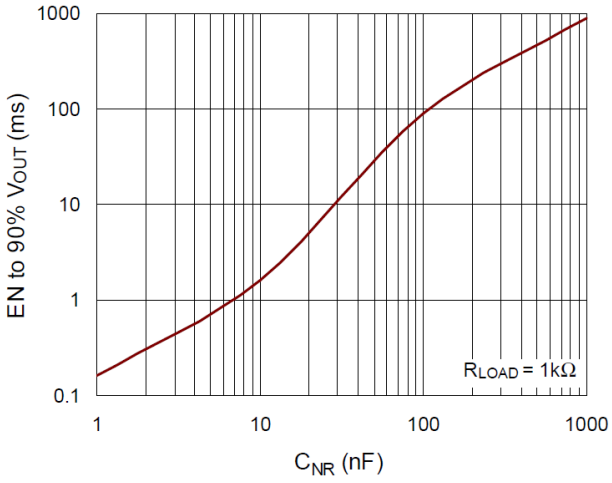

### Power On from EN




### Power Off from EN




### Start-Up Time vs. Noise Reduction Capacitance



# 16 Operation

The RTQ2510 is a low noise, high PSRR LDO which supports very low dropout operation. The operating input range is from 2.2V to 6V, the output voltage is programmable as low as 0.8V, and the output current can be up to 1A. The internal compensation network is well designed to achieve fast transient response with good stability.

In steady-state operation, the feedback voltage is regulated to the reference voltage by the internal regulator. When the feedback voltage signal is less than the reference, the output current passing through the power MOSFET will increase. The additional current is sent to the output until the voltage level of the FB pin returns to the reference.

On the other hand, if the feedback voltage is higher than the reference, the power MOSFET current is decreased. The excess charge at the output can be released by the loading current.

## 16.1 Start-Up

The RTQ2510 has a quick-start circuit to charge the noise reduction capacitor ($C_{NR}$). The switch of the quick-start circuit is closed at start up.

To reduce the noise from the bandgap, there is a low-pass (RC) filter consisting of the $C_{NR}$ and the resistance, which is connected with the bandgap, as shown in the Functional Block Diagrams.

At the start-up, the quick-start switch is closed, with only 35kΩ resistance between the bandgap and NR pin. The quick-start switch opens approximately 2ms after the device is enabled, and the resistance between NR and bandgap is about 224kΩ to form a very good low pass filter with great noise reduction performance.

The 35kΩ resistance is used to slow down the reference voltage ramp to avoid inrush current at chip start-up, and the start-up time can be calculated as :

$t_{SS}$ (sec) = 160000 x $C_{NR}$ (F)

It is recommended that the $C_{NR}$ value be larger than 0.01μF to reduce noise, and low-leakage ceramic capacitors are suitable. However, if the $C_{NR}$ value is too large, the start-up time will be extended significantly if the $C_{NR}$ is not fully charged within 2ms and the quick-start switch is opened. The $C_{NR}$ will be charged through a higher resistance of 224kΩ, which will take much longer to complete the start-up process.

## 16.2 Enable and Shutdown Operation

The RTQ2510 goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and bandgap are all turned off, reducing the supply current to only 2μA (max.). If the shutdown mode is not required, the EN pin can be directly tied to VIN pin to keep the LDO on.

## 16.3 Current Limit

The RTQ2510 continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range. Due to the built-in body diode, the pass transistor conducts current when the output voltage exceeds the input voltage. Since the current is not limited, external current protection should be added if the device may work at a reverse voltage state.

## 16.4 Over-Temperature Protection (OTP)

The RTQ2510 has over-temperature protection. When the device triggers the OTP, the device shuts down until the temperature returns to a normal state.

### 16.5 Undervoltage Lockout (UVLO)

The RTQ2510 utilizes an undervoltage lockout circuit to keep the output shutdown until the internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 30μs duration.

# 17 Application Information

***Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.***

The RTQ2510 is a low voltage, low dropout linear regulator with input voltage from 2.2V to 6V and a fixed output voltage from 0.8V to 5.5V.

## 17.1 Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at a specific output current. The dropout voltage $V_{DROP}$ can also be expressed as the voltage drop across the pass-FET at a specific output current ($I_{RATED}$) while the pass-FET is fully operating in the ohmic region, and the pass-FET can be characterized as a resistance $R_{DSON}$. Thus, the dropout voltage can be defined as ($V_{DROP} = V_{VIN} – V_{VOUT} = R_{DSON}$ x $I_{RATED}$).

For normal operation, the suggested LDO operating range is ($V_{VIN} > V_{VOUT} + V_{DROP}$) for good transient response and PSRR ability. Conversely, operating in the ohmic region will severely degrade these performance.

## 17.2 Output Voltage Setting

For the RTQ2510, the voltage on the FB pin sets the output voltage and is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the formula given in the equation below :

$$V_{OUT} = \frac{(R1 + R2)}{R2} \times 0.8$$

Using lower values for R1 and R2 is recommended to reduce the noise injected from the FB pin. Note that R1 is connected from VOUT pin to FB pin, and R2 is connected from FB to GND.

## 17.3 Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the RTQ2510 quiescent current drops to lower than 2μA. Driving the EN pin high (>1.2V, <6V) will turn on the device again. For external timing control (e.g. RC), the EN pin can also be externally pulled to high by adding a 100kΩ or greater resistor from the VIN pin.

## 17.4 Current Limit

The RTQ2510 continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range. Due to the built-in body diode, the pass transistor conducts current when the output voltage exceeds the input voltage. Since the current is not limited, external current protection should be added if the device may operate at a reverse voltage state.

## 17.5 $C_{IN}$ and $C_{OUT}$ Selection

Like any low dropout regulator, the external capacitors of the RTQ2510 must be carefully selected for regulator stability and performance. Using a capacitor of at least 4.7μF is suitable. The input capacitor must be located at a distance of no more than 0.5 inch from the input pin of the chip. Any good quality ceramic capacitor can be used. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it

will provide better PSRR and line transient response.

The RTQ2510 is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with capacitance of at least 4.7μF on the RTQ2510 output ensures stability.

### 17.6 Output Noise

Generally speaking, the dominant noise source is from the internal bandgap for most LDOs. With the noise reduction capacitor connected to the NR pin of the RTQ2510, the noise component contributed from the bandgap will not be significant. Instead, the most significant noise source comes from the output resistor divider and the error amplifier input. For general noise reduction in applications, it is recommended to use a 0.01μF noise-reduction capacitor ($C_{NR}$).

### 17.7 Thermal Considerations

Thermal protection limits power dissipation in the RTQ2510. When the operating junction temperature exceeds 160°C, the OTP circuit initiates the thermal shutdown function and turns off the pass element. The pass element turns on again after the junction temperature decreases by 20°C.

The RTQ2510 output voltage will be close to zero when an output short circuit occurs, as shown in Figure 1. This can reduce the chip temperature and provide maximum safety to end users when an output short circuit occurs.

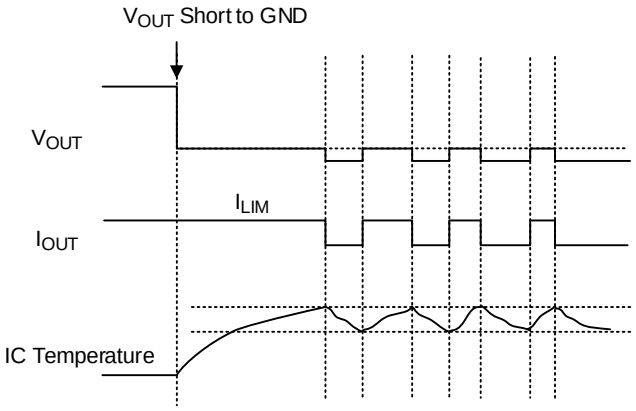



Figure 1. Short-Circuit Protection when Output Short-Circuit Occurs

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a VDFN-8L 3x3 package, the thermal resistance, $\theta_{JA}$, is 45.06°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (45.06°C/W) = 2.22W for a VDFN-8L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

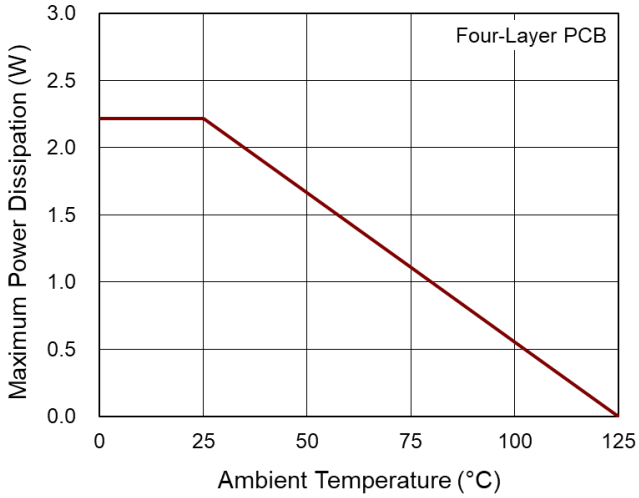



Figure 2. Derating Curve of Maximum Power Dissipation

### 17.8 Layout Considerations

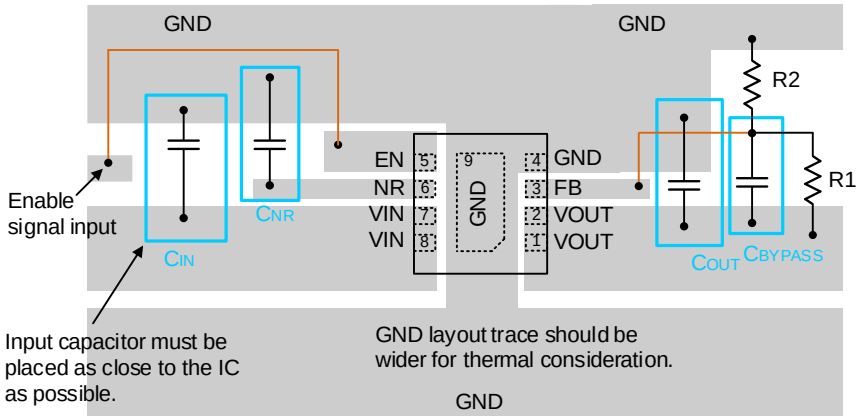
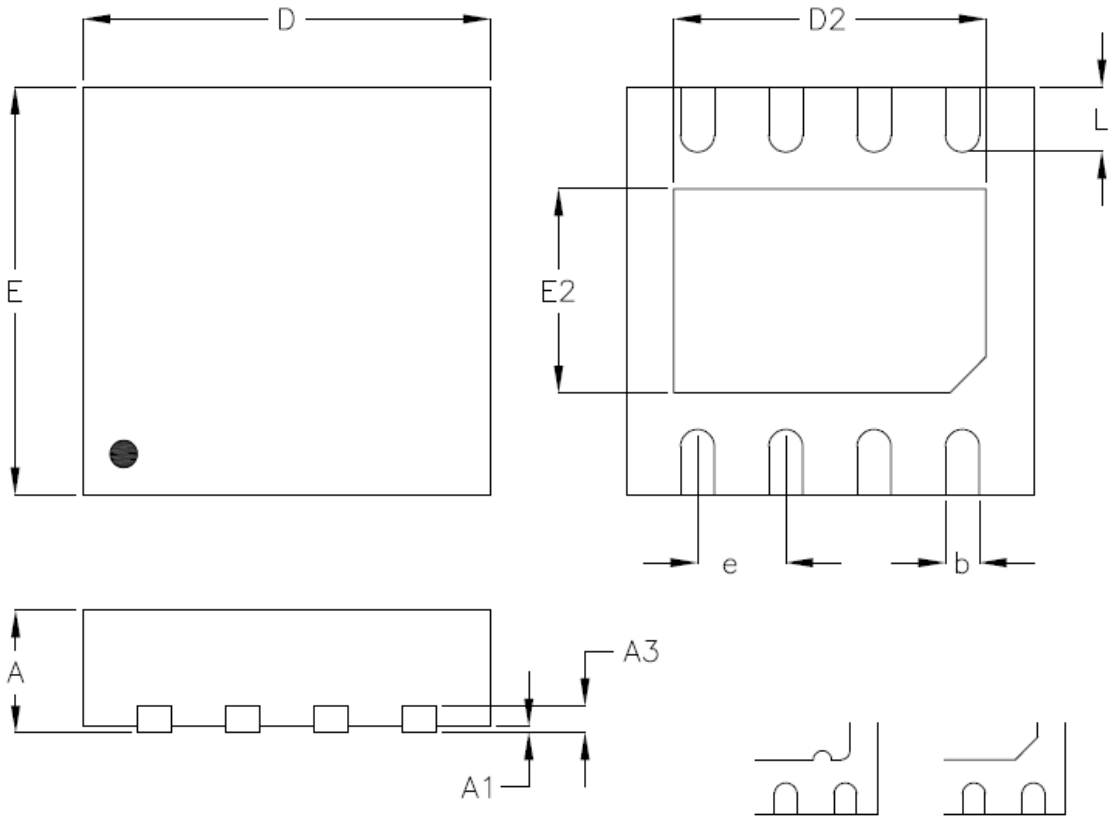



Figure 3. PCB Layout Guide

## 18 Outline Dimension

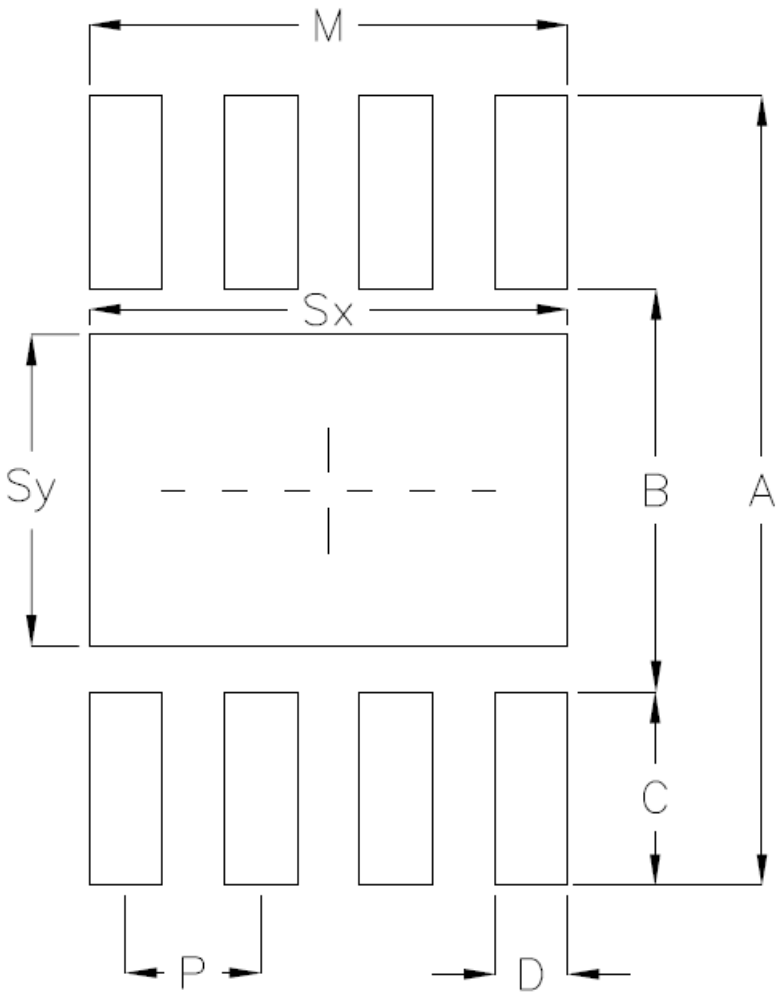



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 0.900 | 0.027 | 0.035 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| D | 2.950 | 3.050 | 0.116 | 0.120 |
| D2 | 2.100 | 2.350 | 0.083 | 0.093 |
| E | 2.950 | 3.050 | 0.116 | 0.120 |
| E2 | 1.350 | 1.600 | 0.053 | 0.063 |
| e | 0.650 | | 0.026 | |
| L | 0.425 | 0.525 | 0.017 | 0.021 |

**V-Type 8L DFN 3x3 Package**

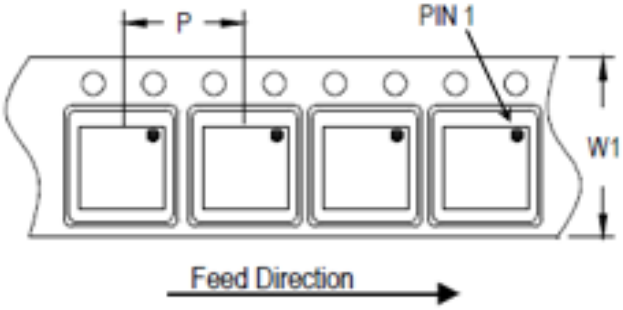
## 19 Footprint Information

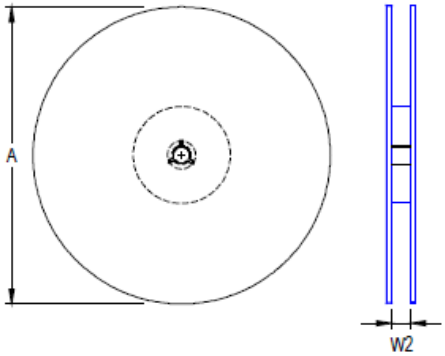


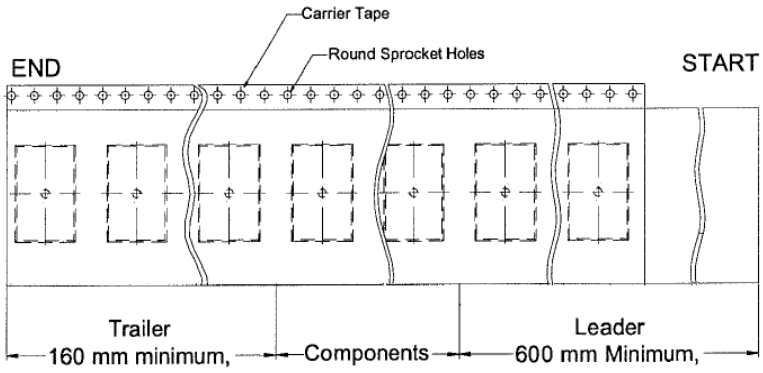

| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | Tolerance |
|---|---|---|---|---|---|---|---|---|---|---|
| | | P | A | B | C | D | Sx | Sy | M | |
| V/W/U/XDFN3*3-8 | 8 | 0.65 | 3.80 | 1.94 | 0.93 | 0.35 | 2.30 | 1.50 | 2.30 | ±0.05 |

# 20 Packing Information

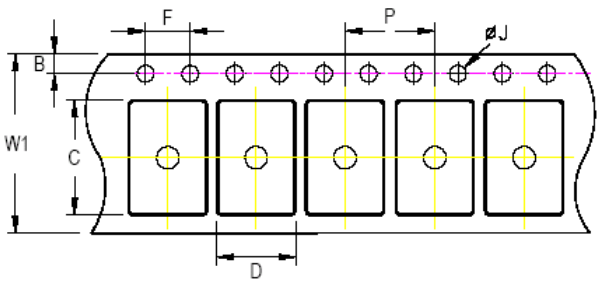
## 20.1 Tape and Reel Data

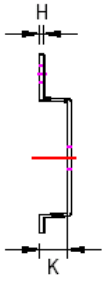



| Package Type | Tape Size (W1) (mm) | Pocket Pitch (P) (mm) | Reel Size (A) | | Units per Reel | Trailer (mm) | Leader (mm) | Reel Width (W2) Min./Max. (mm) |
|---|---|---|---|---|---|---|---|---|
| | | | (mm) | (in) | | | | |
| QFN/DFN 3x3 | 12 | 8 | 180 | 7 | 1,500 | 160 | 600 | 12.4/14.4 |




**C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:**

**- For 12mm carrier tape: 0.5mm max.**

| Tape Size | W1 | P | | B | | F | | ØJ | | H |
|---|---|---|---|---|---|---|---|---|---|---|
| | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Max. |
| 12mm | 12.3mm | 7.9mm | 8.1mm | 1.65mm | 1.85mm | 3.9mm | 4.1mm | 1.5mm | 1.6mm | 0.6mm |

### 20.2 Tape and Reel Packing

| Step | Photo/Description | Step | Photo/Description |
|---|---|---|---|
| 1 |  Reel 7” | 4 |  3 reels per inner box **Box A** |
| 2 |  HIC & Desiccant (1 Unit) inside | 5 |  12 inner boxes per outer box |
| 3 |  Caution label is on backside of Al bag | 6 |  Outer box **Carton A** |

| Container / Package | Reel | | Box | | | | Carton | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Size | Units | Item | Size(cm) | Reels | Units | Item | Size(cm) | Boxes | Unit |
| QFN/DFN 3x3 | 7” | 1,500 | Box A | 18.3*18.3*8.0 | 3 | 4,500 | Carton A | 38.3*27.2*40.0 | 12 | 54,000 |
| | | | Box E | 18.6*18.6*3.5 | 1 | 1,500 | For Combined or Partial Reel. | | | |

### 20.3 Packing Material Anti-ESD Property

| Surface Resistance | Aluminum Bag | Reel | Cover tape | Carrier tape | Tube | Protection Band |
|---|---|---|---|---|---|---|
| $\Omega/cm^2$ | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** |

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## 21 Datasheet Revision History

| Version | Date | Description | Item |
|---|---|---|---|
| 03 | 2024/3/14 | Modify | Ordering Information on P1<br>Absolute Maximum Ratings on P5<br>Recommended Operating Conditions on P5<br>Thermal Information on P5<br>Note 4, Note 5 on P5<br>Application Information on P14, 5 |