#### E Technical Documentation

# <u>RICHTEK®</u>

## **RT9718**

Sample &

Buy

## **Overvoltage Protection IC**

### 1 General Description

The RT9718 is an integrated circuit optimized to protect low voltage system from abnormally high input voltages (up to 30V). The IC monitors the input voltage, battery voltage, and charging current to ensure all three parameters operate within the normal range. When the input voltage exceeds a certain Overvoltage Protection (OVP) threshold voltage level, the IC will turn off the power MOSFET within 1 $\mu$ s to remove the power before any damage occurs. The RT9718 can also provide a voltage output in the absence of battery.

The current in the power MOSFET is limited to prevent the battery from being charged with excessive current. The current limit can be programmed by an external resistor connected between the ILIM and GND pins. The Overcurrent Protection (OCP) function includes a 4-bit binary counter that accumulates during an OCP event. If the total count reaches 16 consecutive times, the power MOSFET is turned off permanently unless the input power is recycled.

The IC also monitors the battery voltage. If the battery voltage exceeds 4.35V and lasts for more than  $180\mu$ s blinking time, the RT9718 will turn off the MOSFET. The internal logic control will permanently turn off the power MOSFET when the battery overvoltage event occurs 16 consecutive times.

The RT9718 is available in a WDFN package. The recommended junction temperature range is  $-40^{\circ}$ C to 125°C, and the ambient temperature range is  $-40^{\circ}$ C to 85°C.

### 2 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

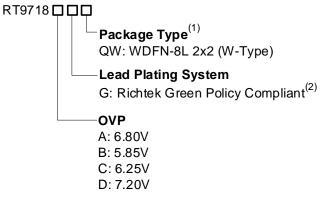
### 3 Features

- Fully Integrated Protection Functions
  - Programmable OCP
  - Input OVP
  - Battery OVP
- Withstand High Input Voltage up to 30V
- Overvoltage Turn-Off Time Less than 1μs
- High Accuracy Protection Thresholds
- Over-Temperature Protection
- High Immunity of False Triggering Under Transients
- Warning Indication Output
- Enable Input
- Thermal Enhanced WDFN Package

### 4 Applications

- Cellular Phones
- Digital Cameras
- Smartphones
- Portable Instruments

## 5 Ordering Information



#### Note 1.

- Marked with <sup>(1)</sup> indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with <sup>(2)</sup> indicated: Richtek products are Richtek Green Policy compliant.



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### 6 Pin Configuration

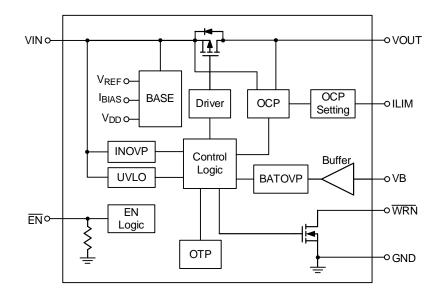
(TOP VIEW)

WDFN-8L 2x2

### 7 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Input power source. The VIN can withstand input voltages up to 30V.
2	GND	Analog ground.
3	NC	No internal connection.
4	WRN	This is an open-drain logic output that turns low when any protection event occurs.
5	EN	Chip enable (active low). To enable the IC, pull this pin low or leave it floating. To disable the IC, force this pin to a high state.
6	VB	Battery voltage monitoring input. This pin is connected to the positive terminal of the battery pack via an isolation resistor.
7	ILIM	Overcurrent Protection (OCP) threshold setting pin. To set the OCP threshold, connect a resistor between this pin and ground (GND).
8	VOUT	Output through the power MOSFET.
9 (Expose Pad)	GND	The exposed pad should be soldered to a large area on the PCB and connected to the ground (GND) to ensure maximum thermal dissipation.

## 8 Functional Block Diagram



### 9 Absolute Maximum Ratings

#### (<u>Note 2</u>)

Supply Input Voltage, VIN	0.3V to 30V
• VOUT, VB	–0.3V to 7V
Other Pins	–0.3V to 6V
• Power Dissipation, $P_D @ T_A = 25^{\circ}C$	
WDFN-8L 2x2	0.606W
Package Thermal Resistance (Note 3)	
WDFN-8L 2x2, θJA	165°C/W
• WDFN-8L 2x2, θJA	20°C/W
Junction Temperature	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Storage Temperature Range	–65°C to 150°C
• ESD Susceptibility ( <u>Note 4</u> )	
HBM (Human Body Model)	2kV

- **Note 2**. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
- **Note 3**.  $\theta_{JA}$  is simulated under natural convection (still air) at  $T_A = 25^{\circ}C$  with the component mounted on a low effective-thermalconductivity single-layer test board on a JEDEC 51-3 thermal measurement standard.  $\theta_{JC}$  is simulated at the bottom of the package.
- Note 4. Devices are ESD sensitive. Handling precautions are recommended.

### **10 Recommended Operating Conditions**

#### (<u>Note 5</u>)

Junction Temperature Range	–40°C to 125°C
Ambient Temperature Range	

Note 5. The device is not guaranteed to function outside its operating conditions.

### **11 Electrical Characteristics**

( $V_{IN}$  = 5V,  $T_A$  = 25°C, unless otherwise specified.)

Parameter	neter Symbol Te		Min	Тур	Max	Unit
Power-On Reset						
		RT9718A	4		6.5	
Operation Voltage	VIN	RT9718B	4		5.5	
Operation Voltage		RT9718C	4		5.9	V
		RT9718D	4		6.9	
Power-On Reset Voltage	VPOR	VPOR rising	2.5	2.7	2.9	V
Power-On Reset Deglitch Time	tDEGLITCH_POR	2		8		ms

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HysteresisImage: hysteresisImage: hysteresisImage: hysteresisImage: hysteresisImage: hysteresisVIN Overvoltage Protection Propagation Delay TimetDLY_VIN_OVP_ PDVouT = VIN x 80%1 $\mu$ sVIN Overvoltage Protection Recovery Delay TimetDLY_VIN_OVP_ RDRD8msOvercurrent Protection ThresholdlocpAs RILIM = 25k\Omega0.9311.07AOvercurrent Protection Blanking TimetbLK_OCPAs RILIM = 25kΩ0.9311.07AOvercurrent Protection Recover Delay TimetbLK_OCP64msVB Overvoltage Protection Rising ThresholdVVB_OVP_RVB rising4.34.354.4VVB Overvoltage Protection HysteresisVVB_OVP_HYSHysteresis30mVVB Overvoltage Protection Falling ThresholdVVB_OVP_FHysteresis30mVVB Overvoltage Protection Blanking TimeVUB_OVP_FHysteresis180 $\mu$ sVB Overvoltage Protection Blanking TimetbLK_VB_OVP_F180 $\mu$ sVB Overvoltage Protection Blanking TimetbLK_VB_OVP_F180 $\mu$ sVB Overvoltage Protection Recover Delay TimetbLK_VB_OVP_F180 $\mu$ sVB Overvoltage Protection Recover Delay TimetbLK_VBVVB=4.4V20nAOver-Temperature Protection	Parameter	Symbol	Test Condit	Min	Тур	Max	Unit	
Shutdown Current         IsHDN $\overline{EN} = 5V$ 65         95 $\muA$ Protections $VIN Overvoltage Protection Threshold         VIN Overvoltage Protection Recovery Delay Time         VIN Overvoltage Protection Protection Protection Protection Protection Protection Protection Recovery Delay Time         VOUT = VIN \times 80\%          6.60         10.0         mV           VIN Overvoltage Protection Recovery Delay Time         UIV_VN_OVP_P VOUT = VIN \times 80\%          8.8          ms           VIN Overvoltage Protection Recovery Delay Time         UIV_VOV_OVP_R VOUT = VIN \times 80\%          8.8          ms           Overcurrent Protection Recovery Delay Time         UIV_VOV_OVP_R VOUT = VIN \times 80\%         0.93         1         1.07         A           Overcurrent Protection Recovery Delay Time         UIV_OOP_R AIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII$	<b>a</b>	VUVLO_F	VuvLo falling	2.45		2.75	V	
Shuldwin Current         ISHDN         EN = 5V         -         65         95         Vin           Protections         VIN_OVP $V_{IN_OVP}$ $V_{IN_OVP}$ $RT9718A$ 6.6         6.8         7           VIN Overvoltage Protection $V_{IN_OVP}$ $V_{IN_OVP}$ $V_{IN_OVP}$ $RT9718D$ 7         7.2         7.4           VIN Overvoltage Protection $V_{IN_OVP}$ $V_{OUT} = V_{IN_N} \times 80^{\circ}$ 60         100         mW           VIN Overvoltage Protection $DU_{V_UN_OVP_}$ $V_{OUT} = V_{IN_N} \times 80^{\circ}$ 60         100         mW           VIN Overvoltage Protection $DU_{V_UN_OVP_}$ $V_{OUT} = V_{IN_N} \times 80^{\circ}$ 7.4         1 $\mu_S$ Qvercurrent Protection $DU_{V_UN_OVP_}$ $NS$ 7.4         1.07         A           Qvercurrent Protection $I_{DCP_}$ $A_S R_{ILIM} = 25k\Omega$ 0.93         1         1.07         A           Qvercurrent Protection $I_{DUVOPRR$ $RS$ R $R$ R           Qvercurrent Protection $I_{DUVOPRR$ $VB_I$	Quiescent Current	lq	ĒN = 0V			500	600	
$ \begin{array}{ c c c c c } \mbox{Vin Overvoltage Protection Threshold} & Vin_OVP & Vin_Tising & RT9718A & 6.6 & 6.8 & 7 \\ \hline RT9718B & 5.6 & 5.85 & 6 \\ \hline RT9718D & 7 & 7.2 & 7.4 \\ \hline Vin Overvoltage Protection Poperation Propagation Delay Time Pop & VouT = Vin x 80% & & & 8 & & ms \\ \hline \mbox{Vin Overvoltage Protection Pop & VouT = Vin x 80% & & & 1 & \mus \\ \hline \mbox{Vin Overvoltage Protection Pop & RD & & & 8 & & ms \\ \hline \mbox{Vin Overvoltage Protection Pop & RD & & & 8 & & ms \\ \hline \mbox{Vin Overvoltage Protection RD & IoLY_VIN_OVP & As RILLM = 25K\Omega & 0.93 & 1 & 1.07 & A \\ \hline \mbox{Overcurrent Protection Rbins & IoLY_OCP_RD & & & 180 & & \mus \\ \hline \mbox{Overcurrent Protection Protection Rbins & Vin_OVP_RD & VB rising & & 64 & & ms \\ \hline \mbox{Overcurrent Protection Protection Rising Threshold & VVB_OVP_R & VB rising & 4.3 & 4.35 & 4.4 & V \\ VB Overvoltage Protection & VVB_OVP_R & VB rising & 4.3 & 4.35 & 4.4 & V \\ VB Overvoltage Protection & VVB_OVP_R & VB rising & & - & 88 & & ms \\ VB Overvoltage Protection & VVB_OVP_F & Hysteresis & & 300 & & mV \\ VB Overvoltage Protection & VVB_OVP_F & & - & 88 & & ms \\ VB Overvoltage Protection & VVB_OVP_F & & - & 88 & & ms \\ VB Overvoltage Protection & IbLY_VB_OVP_F & & - & 20 & nA \\ VB Overvoltage Protection & IbLY_VB_OVP_R & Nysteresis & & 20 & nA \\ VB Overvoltage Protection & TOTP & Rising & & 20 & nA \\ Over-Temperature Protection & TOTP & Rising & & 20 & nA \\ Over-Temperature Protection & TOTP_R & Rising & & - & 20 & ms \\ The VB Pin Leakage Current & IbLY_OTP_RD & & & 88 & & ms \\ Over-Temperature Protection & ToTP_R & Rising & & - & 88 & & ms \\ Over-Temperature Protection & ToTP_R & Rising & & - & 88 & & ms \\ Over-Temperature Protection & ToTP_R & Hysteresis & & 88 & & ms \\ Over-Temperature Protection & ToTP_R & Rising & & - & 88 & & ms \\ Over-Temperature Protection & ToTP_R & Nysteresis & & - & 88 & & ms \\ Over-Temperature Protection & ToTP_R & Nysteresis & $	Shutdown Current	ISHDN	$\overline{EN}$ = 5V		65	95	μΑ	
$ \begin{array}{ c c c c c } \mbox{Vin Over voltage Protection Threshold } & Vin_OVP & Vin Tising & \hline RT9718B & 5.6 & 5.85 & 6.6 \\ \hline R19718C & 6.05 & 6.25 & 6.45 \\ \hline R19718D & 7 & 7.2 & 7.4 \\ \hline Vin Overvoltage Protection & Vin_OVP_HYS & & & & & & & & & & & & & & & & & & &$	Protections							
$ \begin{array}{ c c c c c c } \hline Nn or equation of the state o$				RT9718A	6.6	6.8	7	
$\begin{array}{ c c c c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		Vin ovp	Vin rising	RT9718B	5.6	5.85	6	V
VIN Overvoltage Protection Hysteresis         VIN_OVP_HYS          60         100         mV           VIN Overvoltage Protection Propagation Delay Time         DLV_VIN_OVP_ PD         VOUT = VIN x 80%           1         µs           VIN Overvoltage Protection Recovery Delay Time         DLV_VIN_OVP_ PD         VOUT = VIN x 80%          8          ms           Overcurrent Protection Threshold         IoCP         As RILIM = 25kΩ         0.93         1         1.07         A           Overcurrent Protection Blanking Time         IbLK_OCP         As RILIM = 25kΩ         0.93         1         1.07         A           Overcurrent Protection Recover Delay Time         IbLK_OCP         As RILIM = 25kΩ         0.93         1         1.07         A           Overcurrent Protection Recover Delay Time         IbLK_OCP         As RILIM = 25kΩ         0.93         1         1.07         A           VB Overvoltage Protection Recover Delay Time         IbLK_OCP_RD          180          ms           VB Overvoltage Protection Rising Threshold         VVB_OVP_F         Ibls         4.225          -         V           VB Overvoltage Protection Blanking Time         VB_OVP_OVP_F          8	Threshold		Vin Holling	RT9718C	6.05	6.25	6.45	v
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Propagation Delay Time         PD         VOUL = VIN X 60%          I         I         II           VIN Overvoltage Protection Recovery Delay Time         tDLY_VIN_OVP_R RD          88          ms           Overcurrent Protection Increshold         locp         As RILIM = 25kΩ         0.93         1         1.07         A           Overcurrent Protection Blanking Time         tbLK_OCP         Image: Signature          64          ms           Overcurrent Protection Recover Delay Time         tbLY_OCP_RD         VB rising         4.3         4.35         4.4         V           VB Overvoltage Protection Rising Threshold         VVB_OVP_R         VB rising         4.3         4.35         4.4         V           VB Overvoltage Protection Rysteresis         VVB_OVP_R         VB rising         4.225           V           VB Overvoltage Protection Recover Delay Time         Vb_OVP_VF         Image: Signature          4.225           V           VB Overvoltage Protection Recover Delay Time         tbLK_VB_OVP_R         Image: Signature          8          ms           VB Overvoltage Protection Recover Delay Time         tbLK_VB_OVP_R         Vp_EOVP_R	-	VIN_OVP_HYS				60	100	mV
Recovery Delay Time         RD          0          0          11           Overcurrent Protection Threshold         locp         As RILIM = 25kΩ         0.93         1         1.07         A           Overcurrent Protection Blanking Time         tbLK_OCP          180          μs           Overcurrent Protection Recover Delay Time         tbLY_OCP_RD         VB fising          64          ms           VB Overvoltage Protection Rising Threshold         VVB_OVP_R         VB rising         4.3         4.35         4.4         V           VB Overvoltage Protection Falling Threshold         VVB_OVP_F         Hysteresis          30          mv           VB Overvoltage Protection Falling Threshold         VVB_OVP_F         Hysteresis          30          W           VB Overvoltage Protection Blanking Time         VbL_V_VB_OVP_F          180          μs           VB Overvoltage Protection Blanking Time         tbLK_VB_OVP          180          ms           VB Overvoltage Protection Blanking Time         tbLK_VB_OVP          180          ms           VB			Vout = Vin x 80%				1	μs
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Blanking TimeBLR_OCPIndext of the second seco	-	I <sub>OCP</sub>	As $R_{ILIM} = 25k\Omega$		0.93	1	1.07	А
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Falling ThresholdVVB_OVP_F4.223VVB Overvoltage Protection Blanking TimetBLK_VB_OVP180µsVB Overvoltage Protection Recover Delay TimetDLY_VB_OVP_ RD8msThe VB Pin Leakage CurrentILK_VBV <sub>VB</sub> = 4.4V20nAOver-Temperature Protection ThresholdToTPRising140°COver-Temperature Protection HysteresisToTP_HYSHysteresis8°COver-Temperature Protection Recover Delay TimeToTP_RDHysteresis8°COver-Temperature Protection Recover Delay TimetDLY_OTP_RD8msOver-Temperature Protection Recover Delay TimetbLY_OTP_RD8msOver-Temperature Protection Soft-Start Timetss_OTP8msEN Input Voltage Logic-HighVIH_EN1.5V		V <sub>VB_OVP_HYS</sub>	Hysteresis			30		mV
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Hysteresis20COver-Temperature Protection Recover Delay TimetDLY_OTP_RD8msOver-Temperature Protection Soft-Start Timetss_OTP8msLogicEN Input Voltage Logic-HighVIH_EN1.5V		T <sub>OTP</sub>	Rising			140		°C
Recover Delay Time       IDLY_OTP_RD        8        Ims         Over-Temperature Protection Soft-Start Time       tss_OTP        8        ms         Logic       EN Input Voltage Logic-High       VIH_EN       1.5         V		T <sub>OTP_HYS</sub>	Hysteresis			20		°C
Soft-Start Time     ISS_OTP     ISS_OTP       Logic       EN Input Voltage Logic-High     VIH_EN       1.5		tDLY_OTP_RD				8		ms
EN Input Voltage Logic-High     VIH_EN     1.5      V		tss_otp				8		ms
	Logic						•	
EN Input Voltage Logic-Low VIL_EN 0.4 V	EN Input Voltage Logic-High	V <sub>IH_EN</sub>			1.5			V
	EN Input Voltage Logic-Low	V <sub>IL_EN</sub>					0.4	V

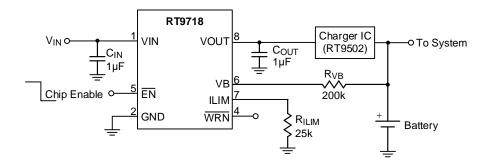


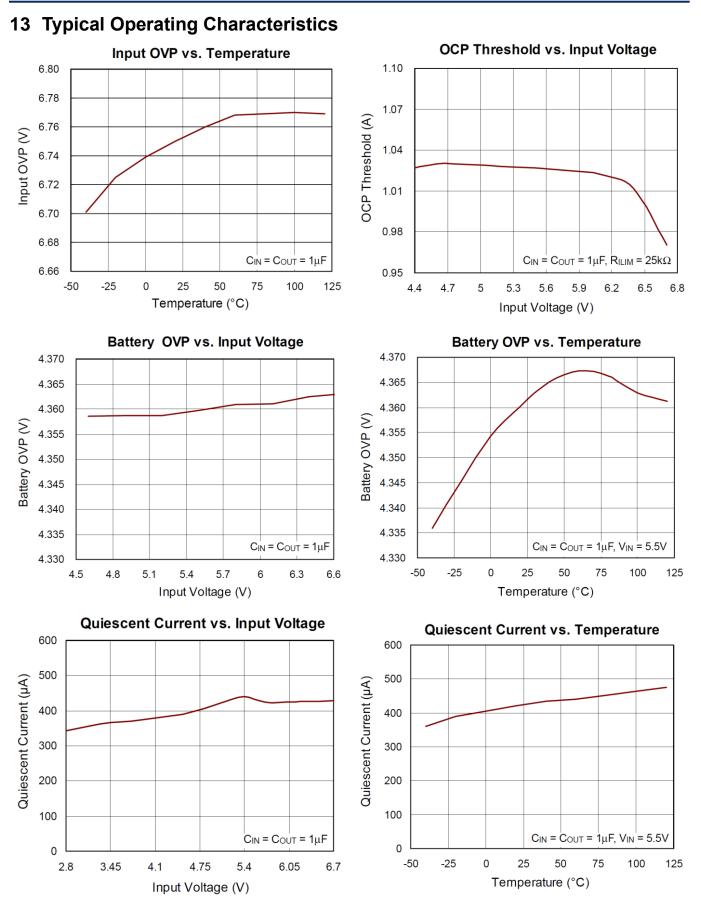


Parameter	Symbol	Test Conditions	Min	Тур	Мах	Unit
EN Internal Pull-Down Resistor	Rpd_en		100	200	400	kΩ
WRN Output Voltage Logic- Low	V <sub>OH_WRN</sub>	Sink 5mA		0.35	0.8	V
WRN Output Logic-High Leakage Current	ILK_WRN				1	μA
Power MOSFET						
On-Resistance	R <sub>ON</sub>	I <sub>OUT</sub> = 500mA, 4.3V < V <sub>IN</sub> < 6.5V		200	300	mΩ



## **12 Typical Application Circuit**

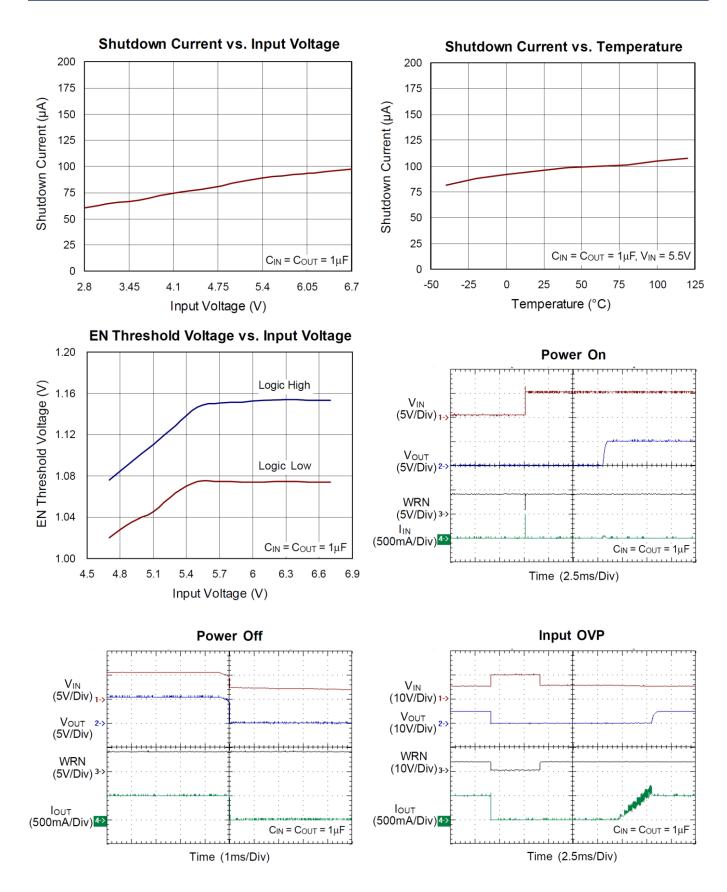




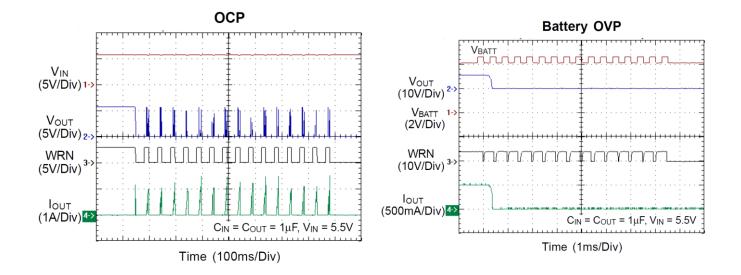
**RT9718** 

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### 14 Application Information

(<u>Note 6</u>)

#### 14.1 Power Up

The RT9718 features a power-on reset (POR) threshold of 2.7V with a built-in hysteresis of 100mV. Before the input voltage reaches this POR threshold, the RT9718 remains off. Once the input voltage exceeds the POR threshold, the RT9718 will initiate a delay of 8ms, after which the soft-start process is activated. The 8ms delay allows any transients at the input to settle during a hot insertion of the power supply before the IC begins operation.

During the soft-start transition, the RT9718 gradually turns on the internal MOSFET to minimize the inrush current.

#### 14.2 Enable Control

The RT9718 features an enable (EN) input. When the  $\overline{EN}$  pin is pulled to a logic high (> 1.5V), the RT9718 will be shut down. When the  $\overline{EN}$  pin is pulled to a logic low (< 0.4V), the RT9718 will be powered on. The  $\overline{EN}$  pin includes an internal pull-down resistor, which mean leaving the  $\overline{EN}$  pin floating will enable the IC.

#### 14.3 Warning Indication Output

The WRN pin is an open-drain output that signals LOW when any protection event occurs, including Input Overvoltage Protection (OVP), Output Overcurrent Protection (OCP), and Battery OVP. Once the protection events are cleared, the WRN pin signals HIGH.

#### 14.4 Over-Temperature Protection (OTP)

The RT9718 monitors its internal temperature to prevent thermal failures. The chip turns off the MOSFET when the internal temperature reaches 140°C. The IC will resume operation once the internal temperature has cooled down by 20°C.

#### 14.5 Input Overvoltage Protection

The RT9718 monitors the input voltage to prevent system failures due to excessive input voltage. The input Overvoltage Protection (OVP) threshold of the RT9718 is set by an internal resistor. When the input voltage exceeds the threshold, the RT9718 outputs a logic signal to turn off the internal MOSFET within 1 $\mu$ s, protecting the electronics in the handheld system from high voltage damage. The hysteresis for the input OVP threshold is 100mV. Once the input voltage returns to normal operating rage, the RT9718 re-enables the MOSFET.

#### 14.6 Battery Overvoltage Protection

The battery Overvoltage Protection (OVP) threshold voltage is typically set at 4.35V, and the RT9718 includes a builtin 180 $\mu$ s blanking time to prevent transient voltage from triggering the battery OVP. If the OVP condition persists after 180 $\mu$ s, the internal MOSFET will be turned off and the WRN pin will output a LOW signal. The battery OVP threshold features a built-in hysteresis of 30mV. Additionally, the control logic incorporates a 4-bit binary counter. Should the battery overvoltage event occurs 16 consecutive times, the MOSFET will be permanently turned off unless the input power or the enable pin is reset.

#### 14.7 RvB Selection

The RT9718 monitors the battery voltage through the VB pin. The RT9718 will be turned off when the battery voltage exceeds the 4.35V battery Overvoltage Protection (OVP) threshold. The VB pin should be connected to the positive terminal of the battery pack via an isolation resistor ( $R_{VB}$ ), which is a critical component. The  $R_{VB}$  affects various parameters, such as the battery OVP threshold accuracy and leakage current at the VB pin. Generally, reducing the

value of R<sub>VB</sub> decreases the battery OVP threshold error, but this also increases the leakage current at the VB pin. Therefore, finding a balance between the battery OVP threshold accuracy and the VB pin leakage current is essential. A resistance value ranging from  $200k\Omega$  to  $1M\Omega$  is permissible for R<sub>VB</sub>.

#### 14.8 Overcurrent Protection (OCP)

The RT9718 monitors the output current to prevent the output shorts or charging the battery with excessive current. The Overcurrent Protection (OCP) threshold can be set via the ILIM pin. The RT9718 features a built-in 180 $\mu$ s delay time to prevent transient noise from triggering the OCP. If the OCP condition persists for 180 $\mu$ s, the internal MOSFET will be turned off, and the WRN pin will output a LOW signal. If the OCP event occurs 16 consecutive times, the internal MOSFET will be permanently turned off unless the input power is recycled or the enable pin is toggled.

The OCP threshold can be set by the resistor connected between the ILIM pin and GND. The OCP threshold can be calculated using the following equation:

 $\mathsf{I_{OCP}} = \frac{25000}{\mathsf{RILIM}}$ 

#### 14.9 Capacitor Selection

To achieve optimal performance with the RT9718, selecting appropriate peripheral capacitors is crucial. These capacitors influence parameters such as the input inrush current and input overshoot voltage. Generally, increasing the input capacitance CIN is necessary to reduce the input overshoot voltage. However, this also results in an increase in the input inrush current. There are two scenarios that can lead to the input overshoot voltage: the first is when the AC adapter is hot-plugged, and the second is when the RT9718 experiences a step-down change. The cable between the AC adapter output and the handheld system input possesses parasitic inductance, which contributes to the input overshoot voltage. Typically, the input overshoot voltage ranges from 1.5 to 2 times the input voltage. It is recommended to use a capacitance of  $1\mu$ F for both CIN and COUT, with a rated voltage that is higher than 1.5 to 2 times the operating voltage.

#### 14.10 Thermal Considerations

Thermal protection limits power dissipation in the RT9718. When the operation junction temperature exceeds 140°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass elements turn on again after the junction temperature cools by 20°C.

The junction temperature should never exceed the absolute maximum junction temperature  $T_{J(MAX)}$ , listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

#### $\mathsf{P}\mathsf{D}(\mathsf{M}\mathsf{A}\mathsf{X}) = \big(\mathsf{T}\mathsf{J}(\mathsf{M}\mathsf{A}\mathsf{X}) - \mathsf{T}\mathsf{A}\big) \; / \; \theta \mathsf{J}\mathsf{A}$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance,  $\theta_{JA}$ , is highly package dependent. For a WDFN-8L 2x2 package, the thermal resistance,  $\theta_{JA}$ , is 165°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T<sub>A</sub> = 25°C can be calculated as below:

 $P_{D(MAX)} = (125^{\circ}C - 25^{\circ}C) / (165^{\circ}C/W) = 0.606W$  for a WDFN-8L 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed  $T_{J(MAX)}$  and the thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

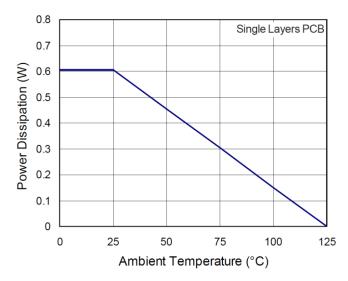
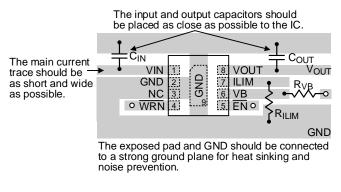


Figure 1. Derating Curve of Maximum Power Dissipation

#### 14.11 Layout Considerations

For best performance of the RT9718 series, the following guidelines should be strictly adhered to:

- Input and output capacitors must be placed close to the IC and connected to ground plane to minimize noise coupling.
- The GND and exposed pad should be connected to a robust ground plane to serve a heat sink.
- Main current traces should be kept as short and as wide as possible to reduce resistance and improve current handling.

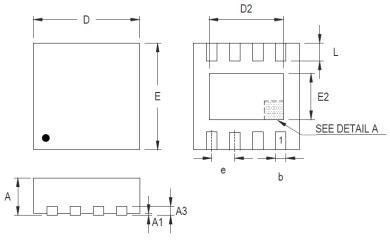


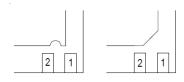


**Note 6**. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

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### **15 Outline Dimension**





DETAIL A Pin #1 ID and Tie Bar Mark Options

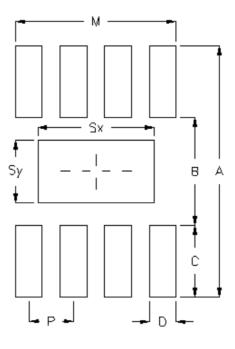
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Cumhal	Dimensions I	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
А	0.700	0.800	0.028	0.031	
A1	0.000	0.050	0.000	0.002	
A3	0.175	0.250	0.007	0.010	
b	0.200	0.300	0.008	0.012	
D	1.950	2.050	0.077	0.081	
D2	1.000	1.250	0.039	0.049	
E	1.950	2.050	0.077	0.081	
E2	0.400	0.650	0.016	0.026	
е	0.5	500	0.0	)20	
L	0.300	0.400	0.012	0.016	

W-Type 8L DFN 2x2 Package



## 16 Footprint Information

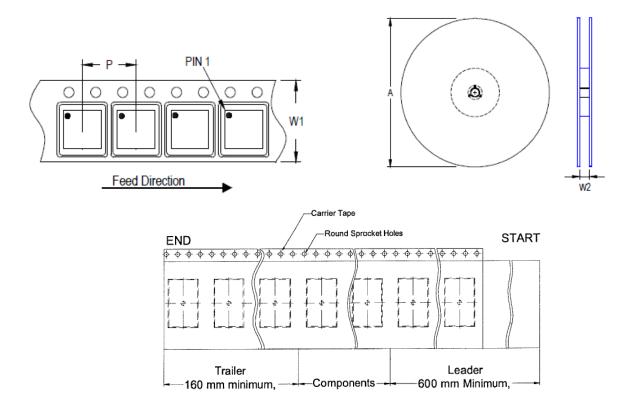


Backago	Number			Footp	orint Dim	nension	(mm)			Tolerance
Package	of Pin	Р	А	В	С	D	Sx	Sy	М	TOIETATICE
V/W/U/XDFN2*2-8	8	0.50	2.80	1.20	0.80	0.30	1.30	0.70	1.80	±0.05

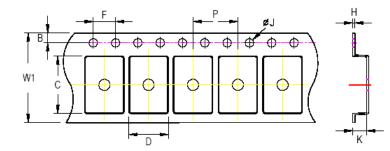
### **17 Packing Information**

#### 17.1 Tape and Reel Data

17.1.1 2500 Units per Reel



Package Type	Tape Size	Pocket Pitch	Reel Size (A)		Units	Trailer	Leader	Reel Width (W2)
	(W1) (mm)	(P) (mm)	(mm) (in)		per Reel	(mm)	(mm)	Min/Max (mm)
(V, W) QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

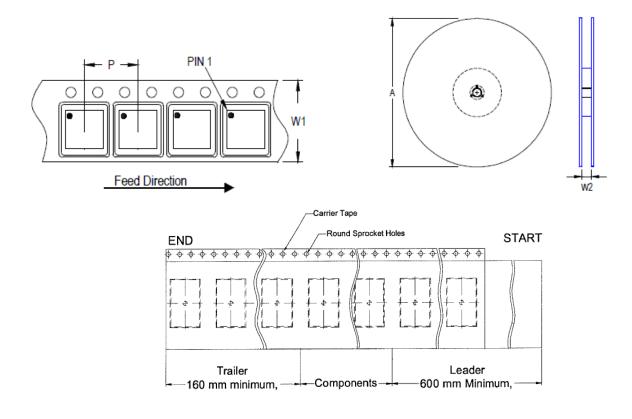
Tana Siza	W1	F	D	E	3	F	=	Q	) M	k	<	Н
Tape Size	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

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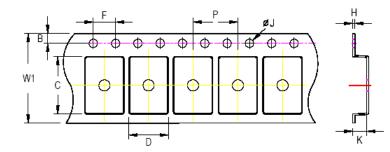




17.1.2 3000 Units per Reel



De de como Trace	Tape Size	Pocket Pitch	Reel Size (A)		Units	Trailer	Leader	Reel Width (W2)	
Package Type	(W1) (mm)	(P) (mm)	(mm)	(in)	per Reel	(mm)	(mm)	Min/Max (mm)	
(V, W) QFN/DFN 2x2	8	4	180	7	3,000	160	600	8.4/9.9	



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tana Siza	W1	Р		В		F		ØJ		К		Н
Tape Size	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

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#### 17.2 Tape and Reel Packing

#### 17.2.1 2500 Units per Reel

Step	Photo/Description	Step	Photo/Description
1	Reel 7"	4	3 reels per inner box <b>Box A</b>
2	HIC & Desiccant (1 Unit) inside	5	12 inner boxes per outer box
3	Caution label is on backside of Al bag	6	Outer box Carton A

Container	Reel		Вох			Carton			
Package	Size	Units	Item	Reels	Units	Item	Boxes	Unit	
(V, W)	7"	2 000	Box A	3	9,000	Carton A	12	108,000	
QFN & DFN 2x2	7"	3,000	Box E	1	3,000	For C	combined or Partial	Reel.	

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#### 17.2.2 3000 Units per Reel

Step	Photo/Description	Step	Photo/Description		
1		4			
	Reel 7"		3 reels per inner box <b>Box A</b>		
2		5			
	HIC & Desiccant (1 Unit) inside		12 inner boxes per outer box		
3		6	RICHTEK IMPARTAR REALER		
	Caution label is on backside of Al bag		Outer box Carton A		

Container	Reel		Вох			Carton			
Package	Size	Units	Item	Reels	Units	Item	Boxes	Unit	
(V, W)	7"	0.500	Box A	3	7,500	Carton A	12	90,000	
QFN & DFN 2x2	<i>("</i>	<i>["</i>	2,500	Box E	1	2,500	For C	combined or Partial	Reel.

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#### 17.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
$\Omega/cm^2$	10⁴ to 10¹¹	10 <sup>4</sup> to 10 <sup>11</sup>				

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### **18 Datasheet Revision History**

Version	Date	Description	Item
05	2024/11/5	Modify	General Description on page 1 - Added the description of temperature Ordering Information on page 1 - Updated description - Added note Electrical Characteristics on page 4, 5, 6 - Updated the parameter and symbol Application Information on page 13 - Added declaration Footprint Information on page 15 - Updated information Packing Information on page 16, 17, 18 - Updated information