RICHTEK®

RT9492

5A 2 to 4 Cell Buck-Boost Switching Battery Charger

1 General Description

The RT9492 is a comprehensive solution that integrates a 5A buck-boost battery charger and system power path management device for 2 to 4 cell Li-Ion and Li-polymer batteries. Its low impedance power path optimizes switch-mode operation efficiency, which not only reduces battery charging time and extends battery life during the discharging phase. The inclusion of an I^2C serial interface allows for a wide range of charging parameters and system settings to be programmed, making the RT9492 a versatile option for various applications.

The recommended junction temperature range is –40°C to 130°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT9492 □□□

Pin 1 Orientation
(2): Quadrant 2, Follow EIA-481

Package Type(1)
QVF: VQFN-29TL 4x4 (FC) (V-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

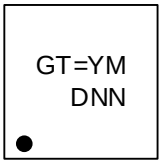
3 Applications

- Smart Phones/Tablets/Chrome Books
- Drones
- Portable Devices and Accessories

4 Features

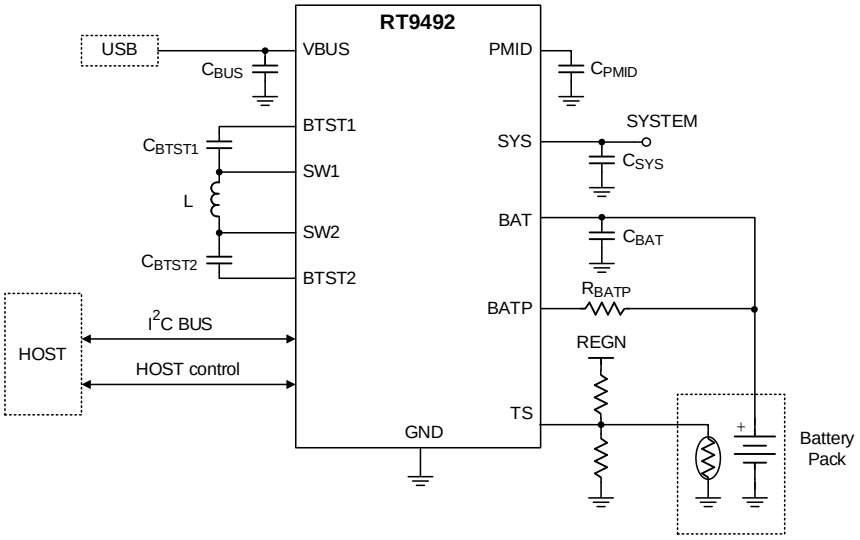
- **Programmable Frequencies: 750kHz/1MHz/1.5MHz**
  - **96.7% Charge Efficiency at 2A with 9V Input and 8V Battery**
  - **Support 3.6V to 24V Input Voltage Range**
  - **Average Input Current Regulation (AICR)**
  - **Minimum Input Voltage Regulation (MIVR)**
- **Support USB On-The-Go (OTG)**
  - **93.4% OTG Efficiency at 2A with 8.4V Battery and 5V Output**
  - **Output Voltage with 10mV Resolution to Support USB-PD**
  - **BAT Current Limit Regulation (BCLR)**
- **Support Dual Input Selection**
- **Support BC1.2, Host Mode and Fast Role Swap (FRS)/Seamless Transition**
- **Support 11-Channel, 16-bit ADC**
- **Low Battery Quiescent Current**
- **High Accuracy for Charger CV and ICHG**
- **Protection**
  - **Over-Temperature Protection (OTP)**
  - **Junction Thermal Regulation (JTR)**
  - **Input Protection (VAC OVP/VBUS OVP/OCP)**
  - **Battery Overvoltage Protection (VBAT OVP)**
  - **System Voltage Protection (VSYS OVP/UVP)**
  - **System Over-Load Protection (VSYS OLP)**
  - **Cycle-by-Cycle Overcurrent Protection (OCP)**
  - **OTG Low Battery Protection (OTG LBP)**
  - **OTG Voltage Protection (OTG OVP/UVP)**

5 Marking Information



GT=: Product Code
YMDNN: Date Code

6 Simplified Application Circuit



7 Device Comparison

Part Number	RT9490	RT9492
DEVICE_ID, REG0x48[6:3]	1100	1110
VAC_OVP, REG0x10[5:4]	7V (Default), 12V, 22V, 26V	7V, 12V, 18V, 26V (Default)
$\overline{PG}$ Pin	Yes	NA
IBAT Pin	Yes	NA
BATN Pin	Yes	NA
TS_ADC LSB, REG0x3F[15:0]	0.098%	0.0963%
Package	WL-CSP-56B 2.93x3.46 (BSC)	VQFN-29TL 4x4 (FC)

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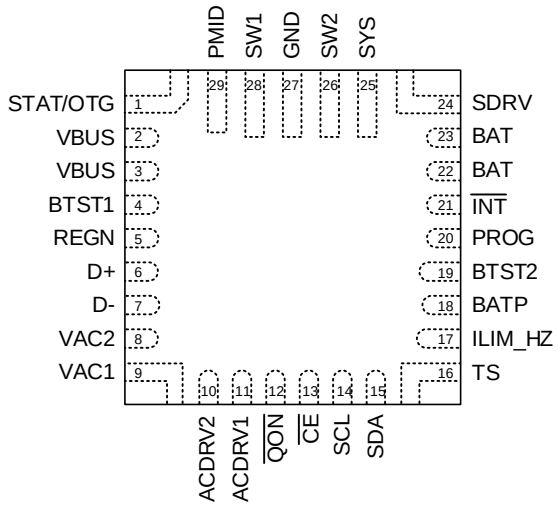
8 Pin Configuration

(TOP VIEW)



VQFN-29TL 4x4 (FC)

9 Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
1	STAT/OTG	DIO	Open-drain charger status output. Connect the STAT pin to a logic rail via 2.2kΩ to 10kΩ resistor. The STAT pin indicates charger status. Open-drain OTG mode enable control input, active high. Connect the OTG pin to a logic rail via 2.2kΩ to 10kΩ resistor.
2, 3	VBUS	P	Charger input voltage. The internal current sensing circuit is connected between VBUS and PMID. Connect two 10μF capacitors from VBUS to GND and place them as close as possible to VBUS.
4	BTST1	P	The high-side switching MOSFET (Q1) driver positive supply. Internally, the BTST1 is connected to the cathode of the bootstrap diode. Connect the 47nF bootstrap capacitor from BTST1 to SW1.
5	REGN	P	PWM low-side driver and internal supply output. Internally, REGN is connected to the anode of the bootstrap diode. Connect a 4.7μF capacitor from REGN to GND. The capacitor should be placed close to the IC. REGN must be used only for RT9492 relative functions.
6	D+	AIO	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary, secondary detection in BC1.2 and manual control mode.
7	D-	AIO	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary, secondary detection in BC1.2 and manual control mode.
8	VAC2	AI	VAC2 voltage sensing. When a voltage on VAC2 exceeds the VAC2_UVLO threshold, it indicates that a input source has been connected to port2. When there is no external AC-RBFET2, the VAC2 must be connected to VBUS.
9	VAC1	AI	VAC1 voltage sensing. When a voltage on VAC1 exceeds the VAC1_UVLO threshold, it indicates that an input source has been connected to port1. When there is no external AC-RBFET1, the VAC1 must be connected to VBUS.

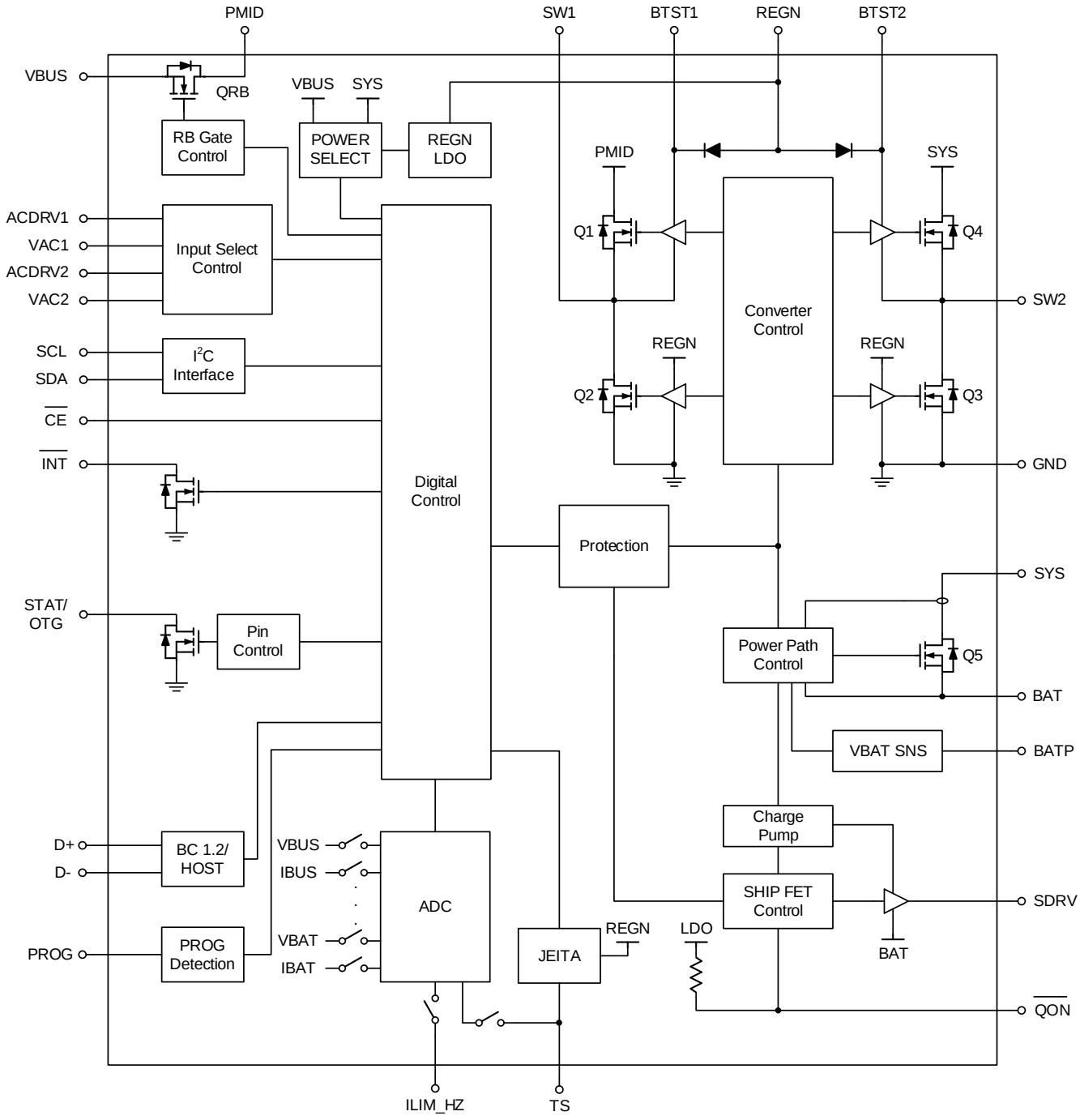
Pin No.	Pin Name	I/O	Pin Function
10	ACDRV2	P	External AC-RB N-channel MOSFET gate driver output. The ACDRV2 is connected to external AC-RBFET2. When the turn-on conditions are met, the charger activates the AC-RBFET2 by increasing the ACDRV2 voltage to a level that is 5V higher than the voltage at the drain of AC-RBFET2 When there is no external AC-RBFET2, the ACDRV2 must be connected to GND.
11	ACDRV1	P	External AC-RB N-channel MOSFET gate driver output. The ACDRV1 is connected to external AC-RBFET1. The charger is designed to turn on the AC-RBFET1 by increasing the voltage of ACDRV1 to a level that is 5V higher than the drain voltage of the AC-RBFET1, provided that the turn-on conditions are satisfied. When there is no external AC-RBFET1, the ACDRV1 must be connected to GND.
12	$\overline{\text{QON}}$	DI	Ship FET control input. When the device is in ship mode, a logic-low duration with $t_{QON\_EXIT\_SHIP\_DLY}$ turns on ship FET to exit ship mode. A logic-low duration with t_{QON_RST} turns off the ship FET, stops converter switching for t_{SYS_RST}, and resumes to provide system reset. The control pin is internally pulled high through a 200kΩ resistor connected to the internal bias circuit.
13	$\overline{\text{CE}}$	DI	Charge enable pin, active low. When this pin is driven low and REG_CHG_EN = 1, battery charging is enabled. Do NOT leave this pin floating.
14	SCL	DI	I^2C interface clock. Connect SCL to the logic rail through a 10kΩ resistor.
15	SDA	DIO	I^2C interface clock. Connect SDA to the logic rail through a 10kΩ resistor.
16	TS	AI	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor (103AT). Program temperature window with a resistor divider from REGN to TS, and then to GND. The resistors used for resistor divider is recommended to have a 1% resistance tolerance. Charge will be suspended when the TS pin voltage falls outside of the programmed range. When the TS pin is not used, it is recommended to connect a 10kΩ resistor from REGN to TS and another 10kΩ resistor from TS to GND.
17	ILIM_HZ	AI	Input current limit setting and HZ mode control. A resistor divider is connected to the ILIM_HZ pin by pull-up resistors from REGN to GND. The pin voltage is calculated as V_{ILIM_HZ} = 1V + 800mΩ x ILIM, where ILIM is the target input current limit. The input current limit for charger is the lower setting between ILIM_HZ and AICR register. When the pin voltage is below 0.75V, the buck-boost converter stops switching and turns on REGN. When the pin voltage is higher than 1V, the converter resumes switching.
18	BATP	AI	Positive battery voltage sensing. Connect to the positive terminal of battery pack. It is recommended to place a 100Ω series resistor between BATP and the positive terminal of battery pack.
19	BTST2	P	The high-side switching MOSFET (Q4) driver positive supply. Internally, the BTST2 is connected to the cathode of the bootstrap diode. Connect the 47nF bootstrap capacitor from BTST2 to SW2.
20	PROG	AI	Charger POR default setting program. A resistor is connected from PROG to GND to set battery cells for default charging profile and switching frequency. The resistor connected to PROG is recommended to have 1% or 2% resistance tolerance.
21	$\overline{\text{INT}}$	DO	Open-drain interrupt output, active low. Connect the INT to a logic rail through 10kΩ resistor. The INT pin sends an active-low pulse to host system in order to communicate the status of the charger device and report any fault.

Pin No.	Pin Name	I/O	Pin Function
22, 23	BAT	P	Battery connection point to the positive terminal of the battery pack. The internal current sensing circuit is connected between SYS and BAT. Connect two 10μF capacitors from BAT to GND and place them as close as possible to BAT.
24	SDRV	P	External N-channel ship FET gate driver output. The SDRV is connected to external ship FET, and the SDRV is always turned off when in ship or shutdown mode. If the ship FET is not utilized, it is mandatory to connect a 1nF/50V capacitor from SDRV to GND.
25	SYS	P	Charger output connection point. Connect to the drain of high-side switching MOSFET (Q4) and the internal current sensing circuit between SYS and BAT. Connect five 10μF and a 0.1μF capacitors from SYS to GND and place them as close as possible to SYS.
26	SW2	P	Switching node two is designed to connect to output inductor. Internally, SW2 is connected to the drain of the low-side switching MOSFET (Q3) and the source of the high-side switching MOSFET (Q4).
27	GND	P	Power Ground.
28	SW1	P	Switching node one is designed to connect to the output inductor. Internally, SW1 is connected to the source of the high-side switching MOSFET (Q1) and the drain of the low-side switching MOSFET (Q2).
29	PMID	P	Connect to the drain of high-side switching MOSFET (Q1). Connect three 10μF and a 0.1μF capacitors from PMID to GND and place them as close as possible to PMID.

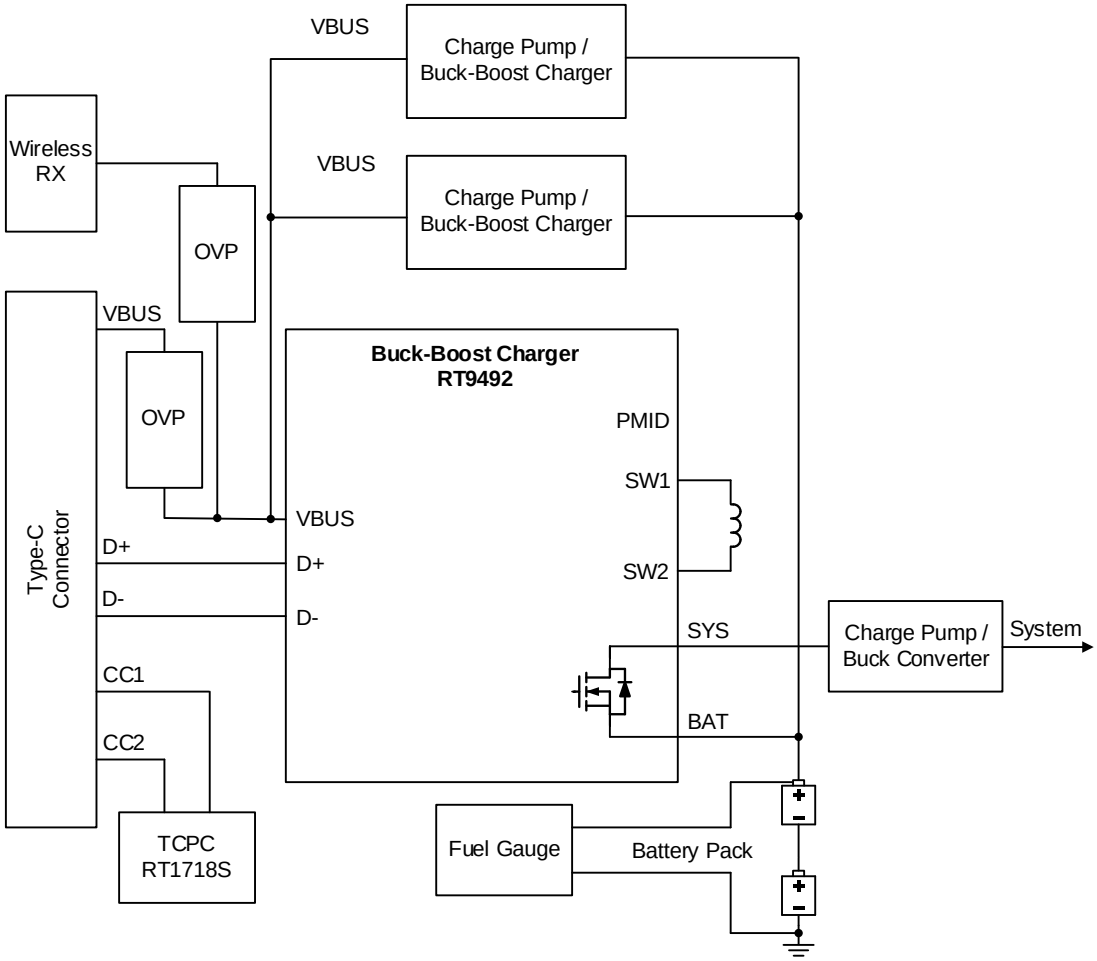
9.1 IO Type Definition

- DIO: Digital Input/Output Pin
- DI: Digital Input Pin
- DO: Digital Output Pin
- AIO: Analog Input/Output Pin
- AI: Analog Input Pin
- P: Power Pin

10 Functional Block Diagram



11 System Block Diagram



12 Absolute Maximum Ratings

(Note 2)

- Voltage Sense Pin Voltage, VAC1, VAC2 ---------- –2V to 30V
- Supply Pin Voltage, VBUS ---------- –2V to 30V
- Terminal Pin Voltage, PMID ---------- –0.3V to 30V
- Terminal Pin Voltage, ACDRV1, ACDRV2, BTST1 ---------- –0.3V to 32V
- Terminal Pin Voltage, BTST2 ---------- –0.3V to 29V
- Terminal Pin Voltage, SW1 ---------- –2V (50ns) to 30V
- Terminal Pin Voltage, SW2 ---------- –2V (50ns) to 23V
- Terminal Pin Voltage, SYS ---------- –0.3V to 23V
- Supply Pin Voltage, BAT ---------- –0.3V to 20V
- Voltage Sense Pin Voltage, BATP ---------- –0.3V to 20V
- Terminal Pin Voltage, SDRV ---------- –0.3V to 26V
- Terminal Pin Voltage, PMID-VBUS ---------- –0.3V to 6V
- Terminal Pin Voltage, BTST1-SW1, BTST2-SW2 ---------- –0.3V to 6V
- Terminal Pin Voltage, SYS-BAT ---------- –0.3V to 16V
- Terminal Pin Voltage, SDRV-BAT ---------- –0.3V to 6V
- Other Pins Voltage, STAT/OTG, SCL, SDA, $\overline{INT}$, $\overline{CE}$, D+, D- ---------- –0.3V to 6V
- Other Pins Voltage for REGN, TS, $\overline{QON}$, ILIM_HZ, PROG ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  VQFN-29TL 4x4 (FC) ---------- 2.33W
- Package Thermal Resistance (Note 3)

  VQFN-29TL 4x4 (FC), θ_{JA} ---------- 45°C/W

  VQFN-29TL 4x4 (FC), θ_{JC} ---------- 3.41°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –55°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings on T_J = 25°C only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

13 Recommended Operating Conditions

(Note 5)

- Voltage Sense Pin Voltage, VAC1, VAC2 ---------- 3.6V to 24V
- Supply Input Voltage Range, VBUS ---------- 3.6V to 24V
- Maximum Input Current, IBUS ---------- 3.3A
- Maximum Input Current, IOTG ---------- 3.32A
- Maximum Output Current (SW2), ISYS (Note 6) ---------- 5A
- Maximum Battery Voltage, VBAT ---------- 18.8V
- Maximum Charge Current, IBAT ---------- 5A
- Maximum Discharge Current, IBAT ---------- 10A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 130°C

Note 5. The device is not guaranteed to function outside its operating conditions.

Note 6. To achieve the maximum output current for ISYS, it is recommended to set the switching frequency to 1MHz.

14 Electrical Characteristics

(V_{BUS_UVLO} < V_{BUS} < V_{BUS_OVP}, T_J = 25°C, unless otherwise specified.) (Note 7)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current						
Battery Discharge Current (BATP) in Ship Mode	$I_{Q\_BAT\_OFF}$	BATP = 8V, no VBUS, I^2C enabled, ADC disabled, SYS no load, in ship mode, measure IBAT	--	2.5	6	μA
Battery Discharge Current (BATP) in Shutdown Mode	$I_{SD\_BAT\_OFF}$	BATP = 8V, no VBUS, I^2C disable, ADC disabled, SYS no load, in shutdown mode, measure IBAT	--	0.6	0.9	μA
Battery Discharge Current (BATP, BAT) in the Battery Only Mode, Q5 is Enabled	$I_{Q\_BAT\_ON}$	V_{BAT} = 8V, no VBUS, Q5 is enabled, I^2C enabled, ADC disabled, SYS no load, measure IBAT	--	18	23	μA
Battery Discharge Current (BATP, BAT) in the Battery Only Mode, Q5 is Enabled	$I_{Q\_BAT\_ADC\_ON}$	V_{BAT} = 8V, no VBUS, Q5 is enabled, I^2C enabled, ADC VBAT enabled, SYS no load, measure IBAT	--	650	--	μA
Input Supply Current (VAC) in HZ Mode	I_{VAC_HZ}	V_{AC} = 5V, HZ mode, no battery, ACDRV enable	--	500	550	μA
Input Supply Current (VBUS) in HZ Mode	I_{VBUS_HZ}	V_{BUS} = 5V, HZ mode, no battery, ACDRV disable	--	354	440	μA
Input Supply Current (VBUS)	I_{BUS_SW}	V_{BUS} = 15V, V_{BAT} = 8V, charge disabled, converter switching, I_{SYS} = 0A, OOA disabled	--	3	--	mA
		V_{BUS} = 15V, V_{BAT} = 8V, charge disabled, converter switching, I_{SYS} = 0A, OOA enable	--	5	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Battery Discharge Current (BATP, BAT) in OTG Mode	I_{BAT_OTG}	V_{BAT} = 8V, V_{OTG} = 5V, OTG mode enabled, converter switching, I_{BUS} = 0A, OOA disabled	--	2	--	mA
		V_{BAT} = 8V, V_{OTG} = 5V, OTG mode enabled, converter switching, I_{BUS} = 0A, OOA enabled	--	5	--	
VAC, VBUS and BAT Power						
VAC Rising Threshold to Turn On the ACDRV	$V_{VAC\_UVLO\_RISE}$	V_{AC} rises until ACFET turns on, measure VAC, VBUS, ACDRV1 and ACDRV2	--	3.4	3.5	V
VAC Falling Threshold to Turn Off the ACDRV	$V_{VAC\_UVLO\_FALL}$	V_{AC} falls until ACFET turns off, measure VAC, VBUS, ACDRV1 and ACDRV2	3	3.2	--	V
VBUS Rising for Active I^2C, No Battery	V_{BUS_UVLO}	VBUS only, V_{BUS} rises to active I^2C	3.45	3.6	3.75	V
VBUS Falling to Turn Off I^2C, No Battery		VBUS only, V_{BUS} falls to turn off I^2C	--	2.4	2.6	V
VBUS Rising Threshold to Start Switching	V_{VBUS_RISE}	VBUS rising	3.45	3.6	3.75	V
VBUS Falling Threshold to Turn off REGN	V_{BUS_FALL}	V_{BUS} falling	3.03	3.2	3.3	V
VAC 26V Overvoltage Rising Threshold	V_{AC_OVP}	V_{AC} rising, VAC_OVP[1:0] = 00, for both VAC1 and VAC2	25.2	26	26.8	V
VAC 26V Overvoltage Falling Threshold		V_{AC} falling, VAC_OVP[1:0] = 00, for both VAC1 and VAC2	24.4	25.2	26	
VAC 18V Overvoltage Rising threshold		V_{AC} rising, VAC_OVP[1:0] = 01, for both VAC1 and VAC2	17.4	18	18.6	
VAC 18V Overvoltage Falling threshold		V_{AC} falling, VAC_OVP[1:0] = 01, for both VAC1 and VAC2	16.9	17.5	18.1	
VAC 12V Overvoltage Rising Threshold		V_{AC} rising, VAC_OVP[1:0] = 10, for both VAC1 and VAC2	11.6	12	12.4	
VAC 12V Overvoltage Falling Threshold		V_{AC} falling, VAC_OVP[1:0] = 10, for both VAC1 and VAC2	11.2	11.6	12	
VAC 7V Overvoltage Rising Threshold		V_{AC} rising, VAC_OVP[1:0] = 11, for both VAC1 and VAC2	6.6	7	7.4	
VAC 7V Overvoltage Falling Threshold		V_{AC} falling, VAC_OVP[1:0] = 11, for both VAC1 and VAC2	6.5	6.8	7.1	
VBUS Overvoltage Rising Threshold	V_{BUS_OVP}	V_{BUS} rising	24	25	26.2	V
VBUS Overvoltage Falling Threshold		V_{BUS} falling	23	24	24.8	
IBUS Overcurrent Rising Threshold	I_{BUS_OCP}	I_{BUS} rising	6.4	8	--	A
BAT for Turn On Q5 and Active I^2C	V_{BAT_UVLO}	V_{BAT} rising	2.4	2.6	2.7	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BAT for Turn Off Q5 and I^2C		V_{BAT} falling	2.2	2.4	2.5	
BATP for Turn On Ship FET and Active I^2C	V_{BATP_UVLO}	V_{BATP} rising	3.3	3.4	3.5	V
BATP for Turn Off I^2C and Ship FET		V_{BATP} falling	2.2	2.4	2.5	
Bad Adapter Detection Falling Threshold	V_{BUS_MIN}	V_{BUS} falling	3.3	3.4	3.5	V
Bad Adapter Detection Hysteresis	$V_{BUS\_MIN\_HYS}$	V_{BUS} rising	140	200	250	mV
Bad Adapter Detection Sink Source	R_{BADSRC}	Sink source from V_{BUS} to GND, V_{BUS} = 5V	--	1.1	--	kΩ
External AC-RBFET Control						
ACDRV Drive Voltage on RBFET	V_{ACDRV}	V_{AC1} = 5V, measured on ACDRV1 to VAC1	4.5	4.9	5.3	V
Power Path						
SYS Minimum Regulation Voltage Setting Range	V_{SYSMIN_RANGE}	V_{SYSMIN} regulation range, measured on SYS	2.5	--	16	V
SYS Minimum Regulation Voltage Step	V_{SYSMIN_STEP}		--	250	--	mV
SYS Minimum Regulation Voltage	V_{SYSMIN}	V_{BAT} < V_{SYSMIN}, Q5 disabled/ enable	V_{SYSMIN}	V_{SYSMIN} + 0.2	--	V
SYS Minimum Regulation Voltage Accuracy	V_{SYSMIN_ACC}	V_{SYSMIN} = 7V	–2	--	2	%
SYS Regulation Voltage Range	V_{SYSREG_RANGE}		3.3	--	19.1	V
SYS Regulation Voltage	V_{SYSREG}	V_{BAT} = 16.8V, V_{BAT} > V_{SYSMIN}, Q5 disabled	16.9	17.1	17.3	V
		V_{BAT} = 12.6V, V_{BAT} > V_{SYSMIN}, Q5 disabled	12.72	12.9	13.14	
		V_{BAT} = 8.4V, V_{BAT} > V_{SYSMIN}, Q5 disabled	8.53	8.7	8.87	
VSYS Overvoltage Rising Threshold	V_{SYS_OVP}	As a percentage of the system regulation voltage, the converter stops switching when V_{SYS} rises	105.5	110	112.5	%
VSYS Overvoltage Falling Threshold		As a percentage of the system regulation voltage, the converter re-starts switching when V_{SYS} falls	95.5	100	102.5	
VSYS Overvoltage Sink Source	R_{SYS_OVP}	Sink source from V_{SYS} to GND	--	0.85	--	kΩ
VSYS Undervoltage Falling Threshold	V_{SYS_UVP}	VSYS falling	2.1	2.2	2.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Battery Charger						
Charge Voltage Setting Range	$V_{BAT\_REG\_RANGE}$		5	--	18.8	V
Charge Voltage Step	$V_{BAT\_REG\_STEP}$		--	10	--	mV
Charge Voltage Setting Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 8.4V	–0.3	--	0.3	%
		V_{BAT_REG} = 12.6V	–0.3	--	0.3	
		V_{BAT_REG} = 16.8V	–0.5	--	0.5	
Charge Current Regulation Setting Range	$I_{CHG\_REG\_RANGE}$		150	--	5000	mA
Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$		--	10	--	mA
Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$	I_{CHG_REG} = 2A, V_{SYSMIN} = 7V, V_{BAT} = 8V (Note 7)	–3.5	--	3.5	%
		I_{CHG_REG} = 1A, V_{SYSMIN} = 7V, V_{BAT} = 8V	–4	--	4	
		I_{CHG_REG} = 0.5A, V_{SYSMIN} = 7V, V_{BAT} = 8V	–7.5	--	7.5	
Pre-Charge Rising Threshold	$V_{PRE\_CHG\_RISE}$	V_{PRE_CHG} = 15% x V_{BAT_REG}, Pre-charge to Fast-charge, V_{BAT_REG} = 18.8V	13	15	17	%
		V_{PRE_CHG} = 62% x V_{BAT_REG}, Pre-charge to Fast-charge, V_{BAT_REG} = 8.4V	60.5	62	63.5	
		V_{PRE_CHG} = 66.5% x V_{BAT_REG}, Pre-charge to Fast-charge, V_{BAT_REG} = 8.4V	65	66.5	68	
		V_{PRE_CHG} = 71.5% x V_{BAT_REG}, Pre-charge to Fast-charge, V_{BAT_REG} = 8.4V	70	71.5	73	
Pre-Charge Hysteresis	$V_{PRE\_CHG\_HYS}$	Fast-charge to Pre-charge	--	1.5	--	%
Pre-Charge Current Setting Range	$I_{PRE\_CHG\_RANGE}$	Default = 120mA	120	--	2000	mA
Pre-Charge Current Step	$I_{PRE\_CHG\_STEP}$		--	40	--	mA
Pre-Charge Accuracy	$I_{PRE\_CHG\_ACC}$	I_{PRE_CHG} = 200mA, V_{SYS_MIN} = 7V, V_{BAT} = 6.5V	–15	--	15	%
End-Of-Charge Current Setting Range	$I_{EOC\_CHG\_RANGE}$	Default = 200mA	120	--	1000	mA
End-Of-Charge Current Step	$I_{EOC\_CHG\_STEP}$		--	40	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
End-Of-Charge Accuracy (Note 8)	$I_{EOC\_CHG\_ACC}$	I_{EOC_CHG} = 120mA, DIS_EOC_FCCM = 0 V_{BUS} = 15V, V_{BAT} = 8.4V	–20	--	20	%
		I_{EOC_CHG} = 200mA, DIS_EOC_FCCM = 0 V_{BUS} = 15V, V_{BAT} = 8.4V	–15	--	15	
		I_{EOC_CHG} = 480mA, DIS_EOC_FCCM = 0 V_{BUS} = 15V, V_{BAT} = 8.4V	–10	--	10	
Trickle-Charge Falling Threshold	$V_{TRICKLE\_CHG\_FALL}$	V_{BAT} falling	1.8	2	2.2	V
Trickle-Charge Rising Threshold	$V_{TRICKLE\_CHG\_RISE}$	V_{BAT} rising	2.05	2.25	2.45	V
Trickle-Charge Current	$I_{TRICKLE\_CHG}$	V_{BAT} < $V_{TRICKLE\_CHG\_RISE}$	80	100	120	mA
Re-Charge Threshold below V_{BAT_REG}	V_{RE_CHG}	V_{BAT} falling, V_{RECHG} = 200mV, V_{BUS} = 15V, V_{BAT_REG} = 8.4V	180	200	230	mV
Input Voltage and Current Regulation						
Minimum Input Voltage Regulation Setting Range	V_{MIVR_RANGE}		3.6	--	22	V
Minimum Input Voltage Regulation Step	V_{MIVR_STEP}		--	100	--	mV
Minimum Input Voltage Regulation Accuracy	V_{MIVR_ACC}	V_{MIVR} = 10.6V	–1	--	1	%
Average Input Current Regulation Setting Range	I_{AICR_RANGE}		0.1	--	3.3	A
Average Input Current Regulation Step	I_{AICR_STEP}		--	10	--	mA
Average Input Current Regulation Accuracy	I_{AICR_ACC}	V_{BUS} = 15V, I_{AICR} = 500mA	450	470	500	mA
		V_{BUS} = 15V, I_{AICR} = 1000mA	900	950	1000	
		V_{BUS} = 15V, I_{AICR} = 2000mA (Note 7)	1800	1900	2000	
		V_{BUS} = 15V, I_{AICR} > 2000mA (Note 7)	–9	--	0	%
BAT Overvoltage Protection						
Battery Overvoltage Rising	V_{BAT_OVP}	V_{BAT} rising, as percentage of V_{BAT_REG}	103	104	105	%
Battery Overvoltage Falling		V_{BAT} falling, as percentage of V_{BAT_REG}	101	102	103	%
Battery Overvoltage Sink Source	R_{BAT_OVP}	Sink source from V_{BAT} to GND	--	1.1	--	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Regulation and Shutdown						
Junction Thermal Regulation Setting Range	$T_{J\_THREG\_RANGE}$	Default = 120°C	60	--	120	°C
Junction Thermal Regulation Step	$T_{J\_THREG\_STEP}$		--	20	--	°C
Junction Thermal Regulation Accuracy	$T_{J\_THREG\_ACC}$	T_{J_THREG} = 120°C	--	120	--	°C
		T_{J_THREG} = 100°C	--	100	--	
		T_{J_THREG} = 80°C	--	80	--	
		T_{J_THREG} = 60°C	--	60	--	
Over-Temperature Protection Rising	T_{OTP}	T_{J_THREG} = 150°C, Temperature rising (Note 7)	130	150	170	°C
		T_{J_THREG} = 130°C, Temperature rising (Note 7)	110	130	150	
		T_{J_THREG} = 120°C, Temperature rising (Note 7)	100	120	140	
		T_{J_THREG} = 85°C, Temperature rising (Note 7)	65	85	105	
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	Temperature falling	--	30	--	°C
NTC Monitor (Charger Mode)						
Battery Temperature COLD Threshold (0°C)	V_{TS_COLD}	V_{TS} rising, the ratio of V_{REGN}	72.3	73.5	74.7	%
		V_{TS} falling, the ratio of V_{REGN}	70.8	72	73.2	
Battery Temperature COOL Rising Threshold	$V_{TS\_COOL\_RISE}$	V_{TS_COOL} = 5°C, V_{TS} rising, the ratio of V_{REGN} (Note 7)	70.6	71.1	71.6	%
		V_{TS_COOL} = 10°C, V_{TS} rising, the ratio of V_{REGN}	67.4	68.5	69.6	
		V_{TS_COOL} = 15°C, V_{TS} rising, the ratio of V_{REGN} (Note 7)	65	65.5	66	
		V_{TS_COOL} = 20°C, V_{TS} rising, the ratio of V_{REGN} (Note 7)	61.9	62.4	62.9	
Battery Temperature COOL Falling Threshold	$V_{TS\_COOL\_FALL}$	V_{TS_COOL} = 5°C, V_{TS} falling, the ratio of V_{REGN} (Note 7)	69.3	69.8	70.3	%
		V_{TS_COOL} = 10°C, V_{TS} falling, the ratio of V_{REGN}	65.9	67	68.1	
		V_{TS_COOL} = 15°C, V_{TS} falling, the ratio of V_{REGN} (Note 7)	63.7	64.2	64.7	
		V_{TS_COOL} = 20°C, V_{TS} falling, the ratio of V_{REGN} (Note 7)	60.6	61.1	61.6	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Battery Temperature WARM Falling Threshold	$V_{TS\_WARM\_FALL}$	V_{TS_WARM} = 40°C, V_{TS} falling, the ratio of V_{REGN} (Note 7)	47.9	48.4	48.9	%
		V_{TS_WARM} = 45°C, V_{TS} falling, the ratio of V_{REGN}	44.2	45	45.8	
		V_{TS_WARM} = 50°C, V_{TS} falling, the ratio of V_{REGN} (Note 7)	40.7	41.2	41.7	
		V_{TS_WARM} = 55°C, V_{TS} falling, the ratio of V_{REGN} (Note 7)	37.2	37.7	38.2	
Battery Temperature WARM Rising Threshold	$V_{TS\_WARM\_RISE}$	V_{TS_WARM} = 40°C, V_{TS} rising, the ratio of V_{REGN} (Note 7)	49.2	49.7	50.2	%
		V_{TS_WARM} = 45°C, V_{TS} rising, the ratio of V_{REGN}	45.2	46	46.8	
		V_{TS_WARM} = 50°C, V_{TS} rising, the ratio of V_{REGN} (Note 7)	42	42.5	43	
		V_{TS_WARM} = 55°C, V_{TS} rising, the ratio of V_{REGN} (Note 7)	38.5	39	39.5	
Battery Temperature HOT Threshold (60°C)	V_{TS_HOT}	V_{TS} falling, the ratio of V_{REGN}	33.4	34	34.7	%
		V_{TS} rising, the ratio of V_{REGN}	34.9	35.5	36.1	
NTC Monitor (OTG Mode)						
Battery Temperature COLD Rising Threshold OTG mode	$V_{TS\_COLD\_OTG\_RISE}$	$V_{TS\_COLD\_OTG}$ = –20°C, V_{TS} rising, the ratio of V_{REGN} (Note 7)	78.7	80	81.3	%
		$V_{TS\_COLD\_OTG}$ = –10°C, V_{TS} rising, the ratio of V_{REGN}	75.7	77	78.3	
Battery Temperature COLD Falling Threshold OTG mode	$V_{TS\_COLD\_OTG\_FALL}$	$V_{TS\_COLD\_OTG}$ = –20°C, V_{TS} falling, the ratio of V_{REGN} (Note 7)	78.2	78.7	79.2	%
		$V_{TS\_COLD\_OTG}$ = –10°C, V_{TS} falling, the ratio of V_{REGN}	74.8	76	77.2	
Battery Temperature HOT Falling Threshold OTG mode	$V_{TS\_HOT\_OTG\_FALL}$	$V_{TS\_HOT\_OTG}$ = 55°C, V_{TS} falling, the ratio of V_{REGN} (Note 7)	37.2	37.7	38.2	%
		$V_{TS\_HOT\_OTG}$ = 60°C, V_{TS} falling, the ratio of V_{REGN}	33.9	34.5	35.1	
		$V_{TS\_HOT\_OTG}$ = 65°C, V_{TS} falling, the ratio of V_{REGN} (Note 7)	32	32.5	33	
Battery Temperature HOT Rising Threshold OTG Mode	$V_{TS\_HOT\_OTG\_RISE}$	$V_{TS\_HOT\_OTG}$ = 55°C, V_{TS} rising, the ratio of V_{REGN} (Note 7)	38.8	39.3	39.8	%
		$V_{TS\_HOT\_OTG}$ = 60°C, V_{TS} rising, the ratio of V_{REGN}	34.9	35.5	36.2	
		$V_{TS\_HOT\_OTG}$ = 65°C, V_{TS} rising, the ratio of V_{REGN} (Note 7)	32	32.5	33	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Overcurrent Threshold						
Q1 Cycle-by-Cycle Overcurrent Threshold	I_{OCP_Q1}		8.55	10.5	12.25	A
Q2 Cycle-by-Cycle Overcurrent Threshold	I_{OCP_Q2}		6.8	7.5	8.25	A
Q3 Cycle-by-Cycle Overcurrent Threshold	I_{OCP_Q3}		6.8	7.5	8.25	A
Q4 Cycle-by-Cycle Overcurrent Threshold	I_{OCP_Q4}		8.55	10.5	12.25	A
System Over-Load Threshold	I_{OCP_BATFET}		11	--	--	A
Internal Sense Resistance and MOSFET Rdson						
Reverse-Blocking MOSFET (QRB) Turn-On Resistance between VBUS and PMID	R_{DSON_QRB}		--	9	--	mΩ
High-Side Switching MOSFET (Q1) Turn-On Resistance between PMID and SW1	R_{DSON_Q1}	V_{REGN} = 4.9V	--	25	--	mΩ
Low-Side Switching MOSFET (Q2) Turn-On Resistance between SW1 and PGND	R_{DSON_Q2}	V_{REGN} = 4.9V	--	34	--	mΩ
Low-Side Switching MOSFET(Q3) Turn-On Resistance between SW2 and PGND	R_{DSON_Q3}	V_{REGN} = 4.9V	--	28	--	mΩ
High-Side Switching MOSFET(Q4) Turn-On Resistance between SW2 and SYS	R_{DSON_Q4}	V_{REGN} = 4.9V	--	17	--	mΩ
BATFET (Q5) Turn-On Resistance between SYS and BAT	R_{DSON_Q5}		--	11	--	mΩ
USB On-The-Go (OTG)						
OTG Low Battery Protection	V_{OTG_LBP}	V_{BAT} falling	2.3	2.5	2.6	V
		V_{BAT} rising	2.5	2.7	2.9	
OTG Voltage Limit Regulation Setting Range	$V_{OTG\_CV\_RANGE}$	Default = 5V	2.8	--	22	V
OTG Voltage Limit Regulation Step	$V_{OTG\_CV\_STEP}$		--	10	--	mV
OTG Voltage Limit Regulation Accuracy	$V_{OTG\_CV\_ACC}$	I_{VBUS} = 0A, V_{OTG_REG} = 5V	–1.5	--	1.5	%
OTG Current Limit Regulation Setting Range	$I_{OTG\_CC\_RANGE}$	Default = 3A	0.12	--	3.32	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OTG Current Limit Regulation Step	$I_{OTG\_CC\_STEP}$		--	40	--	mA
OTG Current Limit Regulation Accuracy	I_{OTG_CC}	I_{OTG_CC} = 3A, V_{BAT} = 8V, V_{OTG_CV} = 5V (Note 7)	–3	--	3	%
		I_{OTG_CC} = 1A, V_{BAT} = 8V, V_{OTG_CV} = 5V	–3	--	3	
		I_{OTG_CC} = 0.48A, V_{BAT} = 8V, V_{OTG_CV} = 5V	–10	--	10	
Battery Current Regulation in OTG Mode	I_{OTG_BAT}	I_{BAT_REG} = 3A, V_{BAT} = 8V, V_{OTG_CV} = 5V (Note 7)	2.8	3	3.2	A
		I_{BAT_REG} = 4A, V_{BAT} = 8V, V_{OTG_CV} = 5V (Note 7)	3.8	4	4.2	
		I_{BAT_REG} = 5A, V_{BAT} = 8V, V_{OTG_CV} = 5V (Note 7)	4.8	5	5.2	
OTG Overvoltage Threshold	V_{OTG_OVP}	As percentage of V_{OTG_CV}, OTG mode, OOA disabled, V_{BUS} rising	104	113	120	%
		As percentage of V_{OTG_CV}, OTG mode, OOA disabled, V_{BUS} falling	90	98	104	
OTG Undervoltage Falling Threshold	V_{OTG_UVP}	V_{BUS} falling	2.1	2.2	2.3	V
PWM						
PWM Switching Frequency	f_{SW}	Oscillator frequency, f_{SW} = 1.5MHz	--	1.5	--	MHz
		Oscillator frequency, f_{SW} = 750kHz	--	750	--	kHz
REGN						
REGN LDO Output Voltage	V_{REGN}	V_{BUS} = 5V, V_{BAT} = 8V, I_{REGN} = 20mA, charge disabled, I_{SYS} = 0A	4.5	4.9	5.1	V
		V_{BUS} = 15V, V_{BAT} = 8V, I_{REGN} = 20mA, charge disabled, I_{SYS} = 0A	4.5	4.9	5.2	
REGN LDO Current Limit	I_{REGN}	V_{BUS} = 5V, V_{BAT} = 8V, V_{REGN} = 4.5V	30	--	--	mA
Current Sink						
VAC1 Discharge Resistance	R_{VAC1_DISCHG}	$V_{AC1\_PD\_EN}$ = 1, V_{AC1} = 5V	0.85	1.1	1.65	kΩ
VAC2 Discharge Resistance	R_{VAC2_DISCHG}	$V_{AC2\_PD\_EN}$ = 1, V_{AC2} = 5V	0.85	1.1	1.65	kΩ
VBUS Discharge Resistance	R_{VBUS_DISCHG}	$V_{BUS\_PD\_EN}$ = 1, V_{BUS} = 5V	0.85	1.1	1.65	kΩ
I^2C Interface (SCL and SDA)						
Input SDA High Threshold Voltage	V_{IH_SDA}	Pull high to 1.8V/1.2V	0.84	--	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input SDA Low Threshold Voltage	V_{IL_SDA}	Pull high to 1.8V/1.2V	--	--	0.4	V
Output SDA Low Threshold Voltage	V_{OL_SDA}	Sink current = 5mA	--	--	0.4	V
High Level SDA Leakage Current	I_{BIAS_SDA}	Pull high to 1.8V	--	--	1	μA
Input SCL High Threshold Voltage	V_{IH_SCL}	Pull high to 1.8V/1.2V	0.84	--	--	V
Input SCL Low Threshold Voltage	V_{IL_SCL}	Pull high to 1.8V/1.2V	--	--	0.4	V
High Level SCL Leakage Current	I_{BIAS_SCL}	Pull high to 1.8V	--	--	1	μA
SCL Clock Frequency	f_{SCL}		--	--	3400	kHz
Control I/O Pin ($\overline{CE}$, $\overline{QON}$, and ILIM_HZ)						
Input $\overline{CE}$ High Threshold Voltage	V_{IH_CE}		1.3	--	--	V
Input $\overline{CE}$ Low Threshold Voltage	V_{IL_CE}		--	--	0.4	V
High Level $\overline{CE}$ Leakage Current	I_{BIAS_CE}	Pull high to 1.8V	--	--	1	μA
Input $\overline{QON}$ High Threshold Voltage	V_{IH_QON}		1.3	--	--	V
Input $\overline{QON}$ Low Threshold Voltage	V_{IL_QON}		--	--	0.4	V
Internal $\overline{QON}$ Pull-Up Voltage	V_{QON}		2.8	3.1	3.4	V
Internal $\overline{QON}$ Pull-Up Resistance	R_{QON}		185	200	230	kΩ
Input ILIM_HZ High Threshold Voltage	$V_{IH\_ILIM\_HZ}$		1	--	--	V
Input ILIM_HZ Low Threshold Voltage	$V_{IL\_ILIM\_HZ}$		--	--	0.75	V
High Level ILIM _HZ Leakage Current	$I_{LK\_ILIM\_HZ}$	V_{ILIM_HIZ} = 4V	–1.5	--	1.5	μA
Control I/O Pin ($\overline{INT}$ and STAT/OTG)						
Output $\overline{INT}$ Low Threshold Voltage	V_{OL_INT}	Sink current = 5mA	--	--	0.4	V
High Level $\overline{INT}$ Leakage Current	I_{BIAS_INT}	Pull high to 1.8V	--	--	1	μA
$\overline{INT}$ Pull-Low Time	$t_{INT\_PULL\_LOW}$	$\overline{INT}$ pull-low time	--	256	--	μs
Output STAT/OTG Low Threshold Voltage	V_{OL_STAT}	Sink current = 5mA	--	--	0.4	V
High Level STAT/OTG Leakage Current	I_{LK_STAT}	Pull high to 1.8V	--	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input STAT/OTG High Threshold Voltage	V_{IH_OTG}	STAT configure to the OTG pin	1.3	--	--	V
Input STAT/OTG Low Threshold Voltage	V_{IL_OTG}	STAT configure to the OTG pin	--	--	0.4	V
D+/D- Detection						
Data Detect Voltage	V_{DAT_REF}	For primary/secondary detection	340	375	400	mV
D+ Current Sink	I_{D+_ISNK}	V_{D+} = 500mV	25	45	65	μA
D- Current Sink	I_{D-_ISNK}	V_{D-} = 500mV	25	45	65	μA
D+/ D- Leakage Current	I_{D+D-_LKG}	HZ mode	−1	--	1	μA
D+ Logic Threshold	V_{LGC}	V_{D+} rising	800	900	1000	mV
D+ Current Source	I_{D+_SRC}	V_{D+} = 200mV	7	10	13	μA
D+ Voltage Source	V_{D+_SRC}		600	650	700	mV
D- Voltage Source	V_{D-_SRC}		600	650	700	mV
D+ Pull-Down Resistance for Connection Check	R_{D+_19K}		16	20	24	kΩ
D- Pull-Down Resistance for Connection Check	R_{D-_19K}		16	20	24	kΩ
D+D- Threshold for Non-Standard Adapter (0.9V)	V_{D+D-_0P9}		0.81	0.9	0.99	V
D+D- Threshold for Non-Standard Adapter (1.5V)	V_{D+D-_1P5}		1.4	1.5	1.6	V
D+D- Threshold for Non-Standard Adapter (2.3V)	V_{D+D-_2P3}		2.2	2.3	2.4	V
D+D- Threshold for CDP	V_{D+D-_CDP}	For host mode, CDP	1.8	2	2.2	V
Across D+/D- Resistance in DCP	R_{DCP}	For host mode, DCP	--	50	150	Ω
ADC Measurement						
Effective Resolution	ADC_{RES}	ADC 16 bits	14	15	--	bits
Conversion-Time	t_{ADC_CONV}		--	3.6	--	ms
ADC VBUS Voltage Reading Range	$V_{BUS\_ADC\_RANGE}$		0	--	30	V
ADC VBUS Voltage Reading Resolution	$V_{BUS\_ADC\_RES}$	LSB	--	1	--	mV
ADC VBUS Voltage Reading Accuracy	$V_{BUS\_ADC\_ACC}$	V_{BUS} = 3.6V to 24V	−100	--	100	mV
ADC IBUS Current Reading Range	$I_{BUS\_ADC\_RANGE}$		0	--	5	A
ADC IBUS Current Reading Resolution	$I_{BUS\_ADC\_RES}$	LSB	--	1	--	mA
ADC IBUS Current Reading Accuracy	$I_{BUS\_ADC\_ACC}$	I_{BUS} = 0.5A to 1A	−100	--	100	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC VAC1 Voltage Reading Range	$V_{AC1\_ADC\_RANGE}$		0	--	30	V
ADC VAC1 Voltage Reading Resolution	$V_{AC1\_ADC\_RES}$	LSB	--	1	--	mV
ADC VAC1 Voltage Reading Accuracy	$V_{AC1\_ADC\_ACC}$	V_{AC1} = 3.6V to 24V	–100	--	100	mV
ADC VAC2 Voltage Reading Range	$V_{AC2\_ADC\_RANGE}$		0	--	30	V
ADC VAC2 Voltage Reading Resolution	$V_{AC2\_ADC\_RES}$	LSB	--	1	--	mV
ADC VAC2 Voltage Reading Accuracy	$V_{AC2\_ADC\_ACC}$	V_{AC2} = 3.6V to 24V	–100	--	100	mV
ADC VSYS Voltage Reading Range	$V_{SYS\_ADC\_RANGE}$		0	--	23	V
ADC VSYS Voltage Reading Resolution	$V_{SYS\_ADC\_RES}$	LSB	--	1	--	mV
ADC VSYS Voltage Reading Accuracy	$V_{SYS\_ADC\_ACC}$	V_{SYS} = 2.5V to 13V	–75	--	75	mV
ADC VBAT Voltage Reading Range	$V_{BAT\_ADC\_RANGE}$		0	--	20	V
ADC VBAT Voltage Reading Resolution	$V_{BAT\_ADC\_RES}$	LSB	--	1	--	mV
ADC VBAT Voltage Reading Accuracy	$V_{BAT\_ADC\_ACC}$	V_{BAT} = 2V to 12.6V	–100	--	100	mV
ADC IBAT Current Reading Range	$I_{BAT\_ADC\_RANGE}$		0	--	8	A
ADC IBAT Current Reading Resolution	$I_{BAT\_ADC\_RES}$	LSB	--	1	--	mA
ADC IBAT Current Reading Accuracy	$I_{BAT\_ADC\_ACC}$	I_{BAT} = 0.5A to 1A	–100	--	100	mA
ADC TS Reading Range	$RATIO_{TS\_ADC\_RANGE}$	Ratio for V_{TS}/V_{REGN}	0	--	99.9	%
ADC TS Reading Resolution	$RATIO_{TS\_ADC\_RES}$	LSB	--	0.0963	--	%
ADC TS Reading Accuracy	$RATIO_{TS\_ADC\_ACC}$	V_{TS} = 0.1V to 4.7V	–2.7927	--	2.7927	%
ADC Die Temperature Reading Range	$T_{DIE\_ADC\_RANGE}$		–40	--	150	°C
ADC Die Temperature Reading Resolution	$T_{DIE\_ADC\_RANGE}$	LSB	--	1	--	°C
ADC Die Temperature Reading Accuracy	$T_{DIE\_ADC\_ACC}$	T_J = 0°C to 85°C (Note 7)	–5	--	5	°C
ADC D+ Voltage Reading Range	$V_{D+\_ADC\_RANGE}$		0	--	3600	mV
ADC D+ Voltage Reading Resolution	$V_{D+\_ADC\_RES}$	LSB	--	1	--	mV

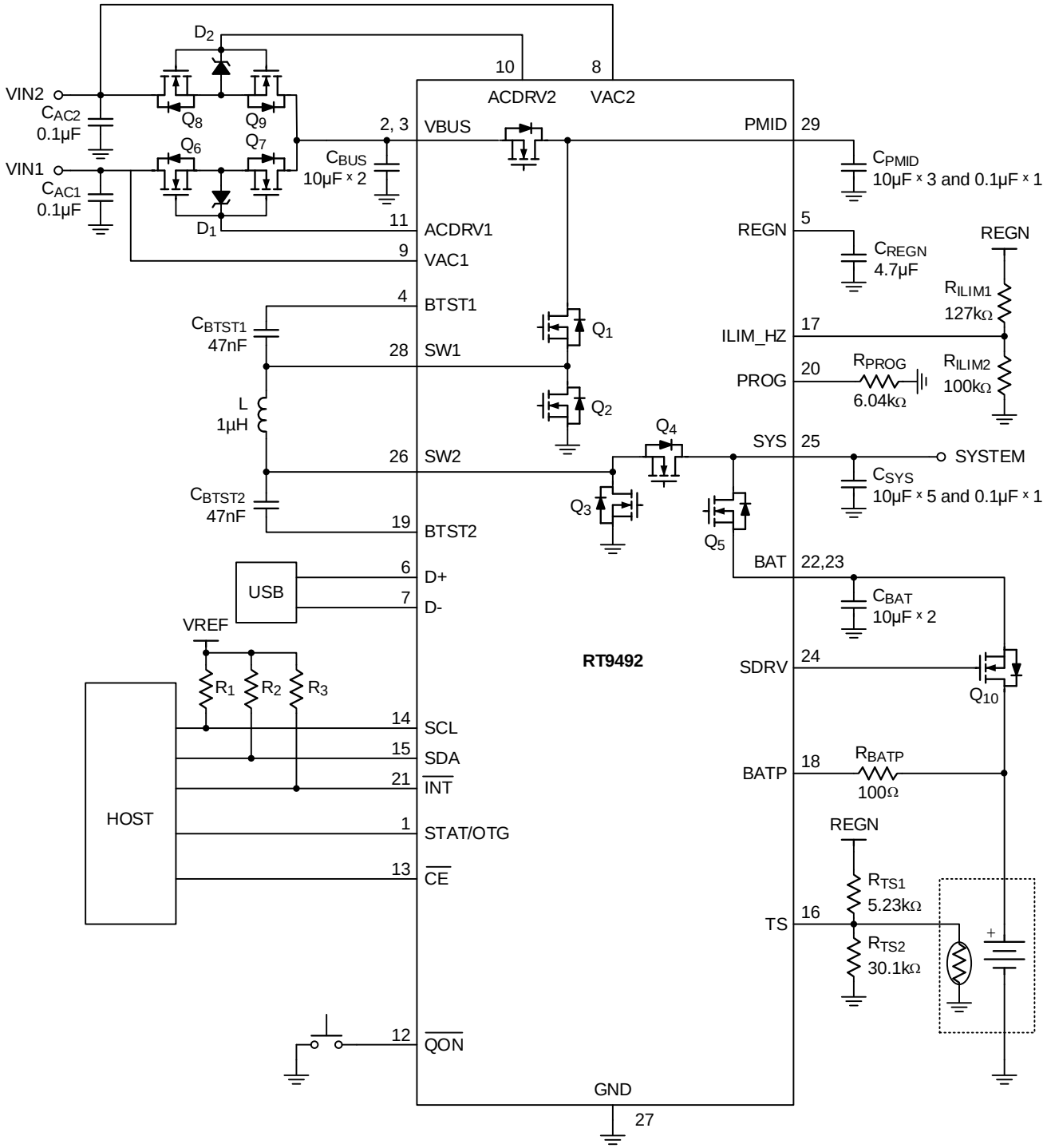
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC D+ Voltage Reading Accuracy	$V_{D+\_ADC\_ACC}$	D+ = 0V to 3.6V, HZ mode	–18	--	18	mV
ADC D- Voltage Reading Range	$V_{D-\_ADC\_RANGE}$		0	--	3600	mV
ADC D- Voltage Reading Resolution	$V_{D-\_ADC\_RES}$	LSB	--	1	--	mV
ADC D- Voltage Reading Accuracy	$V_{D-\_ADC\_ACC}$	D- = 0V to 3.6V, HZ mode	–18	--	18	mV
Timing Requirements						
Charge Safe Timer for Trickle Charge	$t_{TRI\_SAFE\_TMR}$		0.9	1	1.1	hr
Charge Safe Timer for Pre-Charge	$t_{PRE\_SAFE\_TMR}$	PRECHG_TMR = 2hr	1.8	2	2.2	hr
Charge Safe Timer for Fast Charge	$t_{CHG\_SAFE\_TMR}$	FASTCHG_TMR = 5hr	4.5	5	5.5	hr
		FASTCHG_TMR = 8hr	7.2	8	8.8	
		FASTCHG_TMR = 12hr	10.8	12	13.2	
		FASTCHG_TMR = 24hr	21.6	24	26.4	
Back-Ground Charge Timer	$t_{BG\_CHG\_TMR}$	BG_CHG_TMR = 15min	12	15	18	min
		BG_CHG_TMR = 30min	24	30	36	
		BG_CHG_TMR = 45min	36	45	54	
Watchdog Timer						
Watchdog Timer	t_{WDT}	WATCHDOG = 160s	144	160	176	s

Note 7. Specifications are guaranteed by design and/or correlation with statistical process control.

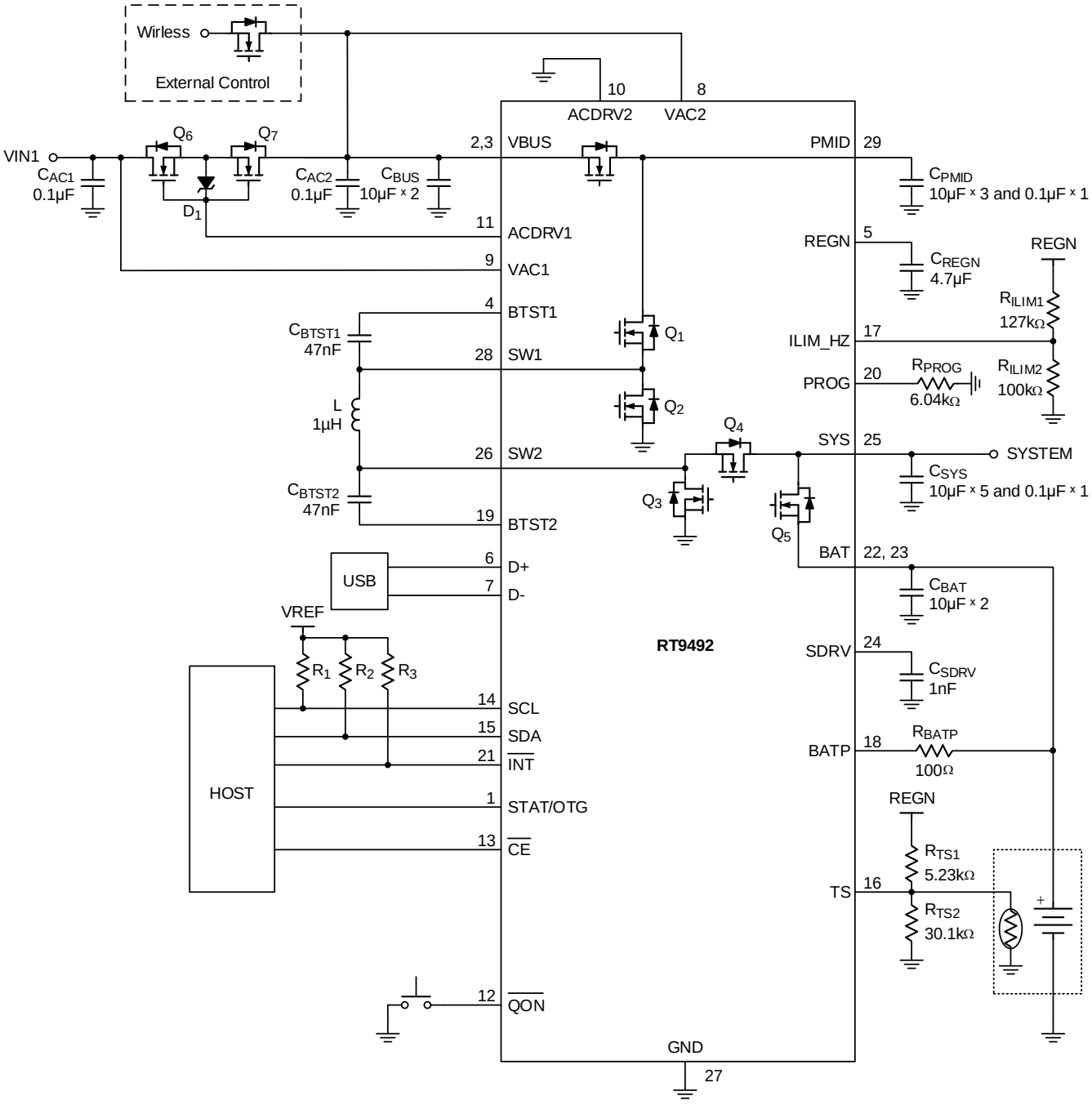
Note 8. Refer to the MIVR section in the Application Information for detailed descriptions.

15 Typical Application Circuit

15.1 The RT9492 with Dual Input and Ship FET



15.2 The RT9492 with Single ACRBFET and No Ship FET



15.3 The RT9492 with Single Input and No Ship FET

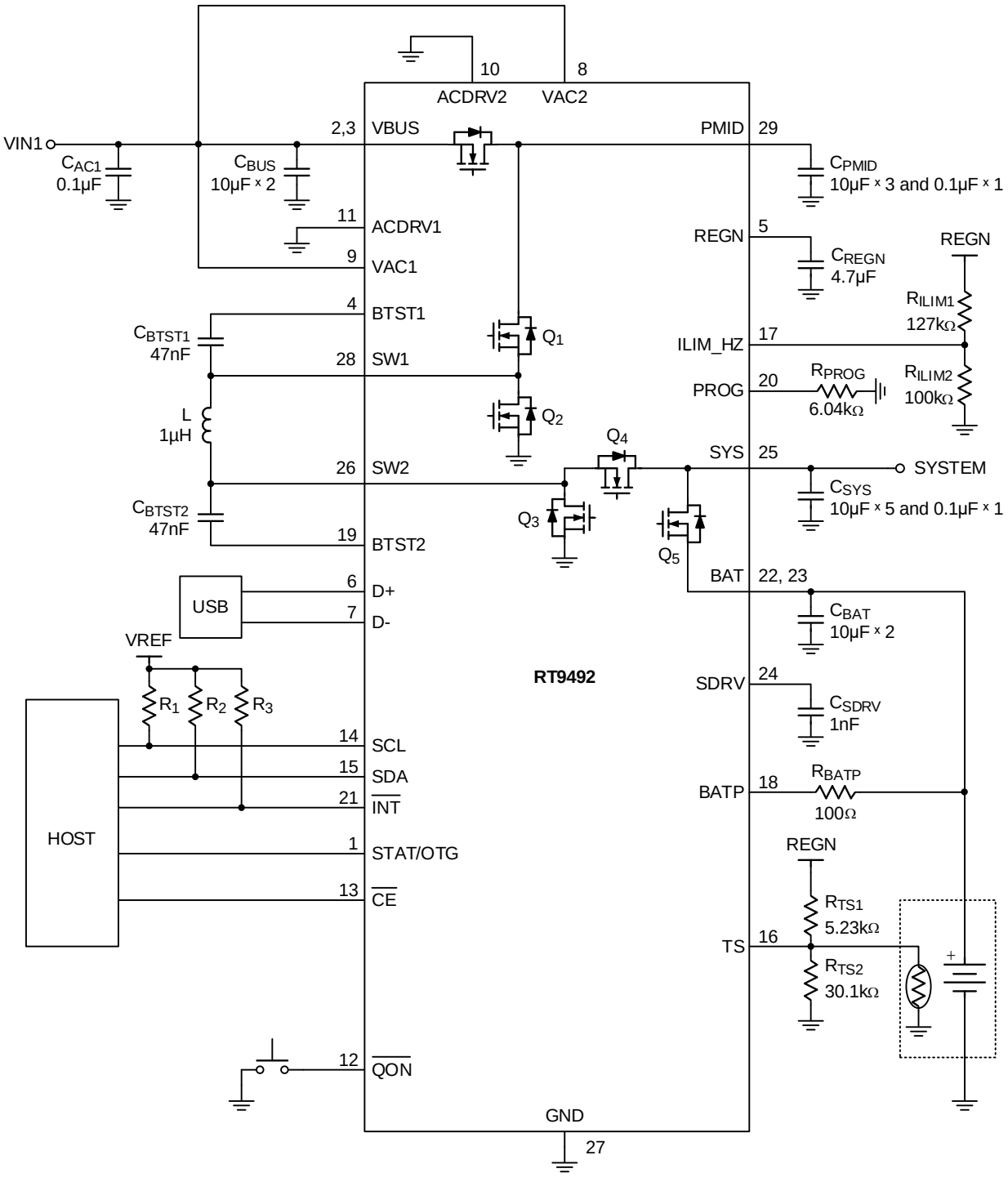
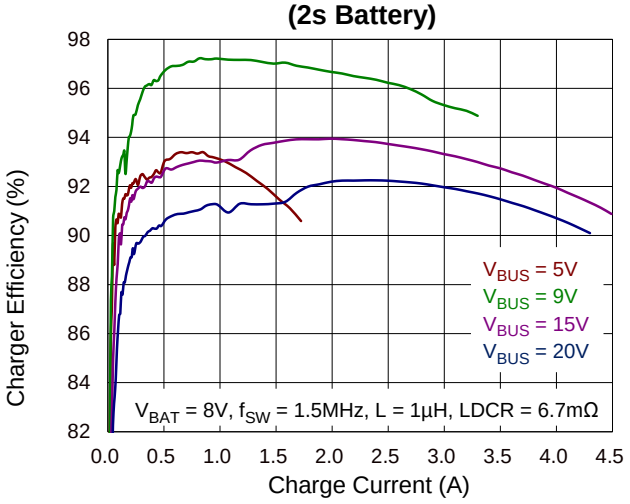


Table 1. Recommended Components Information

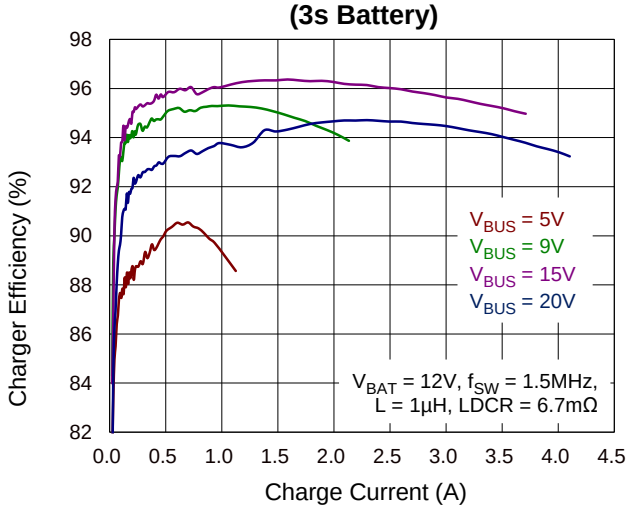
Name	Part Number	Description	Package	Manufacturer
C_{AC1}	0402B104K500CT	0.1μF/50V/X7R	0402	WALSIN
C_{AC2}	0402B104K500CT	0.1μF/50V/X7R	0402	WALSIN
C_{BUS}	GRM188R6YA106MA73	10μF/35V/X5R	0603	MURATA
C_{PMID}	GRM188R6YA106MA73	10μF/35V/X5R	0603	MURATA
C_{PMID}	0402B104K500CT	0.1μF/50V/X7R	0402	WALSIN
C_{BTST1}	GRM033R61C473KE84	47nF/16V/X5R	0201	MURATA
C_{BTST2}	GRM033R61C473KE84	47nF/16V/X5R	0201	MURATA
C_{SYS}	GRM188R61E106MA73	10μF/25V/X5R	0603	MURATA
C_{SYS}	0402B104K500CT	0.1μF/50V/X7R	0402	WALSIN
C_{BAT}	GRM188R61E106MA73	10μF/25V/X5R	0603	MURATA
C_{REGN}	GRM155R60J475ME47D	4.7μF/6.3V/X5R	0402	MURATA
L	PIMB063T-1R0MS-68	1μH/20%/6.7mΩ	6.8x7.3x3.0mm	CYNTEC
	PIMB063T-2R2MS-68	2.2μH/20%/ 13.5mΩ	6.8x7.3x3.0mm	CYNTEC
Q6, Q7, Q8, Q9	AONR36366	N-MOSFET	DFN 3x3 EP	ALPHA and OMEGA
Q10	AON7528	N-MOSFET	DFN 3.3x3.3 EP	ALPHA and OMEGA

16 Typical Operating Characteristics

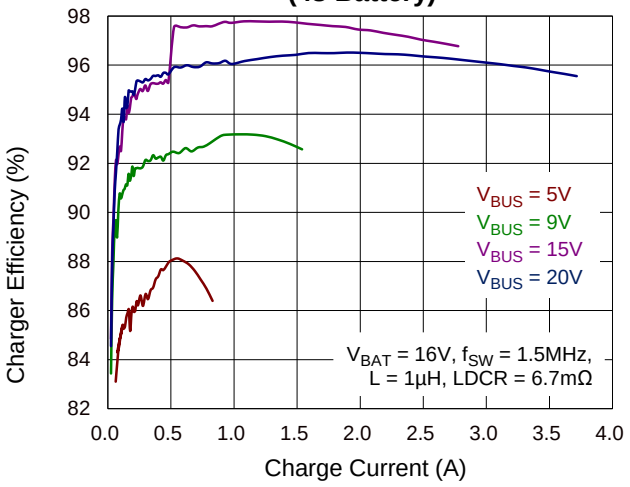
Charger Efficiency vs. Charge Current (2s Battery)



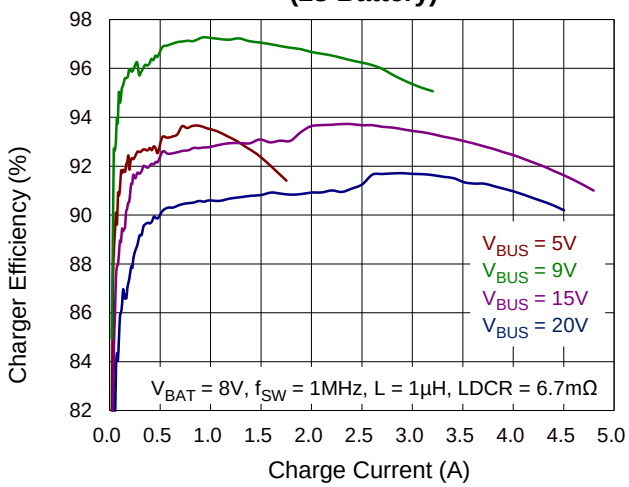
Charger Efficiency vs. Charge Current (3s Battery)



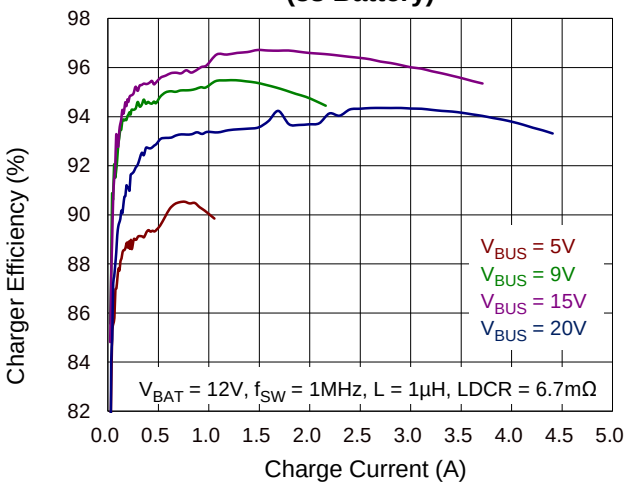
Charger Efficiency vs. Charge Current (4s Battery)



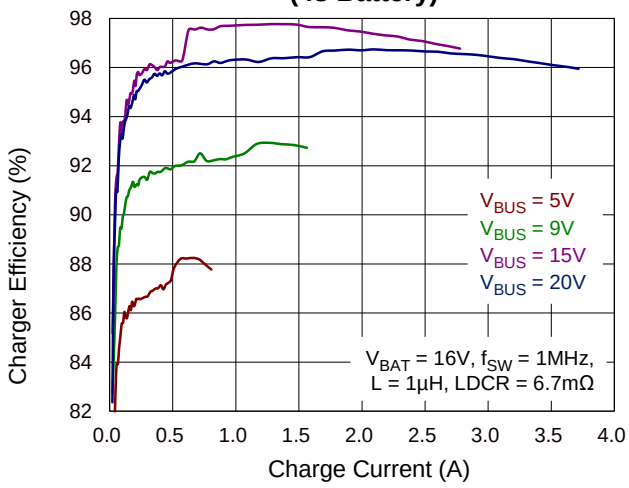
Charger Efficiency vs. Charge Current (2s Battery)



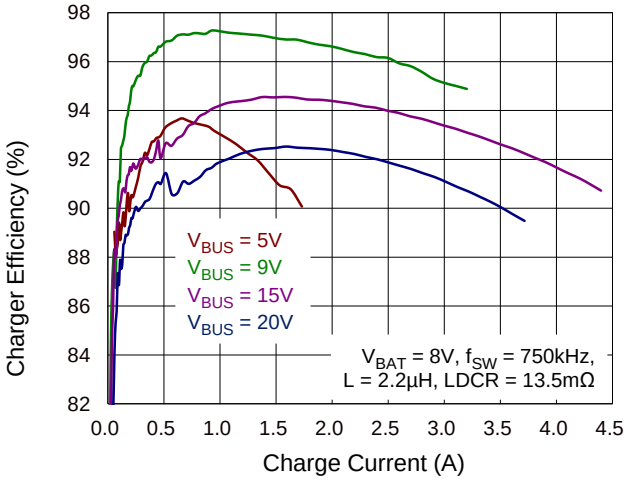
Charger Efficiency vs. Charge Current (3s Battery)



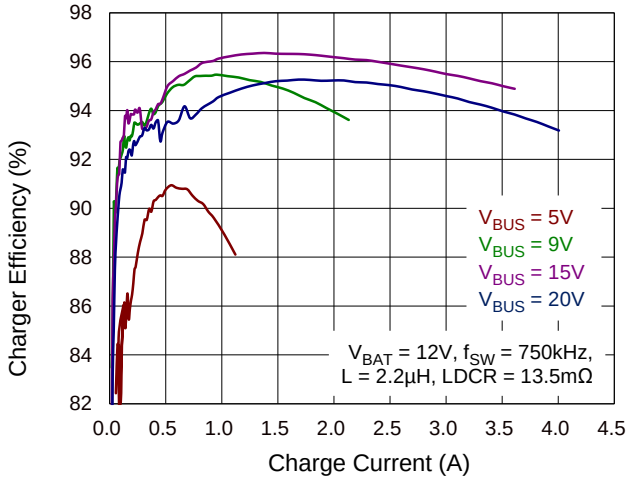
Charger Efficiency vs. Charge Current (4s Battery)



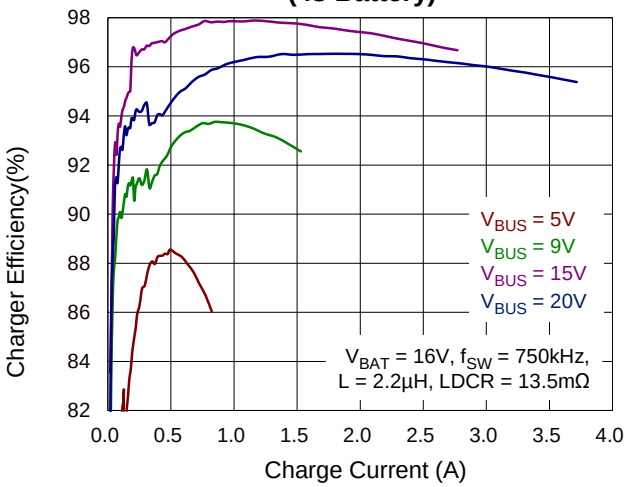
Charger Efficiency vs. Charge Current (2s Battery)



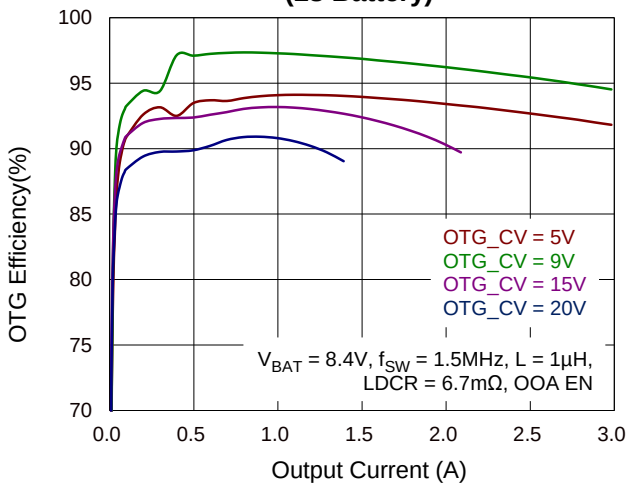
Charger Efficiency vs. Charge Current (3s Battery)



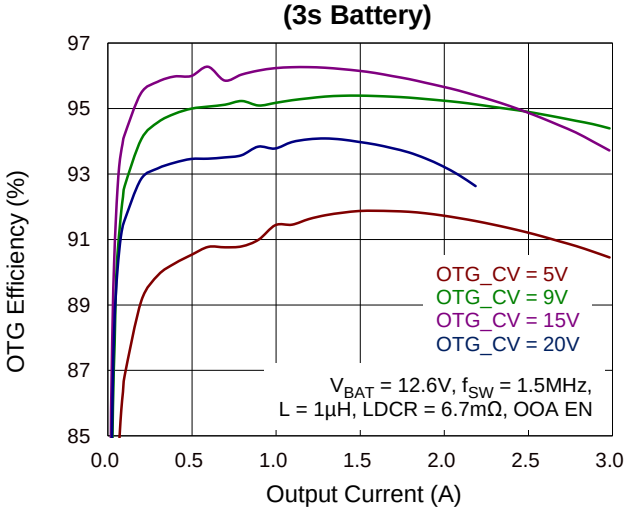
Charger Efficiency vs. Charge Current (4s Battery)



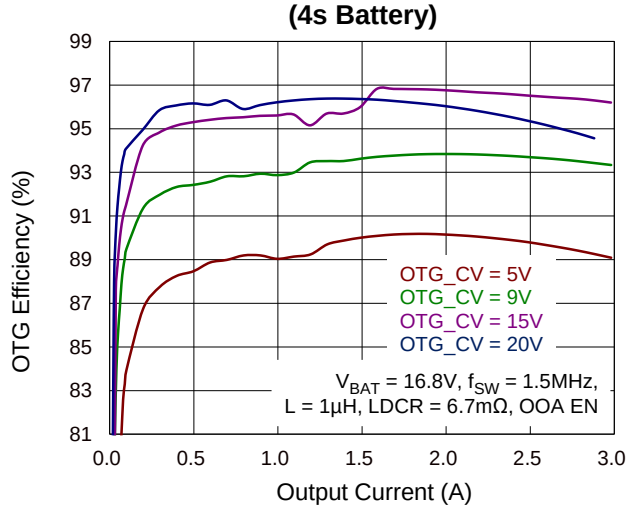
OTG Efficiency vs. Output Current (2s Battery)



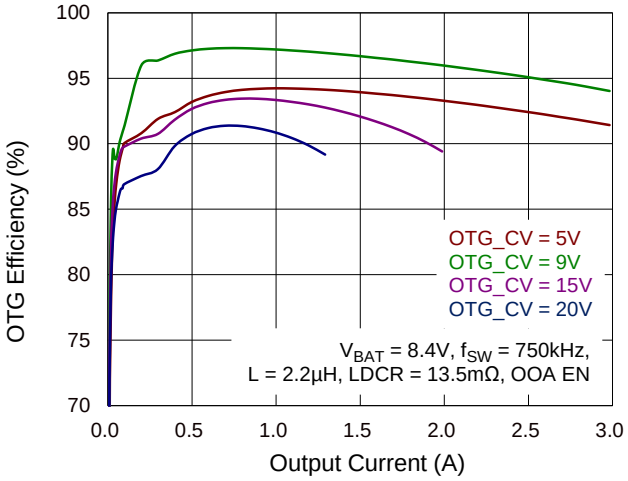
OTG Efficiency vs. Output Current (3s Battery)



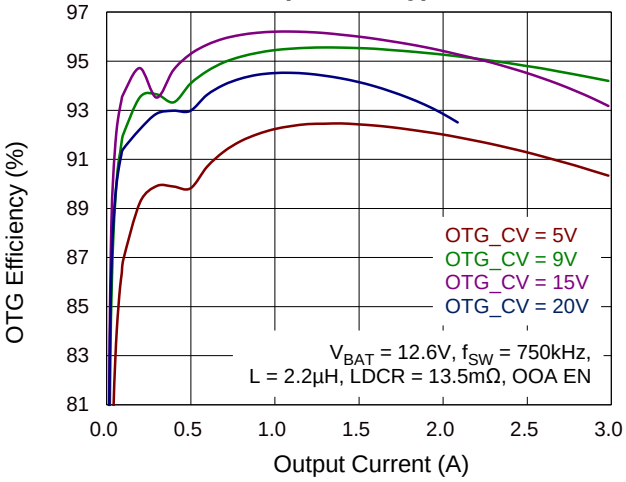
OTG Efficiency vs. Output Current (4s Battery)



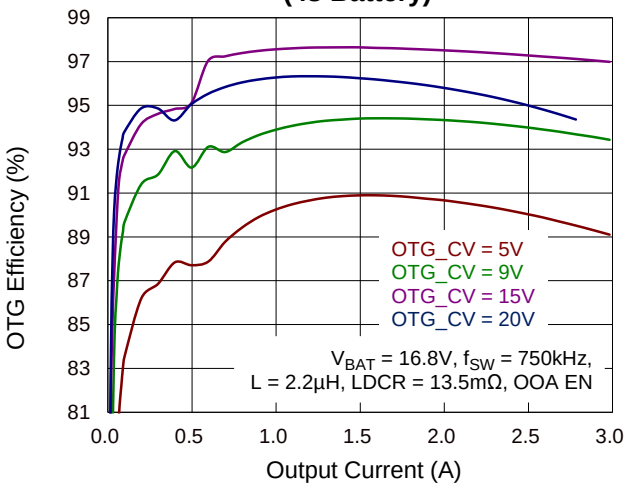
OTG Efficiency vs. Output Current (2s Battery)



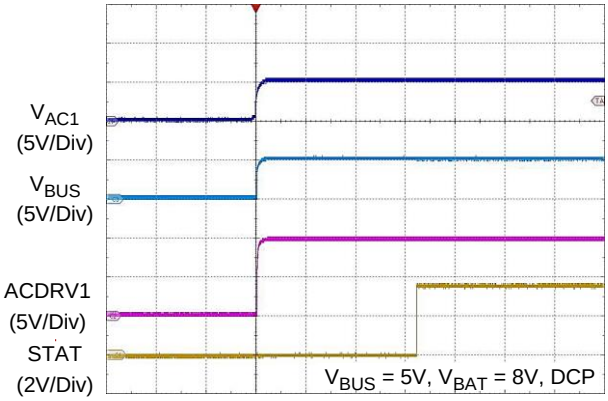
OTG Efficiency vs. Output Current (3s Battery)



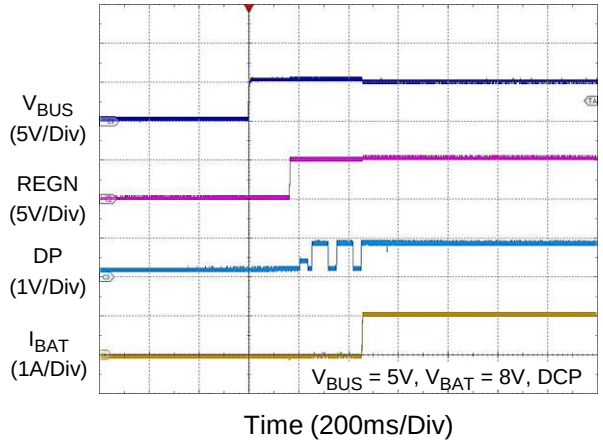
OTG Efficiency vs. Output Current (4s Battery)



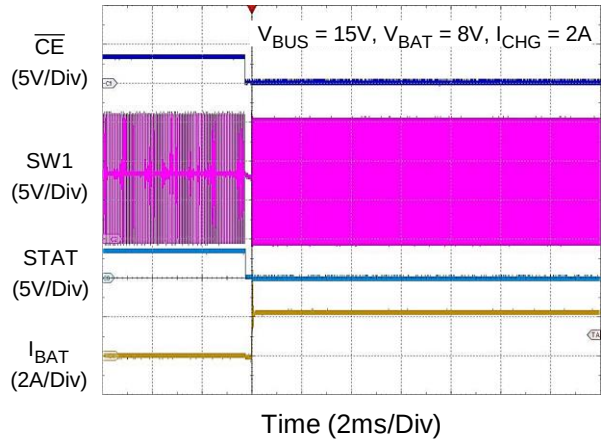
Power-UP with AC_RB1, VAC1 Plug in



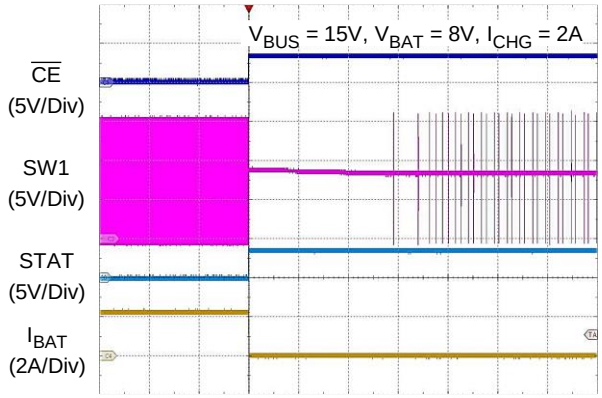
Power-UP with Single Input, VBUS Plug in



Charger Enabled

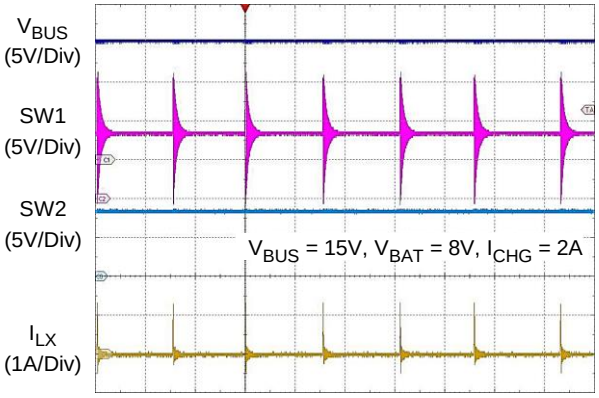


Charger Disabled



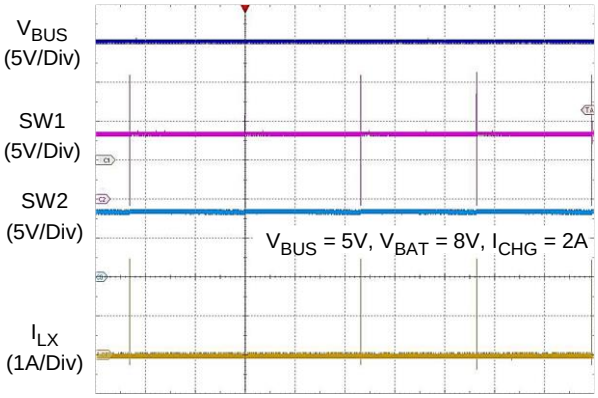
Time (2ms/Div)

Charger Disabled, OOA Enabled



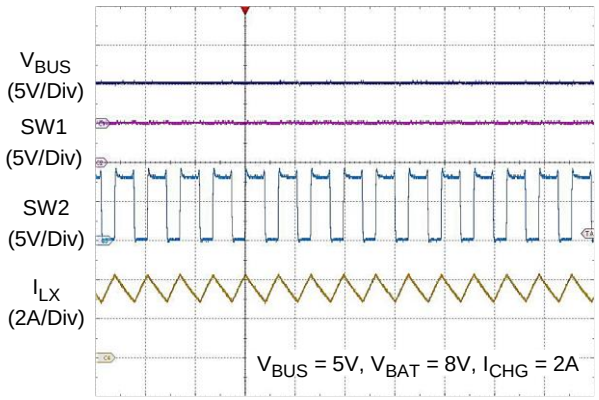
Time (20μs/Div)

Charger Disabled, OOA Disabled



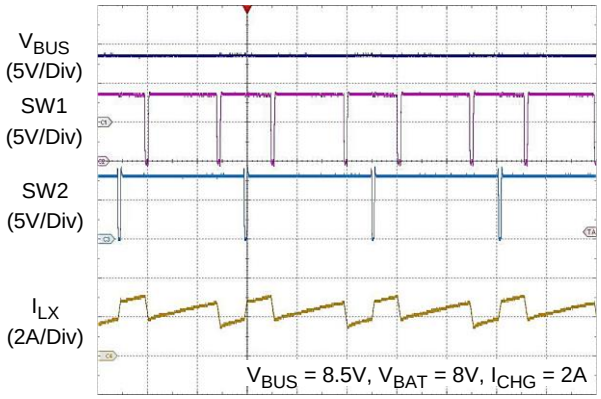
Time (1ms/Div)

Boost Mode, Charger Enabled



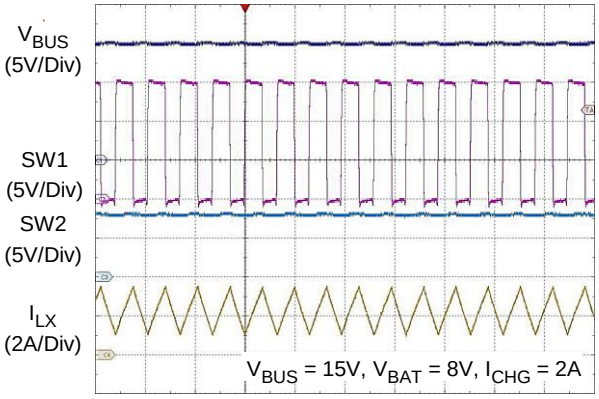
Time (1μs/Div)

Buck-Boost Mode, Charger Enabled



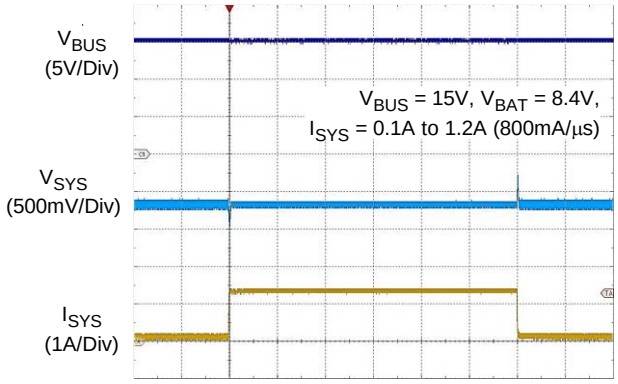
Time (2μs/Div)

Buck Mode, Charger Enabled



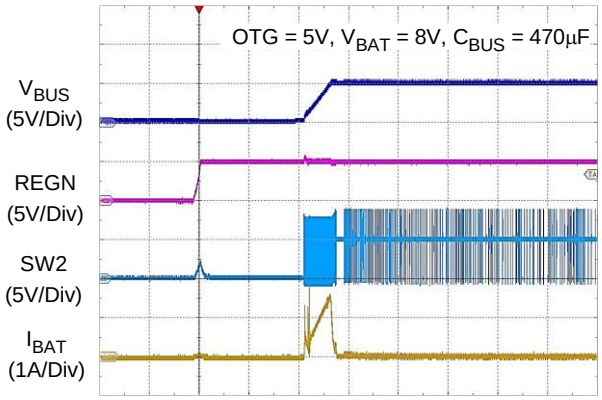
Time (1μs/Div)

System Load Transient, Charger Disabled



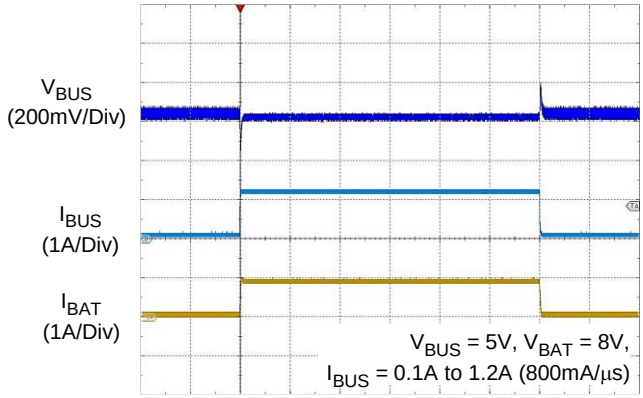
Time (1ms/Div)

OTG Start-Up



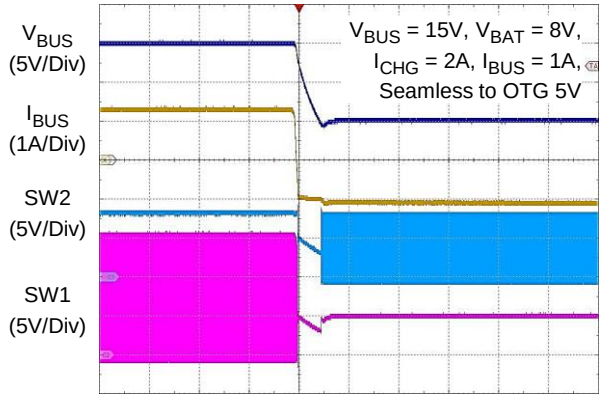
Time (2ms/Div)

OTG Load Transient



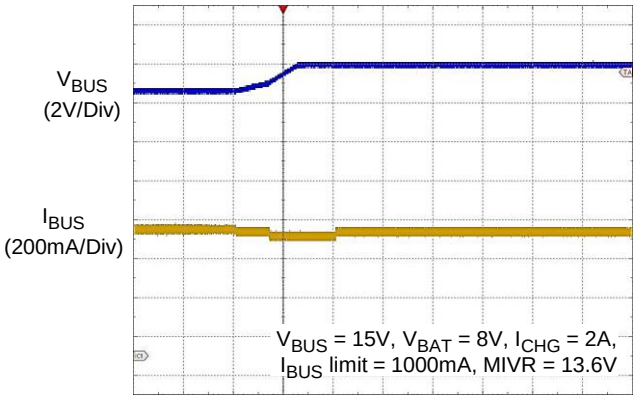
Time (1ms/Div)

Seamless



Time (200μs/Div)

AICC Enabled



Time (50ms/Div)

17 Application Information

(Note 9)

17.1 Power-On-Reset (POR)

The device can be powered from either the battery or the bus. After VBATP rises above V_{BATP_UVLO} and VBAT rises above V_{BAT_UVLO} sequentially, or after VAC1 or VAC2 rises above V_{AC_UVLO} and VBUS rises above V_{BUS_UVLO} sequentially, the I^2C interface will be ready for communication and all the registers are reset to their default values.

17.1.1 The PROG Pin for Cell and Frequency Setting

During the POR stage, the device detects the pull-down resistance on the PROG pin and then sets register 0x0A[7:6] for BATTERY_CELL and register 0x13[5] for PWM_FREQ. Refer to Table 2 for the PROG pin pull-down resistor selection. It is recommended that the pull-down resistor on the PROG pin have a tolerance of ±1% to 2%.

17.1.2 BATTERY_CELL for Default Charging Parameter

After the PROG pin is detected, the BATTERY_CELL will be set by the PROG pull-down resistance, and then the registers listed in Table 3 will be set by BATTERY_CELL for the default charging parameters.

Table 2. The PROG Pin Resistance for Cell and Frequency Setting

Cell	Resistance for Typical Value	Frequency	BATTERY_CELL	PWM_FREQ
2s	6.04kΩ	1.5MHz	01	0
	8.2kΩ	750kHz		1
3s	10.5kΩ	1.5MHz	10	0
	13.7kΩ	750kHz		1
4s	17.4kΩ	1.5MHz	11	0
	27.0kΩ	750kHz		1

Table 3. Default Register Setting for Charging Parameter by BATTERY_CELL

BATTERY_CELL (REG0x0A[7:6])	2s	3s	4s
VSYSMIN (REG 0x00[5:0])	7V	9V	12V
VBAT_REG (REG 0x01[10:0])	8.4V	12.6V	16.8V
VBAT_REG range	5V to 9.99V	10V to 13.99V	14V to 18.8V
ICHG_CTRL (REG 0x03[8:0])	2A	1A	1A

After the POR, the charging parameters shown in Table 3 can be programmed by I^{2}C; however, the VBAT_REG has a programming range that depends on the BATTERY_CELL setting, so the host needs to ensure that the programmed value is within the correct range. If the host programs a value outside this range, the charger will ignore it and retain the original value. The charging parameters in Table 3 can be changed by programming the BATTERY_CELL. When the host needs to program any parameter in REG0x0A, it must program REG0x0A first before programming other registers.

17.1.3 Device Power Up from Battery Only

When only the battery is present and VBATP is above VBATP_UVLO, the SHIPFET turns on to connect VBATP to VBAT. Then, when VBAT is above VBAT_UVLO, the BATFET turns on to connect VBAT to VSYS. The REGN stays off to minimize the quiescent current. The low quiescent current on VBAT and the low R_{DSON} of the BATFET minimize device power consumption and conduction loss, thereby maximizing battery run life.

The device always monitors the discharge current through the BATFET (battery supply mode). When the system is shorted or overloaded (IBAT > IBAT_OCP), if SHIP_FET_PRESENT = 1 (0x14, bit[7]) and EN_BATOC = 1 (0x14, bit[0]), the device turns off the SHIPFET and BATFET immediately to enter Shipping Mode. The device remains in shipping mode until VBUS is plugged in again or other methods are used to exit shipping mode and re-enable the BATFET.

17.2 Dual-Input Power Selection

The charger has two ACDRV drivers to control optional back-to-back N-channel MOSFETs for input power source selection. During the POR, the ACDRV pin detects whether the optional AC-RBFET is present or not, and then updates status to ACRB1_STAT and ACRB2_STAT. Table 4 shows the detailed status.

Table 4. Optional AC-RBFET Status for Input Power Selection

Scenario	AC-RBFET 1 present	AC-RBFET 2 present	ACDRV1 pin	ACDRV2 pin	ACRB1_STAT	ACRB2_STAT
Single Input	N	N	GND	GND	0	0
One AC-RBFET	Y	N	Gate	GND	1	0
	N	Y	GND	Gate	0	1
Dual Input	Y	Y	Gate	Gate	1	1

17.2.1 Single Input

In this scenario, the input power source comes only from VBUS, with both of VAC1 and VAC2 connected to VBUS. After the POR, the control register EN_ACDRV1 and EN_ACDRV2 remain at 0.

17.2.2 One AC-RBFET

In this scenario, only AC-RBFET1 or AC-RBFET2 is present. For example, only AC-RBFET1 is present, the ACDRV1 connects to the gate of AC-RBFET1, and the ACDRV2 pulls down to GND. VAC2 connects to VBUS. After the POR, the register EN_ACDRV2 remains at 0.

1. When VAC1 > V_{AC_UVLO}, the charger sets the register EN_ACDRV1 = 1 to turn on AC-RBFET1.
2. To swap the input source from VAC1 to another power source, the host must first set the register DIS_ACDRV_EN = 1 to force EN_ACDRV1 = 0, turning off AC-RBFET1. After VBUS < V_{BUS_UVLO}, the host enables another power source to directly connect to VBUS for input power source.

17.2.3 Dual Input

In this scenario, both AC-RBFET1 and AC-RBFET2 are present.

1. When VAC1 is plugged in and VAC1 > V_{AC_UVLO}, the charger sets the register EN_ACDRV1 = 1 to turn on AC-RBFET1.
2. When VAC2 is subsequently plugged in and VAC2 > V_{AC_UVLO}, the charger still keeps the register EN_ACDRV1 sets to 1.
3. To swap the input power source from VAC1 to VAC2, the host must set EN_ACDRV1 = 0 and EN_ACDRV2 = 1 at the same time. After the register are programmed, the charger turns off AC-RBFET1.
4. After VBUS < V_{BUS_UVLO}, the charger automatically turns on AC-RBFET2 to swap the input power source from VAC1 to VAC2.
5. When VAC2 is unplugged, after VAC2 < V_{AC_UVLO}, the charger sets EN_ACDRV2 = 0 to turn off AC-RBFET2.
6. After VBUS < V_{BUS_UVLO}, the charger automatically sets EN_ACDRV1 from 0 to 1 to turn on AC-RBFET1.
7. When VAC1 is unplugged and VAC1 < V_{AC_UVLO}, the charger sets EN_ACDRV1 = 0 to turn off AC-RBFET1.

If both VAC1 > V_{AC_UVLO} and VAC2 > V_{AC_UVLO}, and the host sets EN_ACDRV1 = 1 and EN_ACDRV2 = 1, the charger will ignore and keep the original register setting. The charger does not allow both AC-RBFET1 and AC-RBFET2 to be turned on at the same time.

17.3 Device Power-Up from Input Power Source

When input power is present on VBUS, and VBUS is above V_{BUS_UVLO}, the power-up sequence is as follows:

1. Power up the REGN LDO.
2. Poor Source Detection
3. VBUS_STAT detection is based on input source type to set the default AICR register.
4. The device detects the voltage on the ILIM_HZ pin to set ILIM, the final input current limit is based on the minimum value between AICR and ILIM.
5. The device detects voltage on VBUS to set the default MIVR register.
6. Buck-boost converter power-up.

17.4 Power-Up REGN LDO

The REGN LDO supplies power for the internal bias circuit and the buck-boost power MOSFET gate driver. The REGN also provides bias to the TS and ILIM_HZ external resistors and the pull-up rail of STAT and PG. The REGN is enabled when the following conditions are met:

1. VBUS is above VBUS_UVLO
2. The charger is in OTG mode.
3. The ADC TS channel is on (ADC_EN = 1 and TS_ADC_DIS = 0)
4. DPDM manual mode is on (DP_CTRL or DM_CTRL is on)

The REGN is disabled when the following conditions are met:

1. Only VBAT is present, the ADC TS channel is off, DPDM manual mode is off, and the device is not in OTG mode.
2. The device is in HZ mode and BC1.2 is disabled.

17.5 Poor Source Detection

After REGN powers up, the device checks the current capability of the input source. The input source has to meet the following requirements to turn on the buck converter.

1. VBUS is below VBUS_OVP_RISE.
2. VBUS is above VBUS_BAD_ADP and then pulling IBUS_BAD_ADP (typical = 1kΩ).

When the input source passes above conditions, the VBUS_GD_RDY_STAT and the VBUS_GD_RDY_ FLAG turn high, and the $\overline{\text{INT}}$ pin pulses to interrupt the host. If VBUS_GD_RDY_STAT does not turn high, the device repeats poor source detection every 2 seconds. After 7 failures, the device sets the register EN_HZ = 1 and enters Z mode. The register EN_HZ can be cleared to 0 by re-plugging the adapter or by the host setting EN_HZ = 0. When VBUS triggers a poor source detection failure, the BAD_ADAPTER_FLAG turns high and the $\overline{\text{INT}}$ pin pulses to interrupt the host.

17.6 VBUS Source Type Detection

After VBUS_GD_RDY_STAT turns high, the device runs VBUS source type detection. Once detection is completed, the BC12_DONE_STAT and BC12_DONE_ FLAG turn high, and the $\overline{\text{INT}}$ pin pulses to interrupt the host. When VBUS source type detection is completed, the following registers are updated:

1. VBUS_STAT is updated to indicate VBUS source type.
2. The AICR register is automatically updated to the result of VBUS_STAT if AUTO_AICR = 1. The AICR setting results are listed in Table 5.

Table 5. AICR Setting from D+/D- Detection

Detection	AICR Setting	VBUS_STAT
USB SDP	0.5A	0001
USB CDP	1.5A	0010
USB DCP	3.25A	0011
NSDP	3.25A	0101
Special Adapter	1A/2A/2.1A/2.4A	0110

The device supports standard USB BC1.2 and special adapter, detection result is listed in Table 6.

Table 6. AICR Setting from Special Adapter

D+/D- Voltage Threshold	AICR Setting
0.9V < D+ < 1.5V	2A
1.5V < D+ < 2.3V 2.3V < D-	1A
D+ > 2.3V D- < 2.3V	2.1A
D+ > 2.3V D- > 2.3V	2.4A

17.7 Average Input Current Regulation (AICR)

The range of AICR is from 100mA to 3.3A with a 10mA resolution. When the register AUTO_AICR is set to 1, the device automatically changes AICR after VBUS source type detection. Refer to Table 5 and Table 6 for detailed information. After the charger automatically sets AICR, the AICR register is programmable by the host.

17.8 ILIM_HZ Detection

After poor source detection, the charger starts to measure the ADC voltage on the ILIM_HZ pin and calculates ILIM using the equation: V_{ILIM_HZ} = 1V + 800mΩ x ILIM. When the register ILIM_HZ_EN is set to 1, the charger input current limit is set to the minimum value between AICR and ILIM. If the ILIM calculation result is less than 100mA, the charger clamps ILIM at 100mA.

When the ILIM_HZ pin is pulled lower than 0.75V, the charger stops switching and REGN stays on either in charger or OTG mode. The charger resumes switching when the ILIM_HZ pin voltage rises higher than 1V.

17.9 Minimum Input Voltage Regulation (MIVR)

The MIVR function prevents input voltage from dropping due to insufficient current provided from input power source. The VBUS voltage decreases to VMIVR setting level when the overcurrent condition of input power source occurs. The default setting of the VMIVR register is 3.6V, and it can be programmed by the host, with a range from 3.6V to 22V and a 0.1V resolution. If the register AUTO_MIVR is set to 1, after poor source detection, the charger starts to measure the ADC voltage on VBUS before the charger starts switching. The register VMIVR will be set to VBUS − 0.7V when VBUS_ADC < 7V, or set to VBUS − 1.4V when VBUS_ADC ≥ 7V.

During the charging process, if the input voltage changes, and the register FORCE_MIVR_DET is set to 1 by the host, the charger stops switching and measure the ADC voltage on VBUS to re-update VBUS_ADC. According to the above calculation equation, the register VMIVR updates to the new value, and the charger resumes switching.

When DIS_EOC_FCCM is set to 0 to enable FCCM and increase EOC accuracy, the MIVR setting level must be set to a −25% voltage difference from VBAT_REG to avoid the converter from working in buck-boost operation mode when VBUS is unplugged.

17.10 Converter Power-Up

After the input and MIVR are set, the converter is enabled and starts switching. The BATFET stays on unless the charger is disabled (CHG_EN = 0 or EN_PIN is pulled-high).

The device integrates a synchronous PWM controller with high-accuracy current and voltage regulation. The switching frequency can be programmed to 750kHz, 1.5MHz, or 1.0MHz by the register PWM_FREQ and PWM_1MHZ_EN or the PROG pin. The switching frequencies 1.5MHz and 1.0MHz are only for the 1.0μH inductance. The switching frequency 750kHz is only for the 2.2μH inductance.

The device supports PFM control to improve light-load efficiency and also supports OOA (Out-of-Audio) control via the register DIS_CHG_OOA to prevent the converter from switching at audio frequencies.

Table 7. Switching Frequency and Inductor Setting

Frequency	Inductance
750kHz	2.2μH
1.5MHz	1.0μH
1MHz	1.0μH

17.11 OTG Mode Operation

The RT9492 also supports OTG (On-The-Go) mode and enters OTG mode via the register EN_OTG. The maximum output current is up to 3.32A. In OTG mode, the VBUS_STAT register bits are updated to 0111, the VBUS output voltage is 5V, and the output limit current is 3A by default. The output voltage (VOTG), output current limit (IOTG), and input current limit (IBAT_REG) can be programmed by the host. The OTG mode operation can be enabled under the following conditions:

1. VBAT is above the VOTG_LBP rising threshold.
2. EN_OTG is set to high.
3. The voltage at the TS pin is within the acceptable range ($V_{TS\_HOT\_OTG}$ < VTS < $V_{TS\_COLD\_OTG}$).

When the above conditions are met, refer to Table 4 for AC_RBFET configuration for the settings below.

17.11.1 Single Input

In this scenario, there are no AC-RBFETs, the converter starts up with a 4ms delay after the register EN_OTG is set to 1, then the VBUS voltage rises to the VOTG setting.

17.11.2 One AC-RBFET

In this scenario, only AC-RBFET1 or AC-RBFET2 is present. For example, if only AC-RBFET1 is present, when the register EN_OTG is set to 1.

1. The converter starts up with a 4ms delay after the register EN_ACDRV1 is set to 1, then the VAC1 voltage rises to the VOTG setting.
2. If the register DIS_ACDRV_EN is set to 1, the converter starts up with a 4ms delay, then VBUS voltage rises to the VOTG setting.

17.11.3 Dual Input

In this scenario, both of AC-RBFET1 and AC-RBFET2 are present. When the register EN_OTG is set to 1.

1. The converter starts up with a 4ms delay after the register EN_ACDRV1 is set to 1, then the VAC1 voltage rises to the VOTG setting.
2. To swap the OTG output from VAC1 to VAC2, the register EN_ACRDV1 is set to 0 and EN_ACDRV2 is set to 1. The device pulls low the ACDRV1 pin to turn off AC-RBFET1, and pulls up the ACDRV2 pin to turn on AC-RBFET2, then the VAC2 voltage rises to VOTG setting.
3. If register DIS_ACDRV_EN is set to 1, the device forces EN_ACDRV1 and EN_ACDRV2 to 0, the converter starts up with a 4ms delay, then the VBUS voltage rises to the VOTG setting.

In OTG mode, if the host sets EN_ACDRV1 = 1 and EN_ACDRV2 = 1, the device will ignore these settings and keep the original register setting. The charger does not allow to turn on AC-RBFET1 and AC-RBFET2 at the same time.

In OTG mode, the device supports PFM control to improve light-load efficiency, and also supports OOA (Out-of-Audio) control by the register DIS_OTG_OOA to prevent the converter from switching at the audio frequencies.

In OTG mode, the device monitors discharge current from the battery. When the battery discharge current is higher than register IBAT_REG setting, the device starts to decrease the OTG output current to prioritize the system power. If the system power continues to increase and the OTG output voltage falls below OTG_UVP, the converter will turn off to maintain system power.

17.12 IBAT Regulation During OTG Mode

The range of IBAT_REG is from 3A to 5A with a 1A resolution. In OTG mode, when the discharge current from the battery exceeds the IBAT_REG setting, the converter starts to decrease the output voltage to regulate the output power from the battery. The device also supports disabling IBAT_REG after the converter starts switching in OTG mode. If IBAT_REG is set to 11 to disable IBAT_REG before the converter starts switching in OTG mode, the IBAT_REG will be set to default setting.

17.13 Power Path Management

The device provides automatic power path selection to supply system (VSYS) from VBUS, VBAT (battery), or both of them.

17.13.1 SHIPFET Control

The device supports the SDRV driver for an optional SHIPFET. With the optional SHIPFET, after POR, the register SHIP_FET_PRESENT must be set to 1 by the host, and the SHIPFET is controlled by the register SDRV_CTRL.

17.13.2 IDLE

When BATP is higher than the VBAT_UVLO rising threshold, the SDRV pin turns on the SHIPFET, and the device powers on with the default register settings.

17.13.3 Shutdown Mode

To extend battery life during shipping or storage, the device supports an extremely low battery leakage current in shutdown mode. When the device enters shutdown mode, it turns off the SHIPFET, internal BATFET, and internal circuits. The only way for the device to exit shutdown mode and restore power to the system is by plugging in VBUS. All registers return to their default settings when the device exits shutdown mode. The device can enter shutdown mode when operating under the battery-only condition.

17.13.4 Ship Mode

When the device enters ship mode, it turns off the SHIPFET and internal BATFET. The device can exit ship mode to restore power to the system by the following methods:

1. Plug in VBUS.
2. Set SDRV_CTRL to IDLE.
3. Set the RST_ALL or REG_RST bit to reset all registers to default.
4. Press the QON pin from high to low.

The device can enter ship mode when operating under the battery-only condition.

17.13.5 System Power Reset

The device supports system reset via SDRV_CTRL by the host. When entering system power reset, the device turns off the SHIPFET and BATFET; after 600ms, the device restores power to the system and SDRV_CTRL goes back to IDLE. The device can enter system power reset even with VBUS plugged in.

The host can set SDRV_DLY = 1 to turn off the SHIPFET and BATFET immediately or set SDRV _DLY to 0 to delay 10s before turning off the SHIPFET and BATFET.

17.13.6 The QON Pin Operation

The QON pin has two functions to control the SHIPFET and BATFET. The register SHIP_FET_PRESENT must be set to 1 by the host to enable the QON function.

- **Exit Ship Mode**

Press the QON pin from high to low with a deglitch time set by the register QON_EXIT_SHIP_DLY setting time, the device turns on the SHIPFET and BATFET to restore power to the system.

- **SYSTEM Reset**

When the register QON_RST_EN is set to 1, pressing the QON pin from high to low with a deglitch time of 10s will trigger the device to turn off the SHIPFET and BATFET. After 600ms, the device turns on the SHIPFET and BATFET to restore power to the system.

17.14 Battery Charging Management

The device supports a charge current of up to 5A with a 9mΩ BATFET to improve charge efficiency and decrease voltage drop during battery discharging.

17.14.1 Charging Cycle

When battery charging is enabled (the CE pin set to low and EN_CHG = 1), the device autonomously completes a charging cycle without host controls. The device's default parameters are shown in Table 3. The host can also change charging parameters through I^2C.

A charging cycle starts under the following conditions:

1. The buck-boost converter starts.
2. Battery charging is enabled (CE pin is low, EN_CHG = 1)
3. There is no thermal fault on TS.
4. There is no safety timer fault.

The charger is in "end of charge status" when the charging current is below the EOC current threshold, the battery voltage is above recharge voltage threshold, and the device is not in AICR, MIVR, JEITA, CYC_OCP, or thermal regulation.

When the battery voltage discharges below the recharge threshold (threshold set through the VRECHG register bits), the device restarts a new charging cycle automatically. After the charge is complete, toggling the CE pin or CHG_EN can restart a new charging cycle.

17.14.2 Battery Charging Profile

The device charges the battery in five stages: trickle charge, pre-charge, constant current, constant voltage and background charge (optional).

Table 8. Charging Current Setting

Current Parameter	Default Current Setting	CHG_STAT
$I_{TRICKLE\_CHG}$	100mA	001
I_{PRE_CHG}	120mA	010
I_{CHG_REG}	2A (2s)/1A (3s, 4s)	011 (CC Mode)/100 (CV Mode)
I_{EOC_CHG}	200mA	111

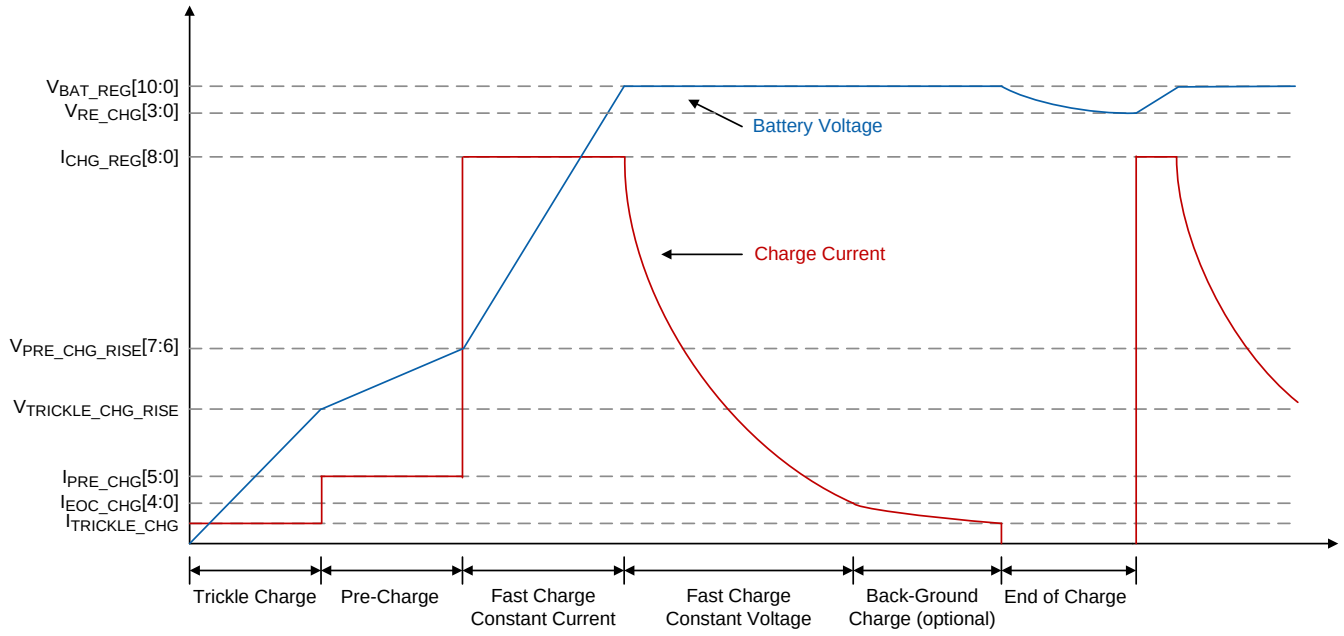


Figure 1. Charging Profile

17.14.3 End of Charge (EOC)

The charger enters end of charge status when the battery voltage is above the recharge threshold and the charge current is below I_{EOC_CHG}. The I_{EOC_CHG} setting range is from 120mA to 1000mA with a 40mA resolution. After EOC, the BATFET turns off if the register EN_TE is set to 1 and BG_CHG_TMR is set to 00. The buck-boost converter continues switching to supply power to the system. The BATFET will turn on again when the battery voltage falls below the recharge voltage threshold or if the device is in battery supply mode during EOC.

When EOC occurs, there are four conditions as shown in Table 9:

Table 9. EOC Status Scenario

	TE = 1 BG_CHG_TMR (disable)	TE = 1 BG_CHG_TMR (counting)	TE = 1 BG_CHG_TMR (timeout)	TE = 0 BG_CHG_TMR (disable)
STAT Pin	High	High	High	Low
CHG_STAT	111	110	111	101
BATFET	OFF	ON	OFF	ON

1. If the device triggers AICR, MIVR, JEITA, CYC_OCP, or thermal regulation status during charging, the actual charging current will be less than the programmed value. In this condition, the EOC function will be disabled, and the safety timer's counter clock rate will be halved.
2. The background charge can be applied after EOC is detected. The background charge is enabled by setting the register BG_CHG_TMR and EN_TE = 1 only. When background charge occurs, the CHG_STAT is set to 110, and the BATFET will turn off after the background charge timer expires.
3. The BG_CHG_TMR gets reset under one of the following conditions:
   - EN_CHG is disabled and then enabled
   - EOC status re-triggered

- The EOC_RST bit is set
- The REG_RST bit is set
- The RST_ALL bit is set

An INT pulse is asserted to the host when entering background charge and when the background charge timer expires.

4. When DIS_EOC_FCCM is set to 1, the IEOC accuracy will be lower than the values in the Electrical Characteristic table. To increase accuracy, set DIS_EOC_FCCM to 0. Refer to the MIVR function for application notice.

17.14.4 Optimized VDS on BATFET

The device deploys a power path function with the BATFET separating the system from the battery. The minimum system voltage is set by the register VSYSMIN. The default VSYSMIN setting is controlled by the PROG pin.

When the battery voltage is below the VSYSMIN setting, the BATFET operates in saturation mode as an LDO, and the system voltage is typically 200mV above the VSYSMIN setting. When the battery voltage rises above VSYSMIN, the BATFET turns fully on to minimize R_{DSON}, optimizing the VDS (voltage different between VSYS and VBAT) on the BATFET.

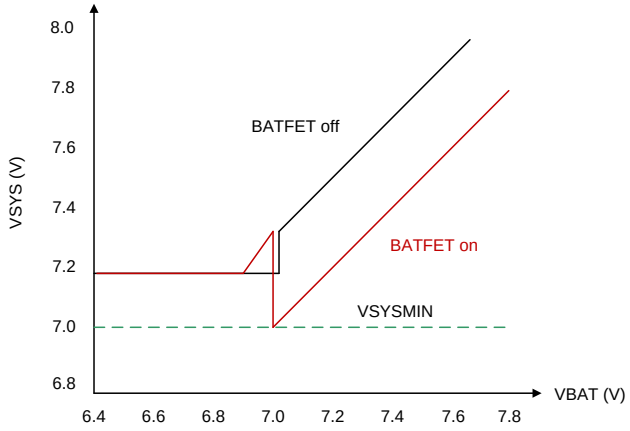


Figure 2. VSYS vs. VBAT for 2s Battery

When the BATFET turns off and the battery voltage is above VSYSMIN, the system is regulated at typically 300mV above the battery voltage. The status register VSYSMIN_STAT is set to 1 when the system is in minimum system voltage regulation.

17.14.5 DIS_LDO Mode

When the battery voltage is below the VSYSMIN setting, the BATFET operates in saturation mode as an LDO, and the maximum charge current will be limited to under 2A. The device supports disabling LDO mode via the register DIS_LDO, which can be set to 1 by the host. When DIS_LDO is set to 1, the BATFET turns fully on even when the battery voltage is below the VSYSMIN setting, and the VSYS will not regulate on VSYSMIN setting. In DIS_LDO mode, the charge current follows the ICHG_CTRL/IPRE_CHG setting. The DIS_LDO mode only operates when the battery voltage is above the $V_{TRICKLE\_CHG\_RISE}$.

17.15 Power Management System

To apply maximum current and avoid overloading the power source on VBUS, the device's Power Management System continuously monitors the power source voltage and current. When the power source is overloaded, either because the current exceeds the AICR or the voltage drops to MIVR, the device will reduce the charge current to prioritize power for the system.

When the charge current is reduced to zero but the power source still triggers AICR or MIVR, the VSYS starts to drop. Once the VSYS drops below VBAT, the device automatically switches to battery supply mode. The BATFET turns fully on, and the battery starts to discharge, so that the system is supported by both the battery and the power source.

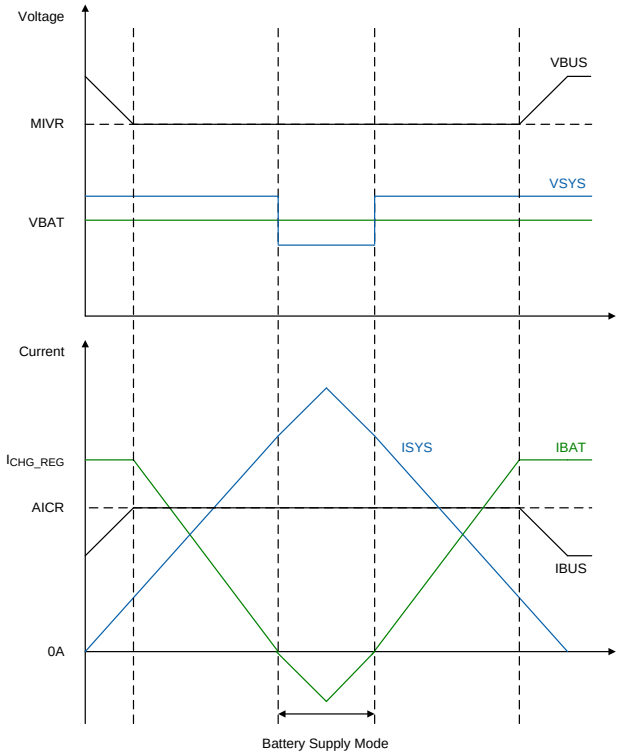


Figure 3. Power Management System

17.15.1 Battery Supply Mode

During charging, when the voltage difference between VBAT and VSYS exceeds 50mV, the BATFET turns on. The BATFET gate driver regulates the gate to minimize the VBAT-VSYS voltage difference, maintaining it at 25mV to prevent frequent transitions in and out of battery supply mode. When the voltage of VBAT-VSYS drops below 0mV, the charger exits battery supply mode and starts to charge the battery.

17.15.2 JEITA Protection During Charge Mode

The device provides a single thermistor input for temperature monitoring. To achieve battery thermal protection, JEITA guidelines were released in 2007. To start a charge cycle, the voltage on the TS pin must be within the T1 to T4 range. The device will stop charging if the battery temperature is lower than T1 (Cold) or higher than T4 (Hot). In this case, the JEITA_COLD_STAT or JEITA_HOT_STAT is set to 1, and an INT is asserted to the host. In the cool temperature range (T1 to T2), the charge current is reduced to 50% or 25% of I_{CHG_REG}, as configured by JEITA_ISET_COOL.

In the warm temperature range (T3 to T4), the voltage setting of V_{BAT_REG} is reduced or remains the same as V_{BAT_REG}, as configured by JEITA_VSET_WARM.

The device offers more flexible settings than JEITA requirements.

In the cool temperature range (T1 to T2), the charger can set the voltage of V_{BAT_REG}, configured by JEITA_VSET_COOL.

In the warm temperature range (T3 to T4), the charge current can be reduced to 50% or 25% of I_{CHG_REG}, configured by JEITA_ISET_WARM.

The device supports temperature threshold settings for COOL (T2) and WARM (T3), configured by TS_COOL and TS_WARM registers.

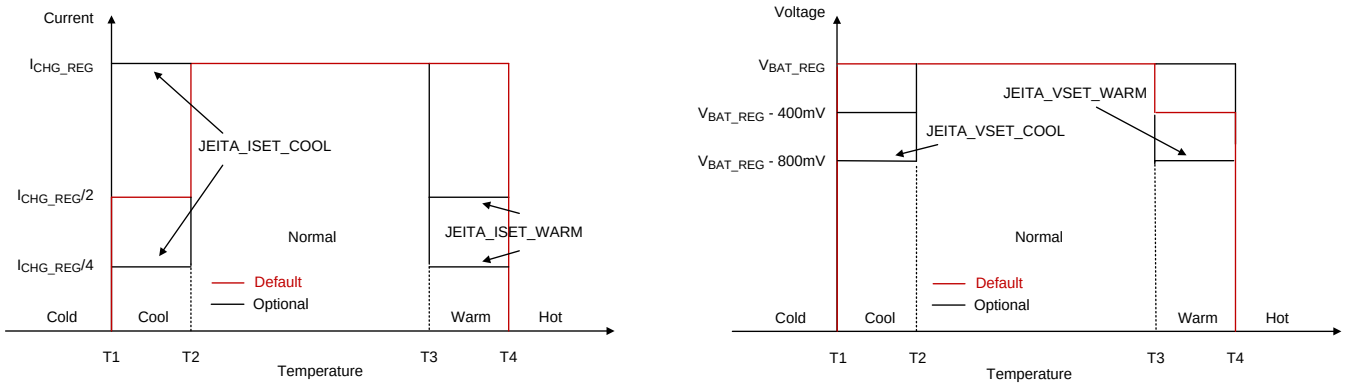


Figure 4. JEITA Protection for Charging Current and Voltage

There are four sections implemented for JEITA protection. Based on R_{HOT} and R_{COLD}, R_{TS1} and R_{TS2} can be calculated using equation (1) and (2). Here, R_{HOT} is the NTC resistance at the battery over-temperature threshold, and R_{COLD} is the NTC resistance at the battery under-temperature threshold.

$$R_{TS1} = V_{REGN} \times [(1/V_{T1} - 1/V_{T4}) / (1/R_{COLD} - 1/R_{HOT})] \quad \text{.....(1)}$$

$$R_{TS2} = R_{TS1} \times [1/(V_{REGN} / V_{T1} - R_{TS1} / R_{COLD} - 1)] \quad \text{.....(2)}$$

17.15.3 Over-Temperature Protection in OTG Mode

To start OTG mode to discharge from the battery, the voltage on the TS pin must be within the T0 to T4 range. The device will stop the converter if the battery temperature is lower than T0 (OTG_COLD) or higher than T4 (OTG_HOT). In such cases, the JEITA_COLD_STAT or JEITA_HOT_STAT is set to 1, and an INT is asserted to the host.

Once the temperature returns to the normal range, OTG mode is recovered.

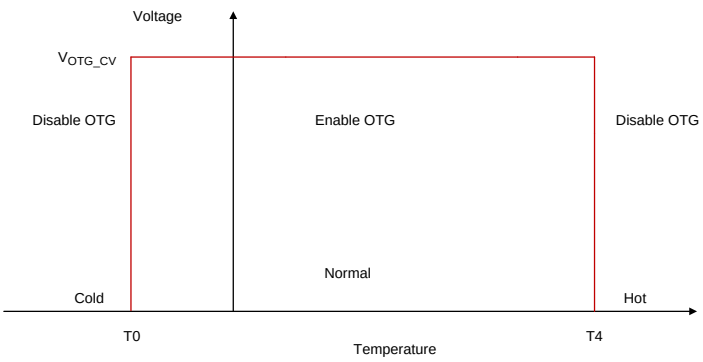


Figure 5. Over-Temperature Protection in OTG Mode

The device supports temperature threshold setting for COLD (T0) and HOT (T4) via the OTG_COLD and OTG_HOT registers.

17.16 Charging Safety Timer

The device has a safety timer to prevent abnormal charging time due to poor battery conditions. The device can set EN_TRICHG_TMR, EN_PRECHG_TMR, and EN_FASTCHG_TMR for each charging stage. When the safety timer expires, the device stops charging, and TRICHG_TMR_STAT, PRECHG_TMR_ STAT, or FASTCHG_TMR_STAT is set to 1, and an INT is asserted to the host. The safety timer can be disabled by the host.

Table 10. Charging Safety Timer

VBAT	Safety Timer
< $V_{TRICKLE\_CHG}$	1 hour
< V_{PRE_CHG}	0.5 hours, 2 hours (Default)
> V_{PRE_CHG}	5 hours, 8 hours, 12 hours (Default), 24 hours

When the charger is in AICR, MIVR, JEITA cool, JEITA warm, thermal regulation, or CYC_OCP, the safety timer's counter clock rate will be half.

For example, if the charger is in AICR status, and timer setting is 12 hours, the actual safety timer will expire in 24 hours. The extended charge timer setting can be disabled by setting TMR2X_EN = 0.

The safety timer will be reset by:

1. Toggling the $\overline{CE}$ pin
2. Disabling/enabling CHG_EN
3. Disabling/enabling safety timer
4. Setting REG_RST or RST_ALL
5. Performing a system power reset

17.17 Adaptive Input Current Control

The AICC function provides an adaptive AICR setting to prevent input voltage drops. When the input power source is overcurrent and the VBUS drops to the MIVR level, setting the EN_AICC bit to 1 will trigger the device to automatically decrease the AICR level step by step until the MIVR event is exited. Once AICC is finished, the EN_AICC bit remains at 1, the adaptive AICR setting is updated in the IAICC register, AICC_STAT is set to 10, and an INT is asserted to the host to indicate AICC_FLAG.

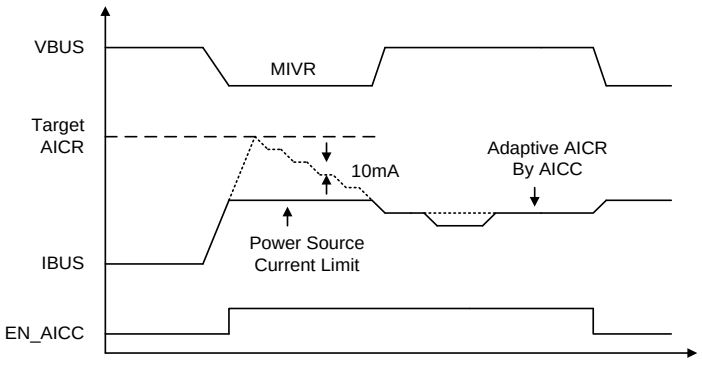


Figure 6. AICC Enable

The device supports re-enabling the AICC function by setting FORCE_AICC to 1. After AICC is completed, FORCE_AICC automatically returns to 0. FORCE_AICC can be set to 1 only after EN_AICC is enabled. The AICC function is enabled only when EN_AICC is set to 1.

17.18 MediaTek Pump Express+ (MTK, PE+)

The device can provide an input current pulse to communicate with an MTK-PE+ high voltage adapter. When the PE_EN bit is enabled, the device can increase or decrease the adapter's output voltage by setting PE10_INC or PE20_CODE to the desired value. After enabling the PE function, the device will generate a VBUS current pattern for the MTK-PE+ adapter to automatically identify whether to increase or decrease the output voltage. Once the PE pattern is finished, the PE_EN bit will clear to 0, and an INT is asserted to the host to indicate the PE_DONE_FLAG.

17.19 Watchdog Timer (WDT)

When the device is controlled by the host, most of the registers can be programmed by the host. The host must write WD_RST = 1 to reset the counter before the watchdog timeout, and it can disable the WDT function by setting the WATCHDOG bits to 00 or the SDRV_CTRL bits to 01 or 10.

When the watchdog timer expires, WDT_STAT and WDT_FLAG are set to high, the $\overline{INT}$ pin pulses to interrupt the host, and the related registers are reset to their default values (refer to Register Description for details). If the device is in watchdog timeout status, the host can write to any registers or set WD _RST = 1 to resume counting.

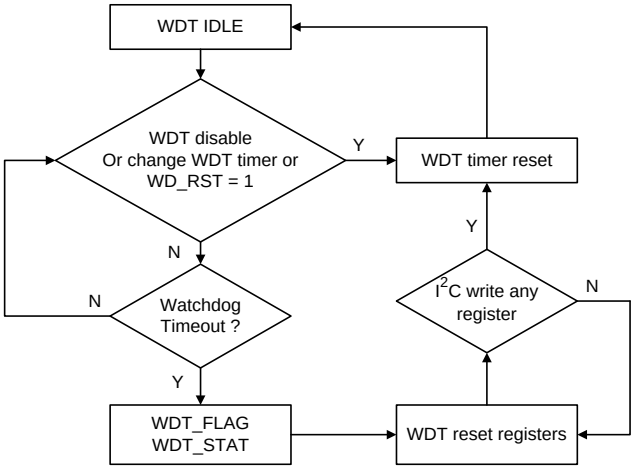


Figure 7. WDT Flow Chart

17.20 Interrupt (INT), Flag, Status and Mask

The RT9492 provides status and flag register bits to show the current or past events that occur on the device. When an interrupt request (IRQ) event occurs, the corresponding flag register bit will be set to 1. The FLAG bit can be cleared after being read by the host. The status bits show the current status of the device and are updated as the status changes. The MASK bit can enable or disable the $\overline{INT}$ pin to send a signal to the host. When the MASK register bit is set to 1, its corresponding IRQ event will not pulse the $\overline{INT}$ pin. The STAT and FLAG bits are still updated even though the MASK bit is set to 1.

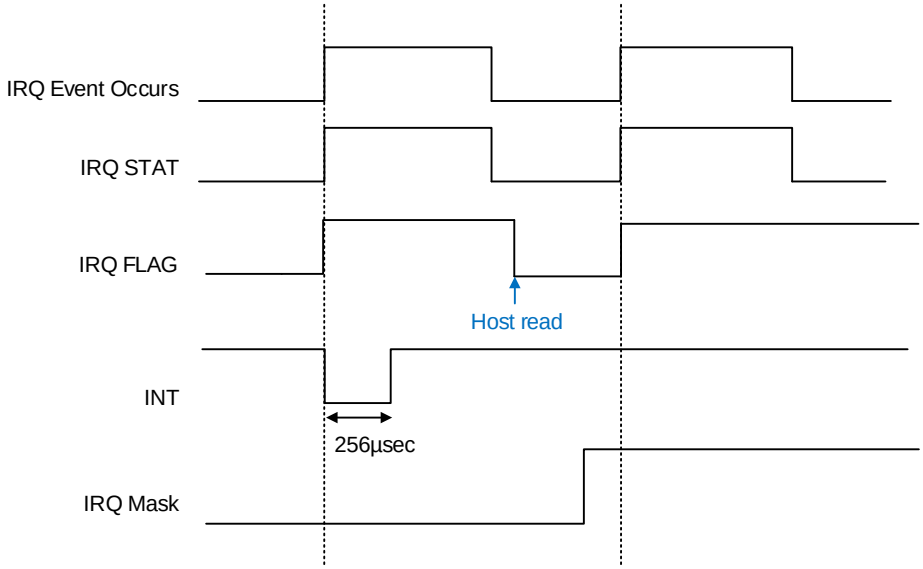


Figure 8. The Operation of Flag, Status, INT, and Mask

17.21 Status Outputs and the OTG Pin Control

17.21.1 Charging Status Indicator (The STAT/OTG Pin)

The device supports multi-function on the STAT/OTG pin. When the DIS_STAT register is set to 0, the STAT/OTG pin is configured as a STAT pin.

The device indicates CHG_STAT and any charge faults on the STAT pin. The STAT pin is an open drain that can be used to drive an LED. The STAT pin function can be disabled by setting DIS_STAT to 1.

Table 11. The STAT Pin State

CHG_STAT	STAT Indicator
Trickle, Pre, Fast charge, IEOC (EOC and TE = 0)	Low
Charge done, Back-Ground charge	High
Not charging (Without any charge fault)	High
Not charging (VBAT_OVP/VSYS_OVP/VBUS_OVP/OTP/Safety timer timeout)	Blinking at 1Hz

17.21.2 Interrupt to Host ($\overline{\text{INT}}$ Pin)

The device reports IRQ to the host via the $\overline{\text{INT}}$ pin, which is an open-drain output. The $\overline{\text{INT}}$ pin generates a low pulse of 256µs when an IRQ event occurs. When an IRQ occurs, the device pulses the INT pin to the host and stores the IRQ event in registers 0x22 to 0x27 and 0x4D until the host reads the IRQ registers. Even if the host doesn't read the IRQ registers to clear the IRQ events, the device will not send an INT pulse again unless any new event occurs. The IRQ events in register 0x22 to 0x27 are unmasked by default, while those in register 0x4D are masked by default.

17.22 Fast Role Swap (FRS)

The device supports multiple functions on the STAT/OTG pin. When the DIS_STAT register is set to 1 and OTG_PIN_EN is set to 1, the STAT/OTG pin is configured as an OTG pin.

The device supports Fast Role Swap (FRS) with the following register settings and steps:

1. Set DIS_STAT to 1 and OTG_PIN_EN to 1.
2. The device starts charging, and CHG_STAT is not in the “Not charging” status.
3. Set EN_OTG to 1 and OTG_EN_CONTROL to 1.

When the adapter is unplugged, and after VBUS drops below the VMIVR setting, and the OTG pin is pulled high, the device switches from charge mode to OTG mode. Refer to the OTG Mode Operation section for detailed OTG settings.

17.23 Seamless Transition

The device supports seamless transition to automatically switch from charge mode to OTG mode to maintain VBUS voltage output after the adapter is unplugged.

The device initiates seamless transition with the following registers settings and steps:

1. The device starts charging, and the CHG_STAT is not in the “Not charging” status.
2. Set SEAMLESS_CONTROL to a value other than 00.

When the adapter is unplugged, and after VBUS drops below the VMIVR setting, the device automatically switches from charge mode to OTG mode to maintain VBUS voltage at the VOTG setting. The register EN_OTG is automatically set to 1, and SEAMLESS_CONTROL is set to 00 by the device. Refer to the OTG Mode Operation section for detailed OTG settings.

17.24 ADC Conversion Operation

The device supports a 16-bit resolution and 11-channel ADC for device information monitoring. The ADC operation is enabled by setting ADC_EN to 1 and setting ADC_CONV_CTRL for either one-shot mode or continuous mode.

After a power-on reset (POR), when ADC_EN is set to 1, the ADC results are updated in the registers for each channel after ADC conversion. In one-shot mode, an INT pulse is asserted to the host to indicate ADC_DONE.

The IBAT_ADC and IBUS_ADC support charging current sensing in charge mode and discharging current sensing in OTG mode, which report results in 2’s complement format. When only the battery is present, the device provides only IBAT_ADC for discharging current sensing. In this case, the IBAT_PIN_EN register must also be set to 1, and the IBAT_ADC will report the result in 2’s complement format.

When TS_ADC, DP_ADC and DM_ADC are enabled, the EN_HZ register must be set to 0. During ADC conversion, the REGN turns on even if the device is powered only by the battery, and RENG remains on when the ADC operates in continuous mode.

17.25 DP/DM Output Control Manual Mode

The device supports DP/DM output control manual mode through the programmed DP_CTRL/DM_CTRL. When DP_CTRL/DM_CTRL is not set to 000, EN_HZ must also be set to 0. After REGN turns on, the manual control output voltage will be provided on DP/DM.

When the adapter is plugged in, the device will ignore the manual control setting during BC1.2 detection. Once BC1.2 is completed, an INT is asserted to the host to indicate BC1.2_DONE and DPDM_DONE, and then the manual control will be enabled.

17.26 DP/DM HOST Mode

The device supports HOST mode to configure the DP/DM as an SDP/CDP/DCP port compatible with the standard BC1.2 through the programmed HOST_MODE register.

17.27 Protections

17.27.1 VBUS Overvoltage Protection in Charge Mode

If the VBUS voltage exceeds the V_{BUS_OVP} rising threshold, the device stops switching immediately and an INT pulse is asserted to the host. When VBUS is overvoltage, the status VBUS_OVP_STAT is set to 1 and the CHG_STAT is set to 000 to stop charging. The device resumes normal operation when the VBUS voltage drops below the V_{BUS_OVP} falling threshold.

17.27.2 VBUS Overvoltage Protection in OTG Mode

If the VBUS voltage exceeds V_{OTG_OVP} rising threshold, the device stops switching immediately and an INT pulse is asserted to the host. When VBUS is overvoltage, the status OTG_OVP_STAT is set to 1. The device resumes normal operation when the VBUS voltage drops below the V_{OTG_OVP} falling threshold.

17.27.3 VAC Overvoltage Protection

If the VAC voltage exceeds the V_{AC_OVP} setting (programmable by the VAC_OVP bits), the device sets EN_ACDRV to 0 to turn off the external ACRBFET, and an INT pulse is asserted to the host. For example, if the VAC1 voltage exceeds the V_{AC_OVP} setting, the EN_ACDRV1 is set to 0, and the status VAC1_OVP_STAT is set to 1. The device resumes to normal operation when the VAC1 voltage drops below the V_{AC_OVP} falling threshold.

17.27.4 IBUS Overcurrent Protection in Charge Mode

The device monitors currents between VBUS and PMID to provide overload protection. If the IBUS current exceeds the I_{BUS_OCP} threshold, the device will set EN_HZ to 1 to stop switching immediately and set DIS_ACDRV_EN to 1 to turn off the external ACRBFETs, and an INT pulse is asserted to the host. The IBUS overload protection can be disabled by setting EN_IBUS_OCP to 0.

17.27.5 OTG Undervoltage Protection

The device monitors OTG output voltage and current to provide VBUS short circuit protection. If the VBUS voltage falls below the V_{OTG_UVP} threshold, the device stops switching. If a short circuit is detected on VBUS, the OTG will hiccup 7 times. If the converter retries are not successful, the EN_OTG bit will be set to 0 to disable OTG mode, and an INT pulse is asserted to the host to indicate OTG_UVP. The hiccup can be disabled by setting DIS_VOTG_UVP_HICCUP to 1; when hiccup is disabled, the converter continues switching even if the VBUS voltage is below the V_{OTG_UVP} threshold.

17.27.6 VSYS Overvoltage Protection

If the VSYS voltage exceeds the V_{SYS_OVP} rising threshold, the device stops switching immediately and an INT pulse is asserted to the host. When VSYS is overvoltage, the status VSYS_OVP_STAT is set to 1. The device provides a resistance sink source on VSYS to bring down the VSYS voltage. The device resumes normal operation when the VSYS voltage drops below the V_{SYS_OVP} falling threshold.

17.27.7 VSYS Undervoltage Protection

The device monitors VSYS output voltage to provide VSYS undervoltage protection. If the VSYS voltage falls below the V_{SYS_UVP} threshold, the device stops switching and an INT pulse is asserted to the host to indicate SYS_UVP. If a UVP circuit is detected on VSYS, the converter will hiccup 7 times. If the converter retries are not successful, the EN_HZ bit will be set to 1 to enter HZ mode. Re-plugging in the adapter or setting EN_HZ to 0 can exit HZ mode and restart the converter to switch. The hiccup can be disabled by setting DIS_VSYS_UVP_HICCUP to 1; when hiccup is disabled, the converter continues switching even if the VSYS voltage is below the V_{SYS_UVP} threshold.

17.27.8 VSYS Short Protection

The device monitors VSYS output voltage to provide VSYS short circuit protection. The VSYS short protection can only be enabled by the following settings:

1. The device must have a SHIPFET.
2. The SHIP_FET_PRESENT register must be set to 1.

When a short circuit is detected on VSYS, the device will set SDRV_CTRL to 10 to immediately enter ship mode, turn off SHIPFET, and assert an INT pulse to the host to indicate VSYS_SHORT.

17.27.9 VBAT Overvoltage Protection

If VBAT voltage exceeds the V_{BAT_OVP} rising threshold, the device stops switching immediately and asserts an INT pulse to the host. When VBAT is overvoltage, the status VBAT_OVP_STAT is set to 1. The device provides a resistance sink source on VBAT to bring down the VBAT voltage. The device resumes normal operation when the VBAT voltage drops below the V_{BAT_OVP} falling threshold.

17.27.10 IBAT Overcurrent Protection

The system overload protection can only be enabled by the following settings:

1. The device must have a SHIPFET.
2. The SHIP_FET_PRESENT register must be set to 1.
3. The EN_BATOC register must be set to 1.

When the system is overloaded ($I_{BAT} > I_{OCP\_BATFET}$), the device sets SDRV_CTRL to 10 to immediately enter ship mode, turn off the SHIPFET, and assert an INT pulse to the host to indicate IBAT_OCP.

17.27.11 Thermal Protection in Charge Mode

The device monitors the internal junction temperature to avoid overheating. In charge mode, the thermal regulation threshold is set at 120°C (programmable via the THREG register). When the junction temperature exceeds the thermal regulation threshold, the device decreases the input current limit. During thermal regulation, the EOC function is disabled, the safety timer's counter clock rate will be halved, and an INT is asserted to the host to indicate THREG.

The thermal regulation protection is active when EN_AICR is set to 1. In addition, the device has over-temperature protection, with the over-temperature protection threshold set at 150°C (programmable via the TOTP register). When the IC junction temperature exceeds the over-temperature protection threshold, the converter turns off immediately and an INT is asserted to the host to indicate a TOTP fault. The converter recovers when the junction temperature drops below $T_{OTP} - T_{OTP\_HYS}$.

17.27.12 Over-Temperature Protection in OTG Mode

The device monitors the internal junction temperature to avoid overheating. In OTG mode, the over-temperature threshold is set at 120°C (programmable via the THREG register). When the junction temperature exceeds the thermal regulation threshold, the device decreases the output current limit, and an INT is asserted to the host to indicate THREG.

The over-temperature protection is active when IBAT_REG is not set at disable.

In addition, the device has over-temperature protection in OTG mode.

17.27.13 Poor Source Detect Protection

The device supports source sink on VBUS to detect whether the adapter is a poor source. When a poor source is detected, the device will hiccup 7 times. If the device retries are not successful, the device will set EN_HZ to 1 and assert an $\overline{INT}$ to the host to indicate BAD_ADAPTER.

Table 12. Protection Summary

Channel	Threshold (Typical)	Deglitch (Typical)	Protection	Reset and Threshold (Typical)
VBUS_OVP	V_{BUS_OVP} rising	NA	The converter stops switching	V_{BUS_OVP} falling
VAC_OVP	V_{AC_OVP} rising	NA	Disable ACDRV1 or ACDRV2 to turn off external MOSFET	V_{AC_OVP} falling
IBUS_OCP	I_{BUS_OCP} rising	2ms	Setting REG0x0F[2] to 1 enters HZ mode to stop converter switching and disables ACDRV1 or ACDRV2 to turn off the external MOSFET.	NA
OTG_OVP	V_{OTG_OVP} rising	NA	The converter stops switching	V_{OTG_OVP} falling
OTG_UVP	V_{OTG_UVP} falling	10ms	The converter starts hiccup. After 7 hiccups, REG0x12[6] is set to 0 to disable OTG. The hiccup behavior can be programmed in REG0x13[2].	V_{OTG_UVP} rising
SYS_OVP	V_{SYS_OVP} rising	128µs	The converter stops switching	V_{SYS_OVP} falling
SYS_UVP	V_{SYS_UVP}	64µs	The converter starts hiccup. After 7 hiccups, REG0x0F[2] is set to 1 to enter HZ to stop converter switching. The hiccup behavior can be programmed in REG0x13[3].	V_{SYS_UVP} + 200mV
SYS_SHORT	V_{BAT} - V_{SYS} rising to 200mV	128µs	With an external SHIPFET, when SYS_SHORT is triggered, the SDRV_CTRL enters ship mode. The SYS_SHORT protection must be enabled by setting REG0x14[7] to 1.	NA
VBAT_OVP	V_{BAT_OVP} rising	2ms	The converter stops switching	V_{BAT_OVP} falling

Channel	Threshold (Typical)	Deglitch (Typical)	Protection	Reset and Threshold (Typical)
IBAT_OCP	I_{OCP_BATFET} rising	3ms	With an external SHIPFET, when IBAT_OCP is triggered, the SDRV_CTRL enters ship mode. The IBAT_OCP protection must be enabled by setting REG0x14[7] to 1.	NA
Thermal Regulation	T_{J_THREG} rising	32ms	Limit converter output power	T_{J_THREG} falling
Poor Source Detect	V_{BUS_MIN} falling	30ms	When a poor source is detected, after 7 hiccups, REG0x0F[2] is set to 1 to enter HZ.	V_{BUS_MIN} rising

17.28 Communication Interface

The device uses an I^2C compatible interface with a 2-wire line (SCL and SDA) to communicate with the host. The SCL and SDA pins are open-drain and need to be connected to the supply voltage via pull-up resistors. The device operates as an I^2C slave device with a 7-bits address of 53H and supports clocks up to 3.4MHz conditionally. To start an I^2C communication, begin with a START (S) condition, and then the host sends the slave address. This address is a 7 bits long followed by an eighth bit which is a data direction bit (R/W). The second byte is the register address. The third byte contains the data for the selected register. End with STOP (P) condition.

17.28.1 I^2C Time-Out Reset

To avoid I^2C hang-ups, a timer runs during I^2C activity. If the SDA remains low for longer than 1 second, the device will reset the I^2C interface to release SDA and return it to a high state. The I^2C hang-up reset function can be disabled by setting the DIS_I2C_TO register to1.

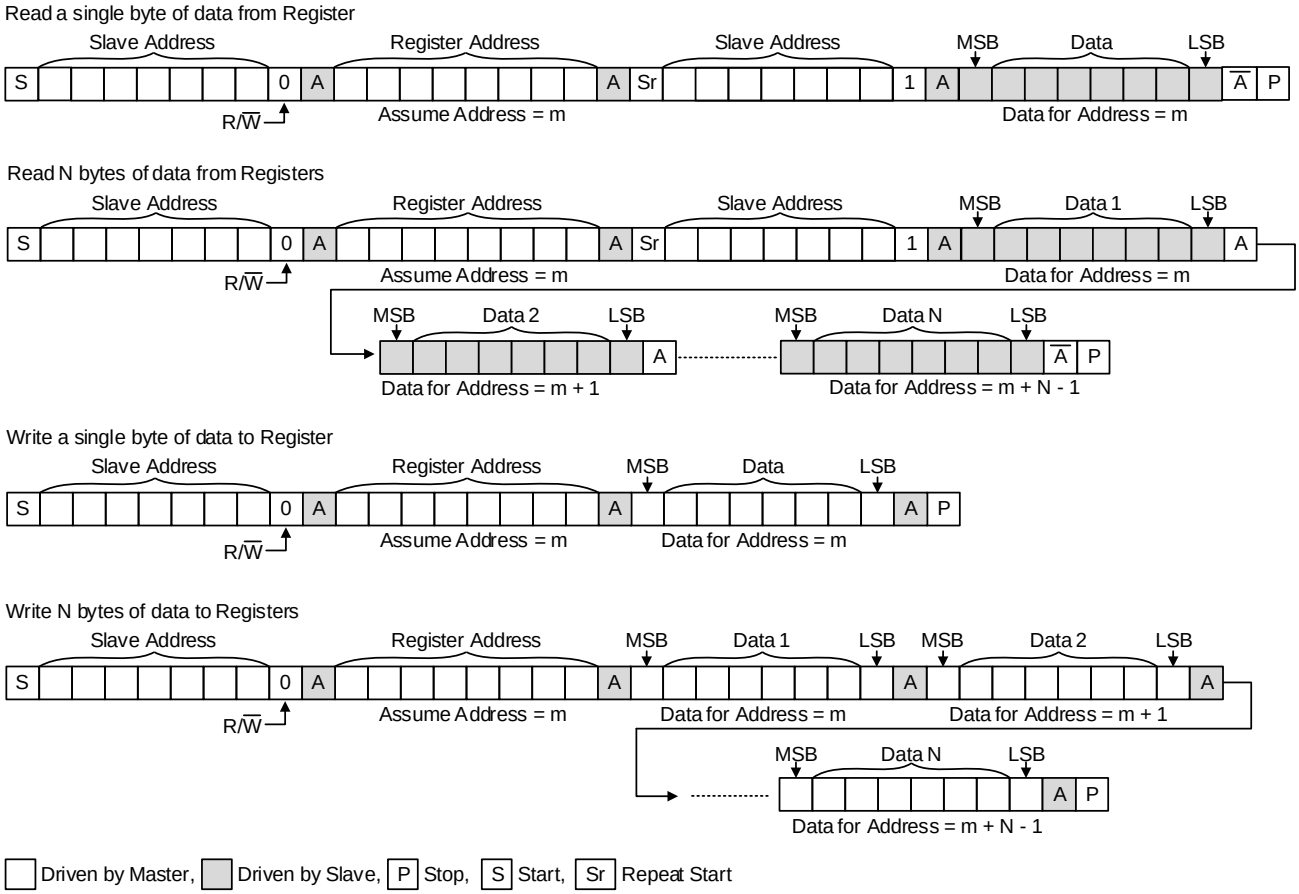


Figure 9. Read and Write Function

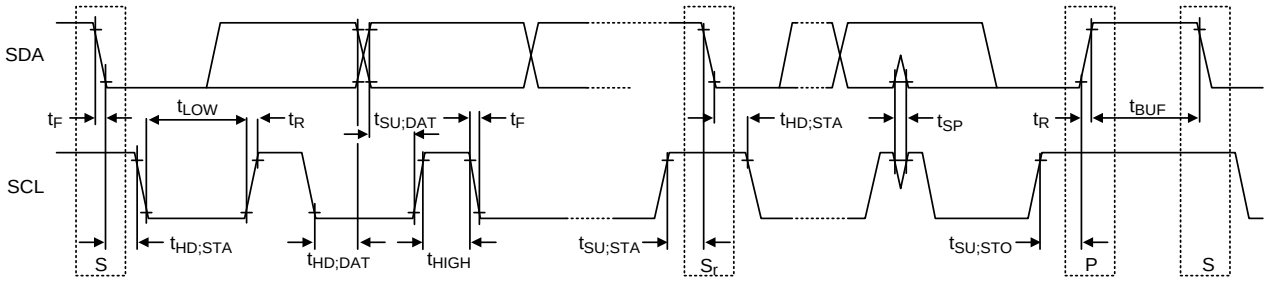


Figure 10. I^2C Waveform Information

17.29 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 130°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-29TL 4x4 (FC) package, the thermal resistance, θ_{JA}, is 45°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (130°C - 25°C) / (45°C/W) = 2.33W for a VQFN-29TL 4x4 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

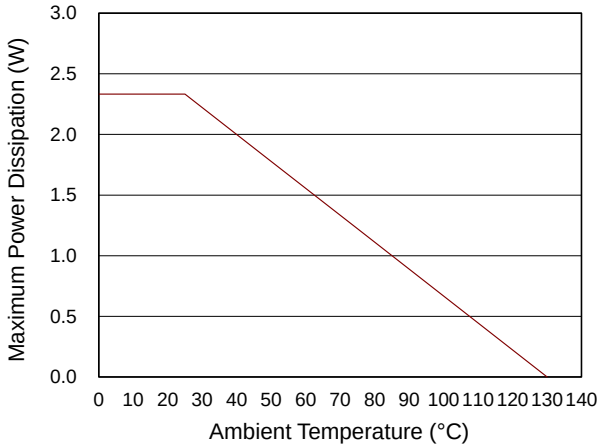


Figure 11. Derating Curve of Maximum Power Dissipation

17.30 Layout Considerations

The RT9492 layout guidelines are shown below, and several suggestions provided.

- The capacitors connected to the PMID pin need to be placed as close as possible to the IC.
- The inductor connected to the SW pin needs to not only route the trace as short as possible to reduce EMI but also ensure the copper area of the trace is wide enough for the operating current.
- The capacitors connected to the VSYS pin needs to be placed as close as possible to the IC. Three 10μF capacitors on the top layer, and two capacitors on bottom layer.
- The capacitors connected to the VBAT pin needs to be placed as close as possible to the IC.
- The 0.1μF capacitor, connected to VAC1/VAC2, PMID and VSYS must be placed close to the IC.
- The GND needs to connect on the top layer with PMID and SYS capacitors. Use ground vias to connect to the main ground as close as possible to the IC.

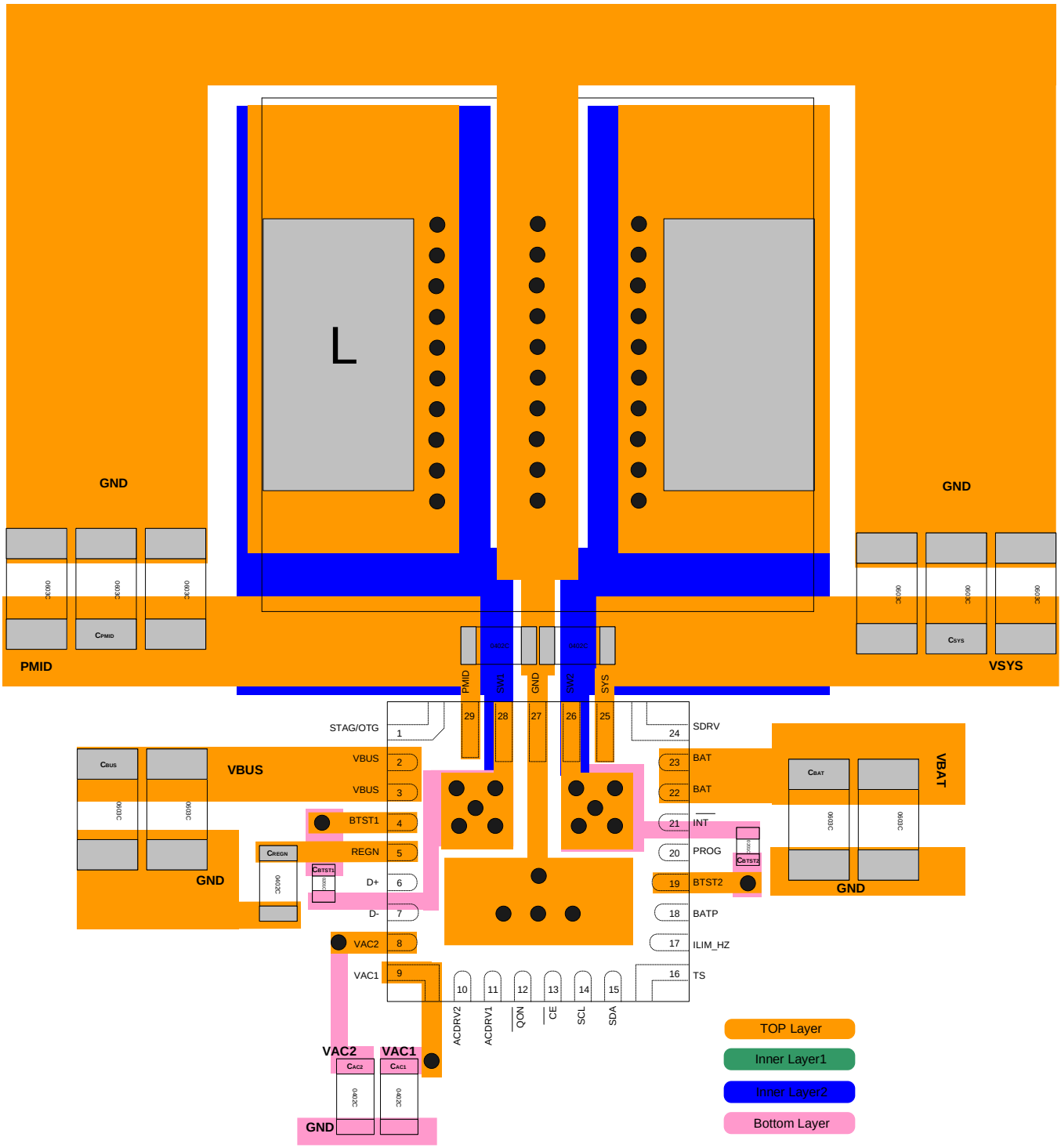


Figure 11. PCB Layout Guide

Note 9. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Functional Register Description

I^2C Slave Address: 1010011 (53H)

R: Read only

R/W: Read and write

RWS: Read and write, also automatically set by particular condition

RWC: Read and write, also automatically cleared by particular condition

RWSC: Read and write, also automatically set/cleared by particular condition

Register Address: 0x00, Register Name: SYS_MIN REGU

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	RESERVED	00	N	N	R	Reserved
5:0	VSYSMIN	NA	N	Y	RWSC	During POR, the device reads the resistance on the PROG pin, identifies the default battery cell count and determines the default VSYSMIN. Changing REG0x0A[7:6] also changes default values. 000000: 2.5V 000001: 2.75V … 000100: 3.5V ... 010010: 7V (2s) … 011010: 9V (3s) … 100110: 12V (4s) … 110101: 15.75V 110110 to 111111: 16V

Register Address: 0x01, Register Name: VCHG_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:11	RESERVED	00000	N	N	R	Reserved
10:0	VBAT_REG	NA	N	Y	RWSC	During POR, the device reads the resistance on the PROG pin, identifies the default battery cell count and determines the default power-on battery voltage. Changing REG0x0A[7:6] also changes default values. 00111110100: 5V … 01101001000: 8.4V (2s) … 10011101100: 12.6V (3s) … 11010010000: 16.8V (4s) … 11101010111: 18.79V 11101011000 to 11111111111: 18.8V

Register Address: 0x03, Register Name: ICHG_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:9	RESERVED	0000000	N	N	R	Reserved
8:0	ICHG_CTRL	NA	Y	Y	RWSC	During POR, the device reads the resistance on the PROG pin, identifies the default battery cell count and determines the default power-on battery charging current. Changing REG0x0A[7:6] also changes default values. 0000000000 to 0000001110: Reserved 000001111: 0.15A … 001100100: 1A (3s, 4s) … 011001000: 2A (2s) … 111110011: 4.99A 111110100 to 111111111: 5A

Register Address: 0x05, Register Name: MIVR_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	VMIVR	00100100	N	N	RWS	MIVR is set to the value based on the VBUS measurement when the adapter plugs in and AUTO_MIVR = 1 00000000 to 00100100: 3.6V (default) 00100101: 3.7V … 01101010: 10.6V … 11011011: 21.9V 11011100 to 11111111: 22V

Register Address: 0x06, Register Name: AICR_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:9	RESERVED	0000000	N	N	R	Reserved
8:0	IAICR	10010 1100	N	Y	RWSC	Based on D+/D- detection results, if AUTO_AICR = 1 000000000 to 000001010: 100mA 000001011: 110mA … 000110010: 500mA … 100101100: 3000mA (default) … 101001010 to 111111111: 3300mA

Register Address: 0x08, Register Name: PRE_CHG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	VPRE_CHG	11	N	Y	R/W	Pre-charge voltage threshold from 00: 15%*VBAT_REG 01: 62%*VBAT_REG 10: 66.5%*VBAT_REG 11: 71.5%*VBAT_REG (default)
5:0	IPRE_CHG	000011	Y	Y	R/W	Pre-charge current 000000 to 000010: Reserved 000011: 0.12A (default) … 110001: 1.96A 110010 to 111111: 2A

Register Address: 0x09, Register Name: EOC_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	RST_ALL	0	N	Y	RWC	All registers and logic reset bit. 0: No action (default) 1: Reset all registers and logic. Reset to 0 after registers and logic reset.
6	REG_RST	0	N	Y	RWC	Reset registers to default values and reset timer. 0: No action (default) 1: Reset register and safety timer Reset to 0 after registers reset.
5	Reserved	0	N	N	R	Reserved
4:0	IEOC	00101	Y	Y	R/W	End-of-charge current 00000 to 00010: Reserved 00011: 0.12A 00100: 0.16A 00101: 0.2A (default) … 11000: 0.96A 11001 to 11111: 1A

Register Address: 0x0A, Register Name: RECHG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	BATTERY_CELL	NA	N	N	R/W	After POR, the device reads the PROG pin resistance to determine the battery cell. 01: 2s 10: 3s 11: 4s This bit is only for 01, 10,11 settings.
5:4	TRECHG	10	Y	Y	R/W	Re-charge deglitch time 00: 64ms 01: 256ms 10: 1024ms (default) 11: 2048ms
3:0	VRECHG	0011	Y	Y	R/W	Re-charge voltage threshold 0000: 50mV 0001: 100mV 0010: 150mV 0011: 200mV (default) … 1110: 750mV 1111: 800mV

Register Address: 0x0B, Register Name: VOTG_REGU

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:11	RESERVED	00000	N	N	R	Reserved
10:0	VOTG	0001101 1100	Y	Y	R/W	OTG voltage regulation 00000000000: 2.8V 00000000001: 2.81V … 00011011100: 5V (default) … 11101111111: 21.99V 11110000000 to 11111111111: 22V

Register Address: 0x0D, Register Name: IOTG_REGU

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	PRECHG_ TMR	0	Y	Y	R/W	Pre-charge safety timer 0: 2hrs (Default) 1: 0.5hrs
6:0	IOTG	1001011	Y	Y	R/W	OTG current limit 0000000 to 0000011: 0.12A 0000100: 0.16A … 1001011: 3A (default) … 1010010: 3.28A 1010011 to 1111111: 3.32A

Register Address: 0x0E, Register Name: SAFETY_TMR_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	BG_CHG_TMR	00	Y	Y	R/W	EOC back-ground charge safety timer 00: Disabled (default) 01: 15 mins 10: 30 mins 11: 45 mins
5	EN_TRICHG_TMR	1	Y	Y	R/W	Trickle charge safety timer enable 0: Disabled 1: Enabled (default)
4	EN_PRECHG_TMR	1	Y	Y	R/W	Pre-charge safety timer enable 0: Disabled 1: Enabled (default)
3	EN_FASTCHG_TMR	1	Y	Y	R/W	Fast-charge safety timer enable 0: Disabled 1: Enabled (default)
2:1	FASTCHG_TMR	10	Y	Y	R/W	Fast-charge safety timer 00: 5hrs 01: 8hrs 10: 12hrs (default) 11: 24hrs
0	TMR2X_EN	1	Y	Y	R/W	The charge safety timer will be double during MIVR, AICR, thermal regulation, and JEITA reduce ICHG. 0: Disable 2x extended charge safety timer 1: Enable 2x extended charge safety timer (default)

Register Address: 0x0F, Register Name: CHG_CTRL 0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	EN_AUTO_ IBATDIS	1	N	Y	R/W	Enable the battery discharging during the battery OVP fault. 0: No action when VBAT during VBAT_OVP 1: Apply a discharging resistance on VBAT during VBAT_OVP (default)
6	FORCE_ IBATDIS	0	N	Y	R/W	Force a battery discharging resistance 0: No action (default) 1: Force a discharging resistance on BAT
5	EN_CHG	1	Y	Y	R/W	Charger Enable 0: Disable charge 1: Enable charge (default)
4	EN_AICC	0	N	Y	R/W	0: Disable AICC function (default) 1: Enable AICC function
3	FORCE_AICC	0	Y	Y	RWSC	0: No action (default) 1: Force AICC function Reset to 0 after AICC is done
2	EN_HZ	0	N	Y	RWSC	Enable HZ mode 0: Disable (default) 1: Enable Reset to 0 when VAC/VBUS presents
1	EN_TE	1	Y	Y	R/W	Charge current termination 0: Disable 1: Enable (default)
0	RESERVED	0	N	N	R	Reserved

Register Address: 0x10, Register Name: CHG_CTRL 1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	RESERVED	00	N	N	R	Reserved
5:4	VAC_OVP	00	N	Y	R/W	VAC1/VAC2_OVP thresholds 00: 26V (default) 01: 18V 10: 12V 11: 7V
3	WD_RST	0	Y	Y	RWSC	Watchdog timer reset 0: No action (default) 1: Reset Reset to 0 after WDT resets
2:0	WATCHDOG	101	N	Y	R/W	Watchdog timer setting 000: Disable 001: 0.5s 010: 1s 011: 2s 100: 20s 101: 40s (default) 110: 80s 111: 160s

Register Address: 0x11, Register Name: CHG_CTRL 2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	FORCE_ DPDM_DET_ EN	0	Y	Y	RWSC	Force D+/D- detection 0: No action (default) 1: Force D+D- detection Reset to 0 while D+D- detection is done
6	BC12_EN	1	Y	Y	R/W	0: Disable BC1.2 detection 1: Enable BC1.2 detection (Default)
5:4	RESERVED	00	N	N	R	Reserved
3	DIS_EOC_ FCCM	1	N	Y	R/W	Enable FCCM for EOC during TD_EOC 0: Enable EOC FCCM 1: Disable EOC FCCM (default)
2:1	SDRV_CTRL	00	N	Y	RWSC	SHIP FET gate driver control mode 00: IDLE (default) 01: Shutdown Mode 10: Ship Mode 11: System Power Reset Reset to 00 when SHIP_FET_PRESENT = 0 or exit shutdown mode or exit ship mode or finish system power reset. Set to ship mode when SHIP_FET_PRESENT = 1 and trigger IBAT_OCP or VSYS_SHORT
0	SDRV_DLY	0	N	Y	R/W	SHIP FET turns off delay time when SDRV_CTRL is not equal to 00. 0: Add 10s delay time (default) 1: Do NOT add 10s delay time

Register Address: 0x12, Register Name: CHG_CTRL 3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	DIS_ACDRV_EN	0	N	N	RWSC	Force both EN_ACDRV1 = 0 and EN_ACDRV2 = 0 0: Not Force (default) 1: Force EN_ACDRV1 = 0 and EN_ACDRV2 = 0 Reset to 0 when VAC1/VAC2 is not present and EN_OTG is disabled.
6	EN_OTG	0	Y	Y	RWSC	OTG mode control 0: Disable OTG (default) 1: Enable OTG (Reset to 0 when OTG_UVP, OTG_LBP occurs. Set to 1 when SEAMLESS is operating)
5:4	RESERVED	00	N	N	R	Reserved
3	QON_EXIT_SHIP_DLY	0	N	Y	R/W	The QON pin pull-low time to exit ship mode 0: 1s (default) 1: 15ms
2	DIS_LDO	0	Y	Y	RWC	Disable BATFET LDO mode in SYSMIN 0: Enable BATFET regulation for SYSMIN (default) 1: Disable BATFET regulation (Reset to 0 when power path is turned off or there is no input detected on VBUS.)
1	DIS_OTG_OOA	0	Y	Y	R/W	Disable OOA in OTG mode 0: Enable OOA function in OTG mode (default) 1: Disable OOA function in OTG mode
0	DIS_CHG_OOA	0	N	Y	R/W	Disable OOA in charge mode 0: Enable OOA function in charge mode (default) 1: Disable OOA function in charge mode

Register Address: 0x13, Register Name: CHG_CTRL 4

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	EN_ACDRV2	0	N	N	RWSC	External ACFET2 gate driver 0: Turn off (default) 1: Turn on (Set to 1 when VAC2 is present, reset to 0 after VAC2 is not present or lock at 0 if there is no external ACFET2.)
6	EN_ACDRV1	0	N	N	RWSC	External ACFET1 gate driver 0: Turn off (default) 1: Turn on (Set to 1 when VAC1 is present, reset to 0 after VAC1 is not present or lock at 0 if there is no external ACFET1.)
5	PWM_FREQ	NA	N	N	RWSC	Switching frequency selection. After POR, the default value is based on the PROG pin. 0: 1.5MHz 1: 750kHz
4	DIS_STAT	0	Y	Y	R/W	The STAT pin output 0: Enable STAT pin output (default) 1: Disable STAT pin output
3	DIS_VSYS_UVP_HICCUP	0	N	Y	R/W	VSYS_UVP hiccup protection 0: Enable VSYS_UVP hiccup protection (default) 1: Disable VSYS_UVP hiccup, converter continues switching
2	DIS_VOTG_UVP_HICCUP	0	N	Y	R/W	OTG mode VOTG UVP hiccup protection 0: Enable VOTG_UVP hiccup protection (default) 1: Disable VOTG_UVP hiccup, converter continues switching
1	FORCE_MIVR_DET	0	N	Y	RWC	Force MIVR detection 0: No action (default) 1: Force the converter stops switching, and ADC VBUS for MIVR detection (Reset to 0 after forced MIVR detection process has been completed.)
0	EN_IBUS_OCP	1	N	Y	R/W	Enable IBUS_OCP 0: Disable 1: Enable (default)

Register Address: 0x14, Register Name: CHG_CTRL 5

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	SHIP_FET_ PRESENT	0	N	N	R/W	The user has to set this bit based on whether a SHIP FET is used or not. 0: No external SHIP FET (default) 1: Use external SHIP FET
6:5	RESERVED	00	N	N	R	Reserved
4:3	IBAT_REG	10	Y	Y	RWC	Battery discharging current regulation during OTG 00: 3A 01: 4A 10: 5A (default) 11: Disable (Back to 10, when THREG_STAT trigger and IBAT_REG = 11)
2	EN_AICR	1	Y	Y	RWC	The AICR Loop control 0: Disable 1: Enable (default) (Reset to 1, when THREG_STAT triggers)
1	ILIM_HZ_EN	1	N	Y	R/W	The ILIM_HZ pin current limit setting 0: Disable 1: Enable (default)
0	EN_IBAT_ OCP	0	Y	Y	RWSC	Enable the battery discharging current OCP 0: Disable (default) 1: Enable (Reset to 0 when SHIP_FET_PRESENT = 0)

Register Address: 0x16, Register Name: THREG_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	THREG	11	Y	Y	R/W	Thermal regulation threshold 00: 60°C 01: 80°C 10: 100°C 11: 120°C (default)
5:4	TOTP	00	Y	Y	R/W	Over thermal protection thresholds 00: 150°C (default) 01: 130°C 10: 120°C 11: 85°C
3	VBUS_PD_EN	0	N	Y	R/W	VBUS pull-down resistor 0: Disable (default) 1: Enable
2	VAC1_PD_EN	0	N	Y	R/W	VAC1 pull-down resistor 0: Disable (default) 1: Enable
1	VAC2_PD_EN	0	N	Y	R/W	VAC2 pull-down resistor 0: Disable (default) 1: Enable
0	THREG_HYS	0	N	Y	R/W	Thermal regulation falling hysteresis 0: 10°C (default) 1: 20°C

Register Address: 0x17, Register Name: JEITA_CTRL 0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	JEITA_VSET	011	Y	Y	R/W	JEITA WARM charge voltage setting 000: Stop charging 001: Set VBAT_REG to VBAT_REG-800mV 010: Set VBAT_REG to VBAT_REG-600mV 011: Set VBAT_REG to VBAT_REG-400mV (default) 100: Set VBAT_REG to VBAT_REG-300mV 101: Set VBAT_REG to VBAT_REG-200mV 110: Set VBAT_REG to VBAT_REG-100mV 111: VBAT_REG = Register setting
4:3	JEITA_ISET_WARM	11	Y	Y	R/W	JEITA WARM charge current setting 00: Stop charging 01: Set ICHG to 25% * ICHG 10: Set ICHG to 50% * ICHG 11: ICHG = Register setting (default)
2:1	JEITA_ISET_COOL	01	Y	Y	R/W	JEITA COOL charge current setting 00: Stop charging 01: Set ICHG to 25% * ICHG (default) 10: Set ICHG to 50% * ICHG 11: ICHG = Register setting
0	RESERVED	0	N	N	R	Reserved

Register Address: 0x18, Register Name: JEITA_CTRL 1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	TS_COOL	01	Y	Y	R/W	TS COOL temperature threshold 00: 71.1% (5°C) 01: 68.4% (10°C) (default) 10: 65.5% (15°C) 11: 62.4% (20°C)
5:4	TS_WARM	01	Y	Y	R/W	TS WARM temperature threshold 00: 48.4% (40°C) 01: 44.8% (45°C) (default) 10: 41.2% (50°C) 11: 37.7% (55°C)
3:2	OTG_HOT	01	Y	Y	R/W	OTG mode TS HOT temperature threshold 00: 37.7% (55°C) 01: 34.4% (60°C) (default) 10: 31.3% (65°C) 11: Disable
1	OTG_COLD	0	Y	Y	R/W	OTG mode TS COLD temperature threshold 0: 80% (–10°C) (default) 1: 77.1% (–20°C)
0	JEITA_DIS	0	Y	Y	R/W	Disable JEITA function 0: NOT disable (default) 1: Disable

Register Address: 0x19, Register Name: AICC_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:9	RESERVED	0000000	N	N	R	Reserved
8:0	IAICC	000000000	N	N	R	AICR current limit by average input current control or the ILIM_HZ pin 000000000: 0mA (default) 000001010: 100mA 000001011: 110mA … 000110010: 500mA … 100101100: 3000mA … 101001010: 3300mA

Register Address: 0x1B, Register Name: CHG_STATUS 0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	AICR_STAT	0	N	N	R	AICR status (charge mode) or OTG_CC status (OTG mode) 0: Normal (default) 1: In AICR/OTG_CC
6	MIVR_STAT	0	N	N	R	MIVR status (charge mode) or OTG_CV status (OTG mode) 0: Normal (default) 1: In MIVR/OTG_CV
5	WDT_STAT	0	N	N	R	Watchdog timer status 0: Normal (default) 1: Watchdog timeout
4	RESERVED	0	N	N	R	Reserved
3	VBUS_GD_RDY_STAT	0	N	N	R	VBUS good ready for charge status 0: VBUS NOT good ready for charge status (default) 1: VBUS good ready for charge status (Notice: after bad adapter detection, EN_HZ = 0, VBUS_OVP = 0)
2	VAC2_PG_STAT	0	N	N	R	VAC2 power-good status 0: VAC2 NOT power-good (default) 1: VAC2 power-good (Notice: above VAC_UVLO threshold, VAC2_OVP = 0)
1	VAC1_PG_STAT	0	N	N	R	VAC1 power-good status 0: VAC1 NOT power-good (default) 1: VAC1 power-good (Notice: above VAC_UVLO threshold, VAC1_OVP = 0)
0	VBUS_PG_STAT	0	N	N	R	VBUS power-good status 0: VBUS NOT power-good (default) 1: VBUS power-good (Notice: above VBUS_UVLO threshold, EN_HZ = 0, VBUS_OVP = 0)

Register Address: 0x1C, Register Name: CHG_STATUS 1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	CHG_STAT	000	N	N	R	Charge status bits 000: Not charging (default) 001: Trickle charge 010: Pre-charge 011: Fast charge (CC mode) 100: Fast charge (CV mode) 101: IEOC (EOC and TE = 0) 110: Back-Ground charging (EOC and TE = 1 and before BATFET turns off) 111: Charge done (EOC and TE = 1 and BATFET turns off)
4:1	VBUS_STAT	0000	N	N	R	VBUS status bits 0000: No input or Input NOT from BC12_EN_CHANNEL (Default) 0001: USB SDP (0.5A) 0010: USB CDP (1.5A) 0011: USB DCP (3.25A) 0100: Adjustable DCP 0101: NSDP/Unknown (3.25A) 0110: Special Adapter (1A/2A/2.1A/2.4A) 0111: In OTG mode 1000: Not verify adapter/Bad adapter 1001: Reserved 1010: Reserved 1011: Device directly powered from VBUS 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
0	BC12_DONE_STAT	0	N	N	R	BC1.2 status bit 0: BC1.2 NOT complete (default) 1: BC1.2 done

Register Address: 0x1D, Register Name: CHG_STATUS 2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	AICC_STAT	00	N	N	R	Average input current control status 00: AICC disabled (default) 01: AICC optimization in progress 10: Maximum input current detected 11: Reserved
5	CDP_PD_STAT	0	N	N	R	CDP primary detection status 0: CDP primary detection does not start (Default) 1: CDP primary detection started (Notice: This bit will be updated when HOST mode is changed.)
4	CDP_DONE_STAT	0	N	N	R	CDP flow status 0: No CDP flow (default) 1: CDP flow done. (Notice: This bit will be updated when HOST mode is changed.)
3	RESERVED	0	N	N	R	Reserved
2	THREG_STAT	0	N	N	R	Thermal regulation status 0: Normal (default) 1: In thermal regulation
1	DPDM_STAT	0	N	N	R	D+/D- detection status bits 0: The D+/D- detection is NOT started yet, or the detection is done (default) 1: The D+/D- detection is ongoing
0	VBAT_PG_STAT	0	N	N	R	VBAT power-good status 0: VBAT NOT power-good (default) 1: VBAT power-good (Notice: VBAT > VBAT_UVLO)

Register Address: 0x1E, Register Name: CHG_STATUS 3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ACRB2_STAT	0	N	N	R	The ACFET2-RBFET2 status 0: ACFET2-RBFET2 is NOT placed (default) 1: ACFET2-RBFET2 is placed
6	ACRB1_STAT	0	N	N	R	The ACFET1-RBFET1 status 0: ACFET1-RBFET1 is NOT placed (default) 1: ACFET1-RBFET1 is placed
5	ADC_DONE_STAT	0	N	N	R	ADC status (in one-shot mode only) 0: ADC is NOT completed (default) 1: ADC is done
4	VSYSMIN_STAT	0	N	N	R	VSYS_MIN regulation status 0: Not in SYS_MIN regulation (VBAT > VSYS_MIN) (default) 1: In SYS_MIN regulation (VBAT < VSYS_MIN)
3	FASTCHG_TMR_STAT	0	N	N	R	Fast charge safety timer status 0: Normal (default) 1: Fast charge safety timer timeout
2	TRICHG_TMR_STAT	0	N	N	R	Trickle charge safety timer status 0: Normal (default) 1: Trickle charge safety timer timeout
1	PRECHG_TMR_STAT	0	N	N	R	Pre-charge safety timer status 0: Normal (default) 1: Pre-charge safety timer timeout
0	RESERVED	0	N	N	R	Reserved

Register Address: 0x1F, Register Name: CHG_STATUS 4

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	RESERVED	0000	N	N	R	Reserved
3	JEITA_COLD_STAT	0	N	N	R	The TS temperature is in the cold range 0: NOT in cold range (default) 1: In cold range
2	JEITA_COOL_STAT	0	N	N	R	The TS temperature is in the cool range 0: NOT in cool range (default) 1: In cool range
1	JEITA_WARM_STAT	0	N	N	R	The TS temperature is in the warm range 0: NOT in warm range (default) 1: In warm range
0	JEITA_HOT_STAT	0	N	N	R	The TS temperature is in the hot range 0: NOT in hot range (default) 1: In hot range

Register Address: 0x20, Register Name: FAULT_STATUS 0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBAT_REG_STAT	0	N	N	R	IBAT regulation in OTG mode 0: Not in battery current regulation (default) 1: In battery current regulation
6	VBUS_OVP_STAT	0	N	N	R	VBUS overvoltage protection status 0: Not in VBUS OVP (default) 1: In VBUS OVP
5	VBAT_OVP_STAT	0	N	N	R	VBAT overvoltage protection status 0: Not in VBAT OVP (default) 1: In VBAT OVP
4:3	RESERVED	00	N	N	R	Reserved
2	CYC_OCP_STAT	0	N	N	R	Converter cycle-by-cycle overcurrent protection status 0: Not in cycle-by-cycle OCP (default) 1: In cycle-by-cycle OCP
1	VAC2_OVP_STAT	0	N	N	R	VAC2 overvoltage protection status 0: Not in VAC2 OVP (default) 1: In VAC2 OVP
0	VAC1_OVP_STAT	0	N	N	R	VAC1 overvoltage protection status 0: Not in VAC1 OVP (default) 1: In VAC1 OVP

Register Address: 0x21, Register Name: FAULT_STATUS 1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VSYS_UVP_STAT	0	N	N	R	VSYS undervoltage protection status 0: Not in VSYS UVP (default) 1: In VSYS UVP
6	VSYS_OVP_STAT	0	N	N	R	VSYS overvoltage protection status 0: Not in VSYS OVP (default) 1: In VSYS OVP
5	OTG_OVP_STAT	0	N	N	R	OTG overvoltage protection status 0: Not in OTG OVP (default) 1: In OTG OVP
4:3	RESERVED	00	N	N	R	Reserved
2	TOTP_STAT	0	N	N	R	IC over-temperature shutdown status 0: Not in OTP (default) 1: In OTP
1:0	RESERVED	00	N	N	R	Reserved

Register Address: 0x22, Register Name: CHG_IRQ_FLAG 0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	AICR_FLAG	0	N	N	R	AICR flag or OTG_CC flag 0: Normal (default) 1: Any change in AICR_STAT/OTG_CC_STAT, read to clear
6	MIVR_FLAG	0	N	N	R	MIVR flag or OTG_CV flag 0: Normal (default) 1: Any change in MIVR_STAT/OTG_CV_STAT, read to clear
5	WDT_FLAG	0	N	N	R	I^2C watchdog timer flag 0: Normal (default) 1: WDT_STAT rising, read to clear
4	BAD_ADAPTER_FLAG	0	N	N	R	Bad adapter detection flag 0: Normal (default) 1: Bad adapter detected, read to clear
3	VBUS_GD_RDY_FLAG	0	N	N	R	VBUS good ready for charge flag 0: Normal (default) 1: Any change in VBUS_GD_RDY_STAT even, read to clear
2	VAC2_PG_FLAG	0	N	N	R	VAC2 power-good flag 0: Normal (default) 1: Any change in VAC2_PG_STAT, read to clear
1	VAC1_PG_FLAG	0	N	N	R	VAC1 power-good flag 0: Normal (default) 1: Any change in VAC1_PG_STAT, read to clear
0	VBUS_PG_FLAG	0	N	N	R	VBUS power-good flag 0: Normal (default) 1: Any change in VBUS_PG_STAT, read to clear

Register Address: 0x23 Register Name: CHG_IRQ_FLAG 1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_FLAG	0	N	N	R	Charge status flag 0: Normal (default) 1: Any change in CHG_STAT, read to clear
6	AICC_FLAG	0	N	N	R	AICC status flag 0: Normal (default) 1:Any change in AICC_STAT, read to clear
5	RESERVED	0	N	N	R	Reserved
4	VBUS_FLAG	0	N	N	R	VBUS status flag 0: Normal (default) 1: Any change in VBUS_STAT, read to clear
3	RESERVED	0	N	N	R	Reserved
2	THREG_FLAG	0	N	N	R	IC thermal regulation flag 0: Normal (default) 1: THREG_STAT rising, read to clear
1	VBAT_PG_ FLAG	0	N	N	R	VBAT power-good flag 0: Normal (default) 1: Any change in VBAT_PG_STAT, read to clear
0	BC1.2_ DONE_FLAG	0	N	N	R	BC1.2 done flag 0: BC1.2 detection not ready (default) 1: BC12_DONE_STAT rising detection done, read to clear

Register Address: 0x24 Register Name: CHG_IRQ_FLAG 2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	RESERVED	0	N	N	R	Reserved
6	DPDM_DONE_FLAG	0	N	N	R	D+/D- detection done flag. 0: D+/D- detection is NOT started or still ongoing (default) 1: D+/D- detection is completed, read to clear
5	ADC_DONE_FLAG	0	N	N	R	ADC done flag (only in one-shot mode) 0: ADC NOT completed (default) 1: ADC done, read to clear
4	VSYSMIN_FLAG	0	N	N	R	VSYSMIN regulation flag 0: Normal (default) 1: Any change in VSYSMIN_STAT, read to clear
3	FASTCHG_TMR_FLAG	0	N	N	R	Fast charge timer timeout flag 0: Normal (Default) 1: FASTCHG_TMR_STAT rising, read to clear
2	TRICHG_TMR_FLAG	0	N	N	R	Trickle charge timer timeout flag 0: Normal (default) 1: TRICHG_TMR_STAT rising, read to clear
1	PRECHG_TMR_FLAG	0	N	N	R	Pre-charge timer timeout flag 0: Normal (default) 1: PRECHG_TMR_STAT rising, read to clear
0	BG_TMR_FLAG	0	N	N	R	Back-ground charge timer flag 0: Normal (default) 1: Back-ground charge timer timeout rising, read to clear

Register Address: 0x25 Register Name: CHG_IRQ_FLAG 3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	RESERVED	000	N	N	R	Reserved
4	OTG_LBP_FLAG	0	N	N	R	The VBAT is under OTG_LBP 0: Normal (default) 1: VBAT<VOTG_LBP is detected, read to clear
3	JEITA_COLD_FLAG	0	N	N	R	JEITA_COLD flag 0: Normal (default) 1: JEITA_COLD_STAT rising, read to clear
2	JEITA_COOL_FLAG	0	N	N	R	JEITA_COOL flag 0: Normal (default) 1: JEITA_COOL_STAT rising, read to clear
1	JEITA_WARM_FLAG	0	N	N	R	JEITA_COOL flag 0: Normal (default) 1: JEITA_WARM_STAT rising, read to clear
0	JEITA_HOT_FLAG	0	N	N	R	JEITA_HOT flag 0: Normal (default) 1: JEITA_HOT_STAT rising, read to clear

Register Address: 0x26 Register Name: CHG_IRQ_FLAG 4

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBAT_REG_FLAG	0	N	N	R	When in OTG, IBAT regulation flag 0: Normal (default) 1: Any change in IBAT_STAT, read to clear
6	VBUS_OVP_FLAG	0	N	N	R	VBUS overvoltage protection flag 0: Normal (default) 1: VBUS_OVP_STAT rising, read to clear
5	VBAT_OVP_FLAG	0	N	N	R	VBAT overvoltage protection flag 0: Normal (default) 1: VBAT_OVP_STAT rising, read to clear
4	IBUS_OCP_FLAG	0	N	N	R	IBUS overcurrent protection flag 0: Normal (default) 1: IBUS > IBUS_OCP occurs, read to clear
3	IBAT_OCP_FLAG	0	N	N	R	IBAT overcurrent protection flag 0: Normal (default) 1: IBAT > IBAT_OCP occurs, read to clear
2	CYC_OCP_FLAG	0	N	N	R	Cycle-by-cycle overcurrent protection flag 0: Normal (default) 1: CYC_OCP_STAT rising, read to clear
1	VAC2_OVP_FLAG	0	N	N	R	VAC2 overvoltage protection flag 0: Normal (default) 1: VAC2_OVP_STAT rising, read to clear
0	VAC1_OVP_FLAG	0	N	N	R	VAC1 overvoltage protection flag 0: Normal (default) 1: VAC1_OVP_STAT rising, read to clear

Register Address: 0x27 Register Name: CHG_IRQ_FLAG 5

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VSYS_UVP_FLAG	0	N	N	R	VSYS undervoltage protection flag 0: Normal (default) 1: VSYS_UVP_STAT rising, read to clear
6	VSYS_OVP_FLAG	0	N	N	R	VSYS overvoltage flag 0: Normal (default) 1: VSYS_OVP_STAT rising, read to clear
5	OTG_OVP_FLAG	0	N	N	R	OTG overvoltage flag 0: Normal (default) 1: OTG_OVP_STAT rising, read to clear
4	OTG_UVP_FLAG	0	N	N	R	OTG undervoltage flag 0: Normal (default) 1: OTG_UVP_STAT rising, read to clear
3	RESERVED	0	N	N	R	Reserved
2	TOTP_FLAG	0	N	N	R	IC over-temperature protection flag 0: Normal (default) 1: TOTP_STAT rising, read to clear
1:0	RESERVED	00	N	N	R	Reserved

Register Address: 0x28 Register Name: CHG_IRQ_MASK 0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	AICR_MASK	0	N	Y	R/W	0: Not mask IRQ of AICR_FLAG (default) 1: Mask IRQ of AICR_FLAG
6	MIVR_MASK	0	N	Y	R/W	0: Not mask IRQ of MIVR_FLAG (default) 1: Mask IRQ of MIVR_FLAG
5	WDT_MASK	0	N	Y	R/W	0: Not mask IRQ of WDT_FLAG (default) 1: Mask IRQ of WDT_FLAG
4	BAD_ADAPTER_MASK	0	N	Y	R/W	0: Not mask IRQ of BAD_ADAPTER_FLAG (default) 1: Mask IRQ of BAD_ADAPTER_FLAG
3	VBUS_GD_RDY _MASK	0	N	Y	R/W	0: Not mask IRQ of VBUS_GD_RDY_FLAG (default) 1: Mask IRQ of VBUS_GD_RDY_FLAG
2	VAC2_PG_MASK	0	N	Y	R/W	0: Not mask IRQ of VAC2_PG_FLAG (default) 1: Mask IRQ of VAC2_PG_FLAG
1	VAC1_PG_MASK	0	N	Y	R/W	0: Not mask IRQ of VAC1_PG_FLAG (default) 1: Mask IRQ of VAC1_PG_FLAG
0	VBUS_PG_MASK	0	N	Y	R/W	0: Not mask IRQ of VBUS_PG_FLAG (default) 1: Mask IRQ of VBUS_PG_FLAG

Register Address: 0x29 Register Name: CHG_IRQ_MASK 1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_MASK	0	N	Y	R/W	0: Not mask IRQ of CHG_FLAG (default) 1: Mask IRQ of CHG_FLAG
6	AICC_MASK	0	N	Y	R/W	0: Not mask IRQ of AICC_FLAG (default) 1: Mask IRQ of AICC_FLAG
5	RESERVED	0	N	N	R	Reserved
4	VBUS_MASK	0	N	Y	R/W	0: Not mask IRQ of VBUS_FLAG (default) 1: Mask IRQ of VBUS_FLAG
3	RESERVED	0	N	N	R	Reserved
2	THREG_MASK	0	N	Y	R/W	0: Not mask IRQ of THREG_FLAG (default) 1: Mask IRQ of THREG_FLAG
1	VBAT_PG_MASK	0	N	Y	R/W	0: Not mask IRQ of VBAT_PG_FLAG (default) 1: Mask IRQ of VBAT_PG_FLAG
0	BC1.2_DONE_MASK	0	N	Y	R/W	0: Not mask IRQ of BC1.2_DONE_FLAG (default) 1: Mask IRQ of BC1.2_DONE_FLAG

Register Address: 0x2A Register Name: CHG_IRQ_MASK 2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	RESERVED	0	N	N	R	Reserved
6	DPDM_DONE _MASK	0	N	Y	R/W	0: Not mask IRQ of DPDM_DONE_FLAG (default) 1: Mask IRQ of DPDM_DONE_FLAG
5	ADC_DONE_ MASK	0	N	Y	R/W	0: Not mask IRQ of ADC_DONE (default) 1: Mask IRQ of ADC_DONEG
4	VSYSMIN_ MASK	0	N	Y	R/W	0: Not mask IRQ of VSYSMIN_FLAG (default) 1: Mask IRQ of VSYSMIN_FLAG
3	FASTCHG_ TMR_MASK	0	N	Y	R/W	0: Not mask IRQ of FASTCHG_TMR_FLAG (default) 1: Mask IRQ of FASTCHG_TMR_FLAG
2	TRICHG_TMR _MASK	0	N	Y	R/W	0: Not mask IRQ of TRICHG_TMR_FLAG (default) 1: Mask IRQ of TRICHG_TMR_FLAG
1	PRECHG_ TMR_MASK	0	N	Y	R/W	0: Not mask IRQ of PRECHG_TMR_FLAG (default) 1: Mask IRQ of PRECHG_TMR_FLAG
0	BG_TMR_ MASK	0	N	Y	R/W	0: Not mask IRQ of BG_TMR_FLAG (default) 1: Mask IRQ of BG_TMR_FLAG

Register Address: 0x2B Register Name: CHG_IRQ_MASK 3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	RESERVED	000	N	N	R	Reserved
4	OTG_LBP_ MASK	0	Y	Y	R/W	0: Not mask IRQ of OTG_LBP_FLAG (default) 1: Mask IRQ of OTG_LBP_FLAG
3	JEITA_COLD_ MASK	0	Y	Y	R/W	0: Not mask IRQ of JEITA_COLD_FLAG (default) 1: Mask IRQ of JEITA_COLD_FLAG
2	JEITA_COOL_ MASK	0	Y	Y	R/W	0: Not mask IRQ of JEITA_COOL_FLAG (default) 1: Mask IRQ of JEITA_COOL_FLAG
1	JEITA_WARM _MASK	0	Y	Y	R/W	0: Not mask IRQ of JEITA_WARM_FLAG (default) 1: Mask IRQ of JEITA_WARM_FLAG
0	JEITA_HOT_ MASK	0	Y	Y	R/W	0: Not mask IRQ of JEITA_HOT_FLAG (default) 1: Mask IRQ of JEITA_HOT_FLAG

Register Address: 0x2C Register Name: CHG_IRQ_MASK 4

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBAT_REG_MASK	0	N	Y	R/W	0: Not mask IRQ of IBAT_REG_FLAG (default) 1: Mask IRQ of IBAT_REG_FLAG
6	VBUS_OVP_MASK	0	N	Y	R/W	0: Not mask IRQ of VBUS_OVP_FLAG (default) 1: Mask IRQ of VBUS_OVP_FLAG
5	VBAT_OVP_MASK	0	N	Y	R/W	0: Not mask IRQ of VBAT_OVP_FLAG (default) 1: Mask IRQ of VBAT_OVP_FLAG
4	IBUS_OCP_MASK	0	N	Y	R/W	0: Not mask IRQ of IBUS_OCP_FLAG (default) 1: Mask IRQ of IBUS_OCP_FLAG
3	IBAT_OCP_MASK	0	N	Y	R/W	0: Not mask IRQ of IBAT_OCP_FLAG (default) 1: Mask IRQ of IBAT_OCP_FLAG
2	CYC_OCP_MASK	0	N	Y	R/W	0: Not mask IRQ of CYC_OCP_FLAG (default) 1: Mask IRQ of CYC_OCP_FLAG
1	VAC2_OVP_MASK	0	N	Y	R/W	0: Not mask IRQ of VAC2_OVP_FLAG (default) 1: Mask IRQ of VAC2_OVP_FLAG
0	VAC1_OVP_MASK	0	N	Y	R/W	0: Not mask IRQ of VAC1_OVP_FLAG (default) 1: Mask IRQ of VAC1_OVP_FLAG

Register Address: 0x2D Register Name: CHG_IRQ_MASK 5

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VSYS_UVP_MASK	0	N	Y	R/W	0: Not mask IRQ of VSYS_UVP_FLAG (default) 1: Mask IRQ of VSYS_UVP_FLAG
6	VSYS_OVP_MASK	0	N	Y	R/W	0: Not mask IRQ of VSYS_OVP_FLAG (default) 1: Mask IRQ of VSYS_OVP_FLAG
5	OTG_OVP_MASK	0	N	Y	R/W	0: Not mask IRQ of OTG_OVP_FLAG (default) 1: Mask IRQ of OTG_OVP_FLAG
4	OTG_UVP_MASK	0	N	Y	R/W	0: Not mask IRQ of OTG_UVP_FLAG (default) 1: Mask IRQ of OTG_UVP_FLAG
3	RESERVED	0	N	N	R	Reserved
2	TOTP_MASK	0	N	Y	R/W	0: Not mask IRQ of TOTP_FLAG (default) 1: Mask IRQ of TOTP_FLAG
1:0	RESERVED	00	N	N	R	Reserved

Register Address: 0x2E Register Name: ADC_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ADC_EN	0	Y	Y	R/W	ADC control 0: Disable (default) 1: Enable (Reset to 0, when one shot conversion finishes.)
6	ADC_CONV_CTRL	0	N	Y	R/W	ADC conversion control 0: Continuous conversion (default) 1: One shot conversion
5:0	RESERVED	000000	N	N	R	Reserved

Register Address: 0x2F Register Name: ADC_CNANNEL 0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBUS_ADC_DIS	0	N	Y	R/W	IBUS ADC control 0: Enable (default) 1: Disable
6	IBAT_ADC_DIS	0	N	Y	R/W	IBAT ADC control 0: Enable (default) 1: Disable
5	VBUS_ADC_DIS	0	N	Y	R/W	VBUS ADC control 0: Enable (default) 1: Disable
4	VBAT_ADC_DIS	0	N	Y	R/W	VBAT ADC control 0: Enable (default) 1: Disable
3	VSYS_ADC_DIS	0	N	Y	R/W	VSYS ADC control 0: Enable (default) 1: Disable
2	TS_ADC_DIS	0	N	Y	R/W	TS ADC control 0: Enable (default) 1: Disable
1	TDIE_ADC_DIS	0	N	Y	R/W	TDIE ADC control 0: Enable (default) 1: Disable
0	RESERVED	1	Y	Y	R/W	Reserved

Register Address: 0x30 Register Name: ADC_CNANNEL 1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	DP_ADC_DIS	0	N	Y	R/W	D+ ADC control 0: Enable (default) 1: Disable
6	DM_ADC_DIS	0	N	Y	R/W	D- ADC control 0: Enable (default) 1: Disable
5	VAC2_ADC_DIS	0	N	Y	R/W	VAC2 ADC control 0: Enable (default) 1: Disable
4	VAC1_ADC_DIS	0	N	Y	R/W	VAC1 ADC control 0: Enable (default) 1: Disable
3:0	RESERVED	0000	N	N	R	Reserved

Register Address: 0x31 Register Name: IBUS_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	IBUS_ADC	0	N	N	R	IBUS ADC reading, LSB: 1mA Reported in 2's complement for discharge value. IBUS ADC reports charge value and discharge value. (Notice: Charge: VBUS to PMID; Discharge: PMID to VBUS)

Register Address: 0x33 Register Name: IBAT_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	IBAT_ADC	0	N	N	R	IBAT ADC reading, LSB: 1mA Reported in 2's complement for discharge value. IBAT ADC reports charge value and discharge value. (Notice: Charge: VSYS to VBAT; Discharge: VBAT to VSYS)

Register Address: 0x35 Register Name: VBUS_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	VBUS_ADC	0	N	N	R	VBUS ADC reading, LSB: 1mV

Register Address: 0x37 Register Name: VAC1_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	VAC1_ADC	0	N	N	R	VAC1 ADC reading, LSB: 1mV

Register Address: 0x39 Register Name: VAC2_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	VAC2_ADC	0	N	N	R	VAC2 ADC reading, LSB: 1mV

Register Address: 0x3B Register Name: VBAT_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	VBAT_ADC	0	N	N	R	VBAT ADC reading, LSB: 1mV

Register Address: 0x3D Register Name: VSYS_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	VSYS_ADC	0	N	N	R	VSYS ADC reading, LSB: 1mV

Register Address: 0x3F Register Name: TS_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	TS_ADC	0	N	N	R	TS ADC reading. LSB: 0.0963%

Register Address: 0x41 Register Name: TDIE_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	TDIE_ADC	0	N	N	R	TDIE ADC reading, LSB: 1°C Reported in 2's complement for negative value.

Register Address: 0x43 Register Name: DP_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	DP_ADC	0	N	N	R	D+ ADC reading, LSB: 1mV

Register Address: 0x45 Register Name: DM_ADC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
15:0	DM_ADC	0	N	N	R	D- ADC reading, LSB: 1mV

Register Address: 0x47 Register Name: DPDM_MANU_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	DP_CTRL	000	N	N	R/W	D+ manual control 000: HIZ (default) 001: 0 010: 0.6V 011: 1.2V 100: 2.0V 101: 2.7V 110: 3.3V 111: Reserved
4:2	DM_CTRL	000	N	N	R/W	D- manual control 000: HIZ (default) 001: 0 010: 0.6V 011: 1.2V 100: 2.0V 101: 2.7V 110: 3.3V 111: Reserved
1:0	RESERVED	00	N	N	R	Reserved

Register Address: 0x48 Register Name: DEVICE_INFO

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	RESERVED	0	N	N	R	Reserved
6:3	DEVICE_ID	1110	N	N	R	1110: RT9492
2:0	RESERVED	000	N	N	R	Reserved

Register Address: 0x49 Register Name: PUMP_EXP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	PE_EN	0	Y	Y	RWSC	0: Disable (default) 1: MTK Pump Express process enable (Reset to 0 when PE is done or there is no VBUS)
6	PE_SEL	0	Y	Y	R/W	0: PE 1.0 process select (default) 1: PE 2.0 process select
5	PE10_INC	0	Y	Y	R/W	0: PE 1.0 voltage down (default) 1: PE 1.0 voltage up
4:0	PE20_CODE	00000	Y	Y	R/W	MTK PE 2.0 voltage request setting 00000: 5.5V (default) 00001: 6V … 11101: 20V 11110: Adapter healthy self-testing 11111: Disable cable drop compensation

Register Address: 0x4A Register Name: ADD_CTRL 0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	DIS_I2C_TO	0	Y	Y	R/W	Reset I^2C slave after the RT9492 latches SDA low for 1s. 0: Enable I^2C time-out function (default) 1: Disable I^2C time-out function
6	QON_RST_EN	1	Y	Y	R/W	0: The QON pin = 0 for 10s will NOT do anything 1: The QON pin = 0 for 10s will turn off Ship FET and stop switching to reset system power (default)
5	AUTO_AICR	1	Y	Y	R/W	0: No action 1: Auto set IAICR by BC1.2 done (default)
4	TD_EOC	1	Y	Y	R/W	End-of-charge deglitch time 0: 2ms 1: 64ms (default)
3	EOC_RST	0	Y	Y	RWC	0: No action (default) 1: Reset EOC auto clear after reset EOC done
2	AUTO_MIVR	1	Y	Y	R/W	0: No action 1: Auto set MIVR by VBUS plug-in (default)
1	JEITA_COOL_VSET	1	Y	Y	R/W	0: Set VBAT_REG = JEITA_WARM_VSET setting (REG0x17[7:5]) 1: VBAT_REG = Register setting (default)
0	JEITA_COLD_HOT	0	Y	Y	R/W	0: JEITA_COLD or JEITA_HOT, stop charge/OTG (default) 1: JEITA_COLD or JEITA_HOT, still charge/OTG

Register Address: 0x4B Register Name: ADD_CTRL 1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	RESERVED	000	N	N	R	Reserved
4	PWM_1MHZ_EN	0	N	Y	R/W	Enable PWM frequency 1MHz mode 0: PWM frequency follows PWM_FREQ (default) 1: Enable PWM frequency at 1MHz
3	OTG_PIN_EN	0	Y	Y	R/W	0: The OTG pin function disable (default) 1: The OTG pin function enable
2	OTG_EN_CONTROL	0	Y	Y	R/W	OTG mode enable with the OTG pin 0: Enable OTG mode by OTG_EN bit (default) 1: Enable OTG by both OTG_EN bit and the OTG pin
1:0	SEAMLESS_CONTROL	00	Y	Y	R/W	00: Disable (default) 01: Seamless on VBUS 10: Seamless on VAC1 11: Seamless on VAC2

Register Address: 0x4C Register Name: ADD_CTRL 2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	BC12_EN_CHANNEL	0	Y	Y	R/W	BC1.2 detect channel 0: VAC1 (default) 1: VAC2
6:5	DCDT_SEL	10	Y	Y	R/W	BC1.2 data contact timer 00: Disable DCD timeout function 01: Enable 300ms DCD timeout function 10: Enable 600ms DCD timeout function (default) 11: Wait data contact
4	VLGC_OPT	0	Y	Y	R/W	Enable primary detection high reference voltage option 0: Disable (default) 1: Enable
3	DPDM_CMP_HYS_EN	1	Y	Y	R/W	DPDM detection hysteresis enable control 0: Disable 1: Enable (default)
2	SPEC_TA_EN	1	Y	Y	R/W	0: Disable special TA detection 1: Enable special TA detection (default)
1:0	HOST_MODE	00	Y	Y	R/W	Host mode setting in OTG 00: DPDM floating (default) 01: SDP 10: CDP 11: DCP

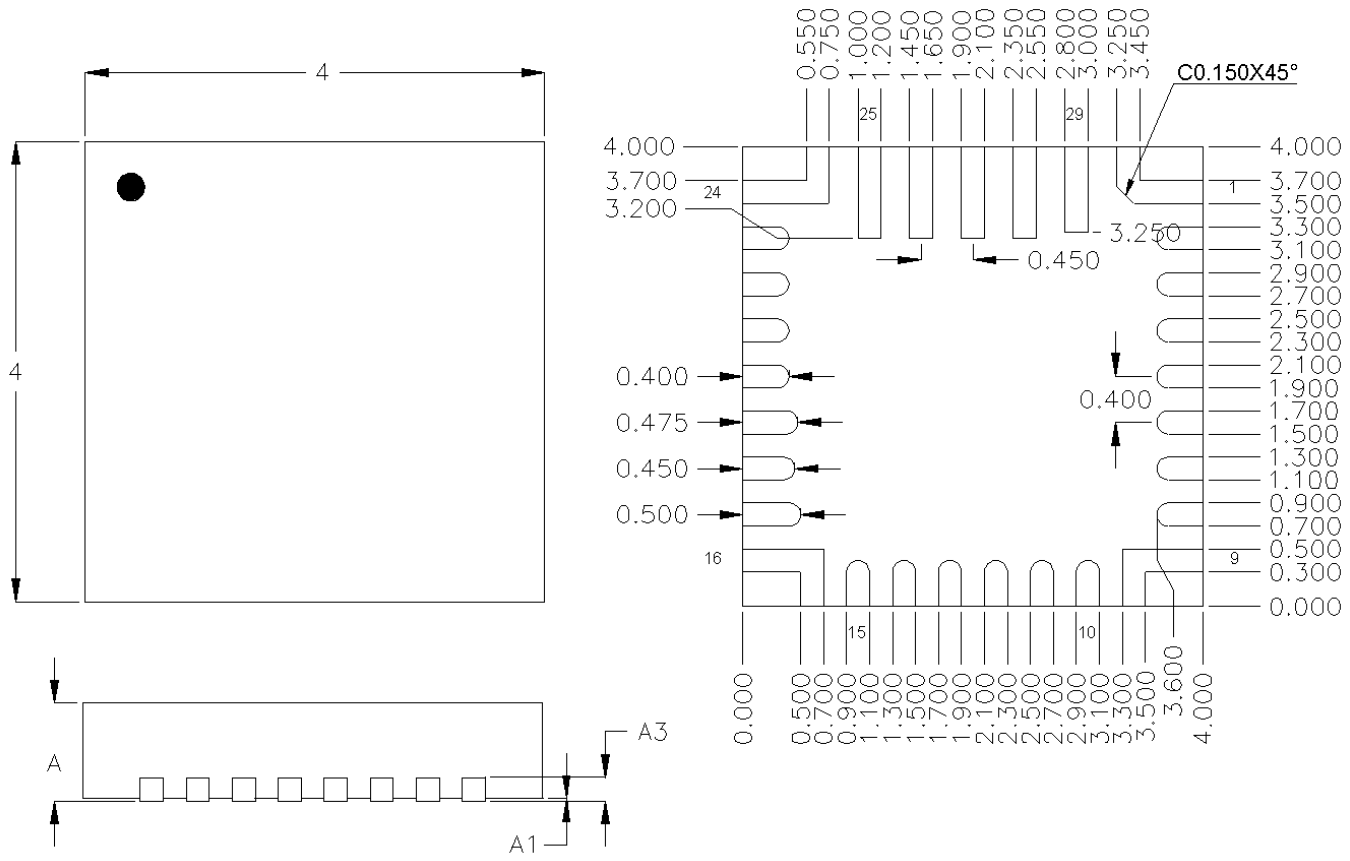
Register Address: 0x4D Register Name: CHG_IRQ_FLAG 6

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IEOC_FLAG	0	N	N	R	IEOC flag 0: Not trigger IEOC (default) 1: Trigger IEOC STAT, read to clear
6	VSYS_ SHORT_FLAG	0	N	N	R	Short circuit protect between VSYS-VBAT flag 0: Not trigger VSYS_SHORT (default) 1: Trigger VSYS_SHORT, read to clear
5	REGN_PROT ECT_FLAG	0	N	N	R	REGN overcurrent or undervoltage protection flag 0: Not trigger REGN_PROTECT (default) 1: Trigger REGN_PROTECT, read to clear
4	PE_DONE_ FLAG	0	N	N	R	Pump Express process flag 0: PE_DONE_FLAG not set (default) 1: While PE processing done, read to clear
3	VBUS_ UNDER_MIVR _FLAG	0	N	N	R	VBUS falling under MIVR flag 0: VBUS not falling under MIVR (default) 1: VBUS falling under MIVR, read to clear
2	VRECHG_ FLAG	0	N	N	R	Recharger event flag 0: No event happened (default) 1: VBAT < VRECHG after EOC, read to clear
1	CDP_PD_ FLAG	0	N	N	R	CDP primary detection status 0: CDP primary detection does not start (default) 1: CDP primary detection starts, read to clear
0	CDP_DONE_ FLAG	0	N	N	R	CDP flow done 0: No CDP flow (default) 1: CDP flow done, read to clear

Register Address: 0x4E Register Name: CHG_IRQ_MASK 6

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IEOC_MASK	1	Y	Y	R/W	0: Not mask IRQ of IEOC_FLAG 1: Mask IRQ of IEOC_FLAG (default)
6	VSYS_ SHORT_ MASK	1	Y	Y	R/W	0: Not mask IRQ of VSYS_SHORT_FLAG 1: Mask IRQ of VSYS_SHORT_FLAG (default)
5	REGN_ PROTECT_ MASK	1	Y	Y	R/W	0: Not mask IRQ of REGN_PROTECT_FLAG 1: Mask IRQ of REGN_PROTECT_FLAG (default)
4	PE_DONE_ MASK	1	Y	Y	R/W	0: Not mask IRQ of PE_DONE_FLAG 1: Mask IRQ of PE_DONE_FLAG (default)
3	VBUS_ UNDER_MIVR _MASK	1	Y	Y	R/W	0: Not mask IRQ of VBUS_UNDER_MIVR_FLAG 1: Mask IRQ of VBUS_UNDER_MIVR_FLAG (default)
2	VRECHG_ MASK	1	Y	Y	R/W	0: Not mask IRQ of VRECHG_FLAG 1: Mask IRQ of VRECHG_FLAG (default)
1	CDP_PD_ MASK	1	Y	Y	R/W	0: Not mask IRQ of CDP_PD_FLAG 1: Mask IRQ of CDP_PD_FLAG (default)
0	CDP_DONE_ MASK	1	Y	Y	R/W	0: Not mask IRQ of CDP_DONE_FLAG 1: Mask IRQ of CDP_DONE_FLAG (default)

19 Outline Dimension

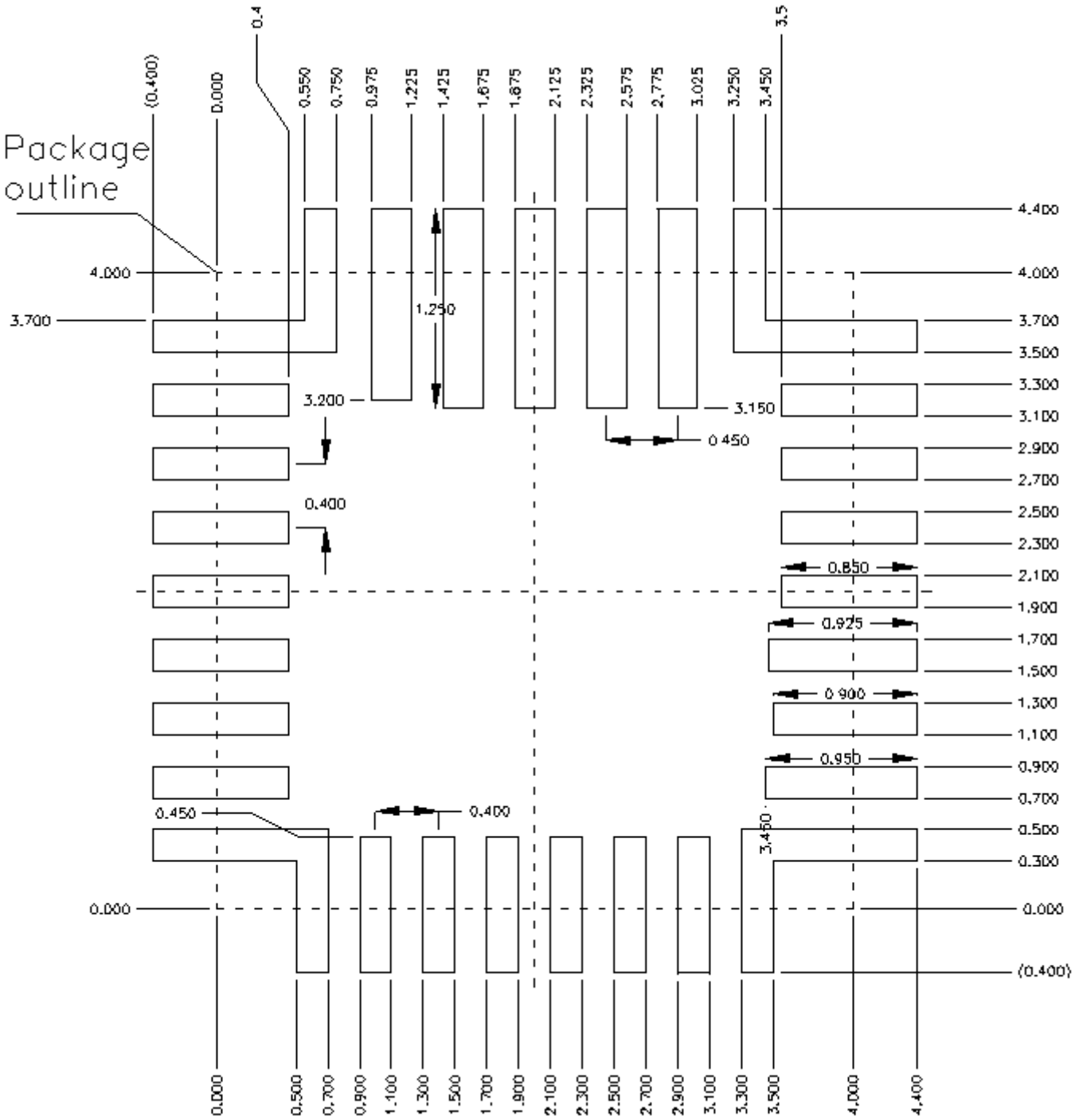


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050

V-Type 29TL QFN 4x4 Package (FC)

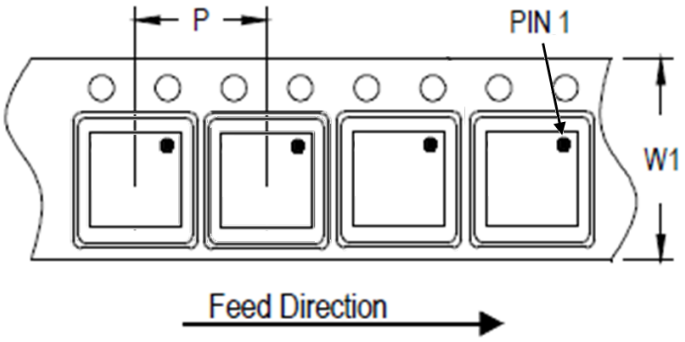
20 Footprint Information

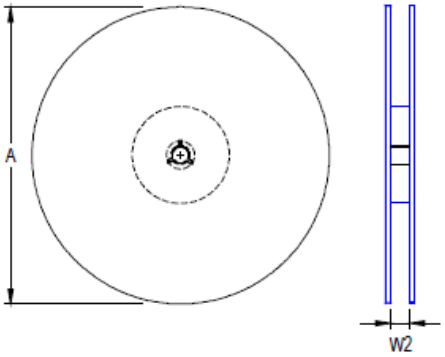


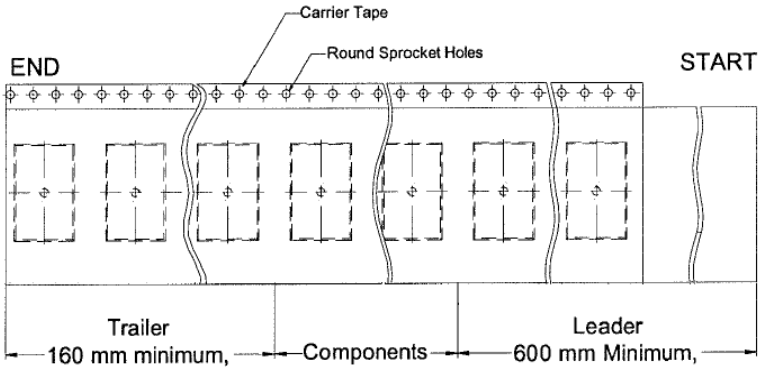
Package	Number of Pin	Tolerance
V/W/U/XQFN4x4-29T(FC)	29	±0.05

21 Packing Information

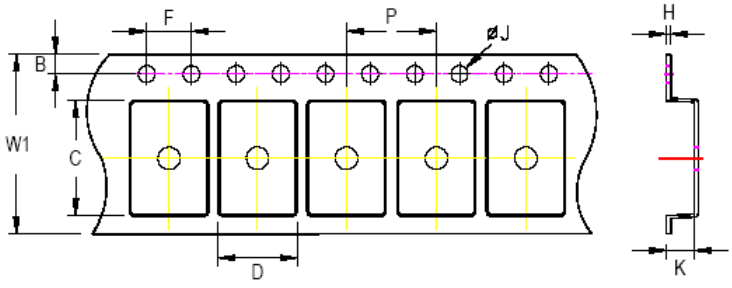
21.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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22 Datasheet Revision History

Version	Date	Description	Item
00	2023/7/5	Final	
01	2023/7/20	Modify	Ordering Information on P1
02	2024/5/9	Modify	Title on P1 General Description on P1 Ordering Information on P1 Device Comparison on P2 Functional Block Diagram on P5 Electrical Characteristics on P8 to 19 Typical Application Circuit on P22, 23 Typical Operating Characteristics on P25, 26, 27 Register Description on P30, 31, 33, 39, 46, 50, 53, 55, 56, 57 Application Information on P63, 64, 65, 69, 70, 72, 74, 75, 76, 79, 80 Packing Information on P84
03	2024/6/13	Modify	Features on P1 Simplified Application Circuit on P1 Note 3 on P9 Outline Dimension on P87
04	2024/10/30	Modify	*Absolute Maximum Ratings on page 10* - Updated Power Dissipation - Updated Package Thermal Resistance *Electrical Characteristics on page 12, 13, 20* - Added IBUS_OCP minimum spec - Added VACDRV specification - Added Current Sink specification range *Application Information on page 37, 38, 46, 47, 54* - Added switching frequency and inductor set description - Corrected SDRV_DLY behavior description - Added Interrupt (INT), Flag, Status and Mask function description - Corrected Poor Source Detect behavior description - Updated Thermal Considerations *Packing Information on page 91* - Updated Tape and Reel Data