3A Single Cell Switching Battery Charger

1 General Description

The RT9470G device are a highly-integrated 3A switch mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Applications

- Smart Phone/Tablet PC
- Personal Information Appliances
- Portable Device and Accessory

3 Ordering Information

RT9470G □

└Package Type

WSC: WL-CSP-30B 2.1x2.5 (BSC)

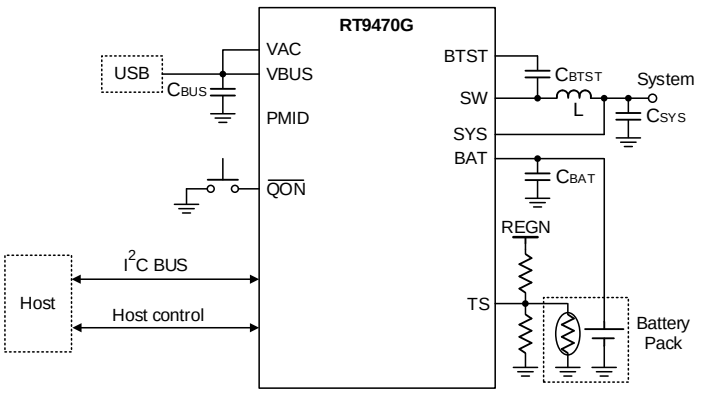
Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

4 Features

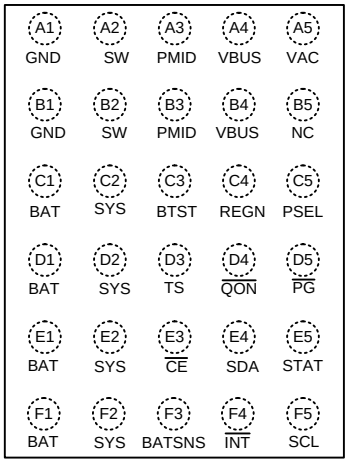
- **High Efficiency, 1.5MHz, Synchronous Switch-Mode Buck Charger**
  - **92% Charge Efficiency at 2A from 5V Input and 3.8V Battery**
  - **Support 3.9V to 13.5V Input Voltage Range**
  - **Average Input Current Regulation (AICR)**
  - **Minimum Input Voltage Regulation (MIVR)**
  - **Minimum Input Voltage Regulation Track (MIVR Track)**
  - **Charge Current Regulation (CCR)**
  - **Charge Voltage Regulation (CVR)**
  - **Charge Voltage Regulation Track (CVR Track)**
  - **Junction Thermal Regulation (JTR)**
- **Supports USB On-The-Go (OTG)**
  - **92% Boost Efficiency at 1A with 3.8V Battery and 5.15V Output**
  - **OTG Current Limit Regulation (OCLR)**
  - **OTG Voltage Limit Regulation (OVLR)**
- **Protection**
  - **Over-Temperature Protection (OTP)**
  - **VBUS Overvoltage Protection (VBUS OVP)**
  - **Battery Overvoltage Protection (VBAT OVP)**
  - **System Overvoltage Protection (VSYS OVP)**
  - **System Undervoltage Protection (VSYS UVP)**
  - **System Over-Load Protection (VSYS OLP)**
  - **Cycle-by-Cycle Overcurrent Protection (OCP)**
  - **OTG Low Battery Protection (OTG LBP)**

5 Simplified Application Circuit



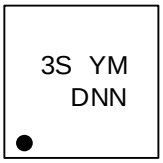
6 Pin Configuration

(TOP VIEW)



WL-CSP-30B 2.1x2.5 (BSC)

7 Marking Information



3S: Product Code
YMDNN: Date Code

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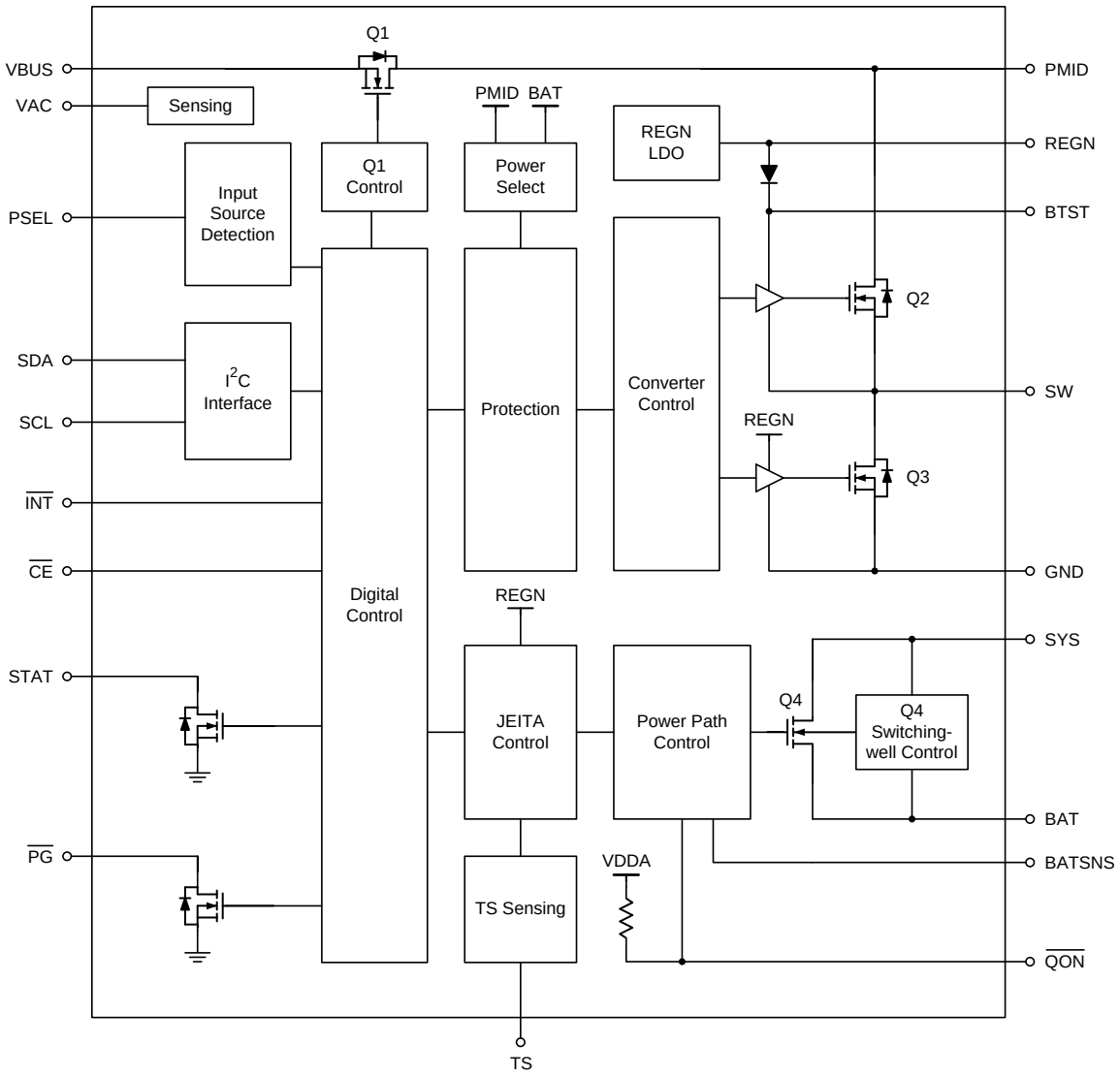
8 Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
A1, B1	GND	P	Power ground.
A2, B2	SW	P	Switching node connecting to output inductor. Internally SW is connected to the source of the high-side switching MOSFET (Q2) and the drain of the low-side switching MOSFET (Q3). Connect a 47nF bootstrap capacitor from SW to BTST.
A3, B3	PMID	P	Connected to the drain of the reverse blocking MOSFET (Q1) and the drain of high-side switching MOSFET (Q2). Connect 10μF capacitor from PMID to GND.
A4, B4	VBUS	P	Charger input voltage. The internal reverse block MOSFET (Q1) is connected between VBUS and PMID with VBUS on source. Connect a 1μF capacitor from VBUS to GND and place it as close as possible to IC.
A5	VAC	AI	Input voltage sensing. This pin must be tied to VBUS.
B5	NC	--	No internal connection.
C1, D1, E1, F1	BAT	P	Battery connection point to the positive terminal of the battery pack. The internal current sensing resistor is connected between SYS and BAT. Connect a 10μF capacitor closely to the BAT pin.
C2, D2, E2, F2	SYS	P	Converter output connection point. The internal current sensing resistor is connected between SYS and BAT. Connect two 10μF capacitors closely to the SYS pin.
C3	BTST	P	PWM high-side driver positive supply. Internally, the BTST is connected to the cathode of the boost-strap diode. Connect the 47nF bootstrap capacitor from SW to BTST.
C4	REGN	P	PWM low-side driver and internal supply output. Internally, REGN is connected to the anode of the bootstrap diode. Connect a 4.7μF capacitor from REGN to GND. The capacitor should be placed close to the IC.
C5	PSEL	DI	Power source selection input. High indicates 0.5A input current limit. Low indicates 2.4A input current limit. Once the device gets into host mode, the host can program different input current limit to AICR register.
D3	TS	AI	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin voltage is out of range. When TS pin is not used, connect a 10kΩ resistor from REGN to TS and a 10kΩ resistor from TS to GND.
D4	$\overline{QON}$	DI	BATFET (Q4) enable control input. When BATFET is in ship mode, a logic low duration turns on BATFET (Q4) to exit shipping mode. When no VBUS, a logic low for t_{QON_RST}, the BATFET turns off for t_{BATFET_RST}, and then re-enable BATFET to provide system reset. Pull-High to internal bias circuit via 250kΩ resistor.
D5	$\overline{PG}$	DO	Open-drain active low power good indicator. Connect the $\overline{PG}$ pin to a logic rail via 2.2kΩ to 10kΩ resistor.
E3	$\overline{CE}$	DI	Charge enable pin. When this pin is driven low, battery charging is enabled.
E4	SDA	DIO	I^2C interface clock. Connect SDA to the logic rail through a 10kΩ resistor.

Pin No.	Pin Name	I/O	Pin Function
E5	STAT	DO	Open-drain charger status output. Connect the STAT pin to a logic rail via 2.2kΩ to 10kΩ resistor. The STAT pin indicates charger status.
F3	BATSNS	AI	Battery voltage sensing pin for charge current regulation. The BATNS pin must be connected to the battery pack as close as possible.
F4	$\overline{INT}$	DO	Open-drain active low interrupt output. Connect the $\overline{INT}$ to a logic rail through 10kΩ resistor. The $\overline{INT}$ pin sends active low pulse to host to report charger device status and fault.
F5	SCL	DI	I^2C interface clock. Connect SCL to the logic rail through a 10kΩ resistor.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 1)

- Voltage Sense Pin Voltage, VAC ---------- –1.4V to 26V
- Supply Pin Voltage, VBUS ---------- –1.4V to 26V
- Terminal Pin Voltage, PMID ---------- –0.3V to 26V
- Terminal Pin Voltage, SW ---------- –0.3V to 16V
- Terminal Pin Voltage, BTST-SW ---------- –0.3V to 6V
- Terminal Pin Voltage, SYS ---------- –0.3V to 6V
- Supply Pin Voltage, BAT ---------- –0.3V to 6V
- Voltage Sense Pin Voltage, BATSNS ---------- –0.3V to 6V
- Other Pins Voltage, STAT, SCL, SDA, $\overline{INT}$, $\overline{CE}$, TS, $\overline{QON}$, REGN ---------- –0.3V to 6V
- Other Pins Voltage, PSEL, $\overline{PG}$ ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-30B 2.1x2.5 (BSC) ---------- 3.37W
- Package Thermal Resistance (Note 2)

  WL-CSP-30B 2.1x2.5 (BSC), θ_{JA} ---------- 29.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

11 Recommended Operating Conditions

(Note 4)

- Voltage Sense Pin Voltage, VAC ---------- 3.9V to 13.5V
- Supply Input Voltage Range, VBUS ---------- 3.9V to 13.5V
- Maximum Input Current, IBUS ---------- 3.2A
- Maximum Input Current, IBUS (VBUS ≥ 12V) ---------- 2A
- Maximum Output Current (SW), ISYS ---------- 3.2A
- Maximum Battery Voltage, VBAT ---------- 4.7V
- Voltage Sense Pin Voltage, BATSNS ---------- 4.7V
- Maximum Charge Current, IBAT ---------- 3.15A
- Maximum Discharge Current, IBAT ---------- 6A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

12 Electrical Characteristics

($V_{BUS\_MIN\_RISE}$ < V_{AC} < $V_{AC\_OVP\_RISE}$ and V_{AC} > V_{BAT} + V_{SLEEP_RISE}, T_A = 25°C, unless otherwise specified) (Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current						
Battery Discharge Current (BAT) in Q4 Disabled	$I_{BAT\_Q4\_DIS}$	V_{BAT} = 4.5V, High-Z mode and I^2C disabled, Q4 disabled	--	15	32	μA
Battery Discharge Current (BAT) in Q4 Enable	$I_{BAT\_Q4\_EN}$	V_{BAT} = 4.5V, High-Z mode and I^2C disabled, Q4 enabled	--	55	85	μA
Input Supply Current (VBUS) in Buck Mode	I_{BUS_HIZ}	V_{BUS} = 5V, High-Z mode and no battery	--	50	86	μA
		V_{BUS} = 12V, High-Z mode and no battery	--	52	88	
Input Supply Current (VBUS) in Buck Mode	I_{BUS_BUCK}	V_{BUS} > $V_{BUS\_MIN\_RISE}$, V_{BUS} > V_{BAT}, converter switching, V_{BAT} = 3.8V, I_{SYS} = 0A	--	5	7	mA
Battery Discharge Current (BAT) in Boost Mode	I_{BAT_BOOST}	V_{BAT} = 4.2V, boost mode, I_{BUS} = 0A, converter switching	--	4	5	mA
VAC, VBUS and BAT Power						
VBUS Operating Range	V_{BUS_OP}	V_{BUS} rising	3.9	--	13.5	V
REGN Turn Off Level with Only VBUS	V_{BUS_UVLO}	V_{BUS} falling	3.0	3.3	3.6	V
Sleep Mode Falling Threshold	V_{SLEEP_FALL}	V_{AC} falling, V_{AC} – V_{BAT}	10	60	120	mV
Sleep Mode Rising Threshold	V_{SLEEP_RISE}	V_{AC} rising, V_{AC} – V_{BAT}	160	250	340	mV
VAC 5.8V Overvoltage rising threshold	$V_{AC\_OVP\_RISE}$	V_{AC} rising	5.5	5.8	6.1	V
VAC 6.5V Overvoltage rising threshold		V_{AC} rising	6.2	6.5	6.8	
VAC 10.9V Overvoltage Rising Threshold		V_{AC} rising	10.3	10.9	11.5	
VAC 14V Overvoltage Rising Threshold		V_{AC} rising	13.3	14	14.7	
VAC 5.8V Overvoltage Hysteresis	$V_{AC\_OVP\_HYS}$	V_{AC} falling	--	300	--	mV
VAC 6.5V Overvoltage Hysteresis		V_{AC} falling	--	300	--	
VAC 10.9V Overvoltage Hysteresis		V_{AC} falling	--	300	--	
VAC 14V Overvoltage Hysteresis		V_{AC} falling	--	300	--	
BAT for Active I^2C, No Adapter	V_{BAT_UVLO}	V_{BAT} rising	2	2.2	2.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Battery Depletion Falling Threshold	$V_{BAT\_DPL\_FALL}$	V_{BAT} falling	2.15	2.38	2.65	V
Battery Depletion Rising Threshold	$V_{BAT\_DPL\_RISE}$	V_{BAT} rising	2.4	2.6	2.8	V
Battery Depletion Rising Hysteresis	$V_{BAT\_DPL\_HYS}$	V_{BAT} rising	--	220	--	mV
Bad Adapter Detection Rising Threshold	$V_{BUS\_MIN\_RISE}$	V_{BUS} rising	3.6	3.8	4	V
Bad Adapter Detection Hysteresis	$V_{BUS\_MIN\_HYS}$	V_{BUS} falling	--	200	--	mV
Bad Adapter Detection Current Source	I_{BADSRC}	Sink current from V_{BUS} to GND	--	40	--	mA
Power Path						
System Regulation Voltage	V_{SYS_MIN}	V_{BAT} < V_{SYS_MIN} = 3.5V, Q4 disabled/enable	3.5	3.5 +0.2	--	V
	V_{SYS}	I_{SYS} = 0A, V_{BAT} > V_{SYS_MIN} = 3.5V, Q4 disabled	--	V_{BAT} +0.05	--	
Top Reverse Blocking MOSFET On-Resistance Between VBUS and PMID	$R_{ON(Q1)}$	–40°C ≤ T_A ≤ 125°C	--	29	--	mΩ
Top Switching MOSFET On- Resistance Between PMID and SW	$R_{ON(Q2)}$	V_{REGN} = 5V, –40°C ≤ T_A ≤ 125°C	--	46	--	mΩ
Bottom Switching MOSFET On-Resistance Between SW and GND	$R_{ON(Q3)}$	V_{REGN} = 5V, –40°C ≤ T_A ≤ 125°C	--	51	--	mΩ
SYS-BAT MOSFET On-Resistance	$R_{ON(BAT-SYS)}$	Measured from BAT to SYS, V_{BAT} = 4.2V, T_J = 25°C	--	14	--	mΩ
Battery Charger						
Charge Voltage Range	$V_{BAT\_REG\_RANGE}$	Default = 4.2V	3.9	--	4.7	V
Charge Voltage Step	$V_{BAT\_REG\_STEP}$		--	10	--	mV
Charge Voltage Setting Accuracy	$V_{BAT\_REG\_ACC}$		–0.5	--	0.5	%
Charge Current Regulation Range	$I_{CHG\_REG\_RANGE}$	Default = 2000mA	0	--	3150	mA
Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$		--	50	--	mA
Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$	V_{BAT} = 3.8V, I_{CHG_REG} < 150mA	–20	--	20	%
		V_{BAT} = 3.8V, 150mA ≤ I_{CHG_REG} < 750mA	–10	--	10	
		V_{BAT} = 3.8V, I_{CHG_REG} ≥ 750mA	–5	--	5	
Pre-Charge Falling Threshold	$V_{PRE\_CHG\_FALL}$	I_{CHG} = 200mA, V_{PRE_CHG} = 3.1V	2.75	2.9	3.05	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pre-Charge Rising Threshold	$V_{PRE\_CHG\_RISE}$	Pre-charge to fast charge, V_{PRE_CHG} = 3.1V	2.95	3.1	3.25	V
Pre-Charge Current Range	$I_{PRE\_CHG\_RANGE}$	Default = 150mA	50	--	800	mA
Pre-Charge Current Step	$I_{PRE\_CHG\_STEP}$		--	50	--	mA
Pre-Charge Accuracy	$I_{PRE\_CHG\_ACC}$	V_{BUS} = 5V, I_{PRE_CHG} = 150mA	–15	--	25	%
End-Of-Charge Current Range	$I_{EOC\_CHG\_RANGE}$	Default = 200mA	50	--	800	mA
End-Of-Charge Current Step	$I_{EOC\_CHG\_STEP}$		--	50	--	mA
End-Of-Charge Accuracy	$I_{EOC\_CHG\_ACC}$	I_{CHG_REG} > 700mA, I_{EOC_CHG} = 200mA, VBAT = 4.2V	–20	--	20	%
		I_{CHG_REG} ≤ 700mA, I_{EOC_CHG} = 200mA, VBAT = 4.2V	–10	--	10	
		I_{CHG_REG} = 600mA, I_{EOC_CHG} = 50mA, VBAT = 4.2V	–25	--	25	
Trickle-Charge Falling Threshold	$V_{TRICKLE\_CHG\_FALL}$	V_{BAT} falling	1.8	2	2.2	V
Trickle-Charge Rising Threshold	$V_{TRICKLE\_CHG\_RISE}$	V_{BAT} rising	2.05	2.25	2.45	V
Trickle-Charge Current	$I_{TRICKLE\_CHG}$	V_{BAT} < $V_{TRICKLE\_CHG\_RISE}$	80	100	120	mA
Re-Charge Threshold Below VBAT_REG	V_{RE_CHG}	V_{BAT} falling, V_{RECHG} = 100mV	70	100	130	mV
		V_{BAT} falling, V_{RECHG} = 200mV	170	200	230	
System Discharge Load Current	I_{SYS_LOAD}	V_{SYS} = 4.2V	--	30	--	mA
Input Voltage and Current Regulation						
Minimum Input Voltage Regulation Range	V_{MIVR_RANGE}	Default = 4.5V	3.9	--	5.4	V
Minimum Input Voltage Regulation Step	V_{MIVR_STEP}		--	100	--	mV
Minimum Input Voltage Regulation Accuracy	V_{MIVR_ACC}	V_{MIVR} = 3.9V and 4.4V	–1.5	--	1.5	%
MIVR Tracking VBAT	$V_{MIVR\_BAT\_TRACK}$	V_{MIVR} = 3.9V, $V_{MIVR\_BAT\_TRACK}$ = 300mV, V_{BAT} = 4V	--	4.3	--	V
MIVR Tracking VBAT Accuracy	$V_{MIVR\_BAT\_TRACK\_ACC}$		–3	--	3	%
Average Input Current Regulation Range	I_{AICR_RANGE}	Default = 0.5A	0.05	--	3.2	A
Average Input Current Regulation Step	I_{AICR_STEP}		--	50	--	mA
Average Input Current Regulation Accuracy	I_{AICR_ACC}	V_{BUS} = 5V, I_{AICR} = 500mA	450	470	500	mA
		V_{BUS} = 5V, I_{AICR} = 900mA	780	840	900	
		V_{BUS} = 5V, I_{AICR} = 1500mA	1300	1400	1500	
		V_{BUS} = 5V, I_{AICR} > 1500mA	–15	--	0	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BAT Overvoltage Protection						
Battery Overvoltage Rising	$V_{BAT\_OVP\_RISE}$	V_{BAT} rising, as percentage of V_{BAT_REG}	103	104	105	%
Battery Overvoltage Falling	$V_{BAT\_OVP\_FALL}$	V_{BAT} falling, as percentage of V_{BAT_REG}	101	102	103	%
Input Reverse Blocking NFET and Regulation						
Junction Thermal Regulation Range	$T_{J\_THREG\_RANGE}$	Default = 120°C	100	--	120	°C
Junction Thermal Regulation Step	$T_{J\_THREG\_STEP}$		--	20	--	°C
Thermal Shutdown Rising	T_{OTP}	Temperature rising	--	160	--	°C
Thermal Shutdown Hysteresis	T_{OTP_HYS}	Temperature falling	--	30	--	°C
NTC Monitor (Charger Mode)						
Battery Temperature COLD Threshold (0°C)	V_{VTS_COLD}	V_{TS} rising, the ratio of V_{REGN}	72.5	73.5	74.5	%
Battery Temperature COOL Threshold (10°C)	V_{VTS_COOL}	V_{TS} rising, the ratio of V_{REGN}	67.5	68.5	69.5	%
Battery Temperature WARM Threshold (45°C)	V_{VTS_WARM}	V_{TS} falling, the ratio of V_{REGN}	44	45	46	%
Battery Temperature HOT Threshold (60°C)	V_{VTS_HOT}	V_{TS} falling, the ratio of V_{REGN}	33.5	34.5	35.5	%
Battery Temperature Hysteresis	V_{VTS_HYS}		--	1.5	--	%
NTC Monitor (OTG Mode)						
Battery Temperature COLD Threshold OTG mode (–20°C)	$V_{VTS\_COLD\_OTG}$	V_{TS} rising, the ratio of V_{REGN}	79	80	81	%
Battery Temperature HOT Threshold OTG mode (60°C)	$V_{VTS\_HOT\_OTG}$	V_{TS} falling, the ratio of V_{REGN}	33.5	34.5	35.5	%
Battery Temperature Hysteresis OTG mode	$V_{VTS\_HYS\_OTG}$		--	1.5	--	%
Charger Overcurrent Threshold						
UGFET Cycle-by-Cycle Overcurrent Threshold	I_{OCP_UG}		5.5	6.5	7.5	A
System Over-Load Threshold	I_{OCP_BATFET}		6	--	--	A
USB On-The-Go (OTG)						
OTG Low Battery Protection	V_{OTG_LBP}	V_{BAT} falling, V_{OTG_LBP} = 2.8V	2.65	2.8	2.95	V
		V_{BAT} rising, V_{OTG_LBP} = 2.8V	2.75	2.9	3.05	
		V_{BAT} falling, V_{OTG_LBP} = 2.5V	2.35	2.5	2.65	
		V_{BAT} rising, V_{OTG_LBP} = 2.5V	2.45	2.6	2.75	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OTG Voltage Limit Regulation Range	$V_{OTG\_CV\_RANGE}$	Default = 5.15V	4.85	--	5.3	V
OTG Voltage Limit Regulation Step	$V_{OTG\_CV\_STEP}$		--	150	--	mV
OTG Voltage Limit Regulation Accuracy	$V_{OTG\_CV\_ACC}$	V_{BAT} = 3.8V, I_{PMID} = 0A, V_{OTG_REG} = 5.15V	–3	--	3	%
OTG Current Limit Regulation Accuracy	I_{OTG_CC}	$I_{OTG\_LIMIT\_REG\_SEL}$ = 1.2A	1.2	1.4	1.6	A
		$I_{OTG\_LIMIT\_REG\_SEL}$ = 0.5A	0.5	0.6	0.7	
OTG Overvoltage Threshold	V_{OTG_OVP}	V_{AC} rising, V_{AC_OVP} = 6.5V	6.2	6.5	6.8	V
OTG Capacitive Load	C_{OTG_LOAD}	V_{BAT} = 3.8V, V_{OTG_REG} = 5.15V, capacitive load plug in	--	--	300	μF
PWM						
PWM Switching Frequency	f_{SW_BUCK}	Oscillator frequency, buck mode	1350	1500	1650	kHz
	f_{SW_BOOST}	Oscillator frequency, boost mode	1350	1500	1650	
Maximum PWM Duty Cycle	D_{MAX}		--	97	--	%
REGN						
REGN LDO Output Voltage	VREGN	V_{BUS} = 9V, I_{REGN} = 40mA	4.5	4.9	5.3	V
		V_{BUS} = 5V, I_{REGN} = 20mA	4.5	4.9	5	
Control I/O Pin ($\overline{CE}$, PSEL, SCL and SDA)						
Input High Threshold Voltage	V_{IH_CTRL}		1.3	--	--	V
Input Low Threshold Voltage	V_{IL_CTRL}		--	--	0.4	V
High Level Leakage Current	I_{BIAS}	Pull high to 1.8V	--	--	1	μA
Control I/O Pin ($\overline{PG}$, STAT and $\overline{INT}$)						
Output Low Threshold Voltage	V_{OL_CTRL}		--	--	0.4	V
$\overline{INT}$ Pull Low Time	$t_{INT\_PULL\_LOW}$	$\overline{INT}$ pull low time	--	256	--	μs
Timing Requirements						
VAC OVP Reaction Time	t_{VAC_OVP}		--	200	--	ns
Bad Adapter Detection Duration	$t_{BAD\_AD\_DETECTION}$		--	30	--	ms
Deglitch Time for Charger EOC	t_{EOC_DGL}		--	256	--	ms
Deglitch Time for Re-Charge	$t_{RE\_CHG\_DGL}$		--	256	--	ms
Charge Safe Timer	$t_{CHG\_SAFE\_TMR}$	Timer = 10hr	9	10	11	hr
Back-Ground Charge Timer	$t_{BG\_CHG\_TMR}$	Timer = 30min	29	30	31	min

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{QON}$ Timing						
$\overline{QON}$ Low Time to Exit Shipping Mode	$t_{SHIPMODE\_EXIT}$		0.9	1.1	1.3	s
$\overline{QON}$ Low Time to Reset System	t_{QON_RST}		9	10	11	s
BATFET Reset Time	t_{BATFET_RST}		430	453	480	ms
Enter Shipping Mode Delay Time	$t_{SHIP\_MODE\_ENTER}$		11	12	13	s
I^2C Clock and Watchdog Timer						
SCL Clock	f_{SCL}	CB ≤ 100pF	--	--	3.4	MHz
		100pF < CB ≤ 400pF	--	--	1.7	
Watchdog Timer	t_{WDT}	Default = 40s	--	40	--	s
Watchdog Reset Wait Time	t_{WDT_WAIT}		--	500	--	ms

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

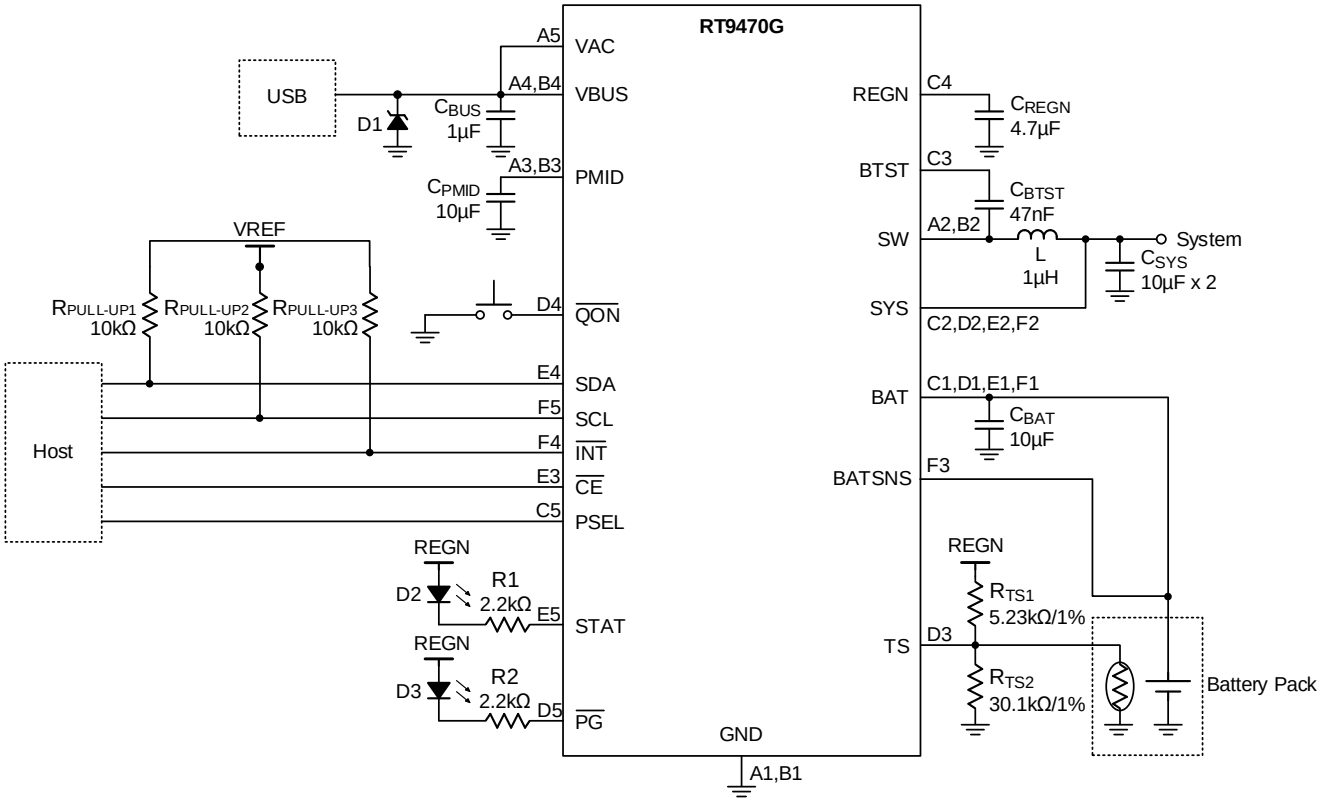
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-9 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Specification is guaranteed by design and/or correlation with statistical process control.

13 Typical Application Circuit

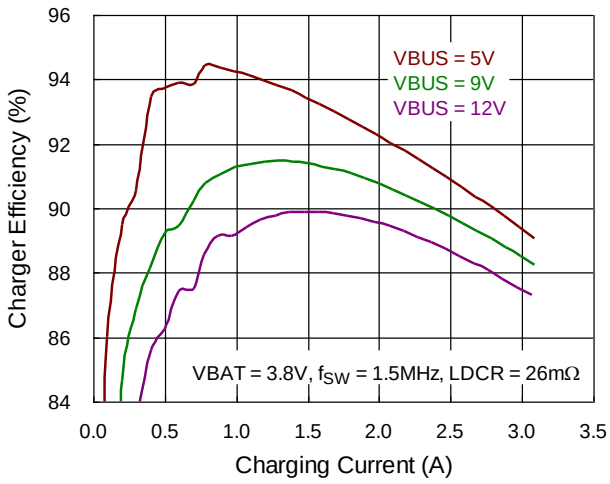


Below are recommended components information

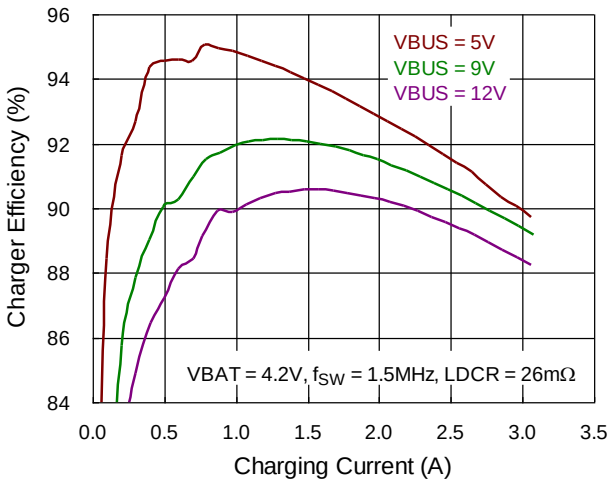
Name	Description	Part Number	Package	Manufacturer
C_{BUS}	1µF/25V/X5R	GRM155R61E105KA12	0402	muRata
C_{PMID}	10µF/25V/X5R	GRM188R61E106MA73	0603	muRata
C_{BTST}	47nF/16V/X5R	GRM033R61C473KE84	0201	muRata
C_{SYS}	10µF/6.3V/X5R	GRM185R60J106ME15	0603	muRata
C_{BAT}	10µF/6.3V/X5R	GRM185R60J106ME15	0603	muRata
C_{REGN}	4.7µF/6.3V/X5R	GRM155R60J475ME47	0402	muRata
L	1µH/20%	CIGT252010EH1R0MNE	2.5 x 2.0 x 1.0mm	Samsung
D1	PTVSHC3N12VU	TVS Diode	DFN2x2-3L	Prisemi

14 Typical Operating Characteristics

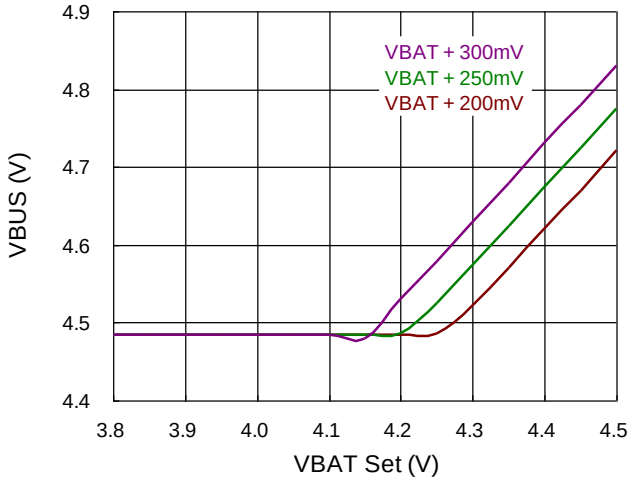
Charger Efficiency vs. Charging Current



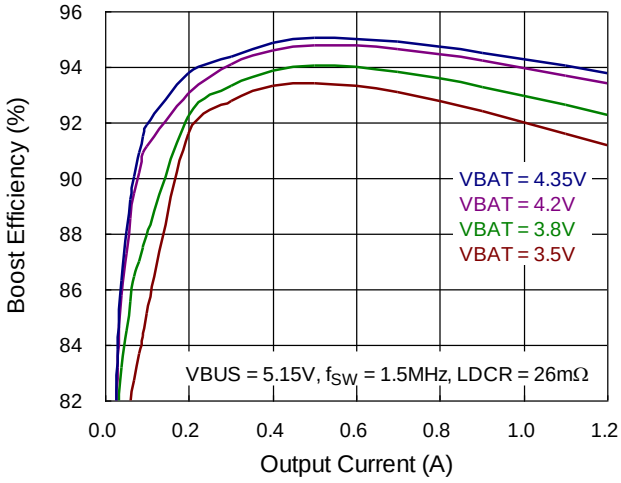
Charger Efficiency vs. Charging Current



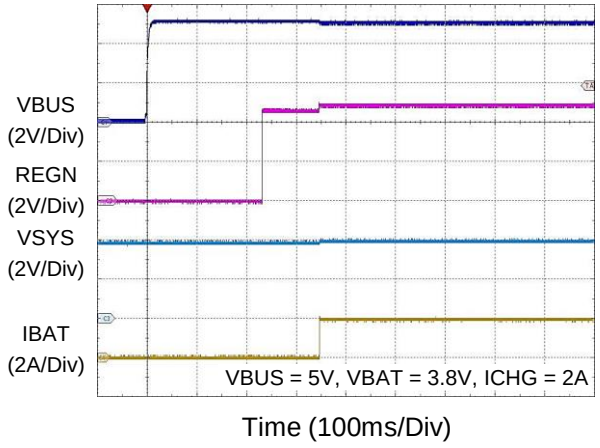
MIVR Tracking VBAT



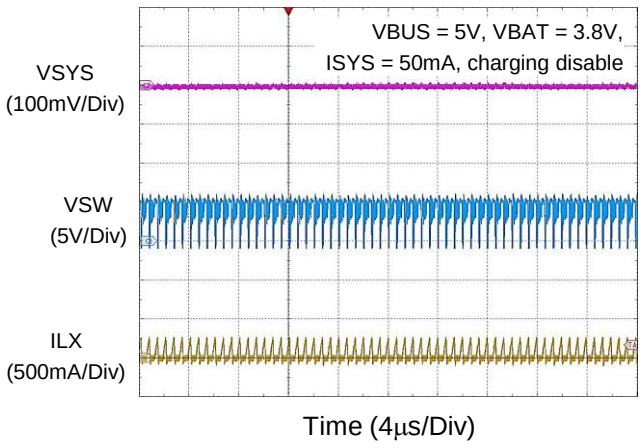
Boost Efficiency vs. Output Current



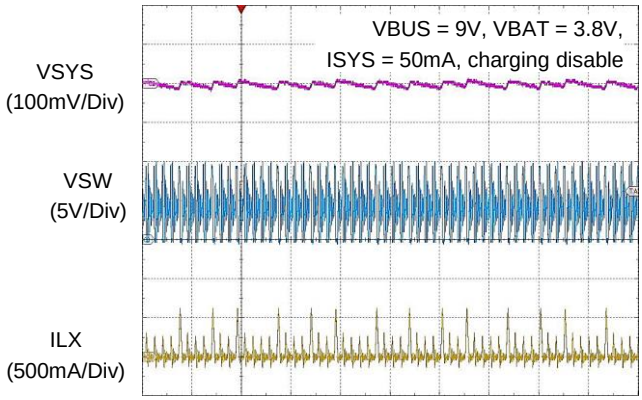
Power-UP with VBUS Plug In



Buck Switching

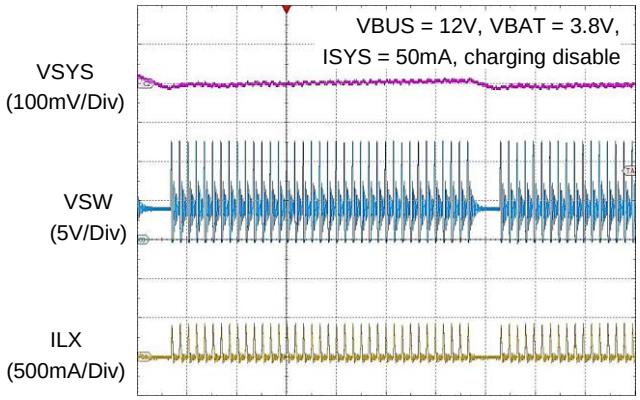


Buck Switching



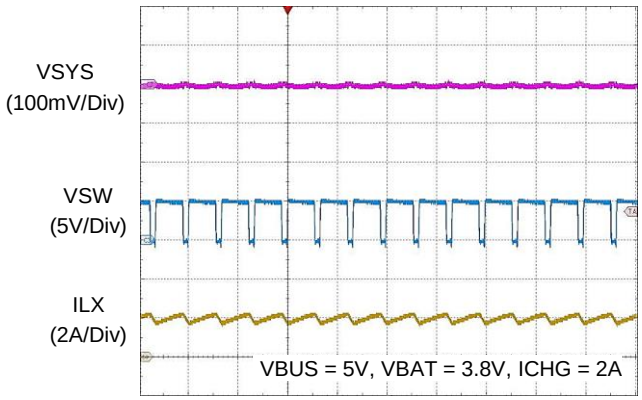
Time (4μs/Div)

Buck Switching



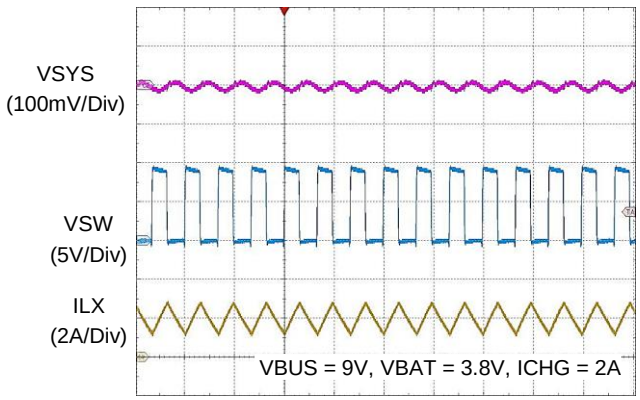
Time (4μs/Div)

Buck Switching



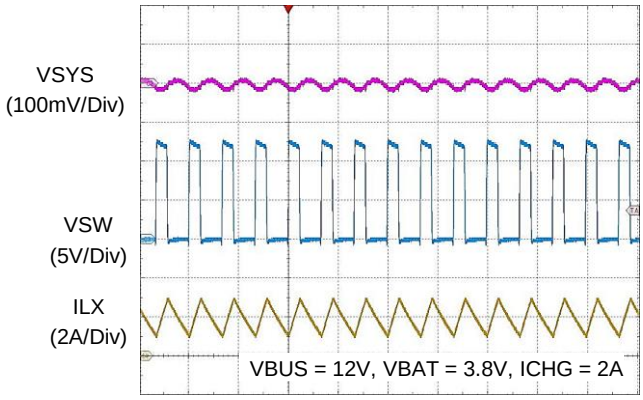
Time (1μs/Div)

Buck Switching



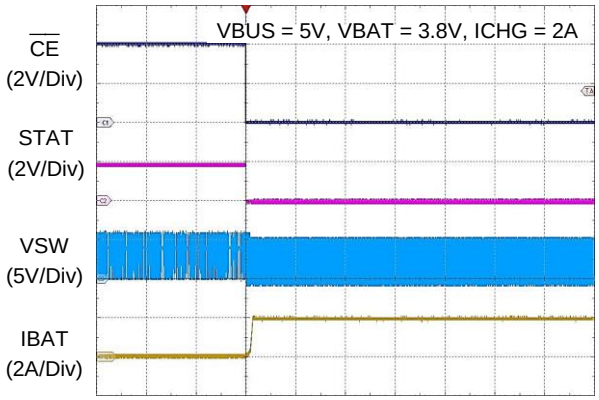
Time (1μs/Div)

Buck Switching



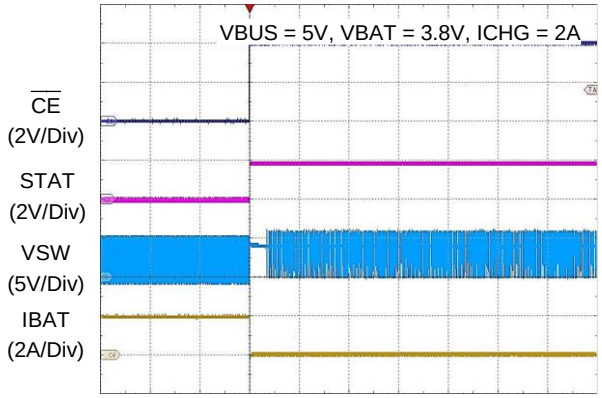
Time (1μs/Div)

Charge Enable



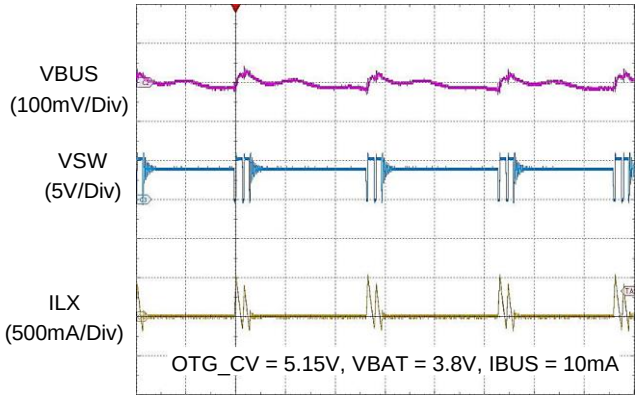
Time (5ms/Div)

Charge Disable



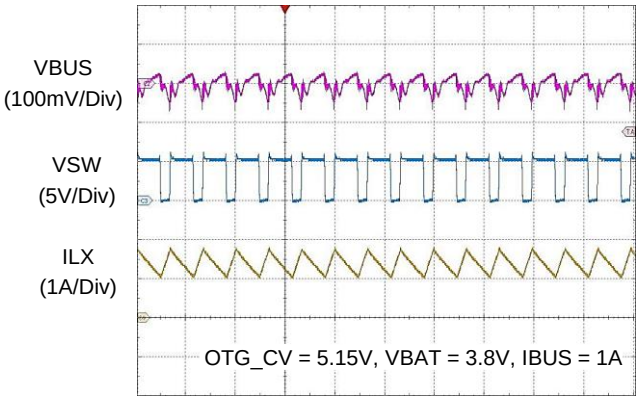
Time (5ms/Div)

Boost Switching



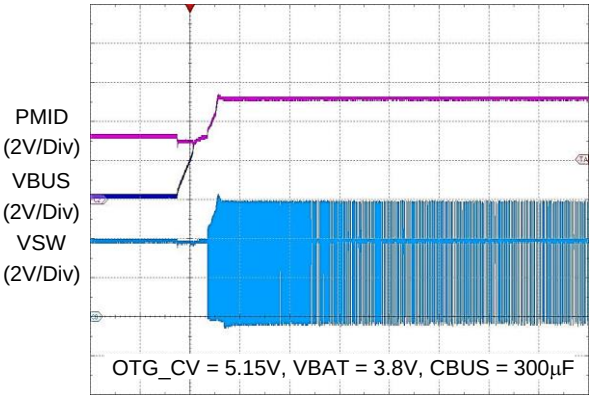
Time (4μs/Div)

Boost Switching



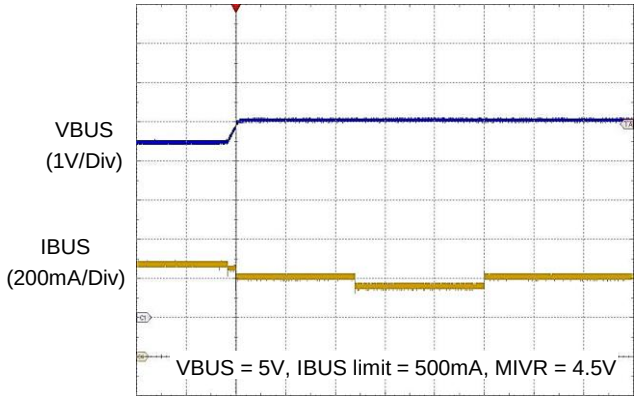
Time (1μs/Div)

Boost Start-Up



Time (2ms/Div)

AICC Enable



Time (50ms/Div)

15 Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

15.1 Power-Up

- **Power-On-Reset (POR)**

  The device powers internal bias circuits from the higher voltage of VBUS and VBAT. When VBUS rises above 1.8V or VBAT rises above V_{BAT_UVLO}, I^2C interface is ready for communication and all the registers are reset to default value.

- **Device Power-Up from Battery Only**

  When only Battery is present and VBAT above $V_{BAT\_DPL\_RISE}$, the BATFET turns on to connect VBAT to VSYS. The REGN stays off to minimize the quiescent current. The low quiescent current on VBAT and low $R_{DS(ON)}$ of BATFET minimize device power consumption and conduction loss maximum battery run life.

  The device always monitors the discharge current through BATFET (Battery Supply Mode). When the system is overloaded or shorted (I_{BAT} > I_{BATFET_OCP}), the device turns off BATFET immediately and sets BATFET_DIS = 1 to enter Shipping Mode until VBUS plugs in again or uses the methods to exit Shipping Mode to re-enable BATFET.

- **Device Power-Up from VBUS**

  When the VBUS is plugged in, the power up sequence is as listed:

  1. Power-up REGN LDO.
  2. Poor Source Detection.
  3. PORT_STAT Detection is based on PSEL or input source type to set default Average Input Current Regulation (AICR) register.
  4. Minimum Input Voltage Regulation (MIVR) setting.
  5. Buck Converter Power-up.

- **Power-Up REGN LDO**

  The REGN LDO supplies the High-side and Low-side MOSFET gate drive. The REGN also provides bias to TS external resistor and pull-up rail of STAT. The REGN is enabled when the below conditions are valid:

  1. VAC above VBAT + V_{SLEEP_RISE} in buck mode or enable OTG bit in boost mode.
  2. After 220ms delay is completed when V_{AC} above VBAT + V_{SLEEP_RISE}.
  3. REGN LDO turns off when device in HZ mode, sleep mode, VBUS overvoltage or OTG disable.

- **Poor Source Detection**

  After REGN powers up, the device checks the current capability of the input source. The input source has to meet following requirements to turn on the buck converter.

  1. VBUS below VAC_OVP_RISE.
  2. VBUS above VBUS_BAD_ADP then pulling I_{BADSRC} (typical = 40mA).

When input source passes above conditions, the ST_VBUS_GD and the FL_VBUS_GD turn to high and $\overline{\text{INT}}$ pin is pulsed for interrupting the host. If ST_VBUS_GD does not turn to high, it repeats poor source detection every 2 seconds.

- **VBUS Source Type Detection**

  After ST_VBUS_GD turns to high, the device runs PSEL pin status. After detection is completed, the ST_CHG_RDY and the FL_CHG_RDY turn to high and $\overline{\text{INT}}$ pin is pulsed for interrupting the host.

  Then the following registers are changed:

  1. Average Input Current Regulation (AICR) register is changed to the result of VBUS source type detection or PSEL pin status automatically if AUTO_AICR = 1.
  2. PORT_STAT bit is updated to indicate VBUS source type.

- **Average Input Current Regulation (AICR)**

  The charger input current is always limited by AICR register. The range of AICR is from 50mA to 3.2A with 50mA resolution.

  1. If the bit AUTO_AICR is set to 0, the device cannot change AICR automatically after VBUS source type detection.
  2. The host can over-write AICR register to change input current limit.
  3. The AICR register setting from PSEL refers to Table 1.
  4. PSEL value updates AICR in real time.

Table 1. AICR Setting from PSEL

PSEL pin	AICR setting	PORT_STAT
High	0.5 A	1101
Low	2.4 A	1111

- **Minimum Input Voltage Regulation (MIVR)**

  The MIVR function prevents input voltage drops due to insufficient current provided from input power source. The VBUS voltage decreases to VMIVR setting level when the overcurrent condition of input power source occurs. The VMIVR register default setting is 4.5V, it can be set by I^2C interface, the range from 3.9V to 5.4V with 0.1V resolution. In addition, the device provides MIVR tracking function by enabling VMIVR_BAT_TRACK register bits. If this tracking function is enabled, the MIVR will be the higher of the VMIVR register and VBAT + VMIVR_ BAT_TRACK offset.

- **Buck Converter Power-Up**

  After the AICR is set, the converter is enabled and starts switching. BATFET stays on unless charger is disabled (CHG_EN = 0) or enters shipping mode (BATFET_DIS = 1).

  The device integrates a synchronous PWM controller with 1.5MHz switching frequency, high-accuracy current and voltage regulation. The device also supports PFM control to improve light-load efficiency. The BUCK_PFM_DIS register bit can be used to prevent PFM operation in buck configuration.

- **Boost Mode Operation (OTG)**

  The device supports OTG (On-The-Go) mode by boost converter operation to deliver power from battery to other portable devices. The maximum boost mode output current is up to 1.2A, which includes USB OTG

500mA output requirement.

The boost operation can be enabled by following condition:

1. VBAT above VOTG_LBP
2. VBUS less than VBAT+V_{SLEEP_FALL}
3. OTG_EN is set to high
4. Voltage at TS pin is within acceptable range (V_{VTS_HOT} < VTS < V_{VTS_COLD})
5. After 30ms delay from OTG_EN is set to high, boost converter powers up.

In boost mode, the IC_STAT register bits is updated to 1111, the VBUS output voltage is 5.15V and output limit current is 1.2A by default, output voltage (OTG_CV) and output current limit (OTG_CC) can be selected through I^2C. The boost output maintained when VBAT is above V_{OTG_LBP}.

15.2 Watchdog Timer (WDT)

When the device is controlled by host, most of the registers can be programmed by host. The host has to write WDT_CNT_RST = 1 to reset counter before watchdog timeout and it can also disable WDT function by setting WDT bits to 00.

When the watchdog timer expired, ST_WDT and FL_WDT turn to high and $\overline{INT}$ pin is pulsed for interrupting the host. After delay 512ms, the related registers are reset to default values. (Refer to Register Descriptions for detail). If the device is watchdog timeout status, host can write any registers or WDT_CNT_RST = 1 to return counting.

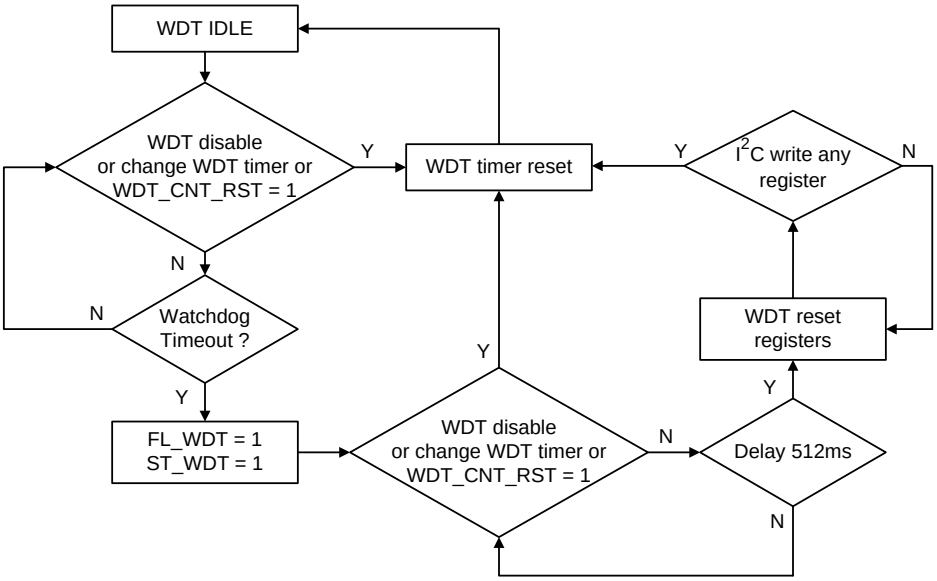


Figure 1. WDT Flow Chart

15.3 Power Path Management

The device provides automatic power path selection to supply system (VSYS) from VBUS, VBAT (battery) or both of them.

- **Enter Shipping Mode (BATFET Disable)**

  To extend battery life when shipping or storage, the device can turn off BATFET to minimize battery leakage current. The host can set BATFET_DIS bit to turn off BATFET immediately or set BATFET_DIS_DLY to delay $t_{SHIP\_MODE\_ENTER}$ to turn off BATFET.

- **Exit Shipping Mode (BATFET Enable)**

  When in shipping mode, one of the following methods can exit shipping mode to restore power for system:

  1. VBUS plug in.
  2. Set BATFET_DIS bit to 0.
  3. Set REG_RST bit to reset all registers to default.
  4. Press $\overline{QON}$ pin from high to low longer than $t_{SHIPMODE\_EXIT}$.

- **$\overline{QON}$ Pin Operations**

  The $\overline{QON}$ pin has two function to control BATFET.

  1. BATFET Enable: $\overline{QON}$ pin transition from high to low with longer than $t_{SHIPMODE\_EXIT}$ deglitch turns on BATFET to exit shipping mode.
  2. SYSTEM Reset: $\overline{QON}$ pin transition from high to low with longer than t_{QON_RST} deglitch and VBUS is not plugged in, it turns off BATFET for t_{BATFET_RST} then it is re-enabled BATFET. This function allows system connect to VSYS to do power-on-reset. This function can be disabled by setting QON_RST_EN bit to 0.

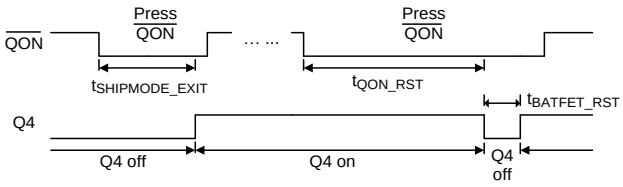


Figure 2. $\overline{QON}$ Timing

15.4 Battery Charging Management

The device has charge current up to 3.15A with 18mΩ BATFET to improve charge efficiency and decrease voltage drop during battery discharging.

- **Charging Cycle**

  When battery charging is enabled ($\overline{CE}$ pin set to low and CHG_EN = 1), the device autonomously completes a charging cycle without host controls. The device default parameters refers as Table 2. The host can also change charging parameters through I^2C.

Table 2. Default Charging Parameters

Default Mode	RT9470G
Charging Voltage	4.2V
Charging Current	2A
Pre-Charge Current	150mA
End of Charge(EOC) Current	200mA
Temperature Profile	JEITA
Fast Charge Safety Timer	10 Hours

A charging cycle starts with following condition:

1. Buck converter starts.
2. Battery charging is enabled ($\overline{CE}$ pin is low, CHG_EN = 1 and ICHG_REG is not 0mA).
3. Without any thermal fault on TS.

4. No safety timer fault.
5. BATFET is turned on (BATFET_DIS = 0).

The charger is in end of charge status when the charging current is below EOC current threshold, battery voltage is above recharge voltage threshold, and device not in AICR, MIVR or thermal regulation.

When battery voltage is discharged below recharge threshold (threshold setting through VRE_CHG register bits), the device restarts a new charging cycle automatically. After the charge is done, toggle CE pin or CHG_EN can restart a new charging cycle.

- **Battery Charging Profile**

The device charges the battery in five status: trickle charge, pre-charge, constant current, constant voltage and back-ground charge (optional).

Table 3. Charging Current Setting

Current Parameter	Default Current Setting	IC_STAT
$I_{TRICKLE\_CHG}$	100mA	0010
I_{PRE_CHG}	150mA	0011
I_{CHG_REG}	2A	0100
I_{EOC_CHG}	200mA	0111

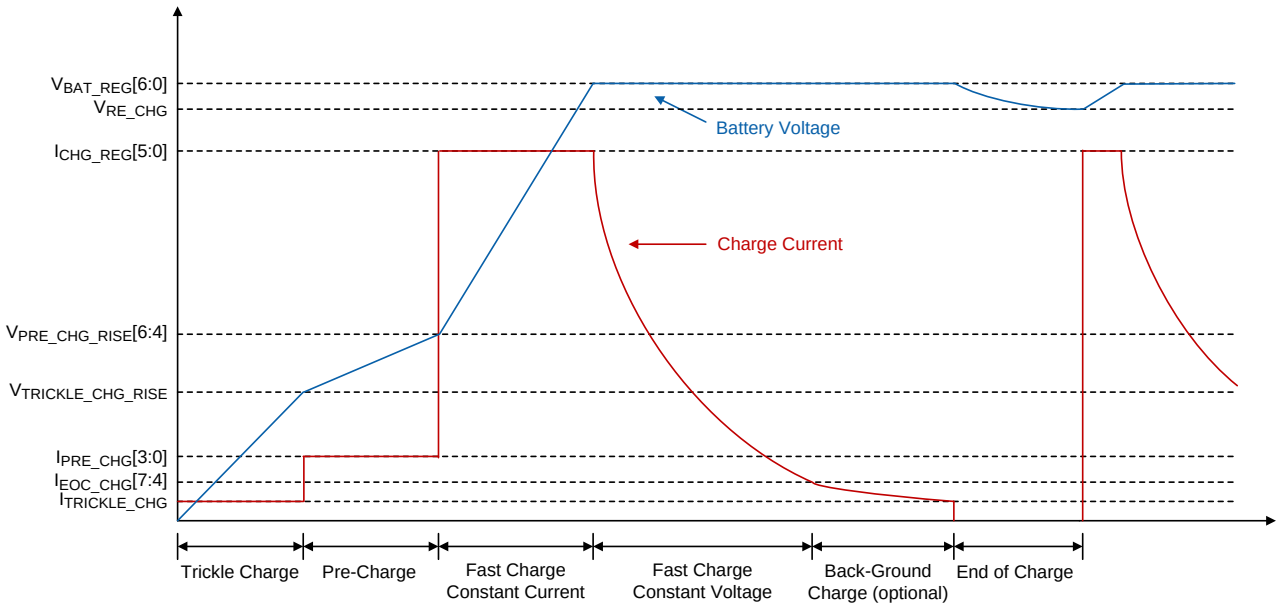


Figure 3. Charging Profile

- **End of Charge (EOC)**

The charger enters end of charge status when battery voltage is above recharge threshold, and the charge current is below I_{EOC_CHG}. I_{EOC_CHG} setting range is from 50mA to 800mA with 50mA resolution. After EOC, the BATFET turns off with TE = 1 and BG_CHG_TMR = 00, and the buck converter keeps switching to supply power to the system. BATFET will turn on again when battery voltage is under recharge voltage threshold or device is in Battery Supply Mode during EOC.

When EOC occurs, there are four conditions as below:

Table 4. EOC Status Scenario

	TE = 1 BG_CHG_TMR (disable)	TE = 1 BG_CHG_TMR (counting)	TE = 1 BG_CHG_TMR (timeout)	TE = 0 BG_CHG_TMR (disable)
ST_EOC	1	1	1	1
ST_CHG_DONE	1	0	1	0
ST_BG_CHG	0	1	0	0
STAT Pin	High	High	High	Low
IC_STAT	0111	0110	0111	0101
BATFET	OFF	ON	OFF	ON

1. If the device triggers AICR, MIVR, JEITA or thermal regulation status during charging, the actual charging current will be less than programmed value. In this condition, EOC function will be disabled and the safety timer's counter clock rate will be half.
2. The back-ground charge can be applied after EOC is detected. The back-ground charge is enabled by setting BG_CHG_TMR and TE = 1 only. When back-ground charge occurs, the IC_STAT is set to 0110, and the BATFET will turn off after back-ground charge timer expires.
3. The BG_CHG_TMR gets reset at one of the following conditions:
   - CHG_EN disable to enable
   - EOC status re-trigger
   - EOC_RST bit is set
   - REG_RST bit is set
   - BG_CHG_TMR value changes

   An $\overline{INT}$ pulse is asserted to host when entering back-ground charge and back-ground charge timer expires.

- **Optimized VDS on BATFET**

  The device deploys power path function with BATFET separating system from battery. The minimum system voltage is set by VSYS_MIN bits (default 3.5V).

  When the battery voltage is under VSYS_MIN setting, the BATFET operates in linear mode (LDO mode) and the system voltage is typically 200mV above the VSYS_MIN setting. When the battery voltage rises above VSYS_MIN, BATFET turns fully on to minimize $R_{DS(ON)}$ for optimizing VDS (voltage different between VSYS and VBAT) on BATFET.

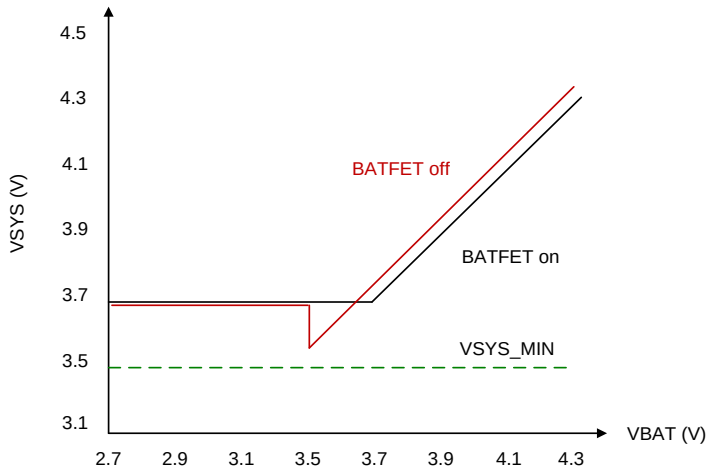


Figure 4. VSYS vs. VBAT

When BATFET turns off and battery voltage is above VSYS_MIN, the system is regulated at typically 50mV above battery voltage. The status register ST_SYS_MIN = 1 when the system is in minimum system voltage regulation.

- **Power Management System**

  To apply maximum current and avoid over loading from the power source on VBUS, the device's Power Management System continuously monitors the power source voltage and current. When power source is overloaded, either the current exceeds the AICR or the voltage drops to MIVR, the device will reduce the charge current to priority power energy for system.

  When the charge current is reduced to zero, but power source still triggers AICR or MIVR, the VSYS starts to drop. Once the VSYS drops under VBAT, the device automatically change to battery supply mode, and the BATFET turns fully on and battery starts to discharge so that the system is supported from both battery and power source.

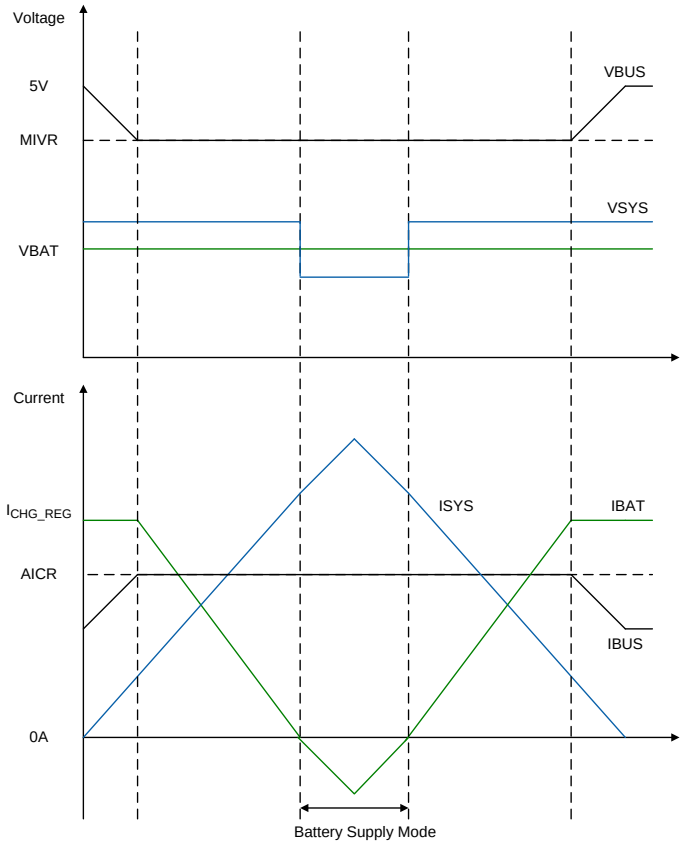


Figure 5. Power Management System

- **Battery Supply Mode**

  During charge status, when voltage difference between VBAT and VSYS above 50mV, the BATFET turns on and the BATFET gate is regulated the gate driver of BATFET to minimize VBAT-VSYS voltage stays at 40mV to prevent entering and exiting the battery supply mode frequently. When the voltage of VBAT-VSYS below 0mV, the charger exits the battery supply mode, and starts to charge battery.

- **JEITA Protection During Charge Mode**

  The device provides a single thermistor input for temperature monitor.

  To achieve battery thermal protection, JEITA guidelines were released in 2007.

  To start a charge cycle, the voltage on TS pin must be in the T1 to T4 range. The device will stop charging if the battery temperature is lower than T1 (Cold) or higher than T4 (Hot) with JEITA_COLD = 0 and JEITA_HOT = 0.

  In this case, the IC_STAT = 1000 for charge fault and an $\overline{INT}$ is asserted to the host.

  In cool temperature range (T1 to T2), the charge current is reduced to 50% or 25% of I_{CHG_REG} (configured by JEITA_COOL_ISET).

  In warm temperature range (T3 to T4), the voltage setting of V_{BAT_REG} is reduced to 4.1V or the same as V_{BAT_REG} (configured by JEITA_WARM_VSET).

  The device provides more flexible settings than JEITA requirement.

  In cool temperature range (T1 to T2), the charger can set voltage of V_{BAT_REG} down to 4.1V (configured by JEITA_COOL_VSET).

  In warm temperature range (T3 to T4), the charge current can be reduced to 50% of I_{CHG_REG} (configured by

JEITA_WARM_ISET).

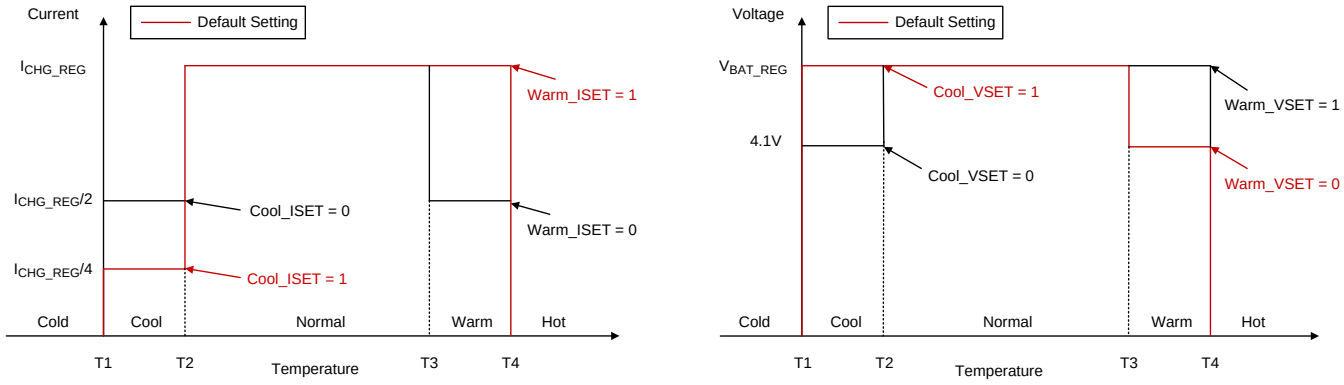


Figure 6. JEITA Protect for Charging Current and Voltage

There are four sections which are implemented for JEITA protection. Base on R_{HOT} and R_{COLD}, R_{TS1} and R_{TS2} can be calculated with equation (1) and (2). Herein, R_{HOT} is the NTC resistance of battery over-temperature threshold, and R_{COLD} is the NTC resistance of battery under-temperature threshold.

$$R_{TS1} = V_{REGN} \times [(1/V_{T1} - 1/V_{T4}) / (1/R_{COLD} - 1/R_{HOT})] \quad \text{.....(1)}$$

$$R_{TS2} = R_{TS1} \times [1/(V_{REGN} / V_{T1} - R_{TS1} / R_{COLD} - 1)] \quad \text{.....(2)}$$

- **Thermal Protect During Boost Mode**

  To start a boost mode to discharge from battery, the voltage on TS pin must be in T0 to T4 range. The device will stop converter if the battery temperature is lower than T0 (COLD_OTG) or higher than T4 (HOT_OTG). In this case, the IC_STAT = 1000 for charge fault and an $\overline{INT}$ is asserted to the host.

  Once temperature returns to normal range, the boost mode is recovered.

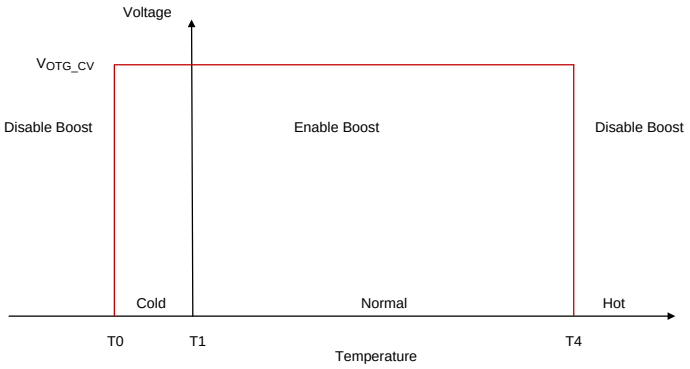


Figure 7. Thermal Protect During Boost Mode

- **Charging Safety Timer**

  The device has safety timer to prevent abnormal charging time due to poor battery condition. The device can be set CHG_SAFE_TMR bits to change timer for fast charge cycle. When the safety timer expires, the device stops charging, the IC_STAT = 1000 for charge fault, ST_CHG_TOUT = 1, and an $\overline{INT}$ is asserted to the host. The safety timer can be disable by setting CHG_SAFE_TMR_EN = 0.

Table 5. Charging Safety Timer

VBAT	Safety Timer
<V_{PRE_CHG}	2 Hours
>V_{PRE_CHG}	5 Hours, 10 Hours (Default), 15 Hours, 20 Hours

When the charger in AICR, MIVR, JEITA cool, JEITA warm or thermal regulation, the safety timer's counter clock rate will be half.

For example, if charger in AICR status, and timer setting is 10 hours, the actual safety timer will expire in 20 hours. The extended charge timer setting can be disabled by setting CHG_SAFE_TMR_2XT = 0.

The safety timer will be reset by:

1. Toggle $\overline{CE}$ pin
2. CHG_EN disable/enable
3. CHG_SAFE_TMR disable/enable
4. REG_RST is set.

- **MediaTek Pump Express+ (MTK, PE+)**

  The device can provide an input current pulse to communicate with an MTK-PE+ high voltage adapter. When PE_EN bit is enabled, the device can increase or decrease adapter output voltage by setting PE10_INC to the desired value. After enabling PE function, the device will generate a VBUS current pattern for the MTK-PE+ adapter to automatically identify whether to increase or decrease output voltage. Once the PE pattern is finished, PE_EN bit will clear to 0, and an INT is asserted to the host to indicate PE_DONE.

- **Adaptive Input Current Control (AICC)**

  The AICC function provides an adaptive AICR setting to prevent input voltage drops. When the input power source is overcurrent and the VBUS drops to the MIVR level, set AICC_EN bit to 1, the device will automatically decrease AICR level step by step until exit MIVR event. Once AICC is finished, AICC_EN bit will clear to 0, and an INT is asserted to the host to indicate AICC_DONE.

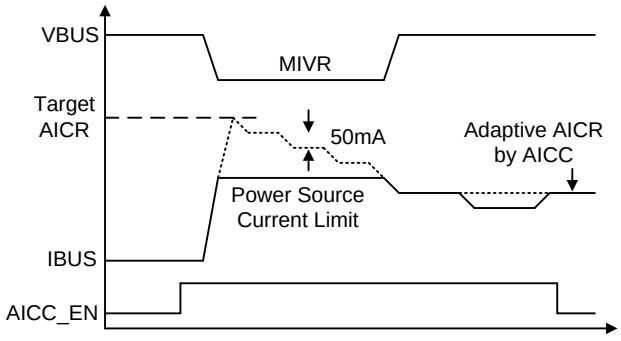


Figure 8. AICC Enable

15.5 Status Outputs

- **Power Good Indicator ($\overline{PG}$ Pin and ST_CHG_RDY Bit)**

  The $\overline{PG}$ pin goes low to indicate a good power source when:

  1. VBUS above $V_{BUS\_MIN\_RISE}$, and I_{BADSRC} is applied.
  2. VBUS above VBAT (not in sleep mode)
  3. VBUS below V_{AC_OVP} threshold setting
  4. HZ = 0 (not in HZ mode)
  5. The charger thermal is under THREG threshold setting
  6. Completed VBUS Source Type Detection

- **Charging Status Indicator (STAT Pin)**

  The device indicates IC_STAT on STAT pin. The STAT pin is an open drain that can be used to drive LED. The STAT pin function can be disable by setting the STAT_EN = 0.

Table 6. STAT Pin State

IC_STAT	STAT Indicator
Trickle, Pre, Fast charge, IEOC-charge (EOC and TE = 0)	Low
Charge done, Back-Ground charge	High
HZ/SLEEP, VBUS ready for charge, OTG	High
Charge fault	Blinking at 1Hz

- **Interrupt to Host ($\overline{INT}$ Pin)**

  The device reports IRQ to host by the $\overline{INT}$ pin, which is an open drain output.

  The $\overline{INT}$ pin generates a pulse low with 256μs when IRQ event occurs. All IRQ events are masked for default setting.

  When a fault occurs, the device pulses an $\overline{INT}$ to the host and keeps IRQ event in register 0x20 to 0x23 until the host reads the IRQ registers. Before the host reads IRQ registers to clean IRQ events, the device will not send any $\overline{INT}$ pulse again unless any new event occurs.

Table 7. STATUS, FLAG and MASK Register Map

Name	STAT	IRQ	MASK
VBUS_GD	Y	Y	Y
CHG_RDY	Y	Y	Y
IEOC	Y	Y	Y
BK_CHG	Y	Y	Y
CHG_DONE	Y	Y	Y
RECHG	N	Y	Y
DETACH	N	Y	Y
BC12_DONE	Y	Y	Y
MIVR	Y	Y	Y
AICR	Y	Y	Y

Name	STAT	IRQ	MASK
CHG_THREG	Y	Y	Y
CHG_BUSUV	Y	Y	Y
CHG_TOUT	Y	Y	Y
CHG_SYSOV	Y	Y	Y
CHG_BATOV	Y	Y	Y
JEITA_HOT	Y	Y	Y
JEITA_WARM	Y	Y	Y
JEITA_COOL	Y	Y	Y
JEITA_COLD	Y	Y	Y
SYS_MIN	Y	Y	Y
SYS_SHORT	N	Y	Y
OTP	Y	Y	Y
VAC_OV	Y	Y	Y
WDT	Y	Y	Y
OTG_CC	Y	Y	Y
OTG_LBP	N	Y	Y
OTG_FAULT	N	Y	Y

15.6 Protections

- **VBUS Overvoltage Protection in Buck Mode**

  If VBUS voltage over V_{AC_OVP} setting (programmable by VAC_OVP bits), the device stops switching immediately and an $\overline{INT}$ pulse is asserted to the host. When VBUS overvoltage, the status ST_VAC_OV = 1 and the IC_STAT = 1000 for charge fault. The device resume to normal operation when VBUS voltage drops below the V_{AC_OVP} threshold.

- **VBUS Overvoltage Protection in Boost Mode**

  When boost mode, VAC_OVP setting is locked at 6.5V even if VAC_OVP threshold is set at 10.5V or 14V. When the output voltage (VBUS) exceeds VAC_OVP threshold, the device stops switching immediately, clear OTG_EN bit to 0 and exit boost mode. The fault (OTG_FAULT) is set to high and an $\overline{INT}$ pulse is asserted to the host to indicate in boost mode. When the output voltage falling $V_{AC\_OVP\_HYS}$ below VAC_OVP threshold, the OTG_EN bit can be set to 1 by the host.

- **IBUS Overload Protection in Boost Mode**

  The device monitors boost output voltage and current to provide VBUS short circuit protection. The device also builds in constant current regulation to allow OTG to adaptive to various types of load. If short circuit is detected on VBUS, the boost will hiccup 7 times. If boost retries are not successful, OTG_EN bit will set to 0 to disable boost mode and INT pulse is asserted to the host to indicate OTG_FAULT.

- **VBUS Soft-Start**

  When the boost function is enabled, the device soft-starts on VBUS to avoid inrush current.

- **VSYS Overvoltage Protection**

  SYSOVP threshold is set at 5.2V. Once VSYS is above SYSOVP level, buck stops switching immediately and an INT pulse is asserted to host to indicate CHG_SYSOV fault. The device provides 30mA current sink on VSYS to bring down the VSYS voltage.

- **VSYS Overcurrent Protection**

  When the system is shorted or overloaded (I_{BAT} > I_{OCP_BATFET}), the device latches off BATFET (forces enter shipping mode) and an INT pulse is asserted to host to indicate SYS_SHORT fault. Exit shipping mode can reset the latch-off condition and turn on BATFET.

- **Battery Overvoltage Protection**

  The BAT_OVP threshold is 4% above the V_{BAT_REG} setting. When battery exceeds overvoltage threshold, the device disables charging immediately and an INT is asserted to the host to indicate CHG_BATOV.

- **Battery Over-Discharge Protection**

  When battery is discharged below $V_{BAT\_DPL\_FALL}$, the BATFET turns off to protect battery over discharged. When VBUS is plugged in, the BAFET turns on to charge battery.

- **Thermal Protection in Buck Mode**

  The device monitors the internal junction temperature to avoid overheat. When in buck mode, the thermal regulation threshold is set at 120°C (programmable by register THREG bits). When junction temperature exceeds thermal regulation threshold, the device decreases the charge current. During thermal regulation, EOC function is disabled, the safety timer's counter clock rate will be half and an INT is asserted to the host indicate CHG_THREG.

  In addition, the device has thermal shutdown to turn off the converter when the IC surface temperature exceeds T_{OTP} (160°C) and an INT is asserted to the host indicate OTP fault. The converter is recovered when the surface temperature is below T_{OTP} (160°C) - T_{OTP_HYS} (30°C).

- **Thermal Protection in Boost Mode**

  The device has thermal shutdown during boost mode. In boost mode, when the IC surface temperature exceeds T_{OTP} (160°C), the OTG_EN bit is set to 0 to disable boost mode and an INT is asserted to the host indicate OTP fault. When the surface temperature is below T_{OTP} (160°C) - T_{OTP_HYS} (30°C), the host can re-enable boost mode by setting OTG_EN bit to 1.

15.7 Communicate Interface

The RT9470G use I^2C compatible interface by 2-wire line (SCL and SDA) to communicate with the host. The SCL and SDA pins are open drain which needs to connect to supply voltage by pull-up resistors. The RT9470G operates as an I^2C slave device with 7-bits address 5BH, supports up to 3.4Mbits conditionally. To start an I^2C communication, beginning with START (S) condition, and then the host sends slave address. This address is 7-bits long followed by an eighth bits which is a data direction bit (R/W). The second bytes is register address. The third bytes contains data to the selected register. End with STOP (P) condition.

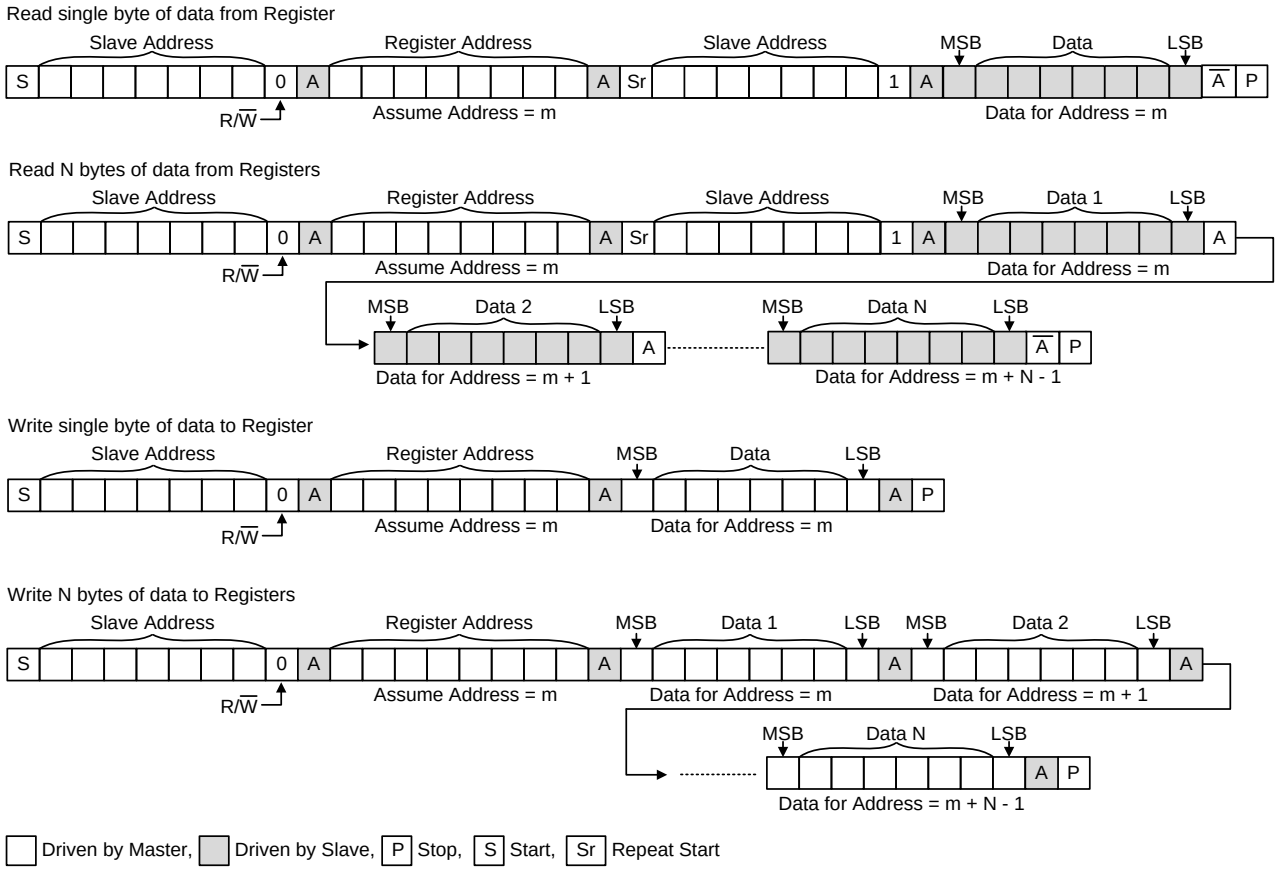


Figure 9. Read and Write Function

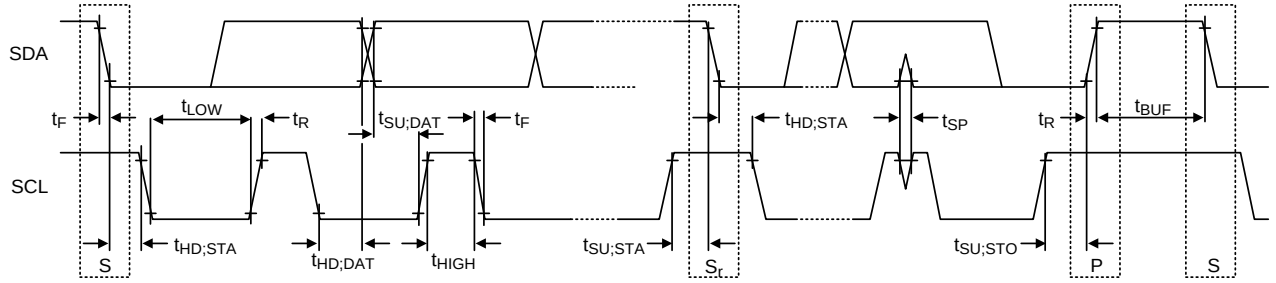


Figure 10. I²C Waveform Information

- **I²C Time-out Reset**

  To avoid I²C hang-ups, a timer runs during I²C activity. If the SDA keep low longer than 1 second, the RT9470G will reset I²C to release SDA goes back to High. The I²C hang-ups reset function can be disable by register 0x01[3] bit.

15.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-30B 2.1x2.5 (BSC) package, the thermal resistance, θ_{JA}, is 29.6°C/W on a standard JEDEC 51-9 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (29.6°C/W) = 3.37W for a WL-CSP-30B 2.1x2.5 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

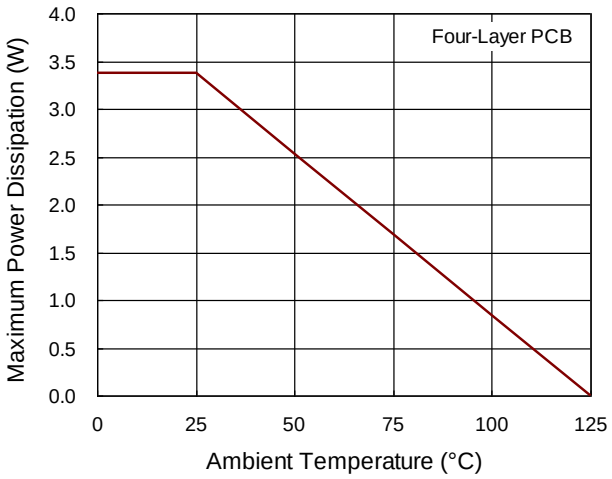


Figure 11. Derating Curve of Maximum Power Dissipation

15.9 Layout Considerations

The RT9470G layout guidelines are shown as below, there are several suggestions provided.

- The capacitor, connected to PMID pin needs to be placed as close as possible to the RT9470G.
- The inductor, connected to SW pin needs to not only router the trace as short as possible to reduce the EMI but also make sure copper area of the trace is enough for the operating current.
- The capacitors, connected to IC pins need to be placed as close as possible to the RT9470G.
- The VBUS needs to router two layers power plane to reduce resistance.
- The SYS needs to router two layers power plane to reduce resistance. Otherwise, the accuracy of ICHG will be affected.

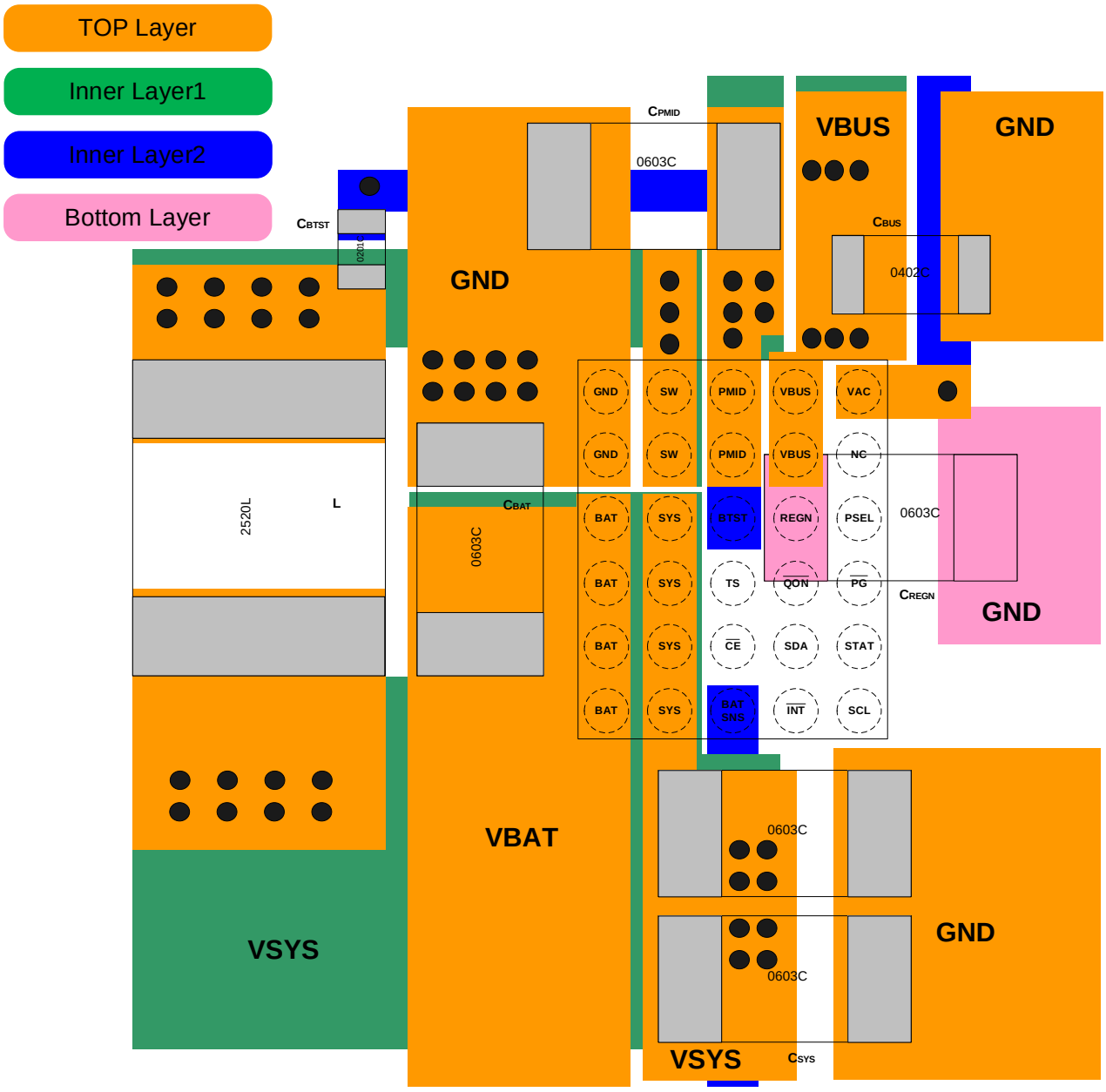


Figure 12. PCB Layout Guide

16 Functional Register Description

I^2C Slave Address: 1011011 (5BH)

R: Read only

R/W: Read and write

RWSC: Read and write, also automatically set/clear by particular condition

Register Address: 0x00, Register Name: OTG_CONFIG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	OTG_CV	10	N	Y	R/W	OTG voltage limit regulation 00: 4.85V 01: 5.0V 10: 5.15V (default) 11: 5.3V
5:2	Reserved	0000	NA	NA	R	Reserved
1	OTG_LBP	0	N	Y	R/W	OTG low battery protection 0: 2.8V (default) 1: 2.5V
0	OTG_CC	1	Y	Y	R/W	OTG current limit regulation 0: 0.5A 1: 1.2A (default)

Register Address: 0x01, Register Name: TOP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	$\overline{QON}$_RST_EN	1	Y	Y	R/W	0: $\overline{QON}$ = 0 for 10s will NOT do anything 1: $\overline{QON}$ = 0 for 10s will turn off BATFET (default)
6	STAT_EN	1	N	Y	R/W	0: STAT pin function disabled 1: STAT pin function enabled (default)
5:4	Reserved	00	NA	NA	R	Reserved
3	DIS_I2C_TO	0	Y	Y	R/W	0: Enable I^2C time-out function (default) 1: Disable I^2C time-out function
2	WDT_CNT_RST	0	Y	Y	RWSC	0: No action 1: Reset watchdog counter (Notice: Back to 0 after watchdog reset)
1:0	WDT	01	Y	Y	R/W	00: Disable watchdog timer reset function 01: 40s (default) 10: 80s 11: 160s

Register Address: 0x02, Register Name: FUNCTION

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	BATFET_DIS	0	N	Y	RWSC	0: Allow BATFET turn on (default) 1: Force BATFET turn off (Notice: Clear by VBUS plug in or $\overline{QON}$ = 0 for 1s, auto set BATFET_DIS = 1 by system overload from BAT to SYS)
6	BATFET_DIS_DLY	1	N	Y	R/W	0: BATFET turn off immediately while BATFET_DIS = 0 1: BATFET turn off with 12s delay while BATFET_DIS = 1 (default)
5	HZ	0	Y	Y	RWSC	0: Normal mode (default) 1: HZ mode (Notice: Clear by VBUS plug in)
4	Reserved	0	NA	NA	R	Reserved
3	BUCK_PFM_DIS	0	N	Y	R/W	0: Enable PFM (default) 1: Disable PFM
2	UUG_FULLON	0	N	Y	R/W	0: Q1 turn on by condition (default) 1: Force Q1 full on
1	OTG_EN	0	Y	Y	RWSC	0: Disable OTG (default) 1: Enable OTG (Notice: Clear by HZ = 1 or $\overline{OTP}$ or OTG_LBP or VBUS_OV or $\overline{QON}$ reset or BATFET_DIS = 1 or auto 7 times hiccup for soft-start fail or overload)
0	CHG_EN	1	Y	Y	R/W	0: Disable charge 1: Enable charge (default)

Register Address: 0x03, Register Name: IBUS

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	AICC_EN	0	Y	Y	RWSC	0: Disable AICC function (default) 1: Enable AICC function (Notice: Auto clear after AICC function done)
6	AUTO_AICR	1	Y	Y	R/W	0: No action 1: Auto set IAICR by BC1.2 done or PSEL change (default)
5:0	IAICR	001010	N	Y	RWSC	Average input current regulation 000000: 50mA 000001: 50mA 000010: 100mA … 001010: 500mA (default) … 111101: 3050mA 111110: 3100mA 111111: 3200mA (Notice: Auto set by BC1.2 done or PSEL change if AUTO_AICR = 1)

Register Address: 0x04, Register Name: VBUS

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	VAC_OVP	01	N	Y	R/W	VAC OVP threshold 00: 5.8V 01: 6.5V (default) 10: 10.9V (6.5V while OTG) 11: 14V (6.5V while OTG)
5:4	VMIVR_BAT_TRACK	00	N	Y	R/W	00: VMIVR by 0x04[3:0] (default) 01: VMIVR = VBAT + 200mV 10: VMIVR = VBAT + 250mV 11: VMIVR = VBAT + 300mV
3:0	VMIVR	0110	N	Y	R/W	Minimum input voltage regulation 0000: 3900mV 0001: 4000mV … 0110: 4500mV (default) ... 1110: 5300mV 1111: 5400mV

Register Address: 0x05, Register Name: PRECHG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	R	Reserved
6:4	VPRE_CHG	100	Y	Y	R/W	Pre-charge voltage threshold 000: 2700mV 001: 2800mV 010: 2900mV 011: 3000mV 100: 3100mV (default) 101: 3200mV 110: 3300mV 111: 3400mV
3:0	IPRE_CHG	0010	Y	Y	R/W	Pre-charge current 0000: 50mA 0001: 100mA 0010: 150mA (default) ... 1110: 750mA 1111: 800mA

Register Address: 0x06, Register Name: REGU

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	R	Reserved
6	THREG	1	Y	Y	R/W	Junction thermal regulation threshold 0: 100°C 1: 120°C (default)
5:4	Reserved	00	NA	NA	R	Reserved
3:0	VSYS_MIN	1001	N	Y	R/W	System minimum voltage 0000: 2600mV 0001: 2700mV … 1001: 3500mV (default) ... 1110: 4000mV 1111: 4100mV

Register Address: 0x07, Register Name: VCHG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VRE_CHG	0	Y	Y	R/W	Re-charge voltage threshold 0: 100mV (default) 1: 200mV
6:0	VBAT_REG	0011110	Y	Y	R/W	Charge voltage 0000000: 3900mV 0000001: 3910mV … 0011110: 4200mV (default) … 1010000: 4700mV 1010000 to 1111111: 4700mV

Register Address: 0x08, Register Name: ICHG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	Reserved	00	NA	NA	R	Reserved
5:0	ICHG_REG	101000	Y	Y	R/W	Charge current 000000: 0mA (disable charge) 000001: 50mA 000010: 100mA 000011: 150mA … 101000: 2000mA (default) … 111101: 3100mA 111111: 3150mA

Register Address: 0x09, Register Name: CHG_TIMER

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_SAFE_TMR_EN	1	Y	Y	R/W	0: Disable charge safe timer 1: Enable charge safe timer (default)
6	CHG_SAFE_TMR_2XT	1	Y	Y	R/W	Double charge safe timer during MIVR, AICR, thermal regulation, and JEITA reduce ICHG 0: Disable 2x extended charge safe timer 1: Enable 2x extended charge safe timer (default)
5:4	CHG_SAFE_TMR	01	Y	Y	R/W	Charge safe timer 00: 5hr 01: 10hr (default) 10: 15hr 11: 20hr
3:0	Reserved	0000	NA	NA	R	Reserved

Register Address: 0x0A, Register Name: EOC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	IEOC_CHG	0011	Y	Y	R/W	End-of-charge current threshold 0000: 50mA 0001: 100mA 0010: 150mA 0011: 200mA (default) ... 1110: 750mA 1111: 800mA
3:2	BG_CHG_TMR	00	Y	Y	R/W	EOC back-ground charge timer 00: 0min (default) 01: 15min 10: 30min 11: 45min
1	TE	1	Y	Y	R/W	0: Disable charge current termination 1: Enable charge current termination (default)
0	EOC_RST	0	Y	Y	RWSC	0: No action 1: Reset EOC (Notice: Back to 0 after reset EOC done)

Register Address: 0x0B, Register Name: INFO

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	REG_RST	0	NA	NA	RWSC	0: No action 1: Reset register (Notice: Back to 0 after register reset)
6:3	DEVICE_ID	1001	NA	NA	R	1001: RT9470G (PSEL, PGB)
2:0	DEVICE_RE	NA	NA	NA	R	Revision

Register Address: 0x0C, Register Name: JEITA

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	JEITA_EN	1	Y	Y	R/W	0: JEITA disable 1: JEITA enable (default)
6	JEITA_COLD	0	Y	Y	R/W	0: COLD do NOT charging/OTG (default) 1: COLD still charging/OTG
5	JEITA_COOL_ISET	1	Y	Y	R/W	0: 50% of I_{CHG} 1: 25% of I_{CHG} (default)
4	JEITA_COOL_VSET	1	Y	Y	R/W	0: V_{BAT_REG} = 4.1V 1: V_{BAT_REG} = Register setting (default)
3	JEITA_WARM_ISET	1	Y	Y	R/W	0: 50% of I_{CHG} 1: I_{CHG} = Register setting (default)
2	JEITA_WARM_VSET	0	Y	Y	R/W	0: V_{BAT_REG} = 4.1V (default) 1: V_{BAT_REG} = Register setting
1	JEITA_HOT	0	Y	Y	R/W	0: HOT do NOT charging/OTG (default) 1: HOT still charging/OTG
0	Reserved	0	NA	NA	R	Reserved

Register Address: 0x0D, Register Name: PUMP_EXP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	PE_EN	0	Y	Y	RWSC	0: Idle (default) 1: Trigger MTK Pump Express process (Notice: Auto clear while PE done or no VBUS)
6	PE_SEL	0	Y	Y	R/W	0: PE 1.0 process select (default) 1: PE 2.0 process select
5	PE10_INC	0	Y	Y	R/W	0: PE 1.0 voltage down (default) 1: PE 1.0 voltage up
4:0	PE20_CODE	00000	Y	Y	R/W	MTK PE 2.0 voltage request setting 00000: 5.5V (default) 00001: 6V … 11101: 20V 11110: Adapter healthy self-testing 11111: Disable cable drop compensation

Register Address: 0x0E, Register Name: DPDM_DET

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	BC12_EN	1	Y	Y	R/W	0: Disable BC1.2 detection 1: Enable BC1.2 detection while VBUS > 3.8V (default) (Notice: For RT9470D only)
6:5	DCDT_SEL	01	Y	Y	R/W	00: Disable DCD timeout function 01: Enable 300ms DCD timeout function (default) 10: Enable 600ms DCD timeout function 11: Wait data contact
4	SPEC_TA_EN	1	Y	Y	R/W	0: Disable Samsung/Apple TA detection 1: Enable Samsung/Apple TA detection (default)
3:1	Reserved	000	NA	NA	R	Reserved
0	DCP_DP_OPT	0	Y	Y	R/W	DCP DP behavior option 0: DP = 0V after BC 1.2 done (default) 1: DP keep 0.6V while DCP port detected

Register Address: 0x0F, Register Name: IC_STATUS

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	PORT_STAT	0000	NA	NA	R	0000: No information 0001 to 0111: Reserved 1000: VBUS = device 1 (2100mA-APPLE-10w) 1001: VBUS = device 2 (2000mA-SAMSUNG-10w) 1010: VBUS = device 3 (1000mA-APPLE-5w) 1011: VBUS = device 4 (2400mA-APPLE-12w) 1100: VBUS = unknown/NSDP (500mA) 1101: VBUS = SDP (500mA)/PSEL = High 1110: VBUS = CDP (1500mA) 1111: VBUS = DCP (2400mA)/PSEL = Low
3:0	IC_STAT	0000	NA	NA	R	0000: HZ/SLEEP 0001: VBUS ready for charge 0010: Trickle-charge 0011: Pre-charge 0100: Fast-charge 0101: IEOC-charge (EOC and TE = 0) 0110: Back-Ground charge (EOC and TE = 1 and before turn off power path) 0111: Charge done (EOC and TE = 1 and power path off) 1000: Charge fault (VAC_OV/CHG_BUSUV/CHG_TOUT/CHG_SYSOV/CHG_BATOV/JEITA_HOT/JEITA_COLD/OTP) 1001 to 1110: Reserved 1111: OTG

Register Address: 0x10, Register Name: STAT0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ST_VBUS_GD	0	NA	NA	R	0: VBUS is not good 1: VBUS is good (Notice: After current capability of the input source detection, and HZ = 0, VAC_OV = 0, VBUS > 3.8V)
6	ST_CHG_RDY	0	NA	NA	R	0: VBUS is not ready for charging 1: VBUS is ready for charging (Notice: After port detection, and HZ = 0, VAC_OV = 0, VBUS > 3.8V)
5	ST_IEOC	0	NA	NA	R	0: Not in EOC state 1: While in EOC state (Notice: Charge current < IEOC level)
4	ST_BG_CHG	0	NA	NA	R	0: Not in EOC state or TE = 0 or BG_CHG_TMR = 00 1: While in EOC state and TE = 1 and BG_CHG_TMR ≠ 00
3	ST_CHG_DONE	0	NA	NA	R	0: Not in EOC state or BATFET on 1: While in EOC state and BATFET off
2:1	Reserved	00	NA	NA	R	Reserved
0	ST_BC12_DONE	0	NA	NA	R	0: BC1.2 process not ready 1: While BC1.2 process done

Register Address: 0x11, Register Name: STAT1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ST_CHG_MIVR	0	NA	NA	R	0: Not in MIVR loop 1: While in MIVR loop
6	ST_CHG_AICR	0	NA	NA	R	0: Not in AICR loop 1: While in AICR loop
5	ST_CHG_THREG	0	NA	NA	R	0: Not in THERMAL loop 1: While in THERMAL loop
4	ST_CHG_BUSUV	0	NA	NA	R	0: Not VBAT < VBUS < 3.8V 1: While VBAT < VBUS < 3.8V
3	ST_CHG_TOUT	0	NA	NA	R	0: Not in charge safety time-out 1: While in charge safety time-out
2	ST_CHG_SYSOV	0	NA	NA	R	0: Not in SYS OV 1: While in SYS OV
1	ST_CHG_BATOV	0	NA	NA	R	0: Not in BAT OV 1: While in BAT OV
0	Reserved	0	NA	NA	R	Reserved

Register Address: 0x12, Register Name: STAT2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ST_JEITA_HOT	0	NA	NA	R	0: Not in BAT is hot 1: While in BAT is hot
6	ST_JEITA_WARM	0	NA	NA	R	0: Not in BAT is warm 1: While in BAT is warm
5	ST_JEITA_COOL	0	NA	NA	R	0: Not in BAT is cool 1: While in BAT is cool
4	ST_JEITA_COLD	0	NA	NA	R	0: Not in BAT is cold 1: While in BAT is cold
3:2	Reserved	00	NA	NA	R	Reserved
1	ST_SYS_MIN	0	NA	NA	R	0: Not in VBAT < VSYS_MIN 1: While in VBAT < VSYS_MIN
0	Reserved	0	NA	NA	R	Reserved

Register Address: 0x13, Register Name: STAT3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ST_OTP	0	NA	NA	R	0: Not OTP 1: OTP
6	ST_VAC_OV	0	NA	NA	R	0: Not VAC_OV 1: VAC_OV (charge or OTG mode)
5	ST_WDT	0	NA	NA	R	0: WDT is counting 1: WDT reset will occur after 500ms
4:3	Reserved	00	NA	NA	R	Reserved
2	ST_OTG_CC	0	NA	NA	R	0: Not in OTG_CC 1: While in OTG_CC
1:0	Reserved	00	NA	NA	R	Reserved

Register Address: 0x20, Register Name: IRQ0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	FL_VBUS_GD	0	NA	NA	R	0: ST_VBUS_GD not rising 1: While ST_VBUS_GD rising, read clear
6	FL_CHG_RDY	0	NA	NA	R	0: ST_CHG_RDY not rising 1: While ST_CHG_RDY rising, read clear
5	FL_IEOC	0	NA	NA	R	0: ST_IEOC not rising 1: While ST_IEOC rising, read clear
4	FL_BG_CHG	0	NA	NA	R	0: ST_BG_CHG not rising 1: While ST_BG_CHG rising, read clear
3	FL_CHG_ DONE	0	NA	NA	R	0: ST_CHG_DONE not rising 1: While ST_CHG_DONE rising, read clear
2	FL_RECHG	0	NA	NA	R	0: While VBAT > VRECHG after EOC 1: While VBAT < VRECHG after EOC, read clear
1	FL_DETACH	0	NA	NA	R	0: ST_VBUS_GD not rising or in ST_VBUS_GD 1: While ST_VBUS_GD falling then VBUS < VBAT or VBUS < 3.3V, read clear
0	FL_BC12_ DONE	0	NA	NA	R	0: BC1.2 process not ready 1: While BC1.2 process done

Register Address: 0x21, Register Name: IRQ1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	FL_CHG_ MIVR	0	NA	NA	R	0: ST_CHG_MIVR not rising 1: While ST_CHG_MIVR rising, read clear
6	FL_CHG_ AICR	0	NA	NA	R	0: ST_CHG_AICR not rising 1: While ST_CHG_AICR rising, read clear
5	FL_CHG_ THREG	0	NA	NA	R	0: ST_CHG_THREG not rising 1: While ST_CHG_THREG rising, read clear
4	FL_CHG_ BUSUV	0	NA	NA	R	0: ST_CHG_BUSUV not rising 1: While ST_CHG_BUSUV rising, read clear
3	FL_CHG_ TOUT	0	NA	NA	R	0: ST_CHG_TOUT not rising 1: While ST_CHG_TOUT rising, read clear
2	FL_CHG_ SYSOV	0	NA	NA	R	0: ST_CHG_SYSOV not rising 1: While ST_CHG_SYSOV rising, read clear
1	FL_CHG_ BATOV	0	NA	NA	R	0: ST_CHG_BATOV not rising 1: While ST_CHG_BATOV rising, read clear
0	Reserved	0	NA	NA	R	Reserved

Register Address: 0x22, Register Name: IRQ2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	FL_JEITA_HOT	0	NA	NA	R	0: ST_JEITA_HOT not rising 1: While ST_JEITA_HOT rising, read clear
6	FL_JEITA_WARM	0	NA	NA	R	0: ST_JEITA_WARM not rising 1: While ST_JEITA_WARM rising, read clear
5	FL_JEITA_COOL	0	NA	NA	R	0: ST_JEITA_COOL not rising 1: While ST_JEITA_COOL rising, read clear
4	FL_JEITA_COLD	0	NA	NA	R	0: ST_JEITA_COLD not rising 1: While ST_JEITA_COLD rising, read clear
3	FL_PE_DONE	0	NA	NA	R	0: FL_PE_DONE not rising 1: While PE processing done, read clear
2	FL_AICC_DONE	0	NA	NA	R	0: FL_AICC_DONE not rising 1: While AICC processing done, read clear
1	FL_SYS_MIN	0	NA	NA	R	0: ST_SYS_MIN not rising 1: While ST_SYS_MIN rising, read clear
0	FL_SYS_SHORT	0	NA	NA	R	0: ST_SYS_SHORT not rising 1: While ST_SYS_SHORT rising, read clear

Register Address: 0x23, Register Name: IRQ3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	FL_OTP	0	NA	NA	R	0: ST_OTP not rising 1: While ST_OTP rising, read clear
6	FL_VAC_OV	0	NA	NA	R	0: ST_VAC_OV not rising 1: While ST_VAC_OV rising, read clear
5	FL_WDT	0	NA	NA	R	0: ST_WDT not rising 1: While ST_WDT rising, read clear
4:3	Reserved	00	NA	NA	R	Reserved
2	FL_OTG_CC	0	NA	NA	R	0: ST_OTG_CC not rising 1: While ST_OTG_CC rising, read clear
1	FL_OTG_LBP	0	NA	NA	R	0: ST_OTG_LBP not rising 1: While ST_OTG_LBP rising, read clear
0	FL_OTG_FAULT	0	NA	NA	R	0: ST_OTG_FAULT not rising 1: While ST_OTG_FAULT rising, read clear

Register Address: 0x30, Register Name: MASK0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	MK_VBUS_GD	1	N	Y	R/W	0: Not mask IRQ of FL_VBUS_GD 1: Mask IRQ of FL_VBUS_GD (default)
6	MK_CHG_RDY	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_RDY 1: Mask IRQ of FL_CHG_RDY (default)
5	MK_IEOC	1	N	Y	R/W	0: Not mask IRQ of FL_IEOC 1: Mask IRQ of FL_IEOC (default)
4	MK_BG_CHG	1	N	Y	R/W	0: Not mask IRQ of MK_BG_CHG 1: Mask IRQ of MK_BG_CHG (default)
3	MK_CHG_DONE	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_DONE 1: Mask IRQ of FL_CHG_DONE (default)
2	MK_RECHG	1	N	Y	R/W	0: Not mask IRQ of FL_RECHG 1: Mask IRQ of FL_RECHG (default)
1	MK_DETACH	1	N	Y	R/W	0: Not mask IRQ of FL_DETACH 1: Mask IRQ of FL_DETACH (default)
0	MK_BC12_DONE	1	N	Y	R/W	0: Not mask IRQ of FL_BC12_DONE 1: Mask IRQ of FL_BC12_DONE (default)

Register Address: 0x31, Register Name: MASK1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	MK_CHG_MIVR	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_MIVR 1: Mask IRQ of FL_CHG_MIVR (default)
6	MK_CHG_AICR	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_AICR 1: Mask IRQ of FL_CHG_AICR (default)
5	MK_CHG_THREG	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_THREG 1: Mask IRQ of FL_CHG_THREG (default)
4	MK_CHG_BUSUV	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_BUSUV 1: Mask IRQ of FL_CHG_BUSUV (default)
3	MK_CHG_TOUT	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_TOUT 1: Mask IRQ of FL_CHG_TOUT (default)
2	MK_CHG_SYSOV	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_SYSOV 1: Mask IRQ of FL_CHG_SYSOV (default)
1	MK_CHG_BATOV	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_BATOV 1: Mask IRQ of FL_CHG_BATOV (default)
0	Reserved	1	NA	NA	R	Reserved

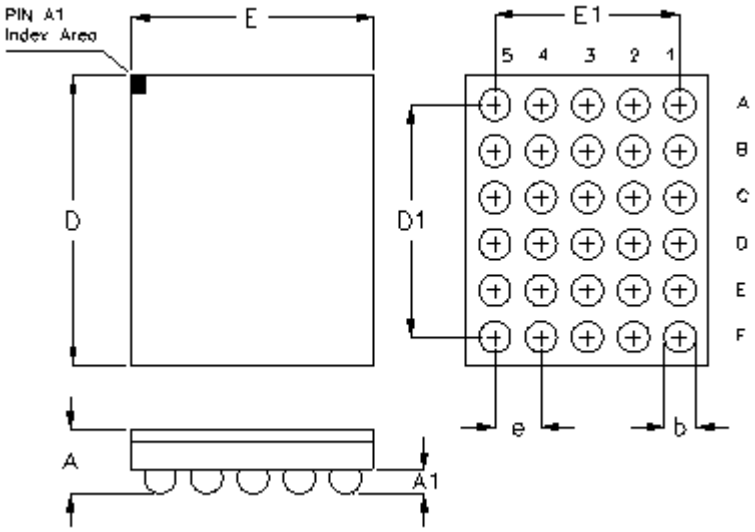
Register Address: 0x32, Register Name: MASK2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	MK_JEITA_HOT	1	N	Y	R/W	0: Not mask IRQ of FL_JEITA_HOT 1: Mask IRQ of FL_JEITA_HOT (default)
6	MK_JEITA_WARM	1	N	Y	R/W	0: Not mask IRQ of FL_JEITA_WARM 1: Mask IRQ of FL_JEITA_WARM (default)
5	MK_JEITA_COOL	1	N	Y	R/W	0: Not mask IRQ of FL_JEITA_COOL 1: Mask IRQ of FL_JEITA_COOL (default)
4	MK_JEITA_COLD	1	N	Y	R/W	0: Not mask IRQ of FL_JEITA_COLD 1: Mask IRQ of FL_JEITA_COLD (default)
3	MK_PE_DONE	1	N	Y	R/W	0: Not mask IRQ of FL_PE_DONE 1: Mask IRQ of FL_PE_DONE (default)
2	MK_AICC_DONE	1	N	Y	R/W	0: Not mask IRQ of FL_AICC_DONE 1: Mask IRQ of FL_AICC_DONE (default)
1	MK_SYS_MIN	1	N	Y	R/W	0: Not mask IRQ of FL_SYS_MIN 1: Mask IRQ of FL_SYS_MIN (default)
0	MK_SYS_SHORT	1	N	Y	R/W	0: Not mask IRQ of FL_SYS_SHORT 1: Mask IRQ of FL_SYS_SHORT (default)

Register Address: 0x33, Register Name: IRQ3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	MK_OTP	1	N	Y	R/W	0: Not mask IRQ of FL_OTP 1: Mask IRQ of FL_OTP (default)
6	MK_VAC_OV	1	N	Y	R/W	0: Not mask IRQ of FL_VAC_OV 1: Mask IRQ of FL_VAC_OV (default)
5	MK_WDT	1	N	Y	R/W	0: Not mask IRQ of FL_WDT 1: Mask IRQ of FL_WDT (default)
4:3	Reserved	11	NA	NA	R	Reserved
2	MK_OTG_CC	1	N	Y	R/W	0: Not mask IRQ of FL_OTG_CC 1: Mask IRQ of FL_OTG_CC (default)
1	MK_OTG_LBP	1	N	Y	R/W	0: Not mask IRQ of FL_OTG_LBP 1: Mask IRQ of FL_OTG_LBP (default)
0	MK_OTG_FAULT	1	N	Y	R/W	0: Not mask IRQ of FL_OTG_FAULT 1: Mask IRQ of FL_OTG_FAULT (default)

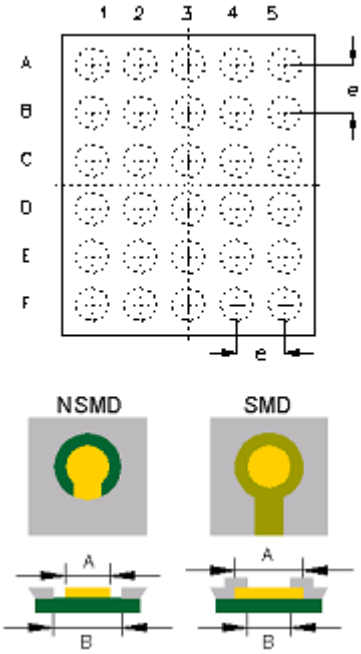
17 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.460	2.540	0.097	0.100
D1	2.000		0.079	0.000
E	2.060	2.140	0.081	0.084
E1	1.600		0.063	0.000
e	0.400		0.016	

30B WL-CSP 2.1x2.5 Package (BSC)

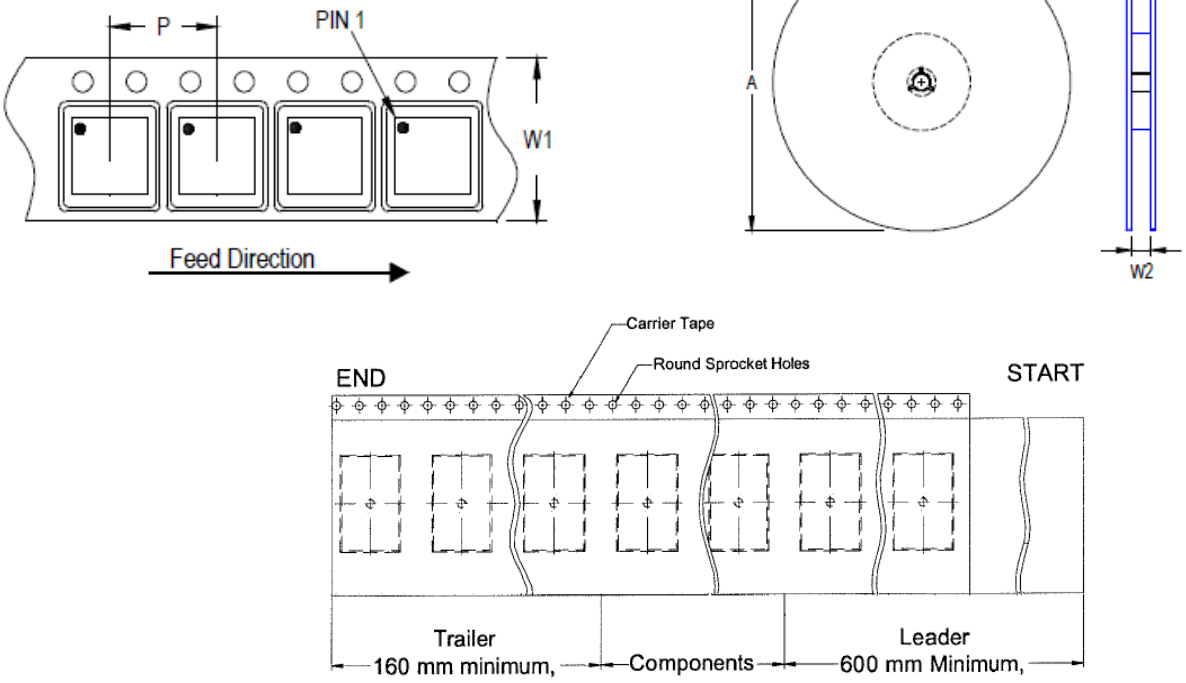
18 Footprint Information



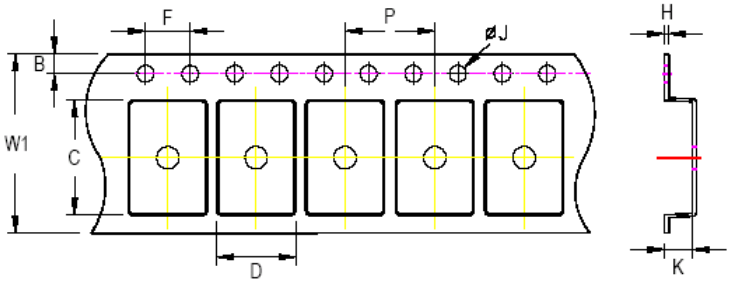
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.1x2.5-30(BSC)	30	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 2.1x2.5	8	4	180	7	3,000	160	600	8.4/9.9



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
WL-CSP 2.1x2.5	7”	3,000	Box A	18.3*18.3*8.0	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	1	3,000	For Combined or Partial Reel.			

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
00T00	2023/11/23	Final	Marking Information on P2