RICHTEK®

RT9125H

50W Stereo, Inductor-Less Digital Audio, Closed-Loop System with 96kHz Extended Audio Processing

1 General Description

The RT9125H is a high-efficiency, I^2S-input, stereo channel audio power amplifier delivering 2x50W into 4Ω BTL (Bridge Tied Load) speaker loads. It can deliver over 94% power efficiency and eliminate the need for heat-sink.

Built-in protection circuits provide over-temperature, overcurrent, overvoltage, DC, and undervoltage protections and report error status.

The RT9125H is an I^2S device receiving all clocks from external sources. A fully programmable data path routes these channels to the internal speaker drivers.

The RT9125H features three band DRC (Dynamic Range Compression) and flexible multi-band biquads for anti-clipping, power limiting, and speaker equalization.

The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT9125H□-□□□□

- **Packing**
  B: Standard
- **Trim Code**
- **Package Type**(1)
  E: RLQFP-64L 10x10 (PP)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

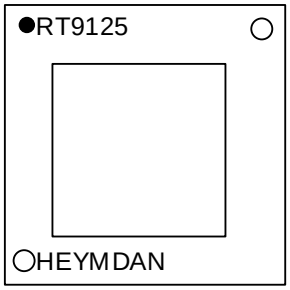
3 Features

- **Flexible Power Supply Range**
  - **PVDD from 4.5V to 26.4V**
  - **DVDD and I/O: 1.8V or 3.3V**
- **Support Wide Range Audio Format**
  - **Bit Resolution up to 32 Bits**
  - **Support TDM (Time-Division Multiplexing) up to 32 Bits**
  - **Sampling Frequency from 8kHz to 96kHz**
- **Excellent Audio Performance**
  - **1x100W PBTL Mode at 2Ω at 23V, THD+N = 1%**
  - **2x50W BTL Mode at 4Ω at 23V, THD+N = 1%**
  - **SNR ≥ 110dB**
  - **Efficiency ≥ 94%**
- **Built-In Programmable DSP (Digital Signal Processor) Function**
  - **36 Programmable Biquads for Speaker Equalization**
  - **Programmable Coefficients for DRC Filters and Supporting Multi-Compression Ratios**
  - **Programmable 128-Tap FIR**
- **Excellent Self-Protection**
  - **UVLO, OVP, OCP, Thermal Foldback, OTP and DCP**
  - **Built-In DC Blocking Filters**
- **Filter-Less Application**
- **64 Pin LQFP Package with the Exposed Thermal Pad**

4 Applications

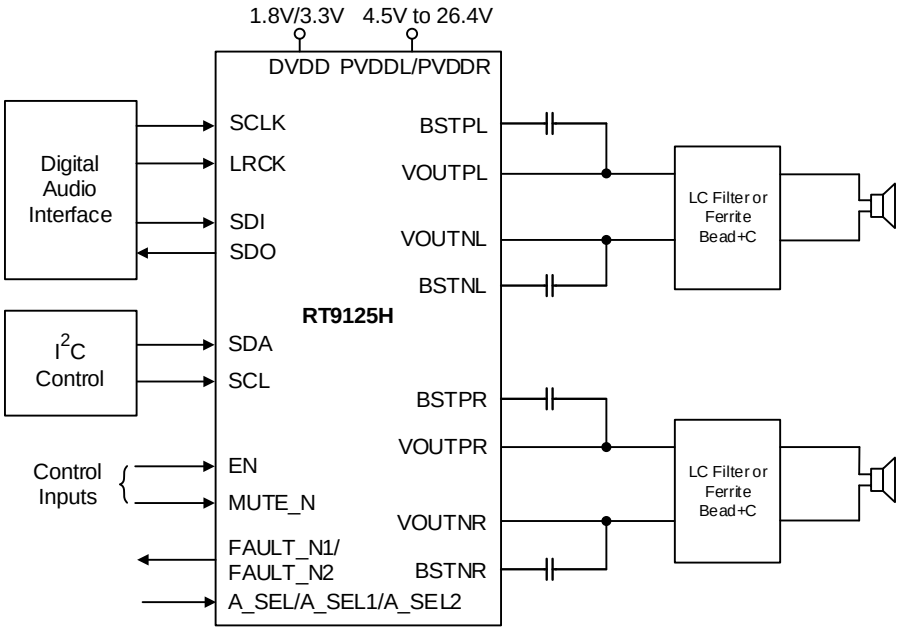
- Bluetooth and WiFi Speakers
- Subwoofers
- Bookshelf Stereo Systems
- Professional And Public Address (PA) Speakers
- Active Crossover and Two-Way Speakers

5 Marking Information



RT9125HE: Product Code
YMDAN: Date Code

6 Simplified Application Circuit



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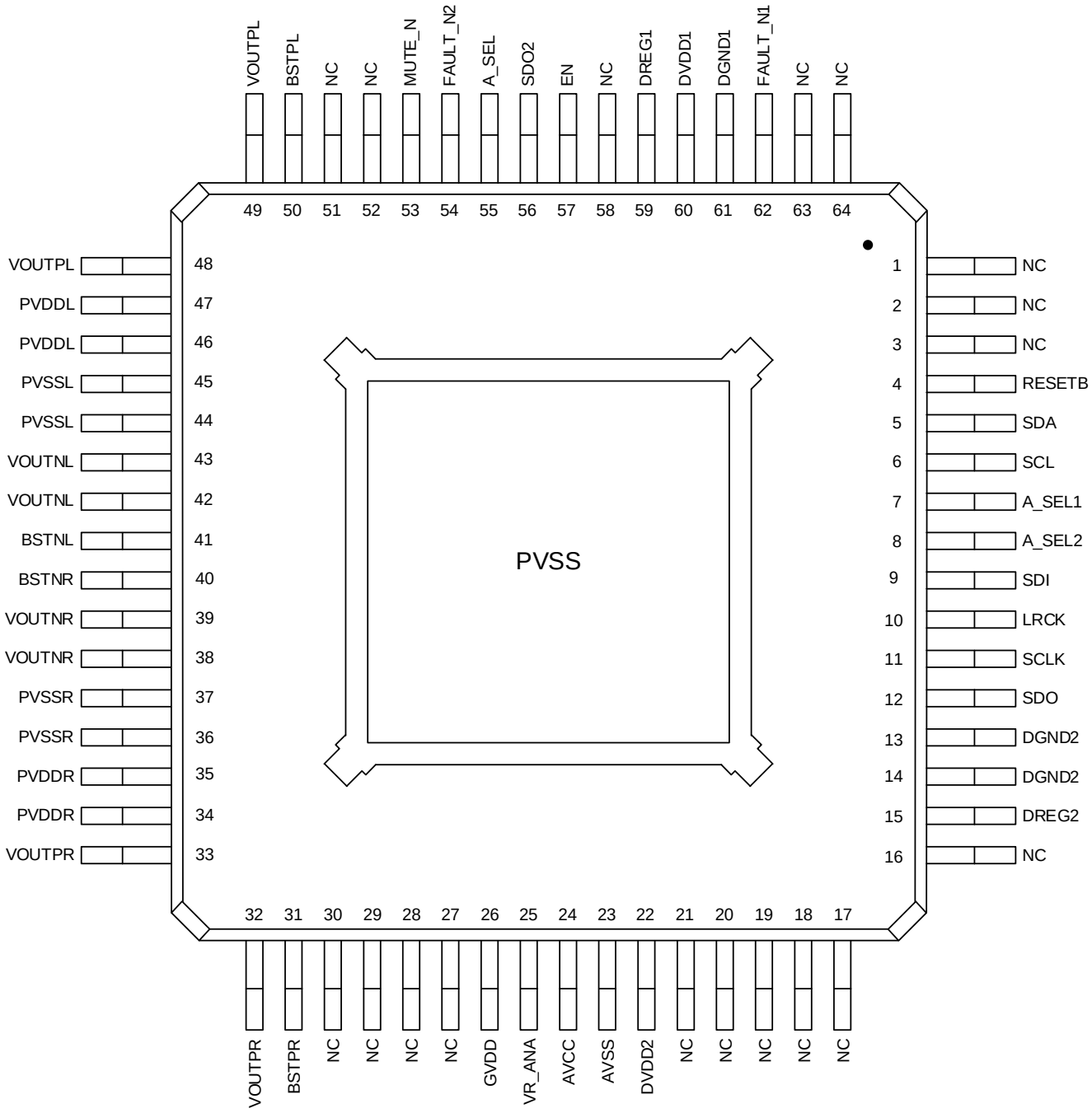
7 Pin Configuration

(TOP VIEW)



RLQFP-64L 10x10 (PP)

8 Functional Pin Description

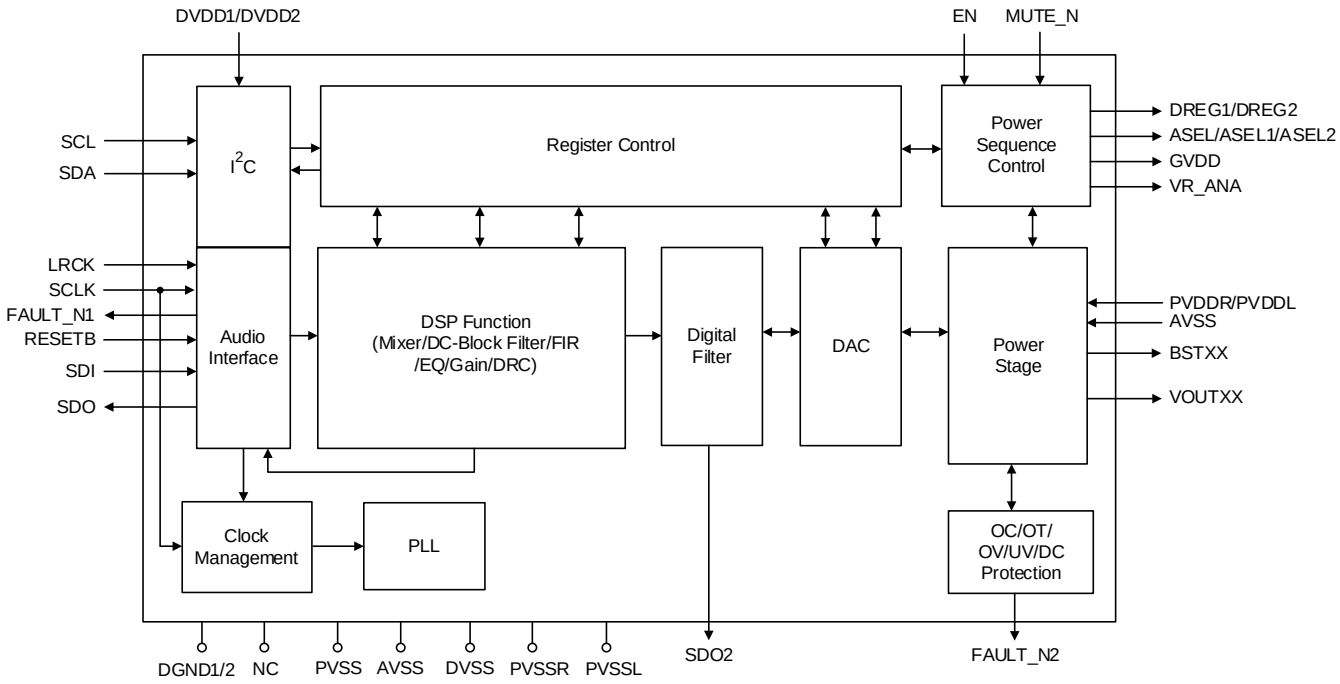
Pin No.	Pin Name	IO	Pin Function
1, 16, 17, 18, 19, 20, 21, 27, 28, 29, 30, 51, 52, 58, 62, 63, 64	NC	P	Tied to main GND.
2, 3	NC	P	Test pin, floating
4	RESETB	DI	RESET, low active.
5	SDA	DIO	I^2C data input/output.
6	SCL	DI	I^2C clock input.
7	A_SEL1	DI	Slave address selection 1.
8	A_SEL2	DI	Slave address selection 2.
9	SDI	DI	I^2S data input.
10	LRCK	DI	I^2S L/R clock input.
11	SCLK	DI	I^2S bit clock input.
12	SDO	DO	I^2S data output for DSP.
13, 14	DGND2	P	Digital GND.
15	DREG2	P	1.8V LDO output
22	DVDD2	P	1.8V or 3.3V power supply for I/O. Connect to DVDD1.
23	AVSS	P	Ground for analog circuits.
24	AVCC	P	26.4V power supply for analog circuits.
25	VR_ANA	P	Analog reference voltage. The typical current is about 11.6mA, and maximum current is about 12mA.
26	GVDD	P	Internal power supply generated by LDO. The typical current is about 4.2mA, and the maximum current is about 5mA.
31	BSTPR	P	Bootstrap supply for VOUTPR.
32, 33	VOUTPR	AO	Positive output of RCH.
34, 35	PVDDR	P	26.4V power supply for RCH.
36, 37	PVSSR	P	Power GND, tied to PVSS.
38, 39	VOUTNR	AO	Negative output of RCH.
40	BSTNR	P	Bootstrap supply of VOUTNR.
41	BSTNL	P	Bootstrap supply of VOUTNL.
42, 43	VOUTNL	AO	Negative output of LCH.
44, 45	PVSSL	P	Power GND, tied to PVSS.
46, 47	PVDDL	P	26.4V power supply for LCH.
48, 49	VOUTPL	AO	Positive output of LCH.
50	BSTPL	P	Bootstrap supply for VOUTPL.
53	MUTE_N	DI	Mute pin, low active.
54	FAULT_N2	DO	Fault indication for AMP portion.
55	A_SEL	DI	Slave address for analog AMP

Pin No.	Pin Name	IO	Pin Function
56	SDO2	DO	I^2S data output for AMP portion.
57	EN	DI	RESET function, low active.
59	DREG1	P	1.2V LDO output.
60	DVDD1	P	1.8V or 3.3V power supply for DSP portion and I/O. Connect to DVDD2.
61	DGND1	P	Digital GND.
62	FAULT_N1	DO	Fault indication for DSP portion.
65 (Exposed Pad)	PVSS	P	Ground.

8.1 IO Type Definition

- P: Power Pin
- DI: Digital Input Pin
- DO: Digital Output Pin
- DIO: Digital Input and Output Pin
- AO: Analog Output Pin

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, AVCC, PVDDL, PVDDR ---------- –0.3V to 31.6V
- Supply Voltage, DVDD1, DVDD2 ---------- –0.3V to 6V
- Speaker Amplifier Output Voltage, VOUTPR, VOUTNR, VOUTNL, VOUTPL ---------- –0.3V to 31V
- BSTPR, BSTNR, BSTNL, BSTPL (Note 3) ---------- –0.3V to 36V
- RESETB, SDA, SCL, FAULT_N2, FAULT_N1 ---------- –0.3V to 6V
- A_SEL1, A_SEL2, A_SEL, LRCK, SCLK, SDI, MUTE_N, EN ---------- –0.3V to DVDD + 0.5V
- VOUTPR, VOUTNR, VOUTPL, VOUTNL (Note 4) ---------- –10V to 37V
- SDO, SDO2 ---------- –0.3V to 6V
- DREG2 ---------- –0.3V to 4V
- VR_ANA, GVDD ---------- –0.3V to 6V
- DREG1 ---------- –0.3V to 1.7V
- Power Dissipation, P_D @ T_A = 25°C

  RLQFP-64L 10x10 (PP) ---------- 2.26W
- Package Thermal Resistance (Note 5)
- RLQFP-64L 10x10 (PP), θ_{JA} ---------- 55.24°C/W
- RLQFP-64L 10x10 (PP), $\theta_{JC(Top)}$ ---------- 0.37°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 6)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. The result is defined when the cross voltage between BST and VOUT is 5V.

Note 4. The switching terminal should be used within AC peak limits. Overshoot and undershoot must be less than 100ns.

Note 5. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at case top of the package. Refer to the EVB user guide for thermal information, which includes the heat sink.

Note 6. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 7)

- Supply Input Voltage, DVDD1 DVDD2 ---------- 3V to 3.6V
- Supply Input Voltage (For 1.8V I/O), DVDD1, DVDD2, DREG2 (Note 8) ---------- 1.74V to 1.98V
- Supply Input Voltage, PVDDL, PVDDR, AVCC ---------- 4.5V to 26.4V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 150°C

Note 7. The device is not guaranteed to function outside its operating conditions.

Note 8. In 1.8 V I/O application, 1.8 V is needed to be supplied from an external voltage source to DVDD1, DVDD2 and VREG2.

12 Electrical Characteristics

(PVDDL = PVDDR = AVCC = 12.7V, DVDD = 3.3V, R_L = 6Ω, T_A = 25°C, f_{SW} = 384kHz, L = 8.2μH, C = 0.47μF, unless otherwise specified.) (Note 9)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
EN, RESETB, MUTE_N	VIH: High-Level Input Voltage	V_{IH}			DVDD x 0.7	--	--	V
	VIL: Low-Level Input Voltage	V_{IL}			--	--	DVDD x 0.3	
FAULT_N1, FAULT_N2	VOL: Low-Level Output Voltage	V_{OL}	I_{PULLUP} = 3mA		--	--	0.4	V
DVDD1+DVDD2 Quiescent Current (Normal Mode)		I_{Q_DVDD}	EN = 3.3V, for DVDD		--	8.5	--	mA
DVDD1+DVDD2 Shutdown Current		I_{DVDD_STBY}	EN = 0V, no load, no LC filter		--	5	15	μA
PVDDL/R+AVCC Quiescent Current (CMH Mode)		I_{Q_P}	EN = 3.3V, switch 25% duty, no load, no LC filter, PWM = 384kHz		--	20.5	--	mA
			EN = 3.3V, switch 25% duty, L = 8.2μH, C = 0.47μF, PWM = 384kHz		--	20	--	mA
			EN = 3.3V, switch 25% duty, L = 6.8μH, C = 0.22μF, PWM = 768kHz		--	20	30	
			PVDD = 12.7V, EN = 3.3V, switch 25% duty, no load, no LC filter, PWM = 768kHz		--	34	--	
PVDDL/R+AVCC Shutdown Current		I_{SD_P}	EN = 0V, no load, no LC filter		--	10	20	μA
Drain-Source On-State Resistance		R_{DSON}	PVDD = 12V, I_O = 500mA, T_J = 25°C	High-Side	--	95	--	mΩ
				Low-Side	--	85	--	
AMP Gain variation		$\Delta A_{V(SPK\_AMP)}$	AMP to AMP gain difference		–0.5	--	0.5	dB
Speaker Gain variation		$\Delta A_{V(L/R\ Ch)}$	L/R channel gain difference		--	--	0.4	dB
Startup Time from Shutdown		t_{ON}	Timing between from 0x05 bit [1:0] set to 01 to the PWM output		--	45	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Volume Ramp Up Time		The ramp up time depends on the setting of register 0x0A. Note: The default setting for register 0x0A is 01.	4.33	--	34.65	ms
PWM Shutdown Time from EN Set to Low	tOFF	Timing from EN set to low to PWM stop output	--	--	200	us
Volume Ramp Down Time		The ramp down time depends on the setting of register 0x0A. Note: The default setting for register 0x0A is 01.	4.33	--	34.65	ms
PWM Switching Frequency	fSW	384kHz mode	--	384	--	kHz
		768kHz mode	--	768	--	
RMS Output Power BD Modulation	PO	THD + N = 10%, (BTL), PVDD = 18V, RL = 6Ω	--	27	--	W
		THD + N = 1%, (BTL), PVDD = 18V, RL = 6Ω	--	23	--	
Total Harmonic Distortion + Noise	THD+N	PVDD = 24V, PO = 1W (BTL), RL = 8Ω	--	0.02	--	%
Output Integrated Noise	Vn	20Hz to 20kHz, A-weighted	--	35	--	μV
Output Offset Voltage	VOS	PVDD = 12V with offset calibration enable	–5	--	5	mV
		PVDD = 24V with offset calibration enable	–5	--	5	
Cross-Talk	XTALK	Output power = 1W, 1kHz with none shielding choke	--	–75	--	dB
		Output power = 1W, 1kHz with shielding choke	--	–110	--	
Signal-to-Noise Ratio	SNR	PVDD = 24V, 1% THD + N, RL = 4Ω	--	113	--	dB
Power Supply Rejection Ratio	PSRR	Frequency @1kHz with 200mVpp ripple	--	73	--	dB
Dynamic Range	DR	Input level –60dBFS	--	113	--	dB
Efficiency	η	PVDD = 12V, output power = 10W + 10W, Load = 8Ω	--	94	--	%
		PVDD = 18V, output power = 1.25W + 1.25W, Load = 6Ω	--	70	--	
Over-Temperature Protection	TOTP	Guaranteed by design	150	160	175	°C
Over-Temperature Protection Hysteresis	TOTP_HYS		--	20	--	°C
Overcurrent Protection	IOCP		6	7	--	A
PVDDL/PVDDR Overvoltage Protection	VOVP		28	--	30	V
PVDDL/PVDDR Undervoltage Protection	VUVP	The PVDD UVP threshold can be programmed, and set from 4V to 20V. Refer to register 0x6C for detailed setting.	3.98	4	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Open Load Detection (OLD)	OLD		16	--	--	Ω
Short Load Detection (SLD)	SLD		--	--	2	Ω
Minimum Load						
PVDD Range (Note 10)	V	BTL, R = 4Ω (Note 11)	--	--	21	V
		BTL, R ≥ 5Ω (Note 11)	--	--	26.4	
		PBTL, R = 2Ω	--	--	21	
		PBTL, R ≥ 3Ω	--	--	26.4	
I^2C Interface Electrical Characteristics						
High-Level Input Voltage (Belongs to the internal 1.8V domain)	V_{IH_I2C}		DVDD x 0.7	--	--	V
Low-Level Input Voltage (Belongs to the internal 1.8V domain)	V_{IL_I2C}		--	--	DVDD x 0.3	V
Digital Output Low (SDA)	V_{OL_I2C}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency	f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3	--	--	µs
Hold Time After (Repeated) Start Condition	$t_{HD;STA}$		0.6	--	--	µs
Repeated Start Condition Setup Time	$t_{SU;STA}$		0.6	--	--	µs
Stop Condition Time	$t_{SU;STO}$		0.6	--	--	µs
Input Data Hold Time	$t_{HD;DAT}$ (IN)		0	--	900	ns
Data Setup Time	$t_{SU;DAT}$		100	--	--	ns
Clock Low Period	t_{LOW}		1.3	--	--	µs
Clock High Period	t_{HIGH}		0.6	--	--	µs
Clock Data Fall Time	t_F		20	--	300	ns
Clock Data Rise Time	t_R		20	--	300	ns
Spike Suppression Time	t_{SP}		--	--	20	ns
Slave Mode I^2S Interface Electrical Characteristics						
High-Level Input Voltage	V_{IH_I2S}		DVDD x 0.7	--	--	V
Low-Level Input Voltage	V_{IL_I2S}		--	--	DVDD x 0.3	V
SDO	V_{OH_I2S}	V_{OH_I2S}	0.7*DVDD	--	--	V
	V_{OL_I2S}	V_{OL_I2S}	--	0.4	--	
High-Level Input Voltage	V_{IH_I2S}	DVDD = 1.8V	1.4	--	--	V
Low-Level Input Voltage	V_{IL_I2S}	DVDD = 1.8V	--	--	0.5	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
SDO	V_{OH_I2S}	V_{OH_I2S}	DVDD = 1.8V	0.7*DVDD	--	--	V
	V_{OL_I2S}	V_{OL_I2S}	DVDD = 1.8V	--	0.2	--	V
Frequency		f_{SCLKIN}		1.024	--	12.288	MHz
Setup Time, LRCK to SCLK Rising Edge		t_{SU1}		10	--	--	ns
Hold Time, LRCK from SCLK Rising Edge		t_{H1}		10	--	--	ns
Setup Time, SDI to SCLK Rising Edge		t_{SU2}		10	--	--	ns
Hold Time, SDI from SCLK Rising Edge		t_{H2}		10	--	--	ns
Rise/Fall Time for SCLK/LRCK		t_{R_I2S} /t_{F_I2S}		--	--	10	ns
I^2S Duty Cycle		%		40	--	60	%

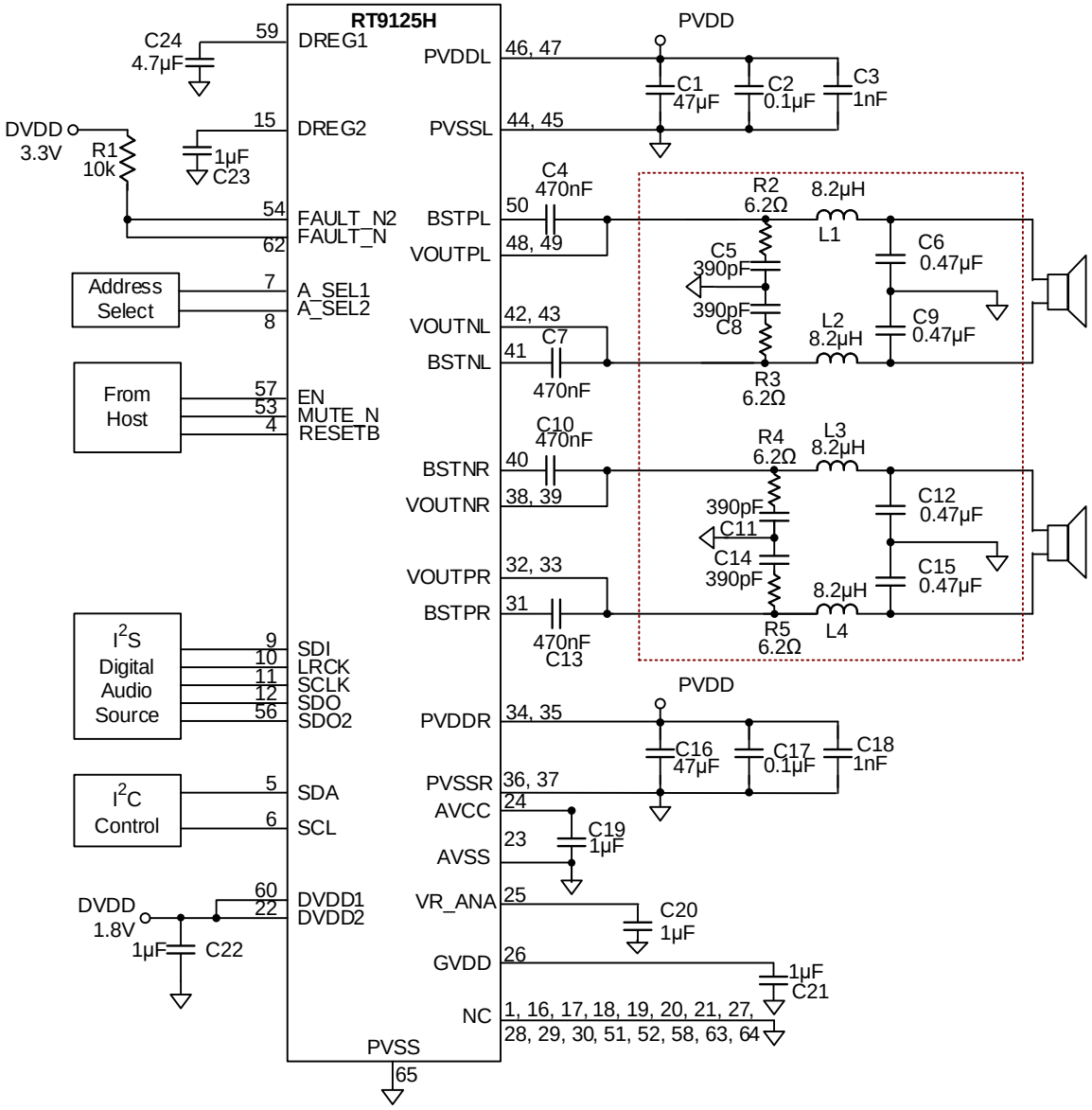
Note 9. Measurements were made using the RT9125H evaluation board and Audio Precision System 2722 with an AUX-0025 low-pass filter.

Note 10. If the maximum output power does not exceed the OCP value, there is no need to consider the minimum load.

Note 11. Add a snubber if the output power is over 15W for 4Ω, or 25W for 6Ω. Refer to page 13 and 14 for the BTL snubber circuit, and page 15 and 16 for the PBTL snubber circuit.

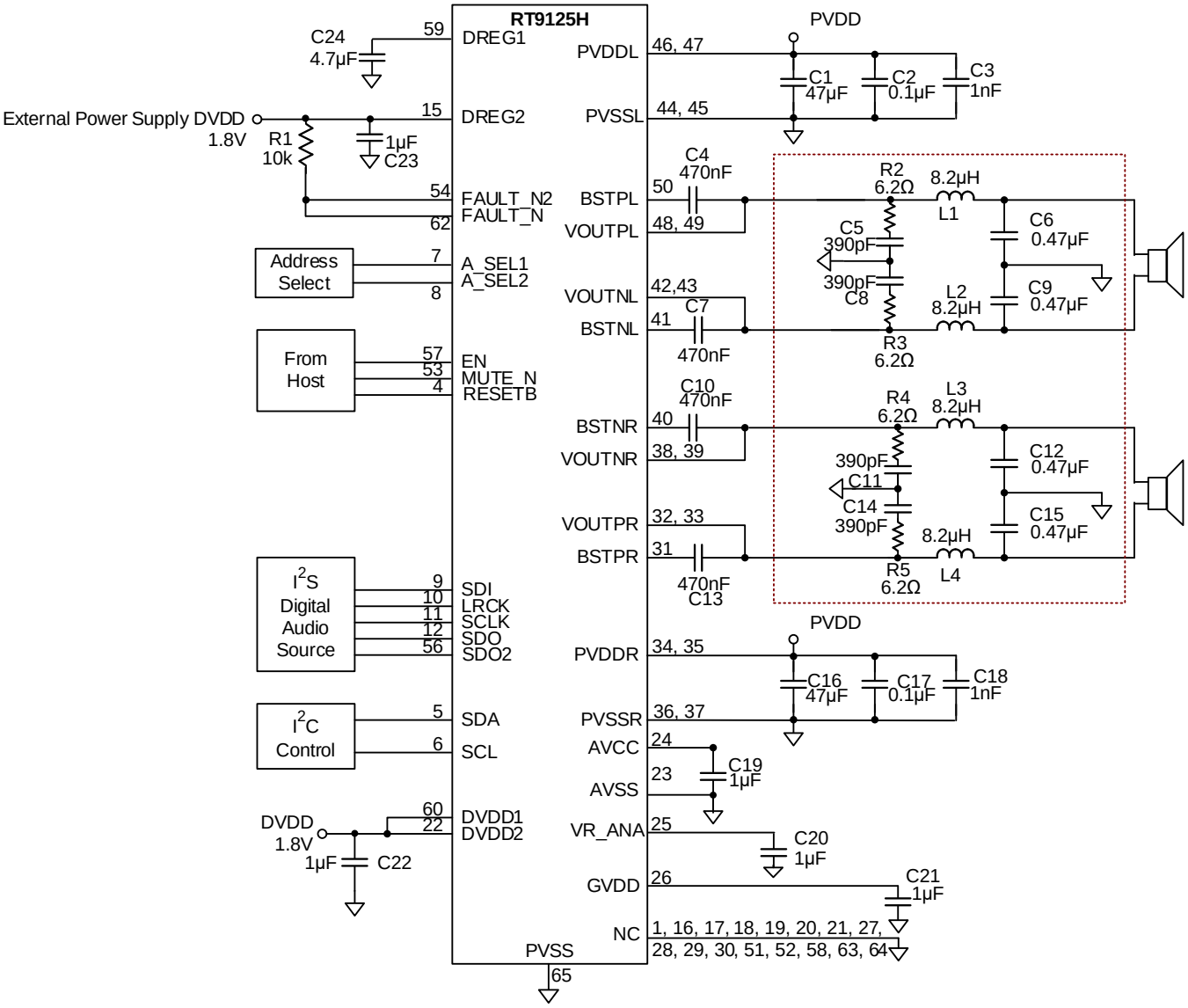
13 Typical Application Circuit

13.1 3.3V I/O Application (BTL)



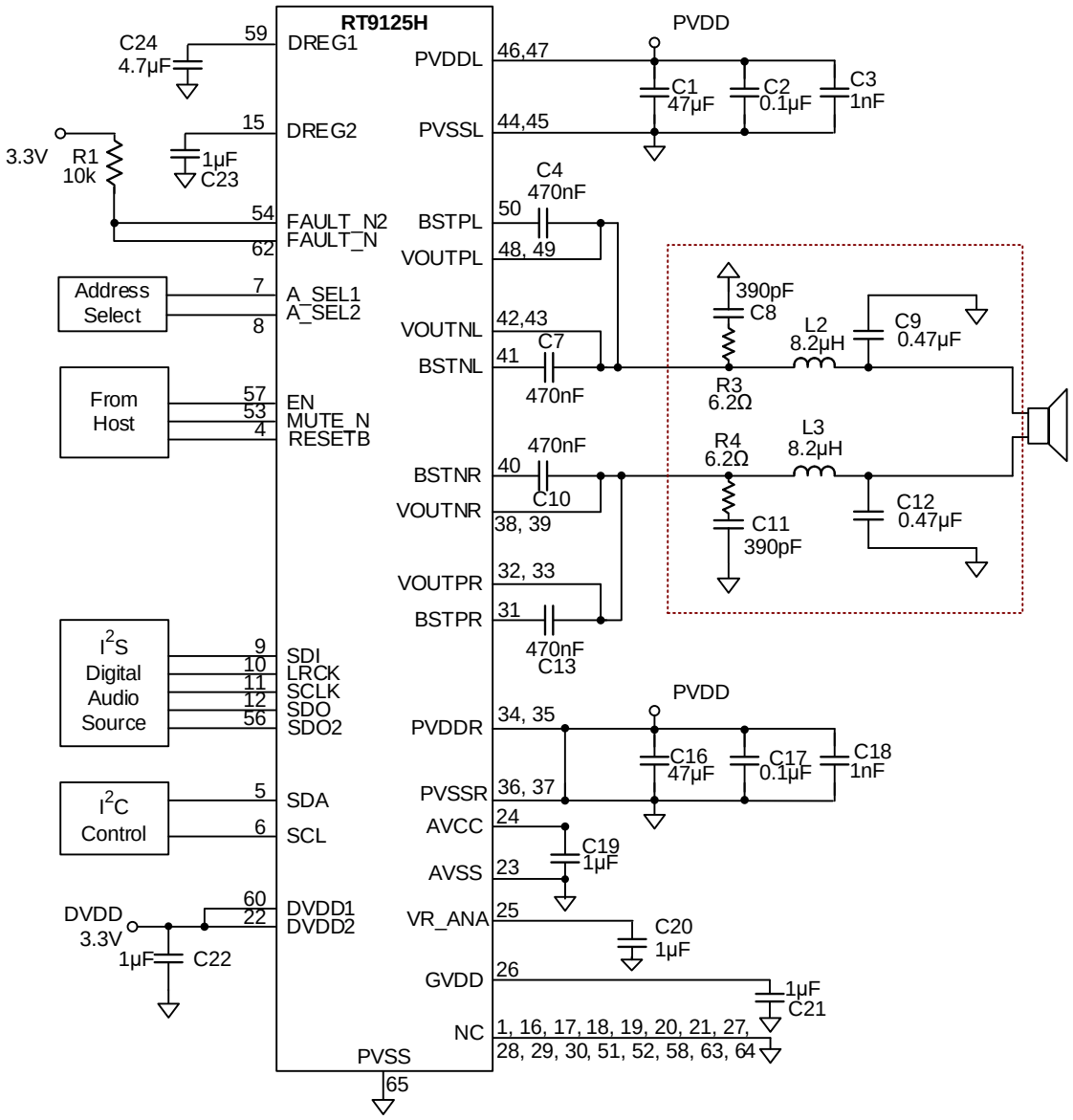
Note 12. For different PWM frequency and LC filter combinations, refer to the Application Information section.

13.2 1.8V I/O Application (BTL)



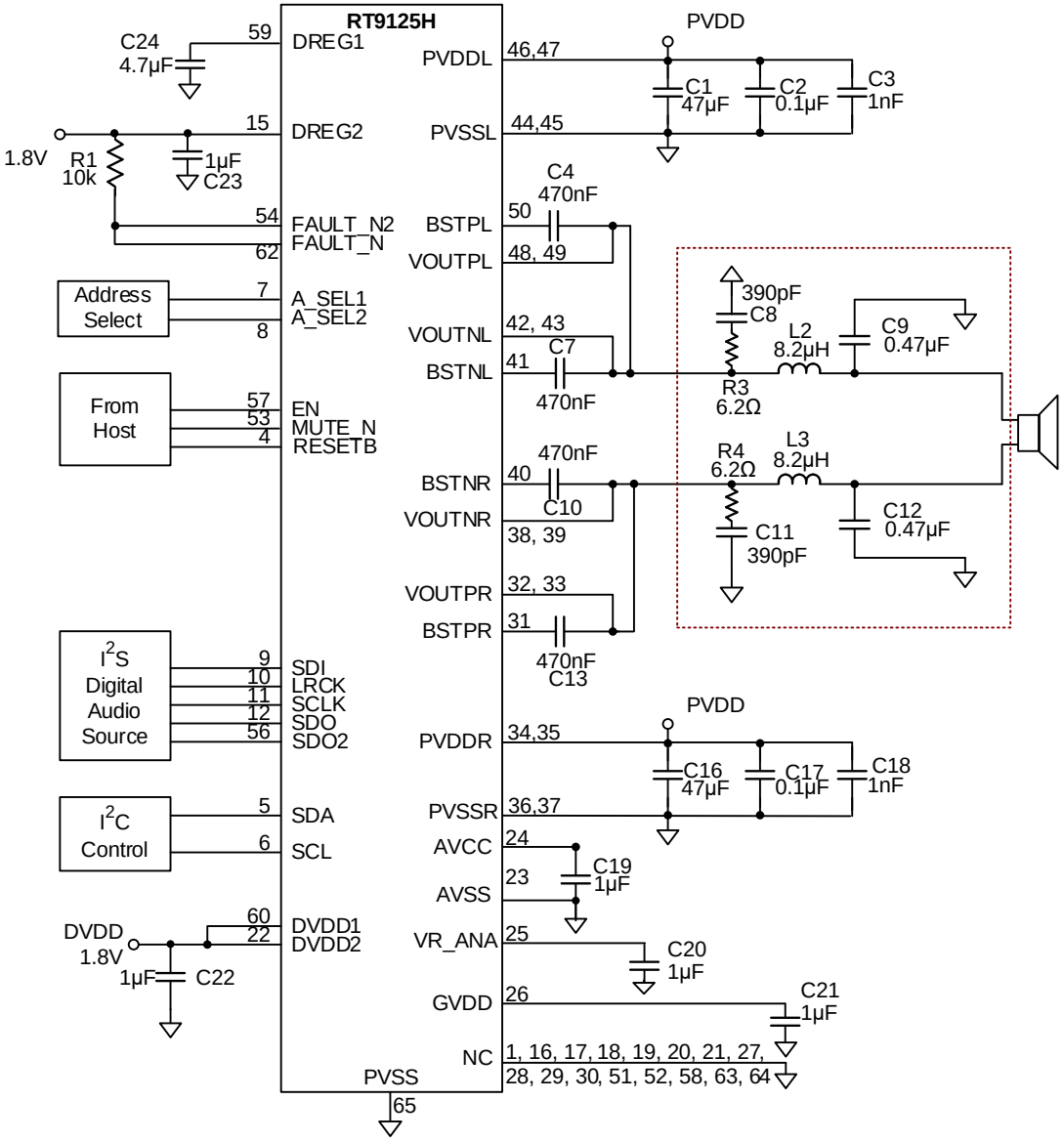
Note 13. For different PWM frequency and LC filter combinations, refer to the Application Information section.

13.3 3.3V I/O Application (PBTL)



Note 14. For different PWM frequency and LC filter combinations, refer to the Application Information section.

13.4 1.8V I/O Application (PBTL)



Note 15. For different PWM frequency and LC filter combinations, refer to the Application Information section.

14 Timing Diagram

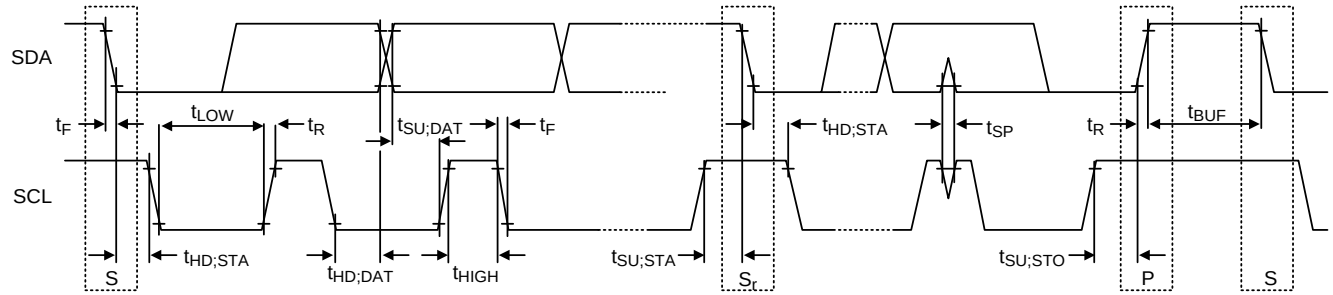


Figure 1. I²C Interface Timing Diagram

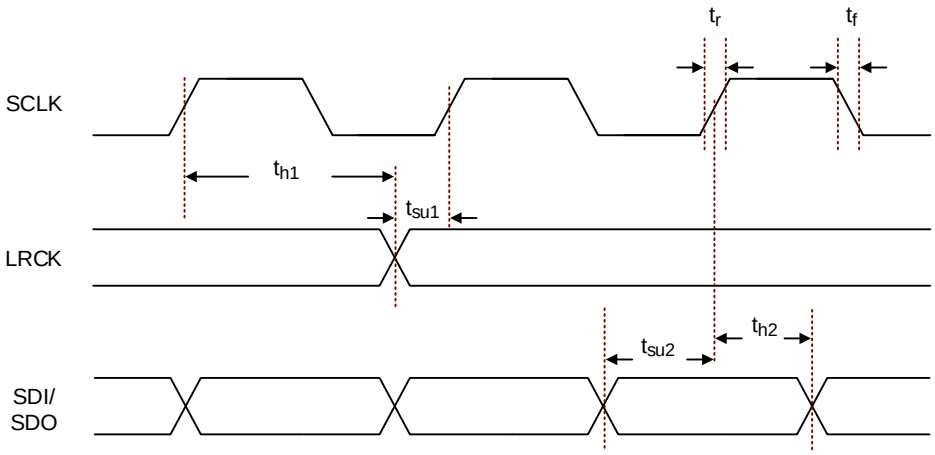
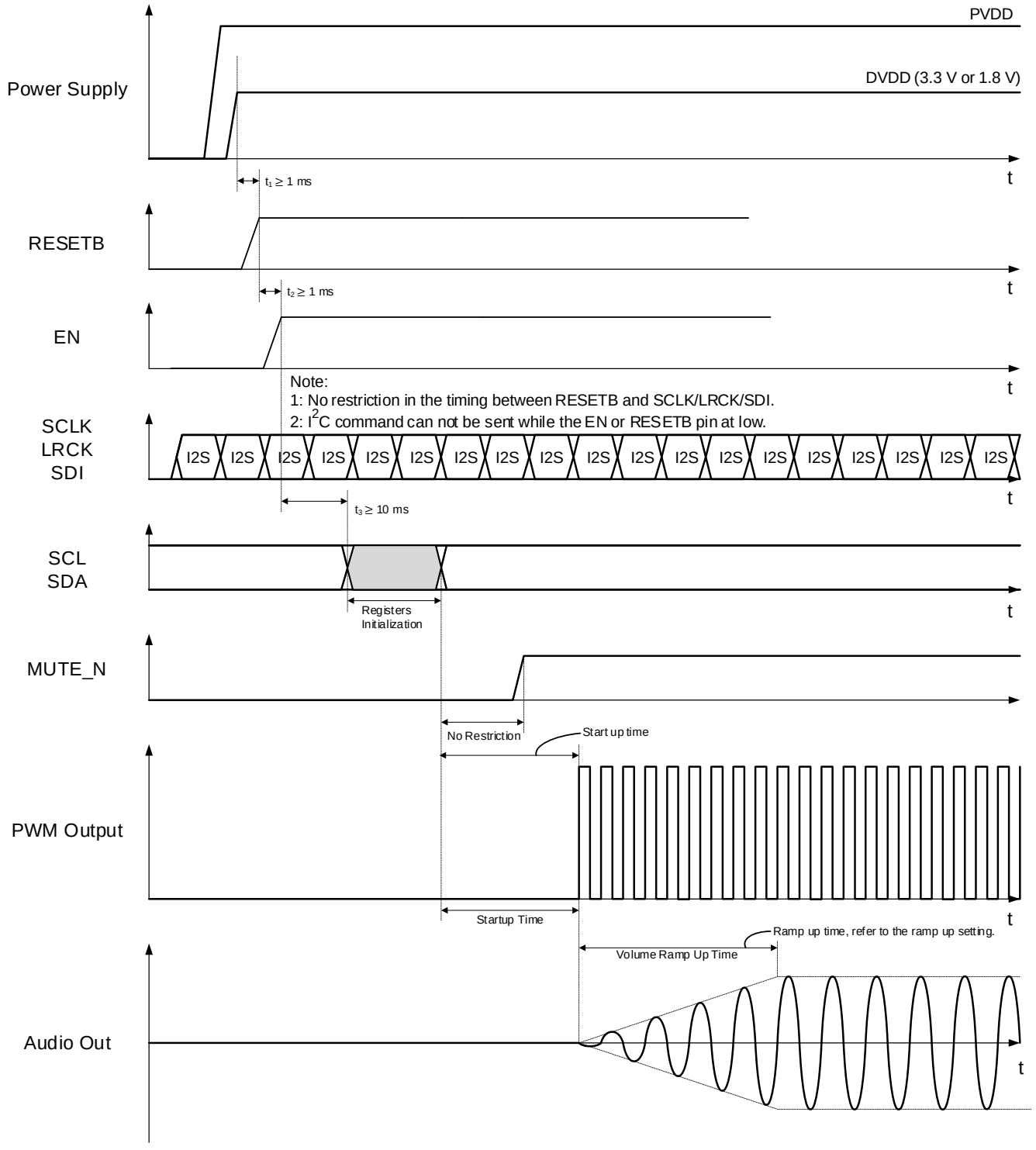


Figure 2. Timing Diagram of Slave Mode I²S Interface

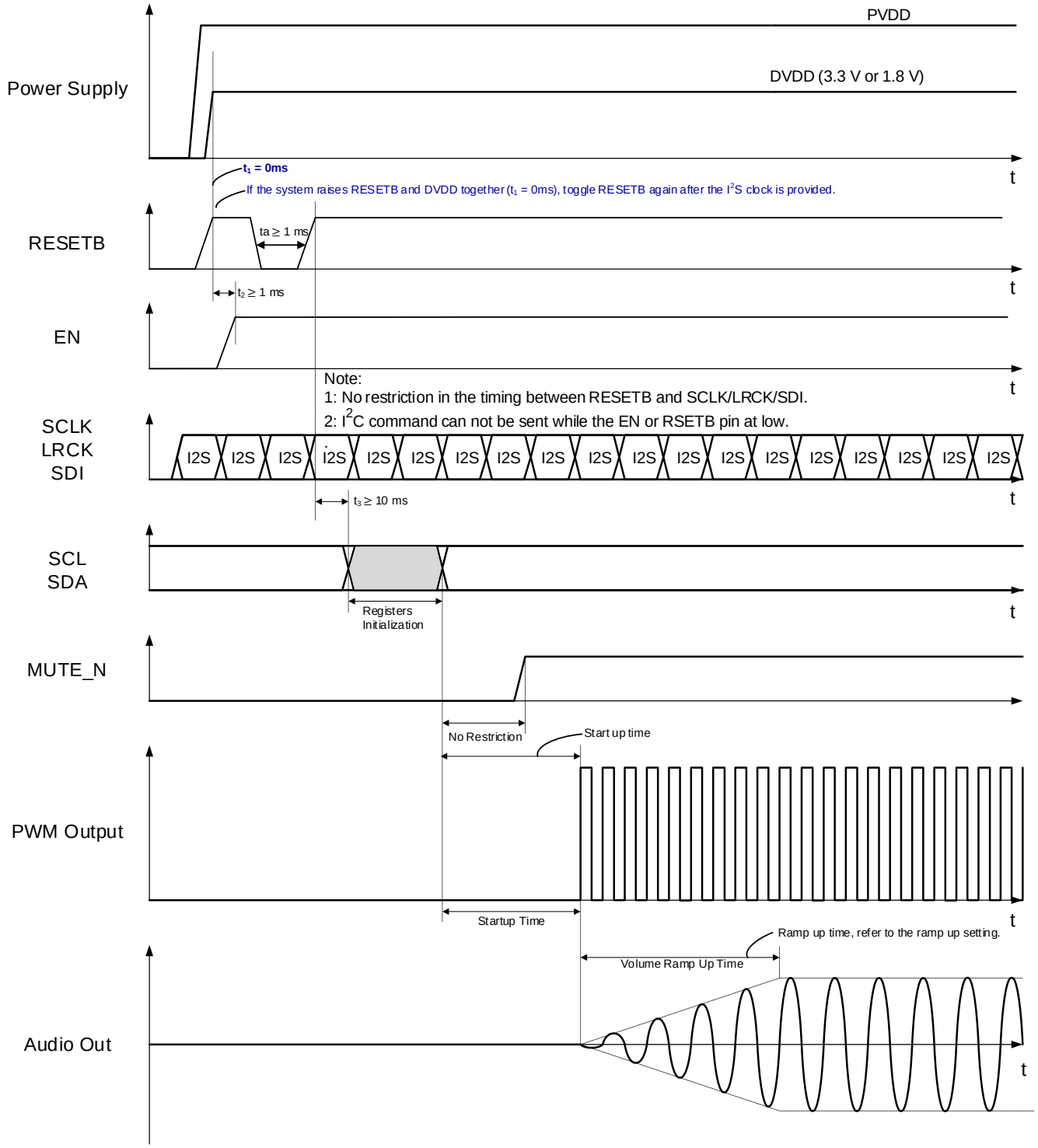
14.1 Turn-On Timing Diagram (1)



Note 16. Follow the timing sequence exactly. Any violation of the sequence is not allowed.

14.2 Turn-On Timing Diagram (2)

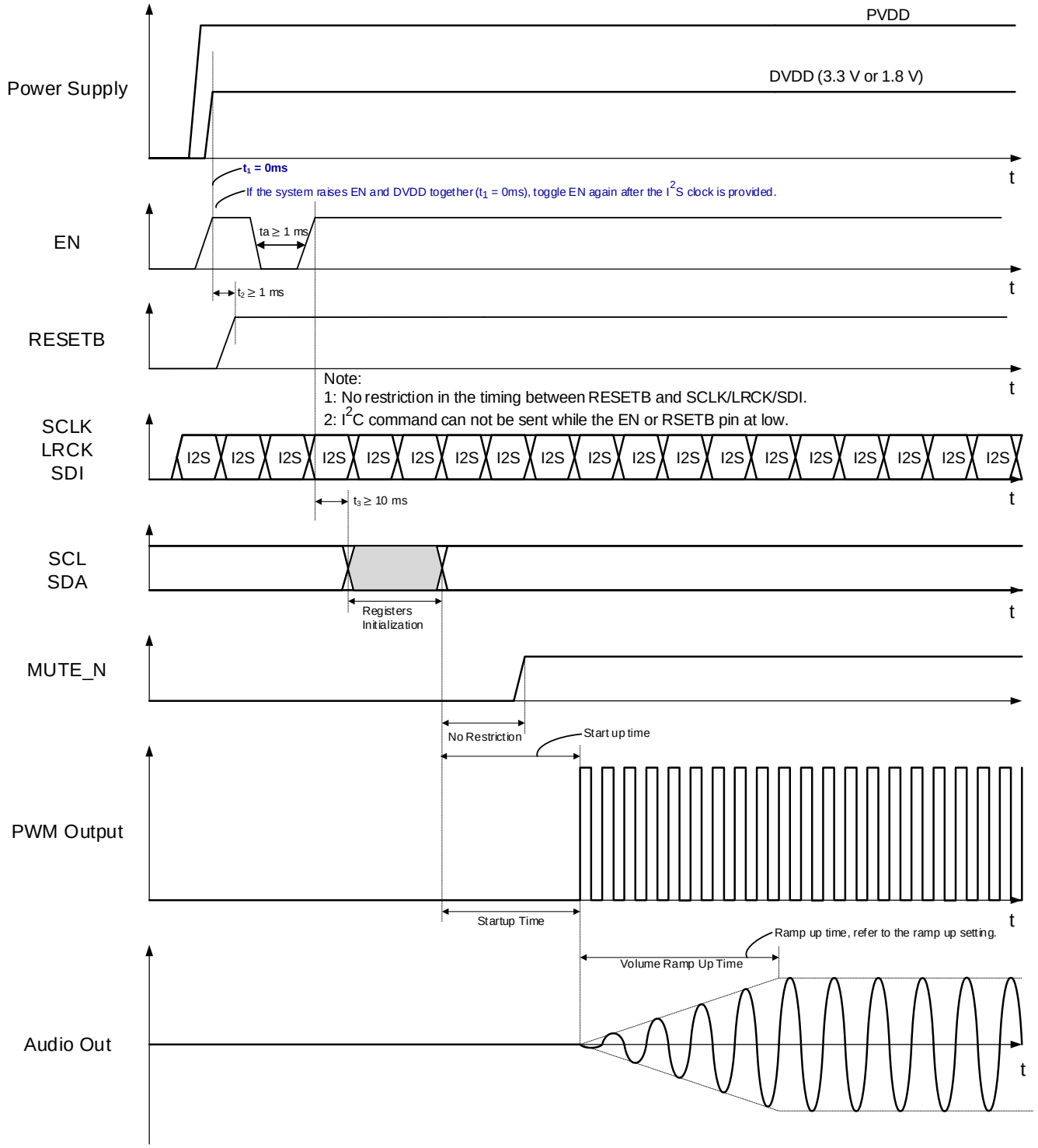
If the system raises RESETB and DVDD together, follow the sequence below.



Note 17. Follow the timing sequence exactly. Any violation of the sequence is not allowed.

14.3 Turn-On Timing Diagram (3)

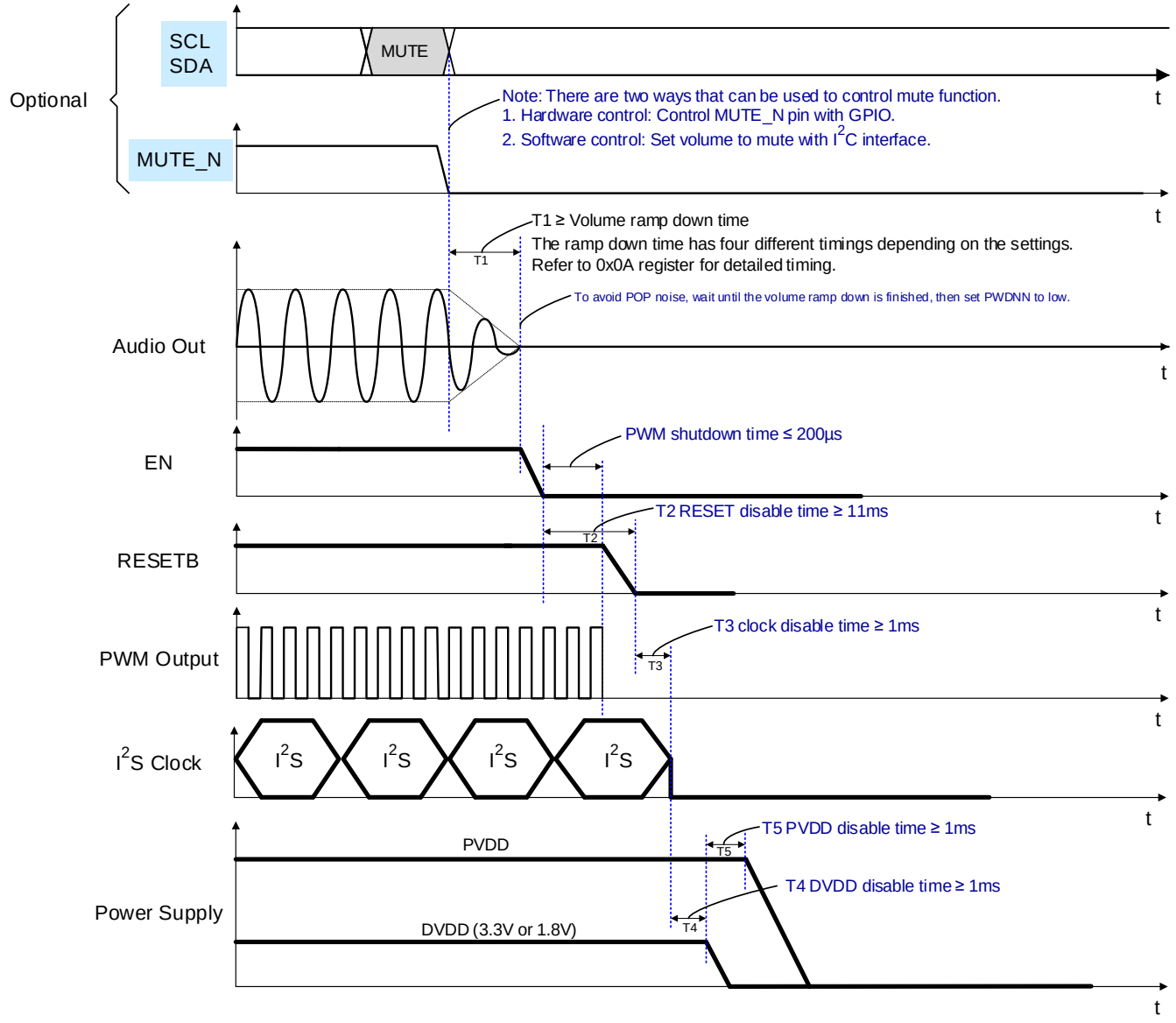
If the system raises EN and DVDD together, follow the sequence below.



Note 18. Follow the timing sequence exactly. Any violation of the sequence is not allowed.

14.4 Turn-Off Timing Diagram (1)

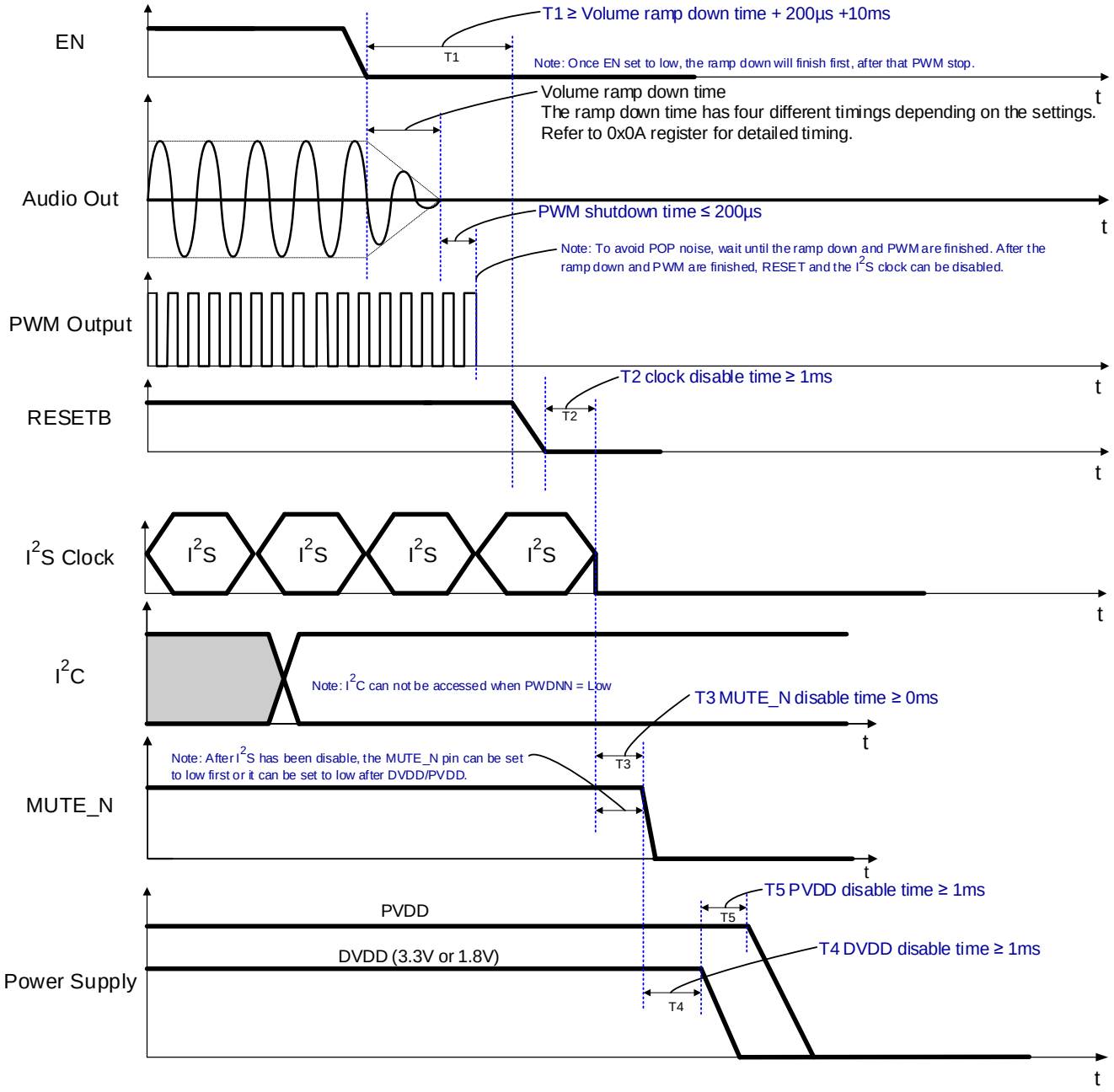
Control flow is as follows: MUTE_N/I2C → Ramp down Finished→ EN → RESET→ PWM→ I^2S Clock → DVDD/PVDD



Note 19. Follow the T1 to T5 timing sequence exactly. Any violation of the T1 to T5 timing sequence is not allowed. For AC off, also follow the T1 to T5 sequence.

14.5 Turn-Off Timing Diagram (2)

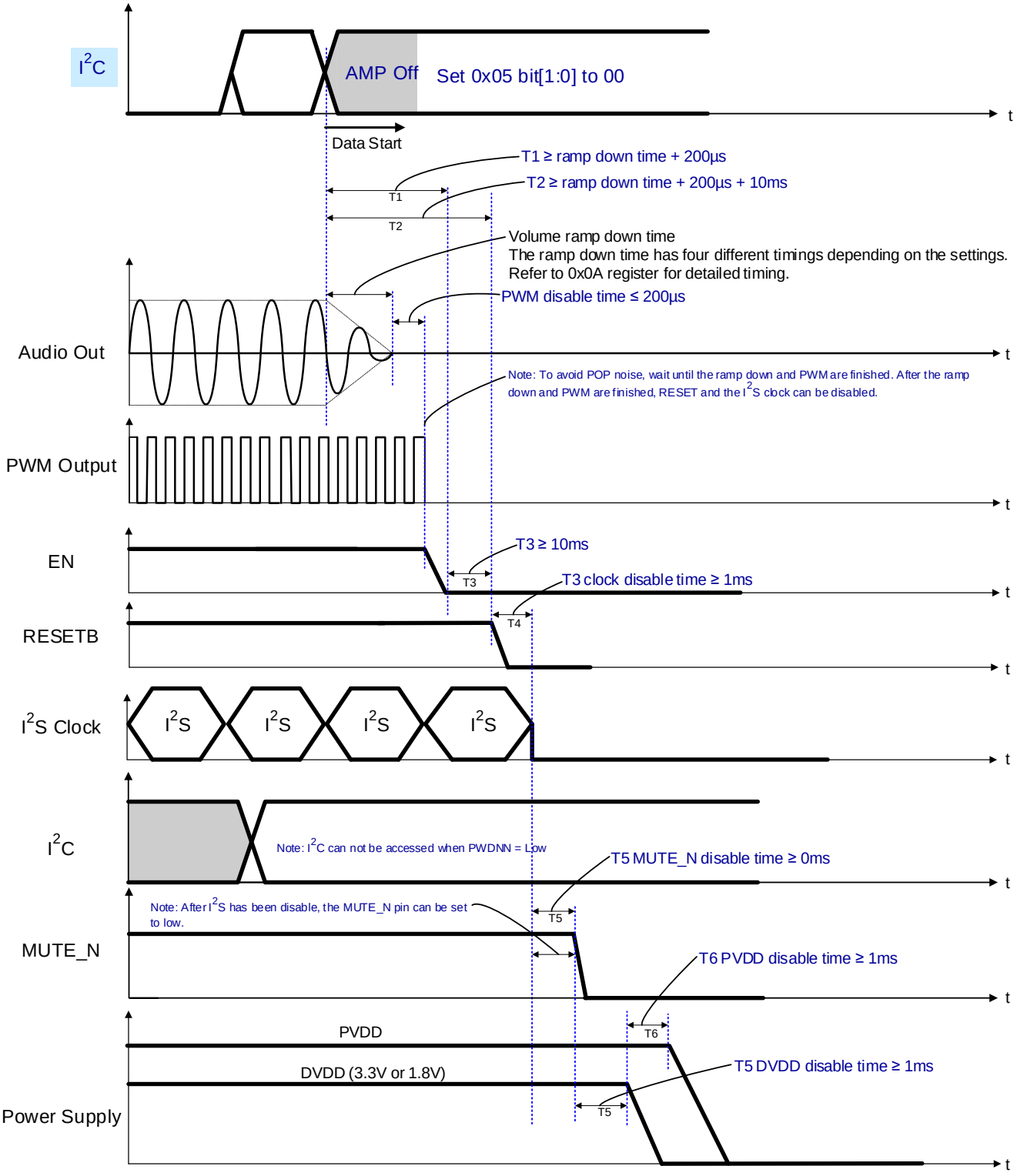
The control flow is EN → Ramp down and PWM Finished → I²S Clock → DVDD/PVDD



Note 20. Follow the T1 to T5 timing sequence exactly. Any violation of the T1 to T5 timing sequence is not allowed. For AC off, also follow the T1 to T5 sequence.

14.6 Turn-Off Timing Diagram (3)

The control flow is as follows: Use I²C to set AMP off → Ramp down and PWM Finished → I²S Clock → DVDD/PVDD



Note 21. Follow the T1 to T6 timing sequence exactly. Any violation of the T1 to T6 timing sequence is not allowed. For AC off, also follow the T1 to T6 sequence.

14.7 Initial Sequence (BTL Mode)

Sequence	reg_addr	reg_size	reg_value	Description	Note
1	0x27	1	0x30	Analog gain	
	0x26	1	0x07		
	0x25	1	0x17		
	0x28	1	0x4E		
2	0x27	1	0x30	Internal setting	
	0x26	1	0x64		
	0x25	1	0xA9		
	0x28	1	0x4E		
3	0x27	1	0x30	Internal setting	
	0x26	1	0x95		
	0x25	1	0xD0		
	0x28	1	0x4E		
4	0x27	1	0x30	CMH threshold. Threshold is 12.5W with 6Ω load.	
	0x26	1	0x94		
	0x25	1	0x65		
	0x28	1	0x4E		
5	0x27	1	0x30	Set the volume from mute to 0dB	
	0x26	1	0x20		
	0x25	1	0x01		
	0x24	1	0x80		
	0x28	1	0x4F		
6	0x08	1	0xF5	Digital Amp on (SRC On) Note: If SRC is enabled, set 0xF5	Digital Amp turns on
	0x08	1	0xD5	Digital Amp on (SRC OFF) Note: If SRC is disabled, set 0xD1	Digital Amp turns on
7	0x27	1	0x30	Analog Amp on	Amp turns on
	0x26	1	0x05		
	0x25	1	0xE5		
	0x28	1	0x4E		

14.8 Initial Sequence (PBTL Mode)

Sequence	reg_addr	reg_size	reg_value	Description	Note
1	0x27	1	0x30	Analog gain	
	0x26	1	0x07		
	0x25	1	0x17		
	0x28	1	0x4E		

Sequence	reg_addr	reg_size	reg_value	Description	Note
2	0x27	1	0x30	Internal setting	
	0x26	1	0x64		
	0x25	1	0xA9		
	0x28	1	0x4E		
3	0x27	1	0x30	Internal setting	
	0x26	1	0x95		
	0x25	1	0xD0		
	0x28	1	0x4E		
4	0x27	1	0x30	CMH threshold. Threshold is 21W with 4Ω load.	
	0x26	1	0x94		
	0x25	1	0x6C		
	0x28	1	0x4E		
5	0x27	1	0x30	Set the volume from mute to 0dB	
	0x26	1	0x20		
	0x25	1	0x01		
	0x24	1	0x80		
	0x28	1	0x4F		
6	0x08	1	0xF5	Digital Amp on (SRC On) Note: If SRC is enabled, set 0xF5.	Digital Amp turns on
	0x08	1	0xD5	Digital Amp on (SRC OFF) Note: If SRC is disabled, set 0xD1.	Digital Amp turns on
7	0x27	1	0x30	Analog Amp on	Amp turns on
	0x26	1	0x05		
	0x25	1	0xF5		
	0x28	1	0x4E		

14.9 Command to access AMP Portion

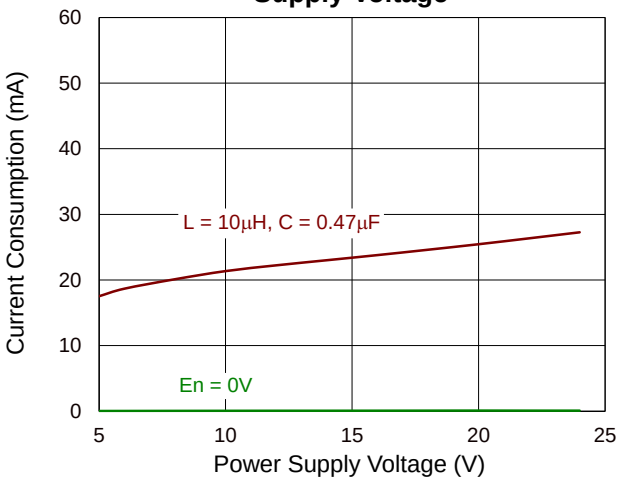
Description
→ Step 1: Set 0x27 to 0x30 to select the AMP address. → Step 2: Set 0x26 to the AMP portion address, where the address is to be set. → Step 3: Set 0x25 to the AMP portion setting. → Step 4: Send the writing command to 0x28. For example (Write): If set address 0x05 to 0x81. I2CW(0x27,{0x30}) I2CW(0x26,{0x05}) I2CW(0x25,{0x81}) I2CW(0x28,{0x4E}) For example (Read): If reading address 0x10. I2CW(0x27,{0x30})

Description
I2CW(0x26,{0x6D}) I2CW(0x28,{0x49}) I2CW(0x27,{0x31}) I2CW(0x28,{0x48}) I2CW(0x28,{0x54}) Note: These 4 commands form a set, and are required to access the AMP portion

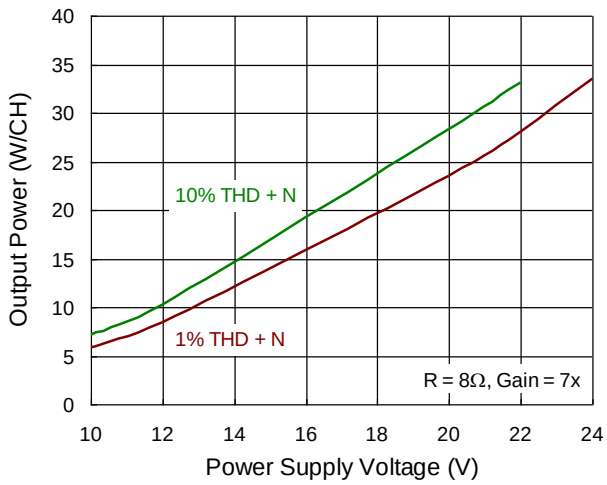
15 Typical Operating Characteristics

15.1 BTL, PWM = 768kHz

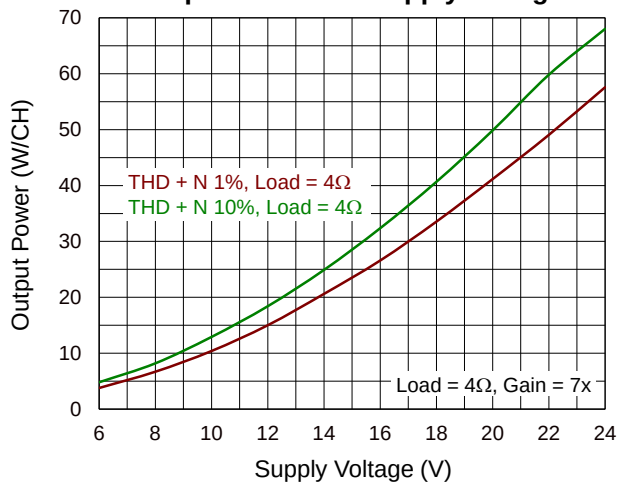
Current Consumption vs. Power Supply Voltage



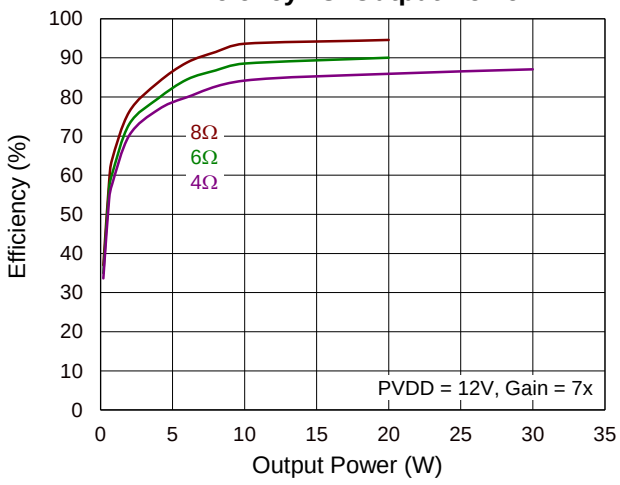
Output Power vs. Power Supply Voltage (BTL)



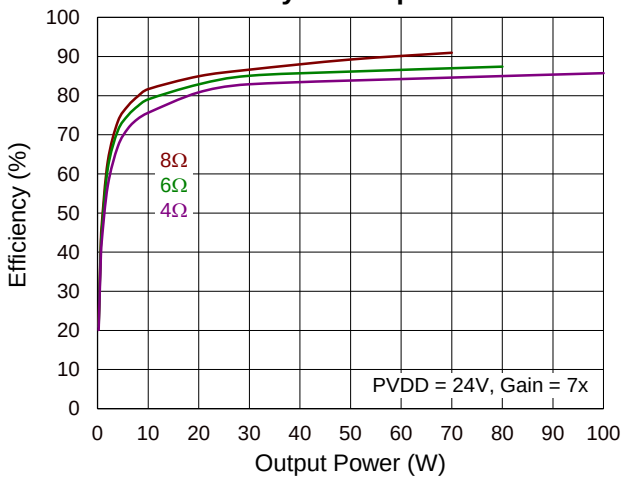
Output Power vs. Supply Voltage



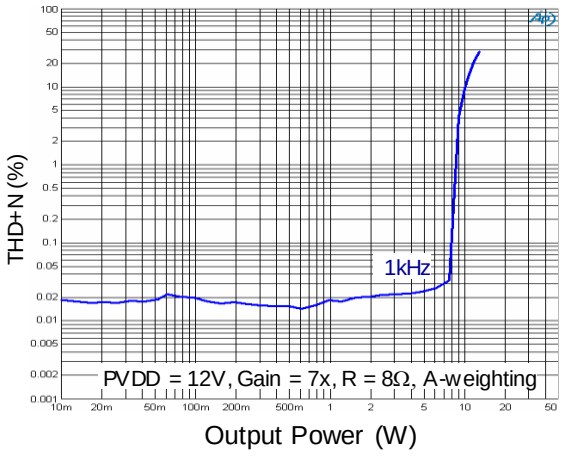
Efficiency vs. Output Power



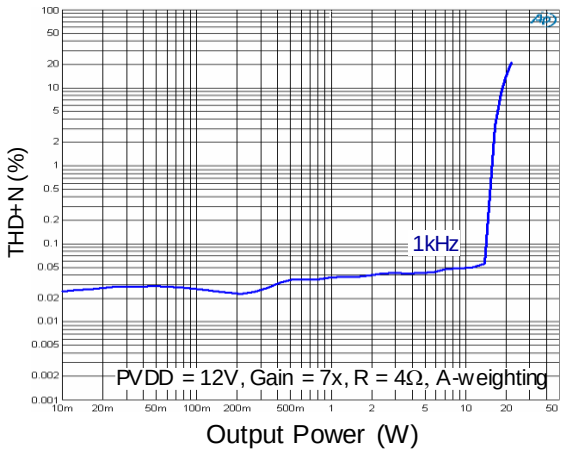
Efficiency vs. Output Power



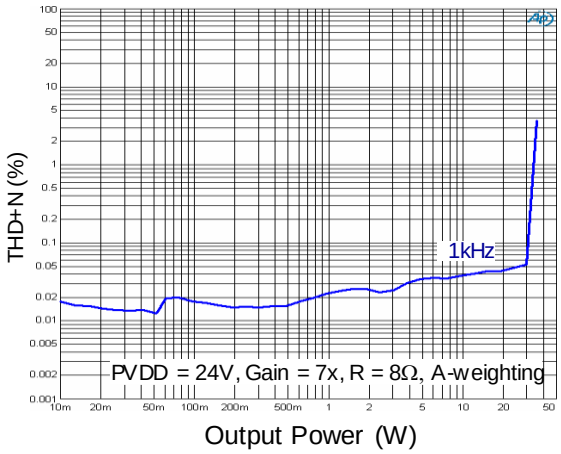
THD + N vs. Output Power (BTL)



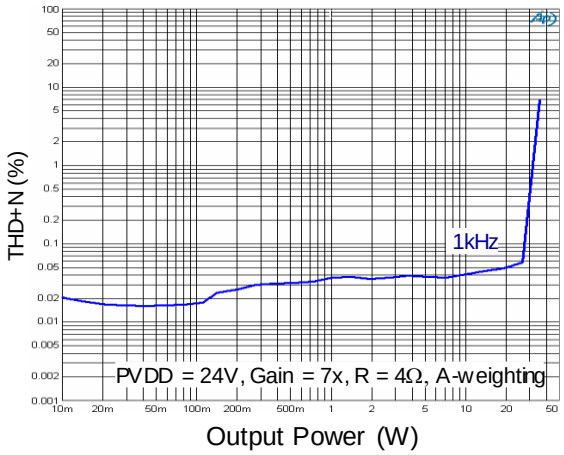
THD + N vs. Output Power (BTL)



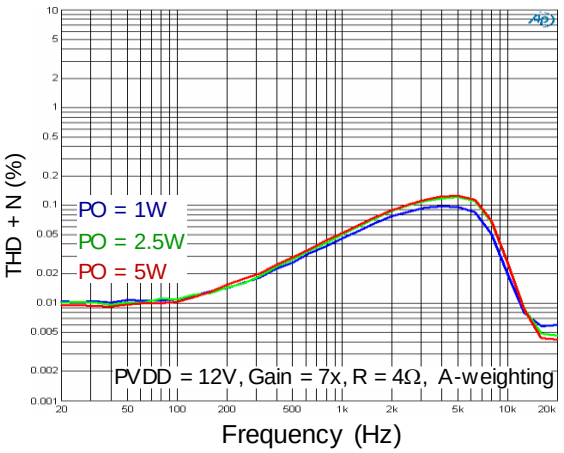
THD + N vs. Output Power (BTL)



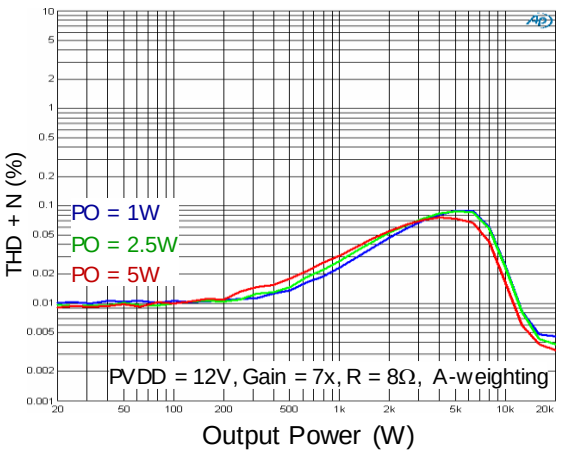
THD + N vs. Output Power (BTL)



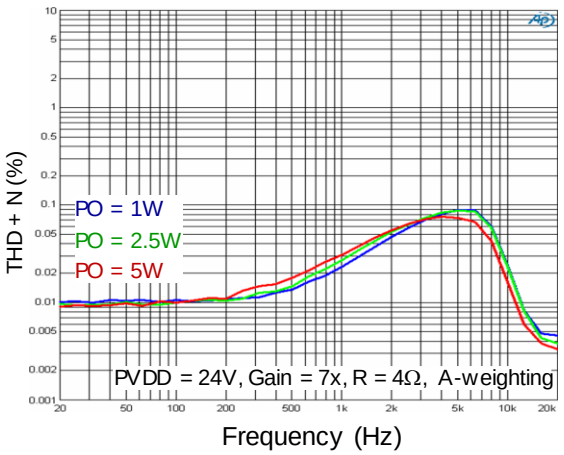
THD + N vs. Frequency (BTL)



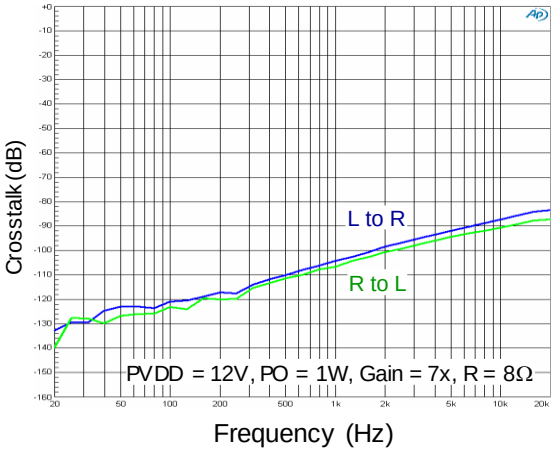
THD + N vs. Frequency (BTL)



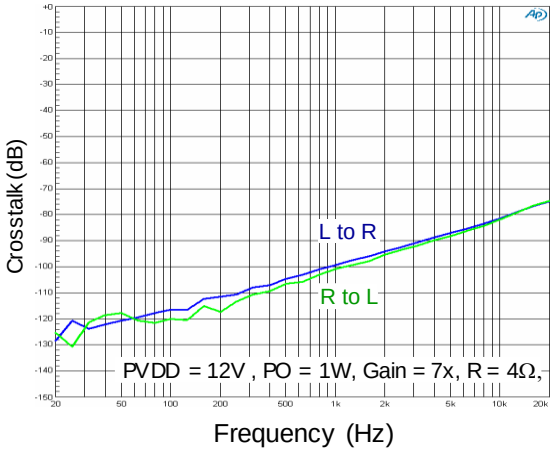
THD + N vs. Frequency (BTL)



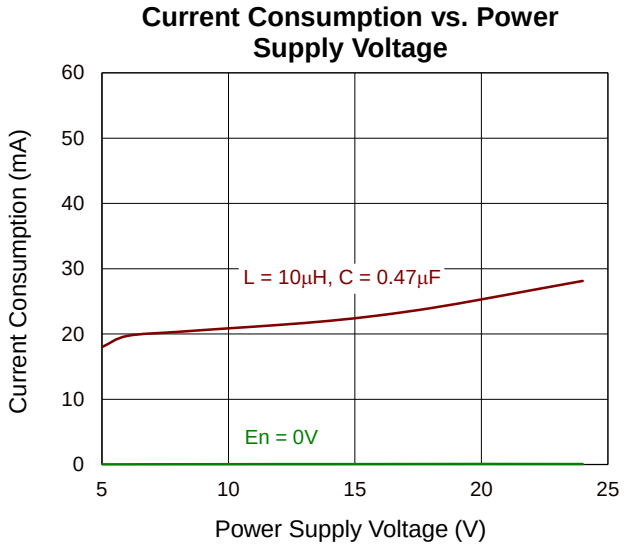
Crosstalk vs. Frequency

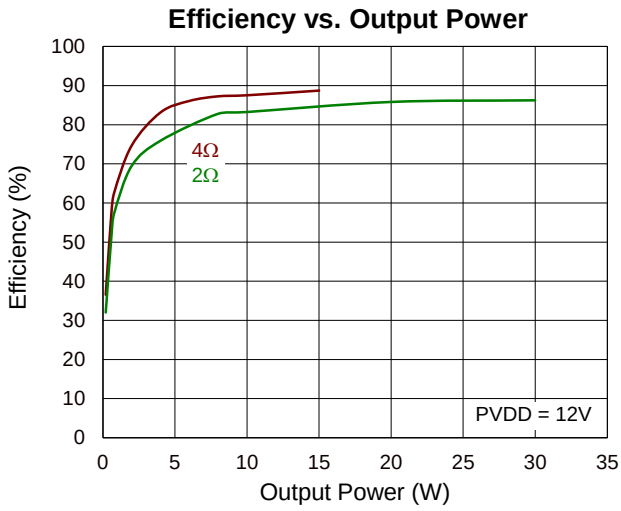


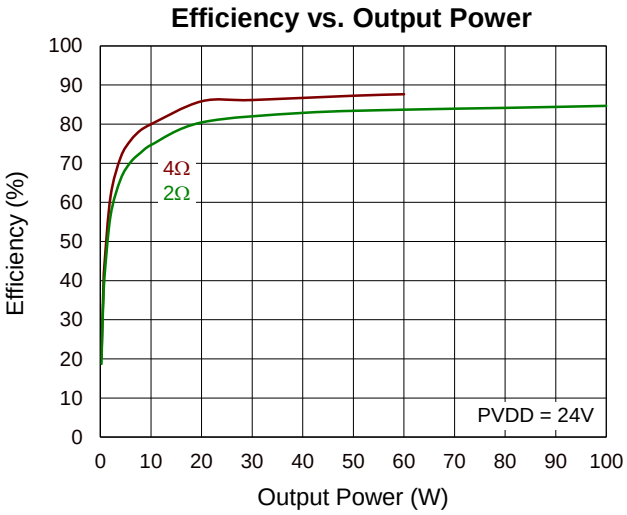
Crosstalk vs. Frequency

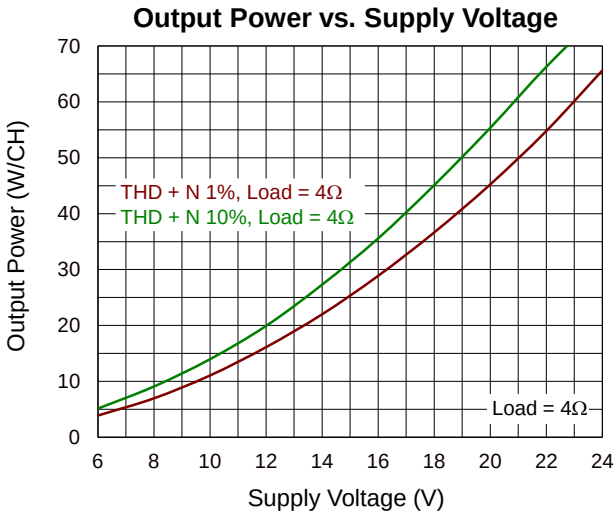


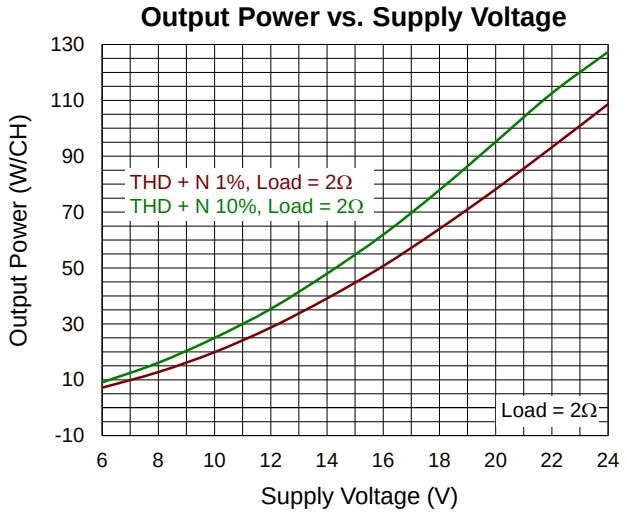
15.2 PBTL, PWM = 768kHz

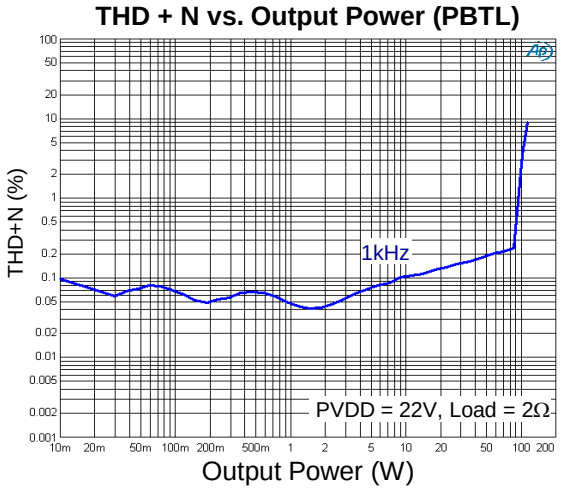




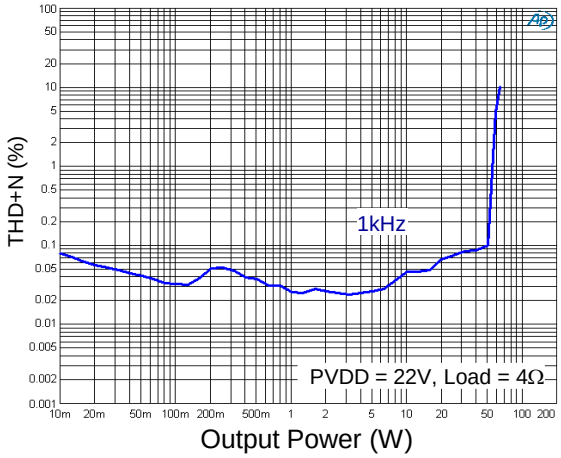




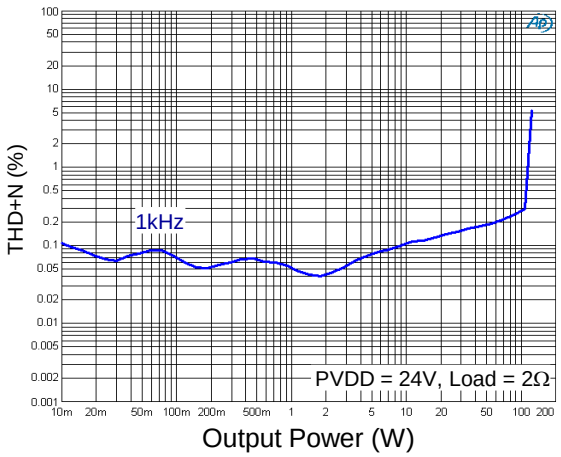




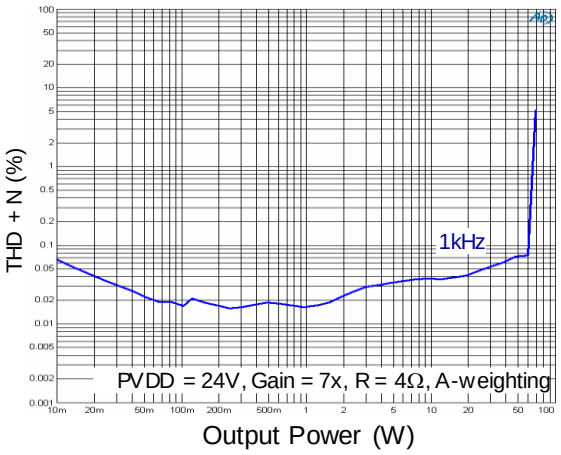
THD + N vs. Output Power (PBTL)



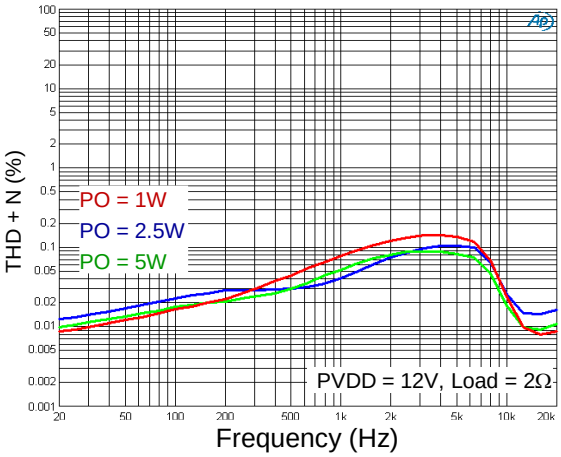
THD + N vs. Output Power (PBTL)



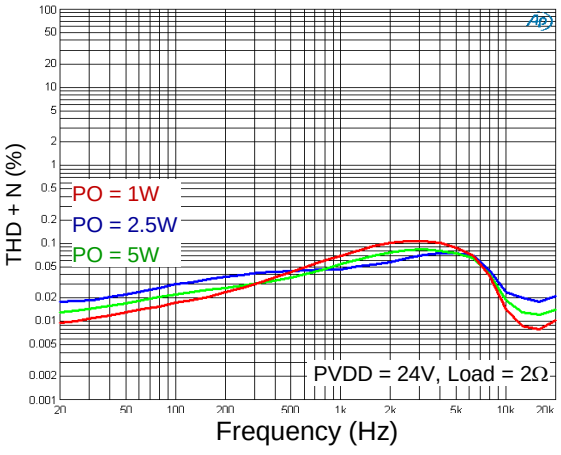
THD + N vs. Output Power (PBTL)



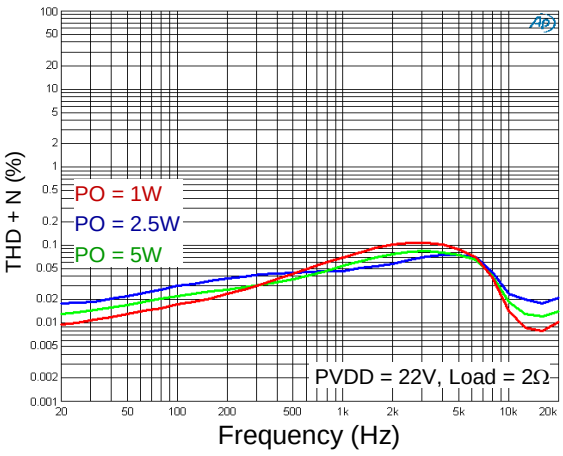
THD + N vs. Frequency (PBTL)



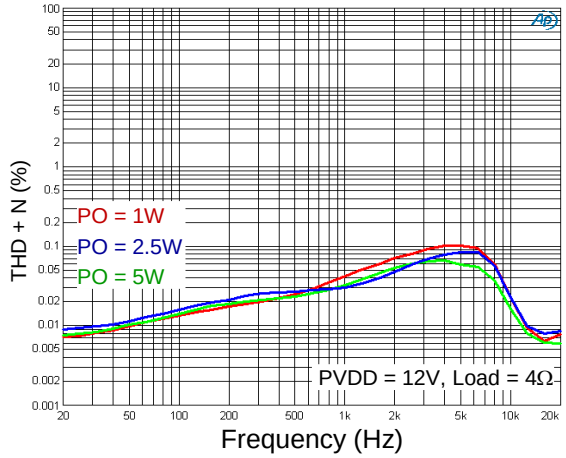
THD + N vs. Frequency (PBTL)



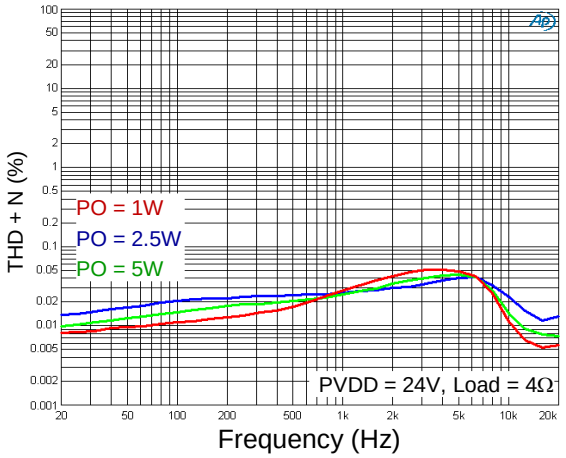
THD + N vs. Frequency (PBTL)



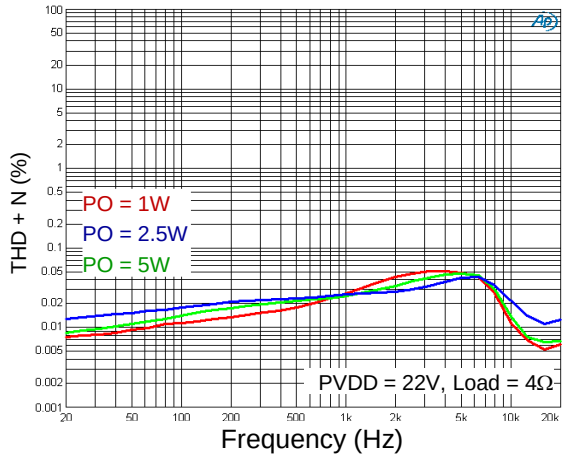
THD + N vs. Frequency (PBTL)



THD + N vs. Frequency (PBTL)

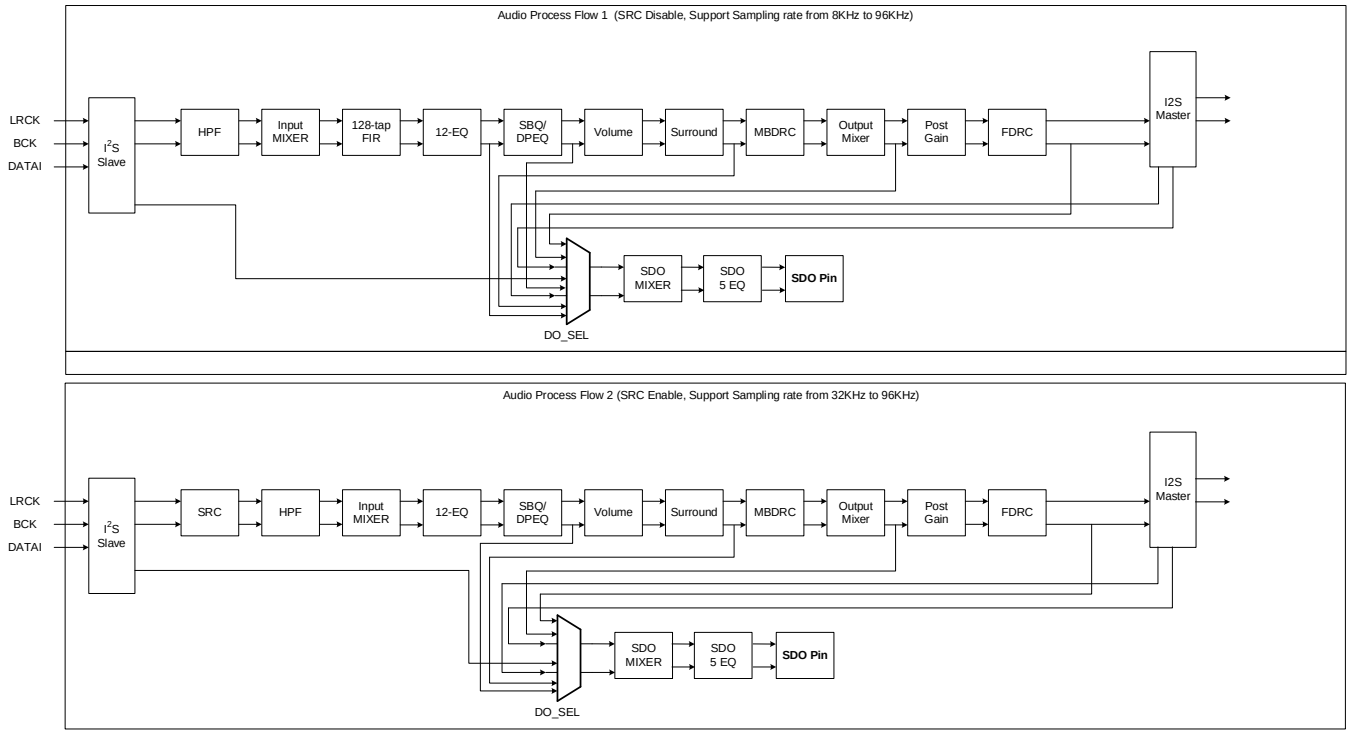


THD + N vs. Frequency (PBTL)



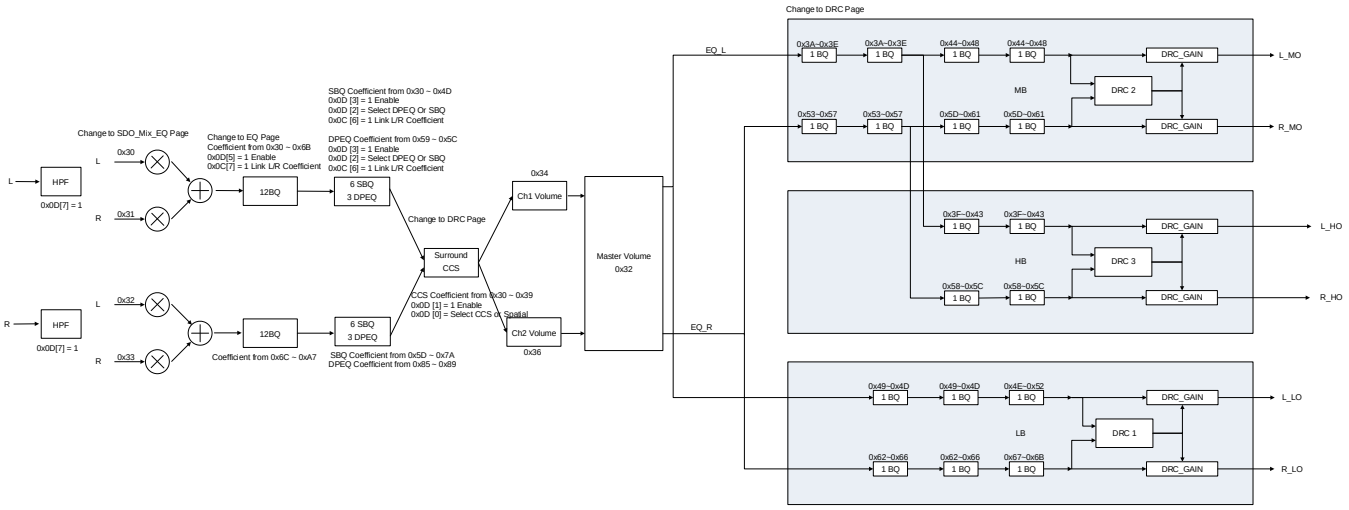
Note 22. Measurements were made using the RT9125H evaluation board and Audio Precision System 2722 with an AUX0025 low-pass filter. All measurements were taken at 1kHz.

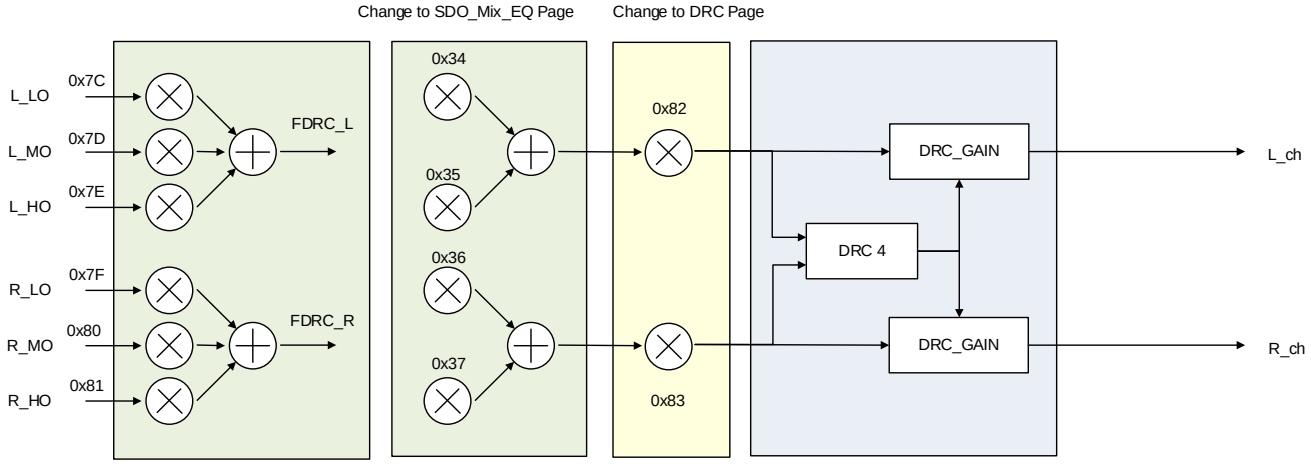
16 Overall Signal Path



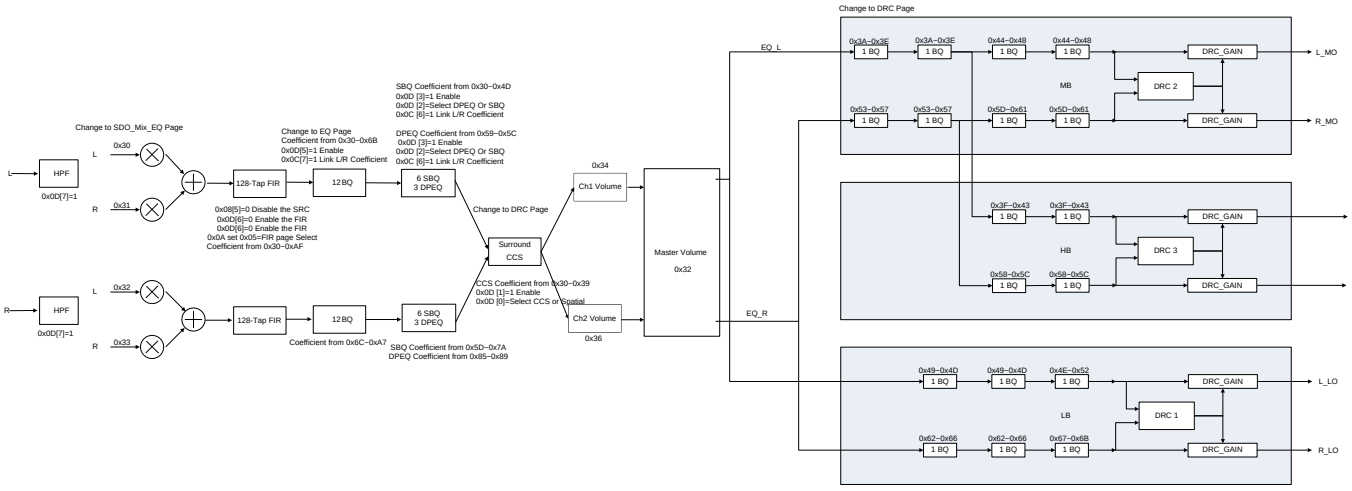
17 Detailed Signal Path

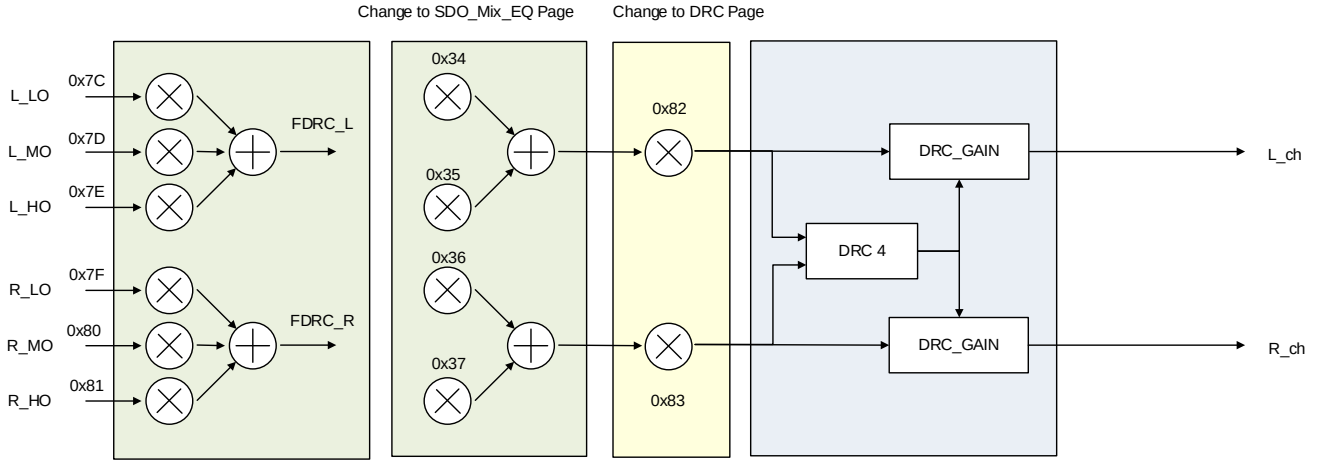
17.1 When SRC Enable





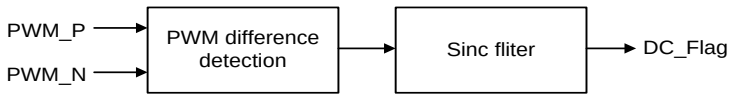
17.2 When SRC Disable





17.3 DC Protection Function (Amp Portion)

This function protects the loudspeaker when there are some DC at the output. The method is to detect DC at final stage (PWM), calculate the difference of the PWM and a Sinc filter to decide the DC level. The IC will shut down when detecting the DC.



Address	BITS	Name	Description
0x14	7:4	Reserved	
	3:2	DC_TH[1:0]	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%
	1	DC_TIME_SEL	Detection time 0: 342ms (default) 1: 684ms
	0	DC_EN	0: DC Protection disable 1: DC protection enable

17.4 Protection Behavior (FAULT_N1, Digital Portion)

If the protection behavior happened, the IC will automatically start detection, the error condition can be checked by the register or FAULT_N1 pin.

17.4.1 Protection Flag

Address	BITS	Name	Description
0x10	1	INT_I2S_FAULT	LRCK/BCK error 0: Normal (default) 1: Fault (write 1 to clear)

17.5 Protection Behavior (FAULT_N2, AMP Portion)

If the protection behavior happened, the IC will automatically start detection, the error condition can be checked by the register or the FAULT_N2 pin.

17.5.1 Protection Flag

Address	BITS	Name	Description
0x10	7	Reserved	
	6	DC_ERR	DC flag report 0: No DC error (default) 1: DC error
	5	SCLK_ERR	0: No SCLK error (default) 1: SCLK error, write 0 to clear flag
	4	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write0 to clear flag
	3	OC_ERR	0: No OC error (default) 1: OC, write 0 to clear flag
	2	OV_ERR	0: No OV error (default) 1: OV, write 0 to clear flag
	1	OT_ERR	0: No OT error (default) 1: OT, write 0 to clear flag
	0	UV_ERR	0: No UV error (default) 1: UV, write 0 to clear flag

17.5.2 Protection Type

Protection	Auto-Recovery	Shutdown Amp (Latch Type)	Fault Pin Pull Low
DC Protection	No	Yes	Yes
OC ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[3]	Yes, but the MASK can be configured by the 0x11 bit[3]
OV ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[2]	Yes, but the MASK can be configured by the 0x11 bit[2]
OT ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[1]	Yes, but the MASK can be configured by the 0x11 bit[1]
UV ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[0]	Yes, but the MASK can be configured by the 0x1 bit[0]

When protection happened, there are 2 types of the protection behaviors to:

1. Latch type: Will shut down the AMP directly.
2. Auto-recovery type: The AMP will enter the auto recovery mode; until the protection behavior stops, the AMP will continue to work.
3. The DC protection only has the latch type.

17.6 Fault Behavior Type Select (FAULT_N2)

If the protection behavior happened, the IC will automatically start detection, there are some error types to be configured as the following list.

Address	BITS	Name	Description
0x12	3	OC_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery 1: Latch
	2	OV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery 1: Latch
	1	OT_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery 1: Latch
	0	UV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery 1: Latch

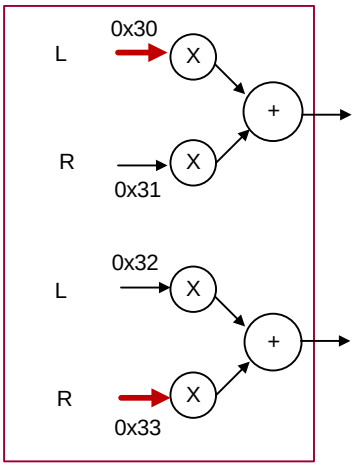
17.6.1 Fault Mask

Address	BITS	Name	Description
0x11	6	DC_ERROR_MASK	Fault mask for 0x10 DC error
	5	SCLK_ERROR_mask	Fault mask for 0x10 SCLK error
	4	LRCK_ERROR_mask	Fault mask for 0x10 LRCK error
	3	OC_ERROR_mask	Fault mask for 0x10 OC error
	2	OV_ERROR_mask	Fault mask for 0x10 OV error
	1	OT_ERROR_mask	Fault mask for 0x10 OT error
	0	UV_ERROR_mask	Fault mask for 0x10 UV error

17.7 Input Mixer (Change to SDO_Mixer_Page)

Block Diagram and Description

→ Input mixer range is from mute to 24dB, 1 step is 0.0625dB.



17.7.1 Input Mixer Control Flow

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	011: DSP signal process (IN/OUT MIXER SDO MIXER/EQ) → Set 0x0A Bit [2:0] with 011, then set below value.
2	0x30	31:0	CH1_IN_MIX_0	Input mixer for L ch
3	0x31	31:0	CH1_IN_MIX_1	Input mixer for R ch
4	0x32	31:0	CH2_IN_MIX_0	Input mixer for L ch
5	0x33	31:0	CH2_IN_MIX_1	Input mixer for R ch
6	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → After setting finished, set 0x0A Bit [2:0] with 000 to control page.

17.7.2 Mixer Gain Setting

Address	BITS	Name	Equation
0x30, 0x31, 0x32, 0x33	31:0	mix_1[31:0] mix_0[31:0]	Equation: 20Log (Dec / 67108864) Range: 24dB (0X3F654E69) to Mute (0x00000000) Example: 6dB, Gain = 20Log (133899787 / 67108864) = 6dB Hex = 0x7FB260B Dec = 133899787

Gain	Dec	Hex
6dB	133899787	0X7FB260B
. . .	. . .	. . .
0	67108864	0X04000000
. . .	. . .	. . .

17.7.3 Mixer Gain Inverse Setting

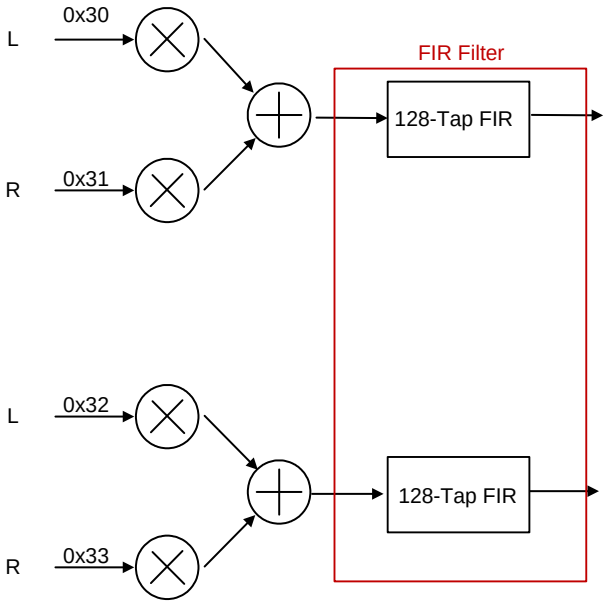
Address	BITS	Name	Equation
0x30, 0x31, 0x32, 0x33	31:0	mix_1[31:0] mix_0[31:0]	Equation: 20Log (Dec / 67108864) Range: 24dB (0X3F654E69) to Mute (0x00000000) Example: 6dB, Gain = 20Log (133899787 / 67108864) = 6dB Hex = 0xF804D9F5 Dec = –133899787

Gain	Dec	Hex
6dB	–133899787	0X F804D9F5
. . .	. . .	. . .
0	–67108864	0XFC000007
. . .	. . .	. . .

17.8 FIR Filter (When SRC disable)

Block Diagram and Description

→ There is a 128 tap FIR filter



17.8.1 FIR Control Flow

Step	Address	BITS	Name	Description
1	0x09	7:6	DSP_FIOW_SET	DSP flow set → Set 0x09 Bit[7:6] with 00, then set below.
2	0x08	5	SSRC_EN	Sampling rate converter enable internal process with 88.2k/96kHz sampling rate (support input Fs = 32kHz, 44.1k/48kHz) 0: Disable 1: Enable (default)
3	0x0D	6	FIR_EN	0: Bypass (default) 1: Enable
4	0x0A	2:0	REG_PAGE_SEL	101: DSP signal process (FIR) → Set 0x0A Bit[2:0] with 101, then set the coefficient.

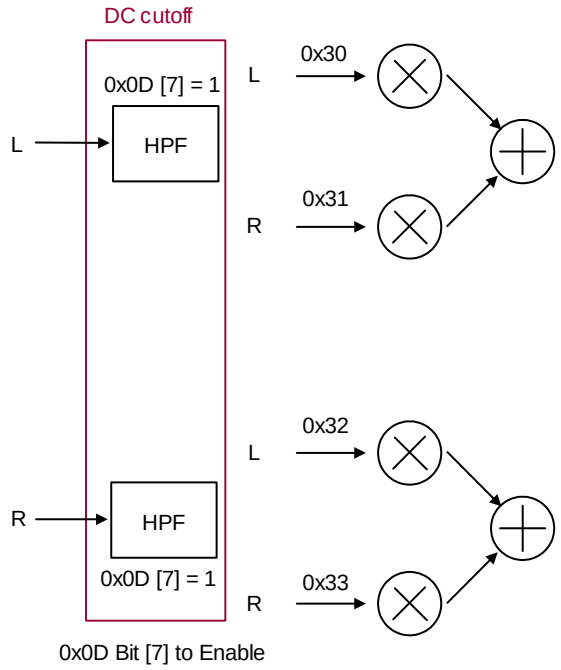
17.8.2 FIR Coefficient

Address	BITS	Name	Description
0x30 to 0xAF	31:0	FIR_TAP1 to FIR TAP128	FIR Coefficient

17.9 Input High Pass Filter (Control Page)

Block Diagram and Description

→ There are DC-Cut filter for each channel.



Address	BITS	Name	Description
0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to set.
0x0D	7	HPF_EN	0: Input high-pass filter disable 1: Input high-pass filter enable (default)

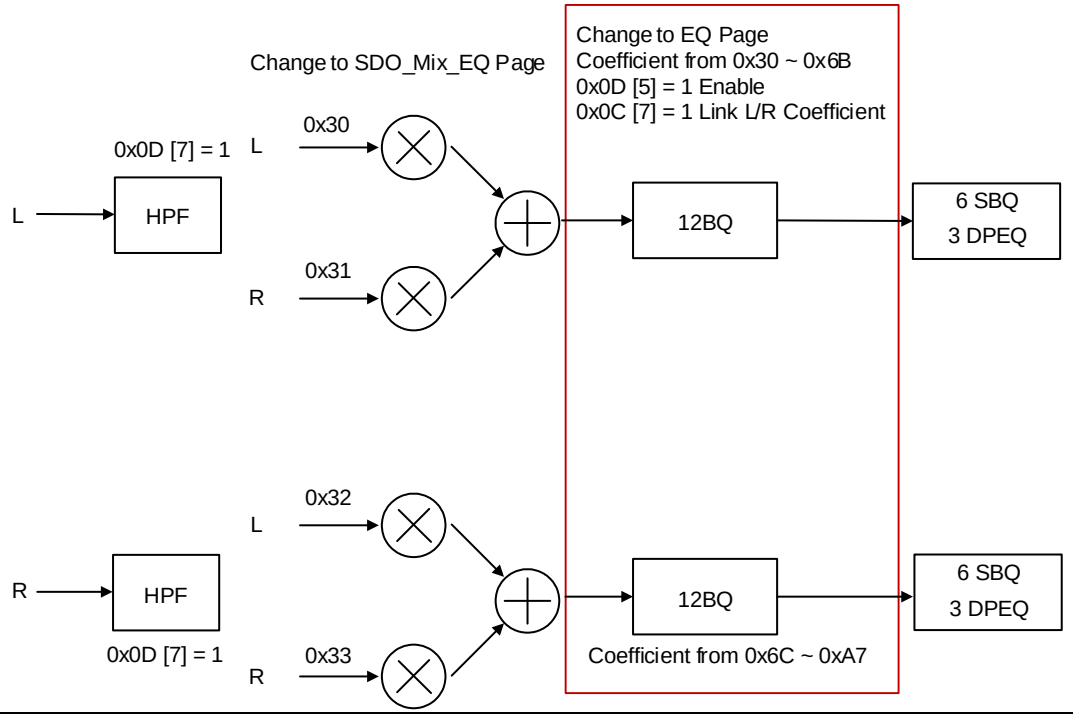
17.10 EQ Link and Bypass (Control Page)

Block Diagram and Description

→ Link L/R channel EQ parameter automatically and using the same parameter.

→ EQ_BYPASS can bypass the EQ path in signal path. Each EQ band has disable bit.

→ EQ link and bypass control will be controlled at control page.



17.10.1 EQ Function Control Flow

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x0C bit 5, and bit 7.
2	0x0D	5	EQ_EN	EQ filter enable 0: Bypass (default) 1: Enable
3	0x0C	7	EQ_Link_All	EQ1 to EQ12 0: CH1, CH2 independent 1: Take CH1 coefficients to CH2 (default)
4	0x0A	2:0	REG_PAGE_SEL	001: DSP signal process (EQ) → Select this page to control the EQ coefficient.

17.10.2 EQ Coefficient

Address	BITS	Name	Description
0x30 to 0x6B	4	CH1_EQ1_B0 to CH1_EQ12_A2	Coefficient for Ch1 EQ1 to Ch1 EQ 12
0x6C to 0xA7	4	CH2_EQ1_B0 to CH2_EQ12_A2	Coefficient for Ch2 EQ1 to Ch2 EQ 12

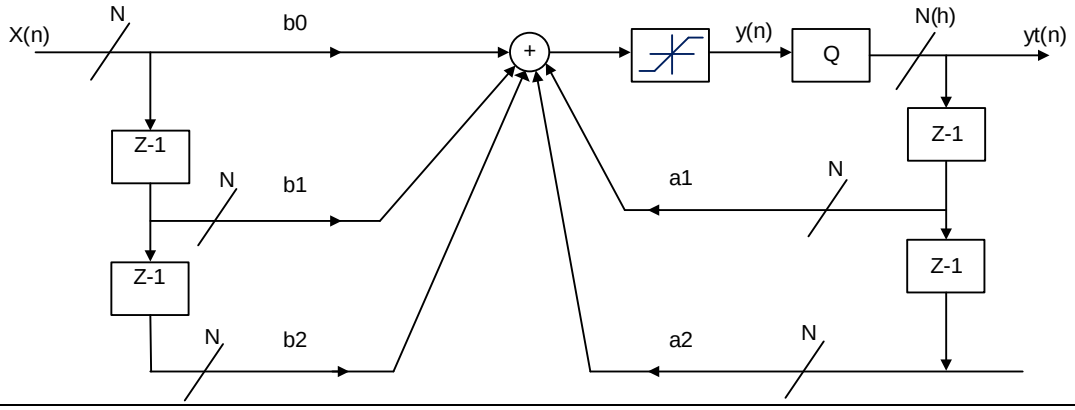
17.11 EQ

Block Diagram and Description

→ There are 12 Bands of Bi-Quad filter for each channel. So there are 18 bands of the Bi-Quad can be used including the smooth Bi-Quad.

EQ parameter: b0/b1/b2/a1/a2

Update coefficient after writing 5 coefficients

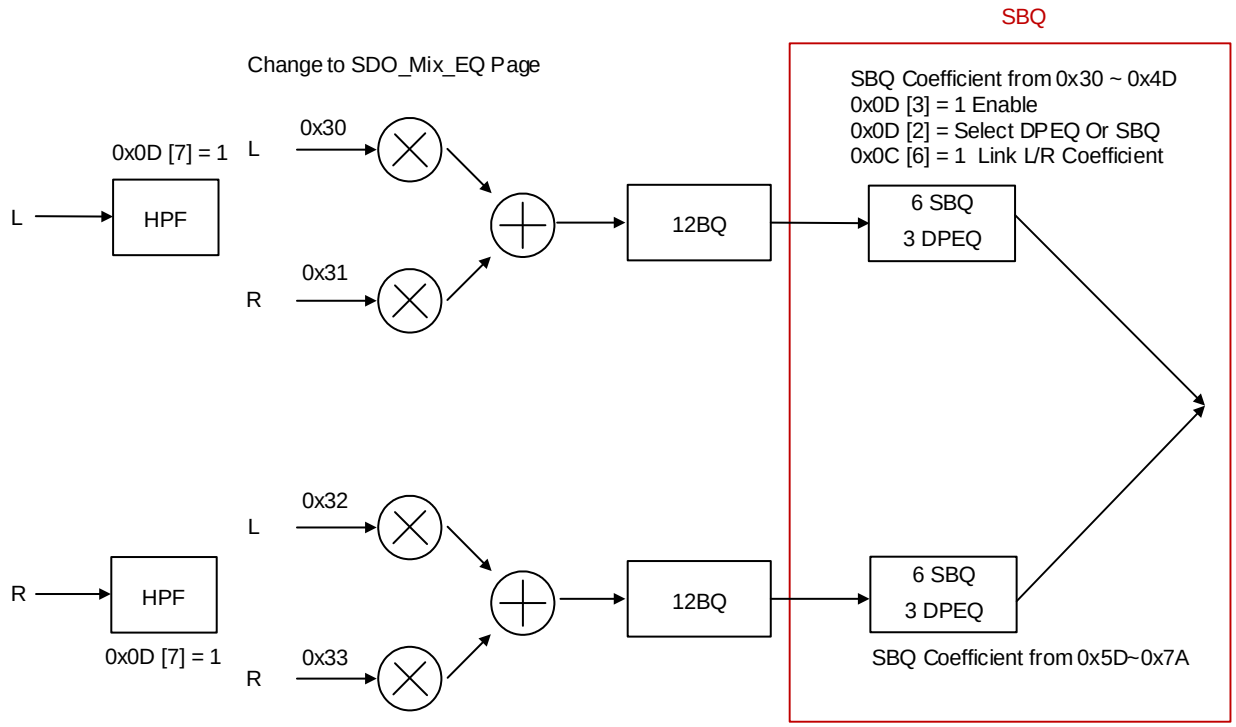


17.12 Smooth Bi-Quad

Block Diagram and Description

→ Smooth biquad is identical biquad filter with coefficient updated smoothly.

→ New coefficients update linearly/exponentially to avoid undesirable sound during setting new coefficient for biquad.



→ One smooth-BQ consists of 2 BQs to process the same audio signal in parallel. One of the BQs uses current coefficients and the other one uses updating coefficients to generate the outputs, BQ_1_output and BQ_2_output, respectively.

→ For a-filter smooth, the output of smooth-BQ is the summation of BQ_1_output and BQ_2_output using the below equations.

SBQ_output[n] = a_1[n] * BQ_1_output[n]+a_2[n] * BQ_2_output[n]

a_1[n] = (1-AS) + AS * a_1[n-1], if BQ_1 is the current active BQ and a_1[0] = 1

a_2[n] = (1-AS) + AS * a_2[n-1], if BQ_2 is the updating BQ and a_2[0] = 0

If SBQ_UPDATE is triggered, a_1[n] = 0 and a_2[n] = 1 after TS samples

→For linear smooth, the equations for smooth-BQ are listed below.

a_1[n] = a_1[n-1] - 1/TS, if BQ_1 is the active BQ and a_1[0] = 1

a_2[n] = a_2[n-1] + 1/TS, if BQ_2 is the updating BQ and a_2[0] = 0

If SBQ_UPDATE is triggered, a_1[n] = 0 and a_2[n] = 1 after TS samples. When linear smooth is used, the TS shall be the power of 2 for design simplicity.

Note: When using SMBQ, DPEQ cannot be used.

17.12.1 Smooth EQ Function Control Flow (Control Page)

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x0D, and 0x30.
2	0x0D	3	SMEQ_DPEQ_EN	Smooth EQ filter enable 0: Bypass (default) 1: Enable
3	0x0D	2	SMEQ_DPEQ_SEL	SMEQ DPEQ select 0: Smooth EQ (default) 1: Dynamic EQ
4	0x0C	6	SMEQ_DPEQ_LINK	Write coefficient option for SMEQ/DPEQ 0: L/R independent 1: L/R write the same data (default)
5	0x30	1:0	SBQ_UPDATE	Trigger smooth BQ coefficients update: 00: No update (default) 01: SBQ_BK1 to SBQ13, SBQ_BK2 to SBQ14 10: SBQ_BK1 to SBQ15, SBQ_BK2 to SBQ16 11: SBQ_BK1 to SBQ17, SBQ_BK2 to SBQ18
6	0x30	3	SMOOTH_DONE	Report status of smooth transition (after TS), 1 = done
7	0x30	6:4	SMOOTH_BQ_TS	SBQ smooth time select 000: 8 samples 001: 16 samples 010: 32 samples 011: 64 samples 100: 128 samples 101: 256 samples 110: 512 samples 111: 1024 samples (Recommended) (default)
8	0x0A	2:0	REG_PAGE_SEL	010: DSP signal process (SBQ/DPEQ) → Select this page to control the EQ coefficient.

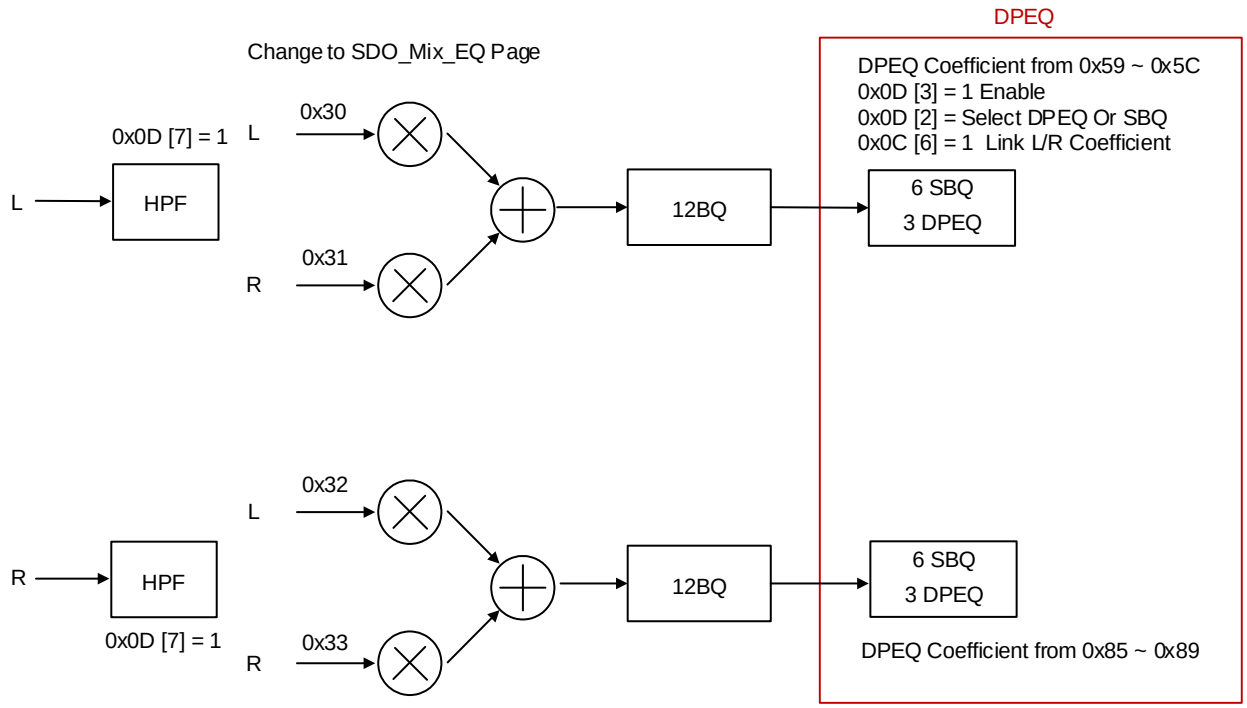
17.12.2 Smooth EQ Coefficient (Change to SBQ_DPEQ_Page)

Address	BITS	Name	Description
0x30to 0x4D	4	CH1_SEQ13 to CH1_ SEQ18	Coefficient for Ch1 SEQ13 to Ch1 SEQ18 coefficient
0x5D to 0x7A	4	CH2_SEQ13 to CH2_ SEQ18	Coefficient for Ch2 SEQ13 to Ch2 SEQ18 coefficient
0x4E to 0x57	4	CH1_SEQ_BK1 to CH1_SEQ_BK2	Coefficient for Ch1 SEQ13 to Ch18 SEQ update coefficient
0x7B to 0x84	4	CH2_SEQ_BK1 to CH2_SEQ_BK2	Coefficient for Ch2 SEQ13 to Ch18 SEQ update coefficient

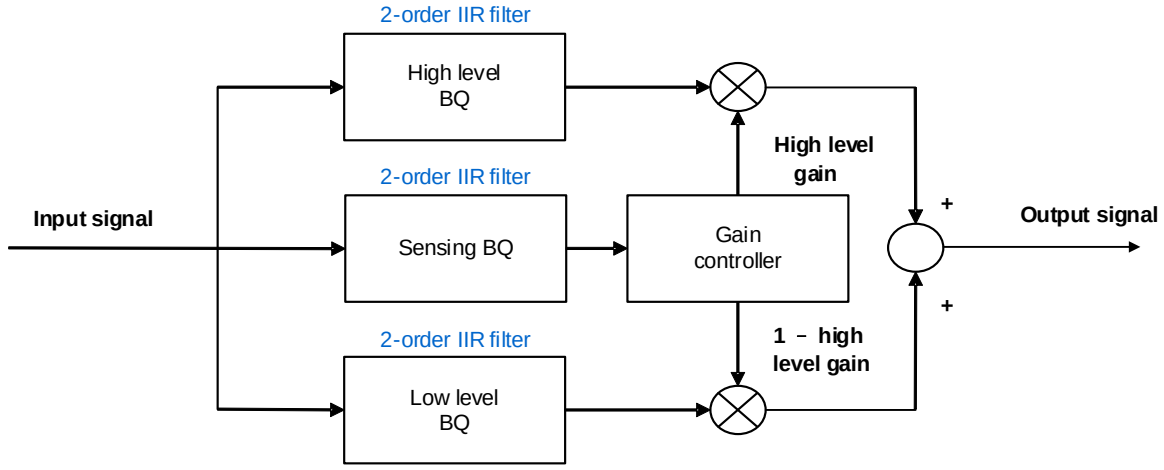
17.13 DPEQ

Block Diagram and Description

→ The dynamic equalizer provides the ballistic control of a dynamic range compressor to the conventional equalizer allowing time-varying adjustment of equalization curve.



→ Flow Chart



Note: When using DPBQ, SMBQ cannot be used.

17.13.1 DPEQ Function Control Flow (Control Page)

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x0D, and 0x0C.
2	0x0D	3	SMEQ_DPEQ_EN	0: Bypass (default) 1: Enable
3	0x0D	2	SMEQ_DPEQ_SEL	SMEQ DPEQ select 0: Smooth EQ (default) 1: Dynamic EQ
4	0x0C	6	SMEQ_DPEQ_SEL	Write coefficient option for SMEQ/DPEQ 0: L/R independent 1: L/R write the same data (default)
5	0x0A	2:0	REG_PAGE_SEL	010: DSP signal process (SBQ/DPEQ) → Select this page to control the EQ coefficient.

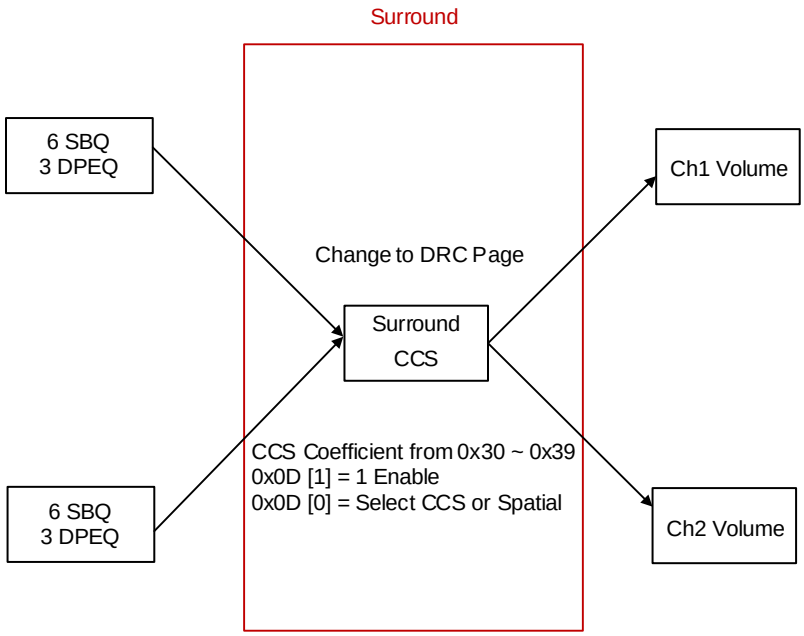
17.13.2 DPEQ Coefficient (Change to SBQ_DPEQ_Page)

Address	BITS	Name	Description
0x30 to 0x5C	4	CH1_DPEQ1 to CH1_DPEQ3	Coefficient for Ch1 DPEQ1 to Ch1 DPEQ3
0x5D to 0x89	4	CH2_DPEQ1 to CH2_DPEQ3	Coefficient for Ch2 DPEQ1 to Ch2 DPEQ3

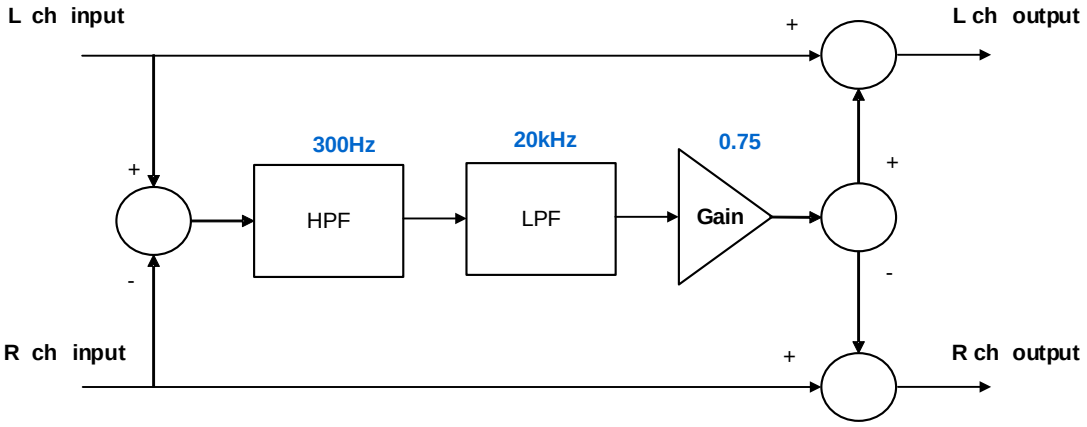
17.14 Surround (Spatializer)

Block Diagram and Description

→ Spatializer is a method to increase the field of sound for a broader and more encompassing audio experience.



→ Flow Chart



Note: When using Surround, CCS cannot be used.

17.14.1 Surround Function Control Flow (Control Page)

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x0D, and 0x0C.
2	0x0D	1	SURROUND_EN	Surround enable 0: Bypass (default) 1: Enable
3	0x0D	0	SURROUND_SEL	Select Surround (Spatializer) or CCS 0: Spatializer (default) 1: CCS
4	0x0C	5	Surround_LINK	Write coefficient option for SURROUND EQ 0: L/R independent 1: L/R write the same data (default)
5	0x0A	2:0	REG_PAGE_SEL	100: DSP signal process (SBQ/DPEQ) → Select this page to control the surround coefficient.

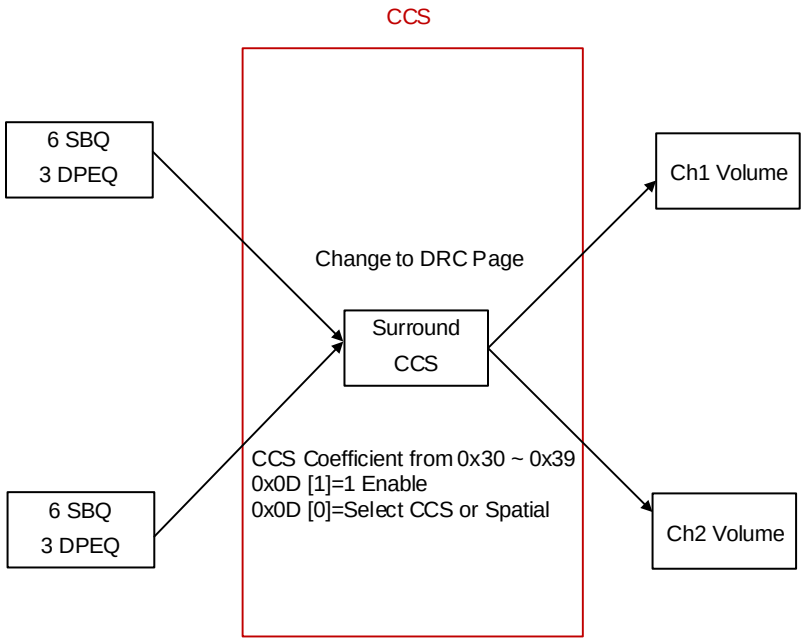
17.14.2 Surround Coefficient (Change to DRC Page)

Address	BITS	Name	Description
0x30 to 0x39	4	SURROUND_H1_B0 to SURROUND_H2_A2	Surround Bi-Quad Coefficient setting

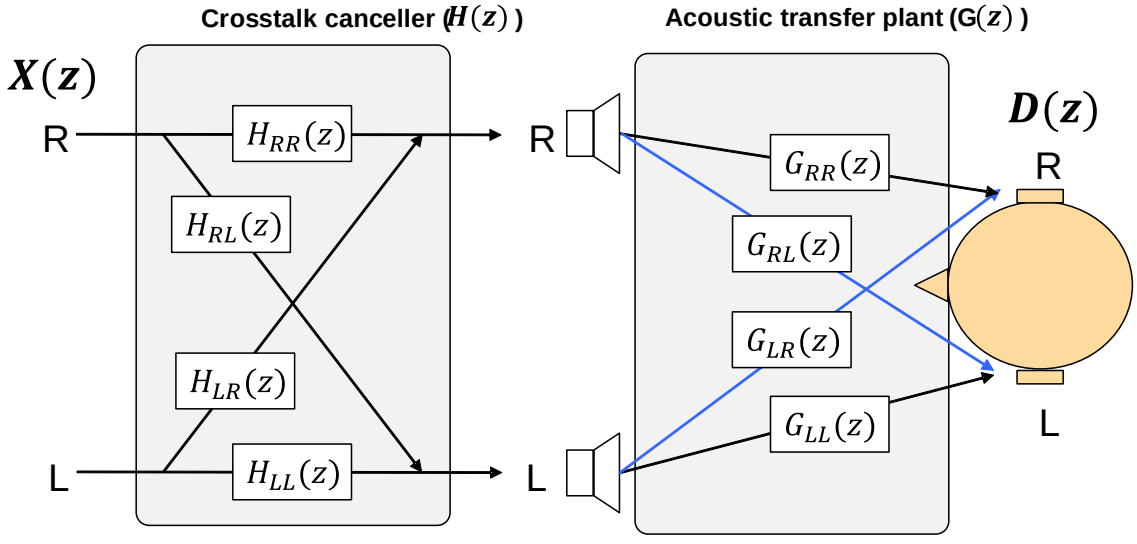
17.15 CCS (Cross Talk Cancellation System)

Block Diagram and Description

→ In general terms, any unwanted leakage between parallel information channels is considered crosstalk.



→ Flow Chart



Note: When using CCS, Surround cannot be used.

17.15.1 CCS Function Control (Control Page)

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x0D, and 0x0C.
2	0x0D	1	SURROUND_EN	Surround enable 0: Bypass (default) 1: Enable
3	0x0D	0	SURROUND_SEL	Select Surround (Spatializer) Or CCS 0: Spatializer (default) 1: CCS
4	0x0C	5	Surround_LINK	Write coefficient option for SURROUND EQ 0: L/R independent 1: L/R write the same data (default)
5	0x0A	2:0	REG_PAGE_SEL	100: DSP signal process (DRC) → Select this page to control the surround coefficient.

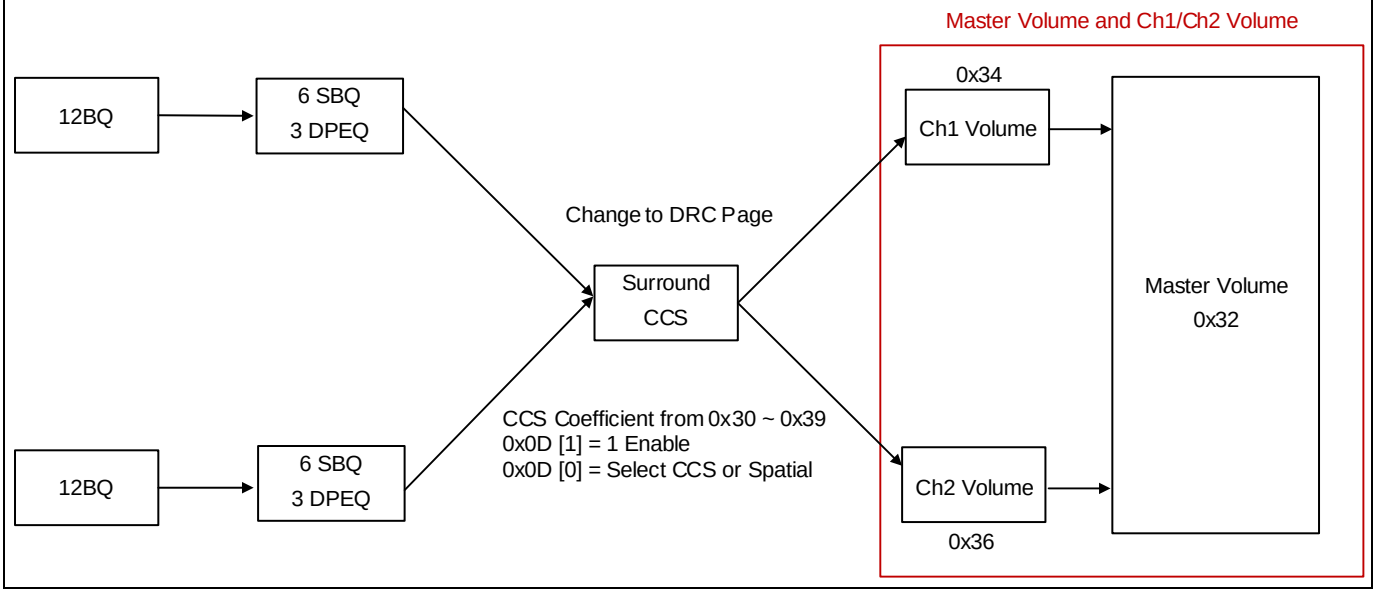
17.15.2 CCS Coefficient (Change to DRC Page)

Address	BITS	Name	Description
0x30 to 0x39	4	CCS_H1_B0 to CCS_H2_A2	CCS Bi-Quad Coefficient setting

17.16 Master Volume and Ch1/Ch2 Volume (Control Page)

Block Diagram and Description

→ The RT9125H has separate L/R channel volume control, also has the mater volume to control both L/R channel volume.



17.16.1 Volume Function Control

Address	BITS	Name	Description
0x32	10:0	MS_VOL	24dB to –103.9375dB, 0.0625dB per step
0x34	**10:0**	CH1_VOL	24dB to –103.9375dB, 0.0625dB per step
0x36	10:0	CH2_VOL	24dB to –103.9375dB, 0.0625dB per step

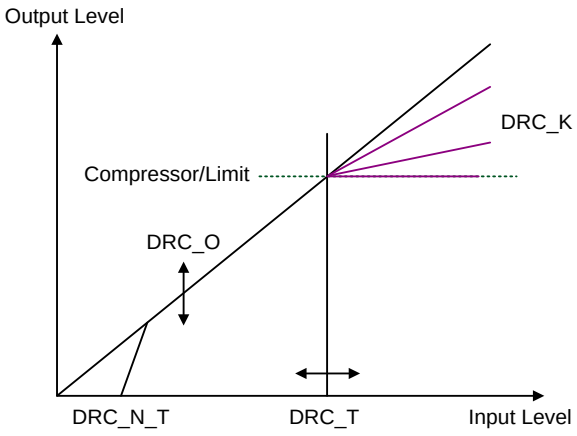
17.16.2 Master Volume and Ch1/Ch2 Gain Equation

Equation

Equation: 24dB - (Dec * 0.0625)
Range: 24dB (0X000) to mute (0x7ff)
Example: 10dB, Hex = 0xE0
Dec = 224
Gain = 24dB - (224 * 0.0625) = 10dB

Gain	Dec	Hex
24dB	0	0x00
10dB	224	0XE0
. . .	. . .	. . .
0dB	384	0x180
. . .	. . .	. . .

17.17 Multi-Band DRC (Change to DRC Page)

DRC Description	Address	Description
DRC_T: Threshold	0x98, 0x99, 0x9A, 0x9B	
DRC_K: Compress ratio	0x94, 0x95, 0x96, 0x97	
DRC_O: Make up gain	0xA0, 0xA1, 0xA2, 0xA3	
DRC_N_T: Noise gate threshold	0x9C, 0x9D, 0x9E, 0x9F	
Noise Gate Enable (Control Page)	0x0F	

17.17.1 DRC Noise Gate Control Flow

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x0F.
2	0x0F	3	DRC4_N_EN	1: DRC4 Noise gate enable 0: DRC4 Noise gate disable (default)
		2	DRC3_N_EN	1: DRC3 Noise gate enable 0: DRC3 Noise gate disable (default)
		1	DRC2_N_EN	1: DRC2 Noise gate enable 0: DRC2 Noise gate disable (default)
		0	DRC1_N_EN	1: DRC1 Noise gate enable 0: DRC1 Noise gate disable (default)

17.17.2 DRC Coefficient Control Flow (Change to DRC Page)

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	100: DSP signal process (DRC) → Select this page to control the below coefficient.

Address	BITS	Name	Description
Coefficient 1			
0x6C	31:0	DRC1_RMS_AE	DRC 1 AE
0x6D	31:0	DRC1_RMS_1-AE	DRC 1 1-AE
0x6E	31:0	DRC1_GAIN_AA	DRC 1 Attack time AA
0x6F	31:0	DRC1_GAIN_AD	DRC 1 Release time AD
0x98	31:0	DRC1_T	DRC1 threshold
0x94	31:0	DRC1_K	DRC1 compression ratio
0xA0	31:0	DRC1_O	DRC1 make up gain
0x70	31:0	DRC2_RMS_AE	DRC 2 AE
0x71	31:0	DRC2_RMS_1-AE	DRC 2 1-AE
0x72	31:0	DRC2_GAIN_AA	DRC 2 Attack time AA
0x73	31:0	DRC2_GAIN_AD	DRC 2 Release time AD
0x99	31:0	DRC2_T	DRC2 threshold
0x95	31:0	DRC2_K	DRC2 compression ratio
0xA1	31:0	DRC2_O	DRC2 make up gain
0x74	31:0	DRC3_RMS_AE	DRC 3 AE
0x75	31:0	DRC3_RMS_1-AE	DRC 3 1-AE
0x76	31:0	DRC3_GAIN_AA	DRC 3 Attack time AA
0x77	31:0	DRC3_GAIN_AD	DRC 3 Release time AD
0x9A	31:0	DRC3_T	DRC3 threshold

Address	BITS	Name	Description
0x96	31:0	DRC3_K	DRC3 compression ratio
0xA2	31:0	DRC3_O	DRC3 make up gain
0x78	31:0	DRC4_AE	DRC 4 AE
0x79	31:0	DRC4_1-AE	DRC 4 1-AE
0x7A	31:0	DRC4_AA	DRC 4 Attack time AA
0x7B	31:0	DRC4_AD	DRC 4 Release time AD
0x9B	31:0	DRC4_T	DRC4 threshold
0x97	31:0	DRC4_K	DRC4 compression ratio
0xA3	31:0	DRC4_O	DRC4 make up gain
0x9C	31:0	DRC1_N_T	DRC1 noise gate of the DRC
0x9D	31:0	DRC2_N_T	DRC2 noise gate of the DRC
0x9E	31:0	DRC3_N_T	DRC3 noise gate of the DRC
0x9F	31:0	DRC4_N_T	DRC4 noise gate of the DRC
0xB4	7:0	DRC4_DELAY	DRC4 Delay 2
Coefficient 2			
0x84	31:0	DRC1_RMS_AE_2	DRC 1 AE 2
0x85	31:0	DRC1_RMS_1-AE_2	DRC 1 1-AE 2
0x86	31:0	DRC1_GAIN_AA_2	DRC 1 Attack time AA 2
0x87	31:0	DRC1_GAIN_AD_2	DRC 1 Release time AD 2
0xA8	31:0	DRC1_T_2	DRC1 threshold 2
0xA4	31:0	DRC1_K_2	DRC1 compression ratio 2
0xB0	31:0	DRC1_O_2	DRC1 make up gain 2
0x88	31:0	DRC2_RMS_AE_2	DRC 2 AE 2
0x89	31:0	DRC2_RMS_1-AE_2	DRC 2 1-AE 2
0x8A	31:0	DRC2_GAIN_AA_2	DRC 2 Attack time AA 2
0x8B	31:0	DRC2_GAIN_AD_2	DRC 2 Release time AD 2
0xA9	31:0	DRC2_T_2	DRC2 threshold 2
0xA5	31:0	DRC2_K_2	DRC2 compression ratio 2
0xB1	31:0	DRC2_O_2	DRC2 make up gain 2
0x8C	31:0	DRC3_RMS_AE_2	DRC 3 AE 2
0x8D	31:0	DRC3_RMS_1-AE_2	DRC 3 1-AE 2
0x8E	31:0	DRC3_GAIN_AA_2	DRC 3 Attack time AA 2
0x8F	31:0	DRC3_GAIN_AD_2	DRC 3 Release time AD 2
0xAA	31:0	DRC3_T_2	DRC3 threshold 2
0xA6	31:0	DRC3_K_2	DRC3 compression ratio 2
0xB2	31:0	DRC3_O_2	DRC3 make up gain 2
0x90	31:0	DRC4_AE_2	DRC 4 AE 2

Address	BITS	Name	Description
0x91	31:0	DRC4_1-AE_2	DRC 4 1-AE 2
0x92	31:0	DRC4_AA_2	DRC 4 Attack time AA 2
0x93	31:0	DRC4_AD_2	DRC 4 Release time AD 2
0xAB	31:0	DRC4_T_2	DRC4 threshold 2
0xA7	31:0	DRC4_K_2	DRC4 compression ratio 2
0xB3	31:0	DRC4_O_2	DRC4 make up gain 2
0xAC	31:0	DRC1_N_T_2	DRC1 noise gate of the DRC 2
0xAD	31:0	DRC2_N_T_2	DRC2 noise gate of the DRC 2
0xAE	31:0	DRC3_N_T_2	DRC3 noise gate of the DRC 2
0xAF	31:0	DRC4_N_T_2	DRC4 noise gate of the DRC 2
0xB5	7:0	DRC4_DELAY_2	DRC4 Delay 2

17.18 DRC Timing Equation

<table>
<tr><th>DRC Description</th><th>Equation</th></tr>
<tr><td>AA/AE/AD Timing,
6.26 Format</td><td>Equation: AA = (1-e-2.2 / (ta*fs)) * 67108864
ta = AA/AD/AE timing
fs = sampling rate
Example: ta = 0.1ms, fs = 96k
AA = (1-e(-2.2 / (0.0001 * 96000))) * 67108864=13744156
DEC = 1577592
HEX = 0xD1B81C

<table><tr><th>Timing</th><th>T_Dec</th><th>T_Hex</th></tr><tr><td>0.1ms</td><td>13744156</td><td>0xD1B81C</td></tr><tr><td>.
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.</td><td>.
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.</td></tr><tr><td>1000ms</td><td>1536</td><td>0x601</td></tr><tr><td>.
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<tr><td>1-AE</td><td>Equation: 1-AE = (e-2.2/(ta*fs)) * 67108864
ta = 1-AE timing
fs = sampling rate
Example: ta = 0.1ms, fs = 96k
1-AE = (e(-2.2 / (0.0001 * 96000))) * 67108864=53364707
DEC = 53364707
HEX = 0x32E47E3

<table><tr><th>Timing</th><th>T_Dec</th><th>T_Hex</th></tr><tr><td>0.1ms</td><td>13744156</td><td>0x32E47E3</td></tr><tr><td>.
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Note: For peak mode, 1-AE, must be defined by users and there is no limitation.
For RMS mode, there is no need to define the omega value.</td></tr>
</table>

17.18.1 DRC Formula

<table>
<tr><th>DRC Description</th><th>Equation</th></tr>
<tr><td>DRC Threshold/Noise Gate Threshold</td><td>T is the threshold of the DRC
Equation: T = (Threshold) / 0.0625 (dB)
Example: Threshold = –10dB,
10/0.0625 = 160
T_Dec = 160
T_Hex = DEC2HEX (160) = 0xA0

<table><tr><th>Threshold</th><th>T_Dec</th><th>T_Hex</th></tr><tr><td>–10dB</td><td>160</td><td>0x00, 0xA0</td></tr><tr><td>.
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.</td></tr><tr><td>–20dB</td><td>320</td><td>0x01, 0x40</td></tr><tr><td>.
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<tr><td>DRC RATIO: Compress Ratio</td><td>K is the compression ratio of the DRC
Equation: K = Ratio * 125
Example: Ratio = 50%
50 * 125 = 64
K_Dec = 64
K_Hex = DEC2HEX (64) = 0x40

<table><tr><th>Ratio</th><th>K_Dec</th><th>K_Hex</th></tr><tr><td>Full Comp</td><td>128</td><td>0x80</td></tr><tr><td>.
.
.</td><td>.
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.</td><td>.
.
.</td></tr><tr><td>50%</td><td>64</td><td>0x40</td></tr><tr><td>.
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.</td></tr></table></td></tr>
<tr><td>DRC MAKEUP: Make Up Gain</td><td>O is the offset of the DRC
Equation: O = ABS[(Offset-24) / 0.0625]
Example: Offset = 6dB
(6-24) / 0.0625 = 288
O_Dec = 288
O_Hex = DEC2HEX (288) = 0x120

<table><tr><th>Offset</th><th>O_Dec</th><th>O_Hex</th></tr><tr><td>–10dB</td><td>544</td><td>0x02, 0x20</td></tr><tr><td>.
.
.</td><td>.
.
.</td><td>.
.
.</td></tr><tr><td>6dB</td><td>288</td><td>0x01, 0x20</td></tr><tr><td>.
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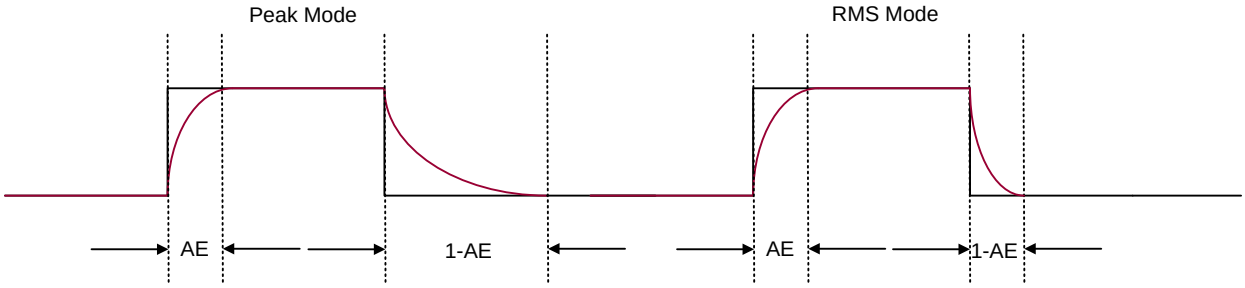
.</td></tr></table></td></tr>
</table>

17.19 Peak Mode RMS Mode (Control Page)

Block Diagram and Description
→ The detecting threshold using different calculated methods. Peak mode: AE and 1-AE is independent RMS mode: AE + (1-AE) = 1



17.19.1 DRC Peak Control Flow

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x0E.
2	0x0E	7	DRC4_PEAK	1: Peak mode (default) 0: RMS mode
		6	DRC3_PEAK	1: Peak mode (default) 0: RMS mode
		5	DRC2_PEAK	1: Peak mode (default) 0: RMS mode
		4	DRC1_PEAK	1: Peak mode (default) 0: RMS mode

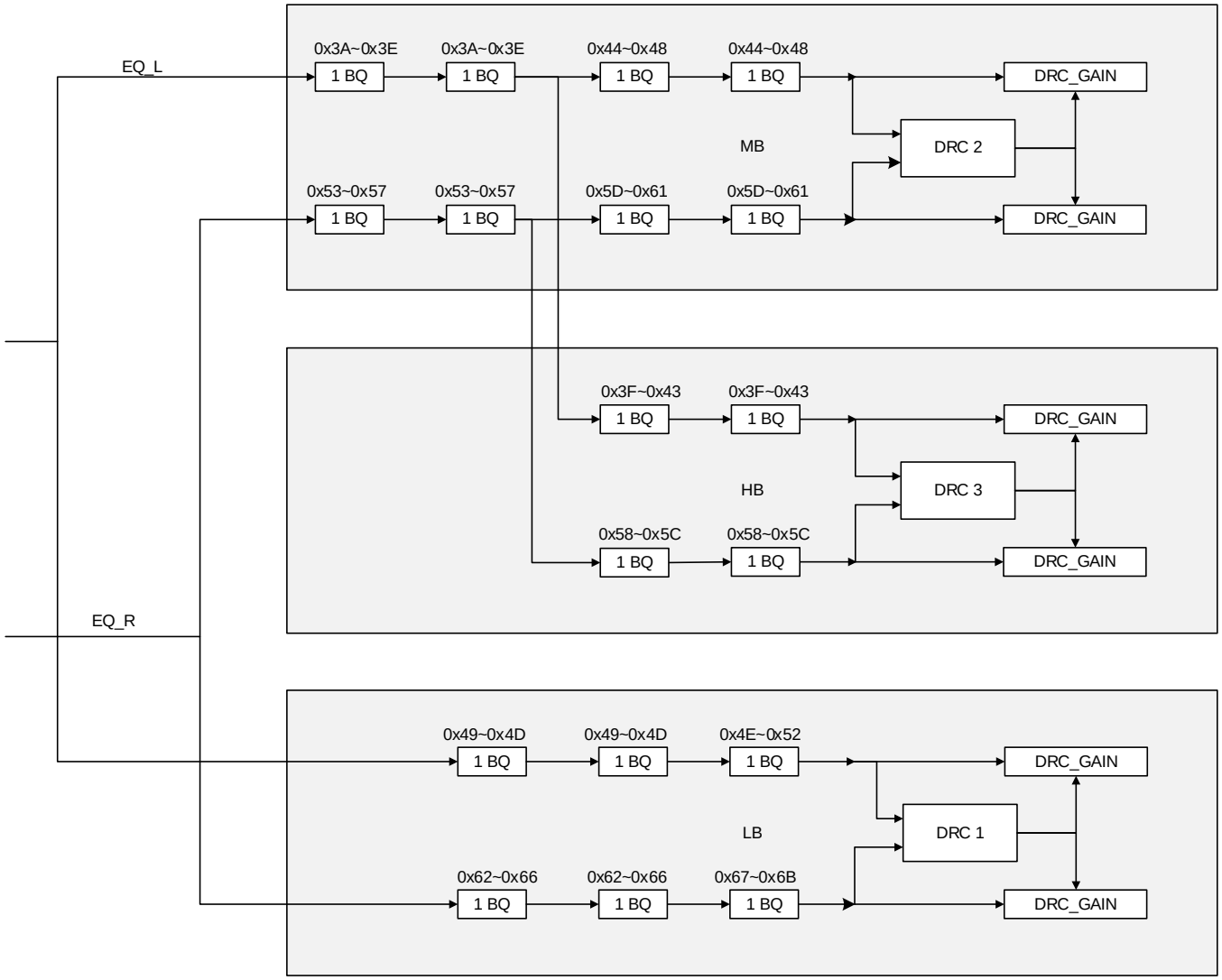
17.20 DRC Enable (Control Page)

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x0F.
2	0x0F	7	DRC4_EN	DRC4 Enable (Final DRC) 1: Enable 0: Disable (default) →When disable, input signal is the same as output signal. → Final stage DRC enable (DRC4)
		6	DRC3_EN	DRC3 Enable (H band) 1: Enable 0: Disable (default) → When disable, input signal is the same as output signal. → Final stage DRC enable (DRC3)
		5	DRC2_EN	DRC2 Enable (M band) 1: Enable 0: Disable (default) → When disable, input signal is the same as output signal. → Final stage DRC enable (DRC2)
		4	DRC1_EN	DRC1 Enable (L_band) 1: Enable 0: Disable (default) → When disable, input signal is the same as output signal. → Final stage DRC enable (DRC1)

17.21 Multi Band DRC EQ

Block Diagram and Description

→ To adjust the cut off frequency of the DRC1, 2, 3



17.21.1 DRC_EQ Link Control Flow (Control Page)

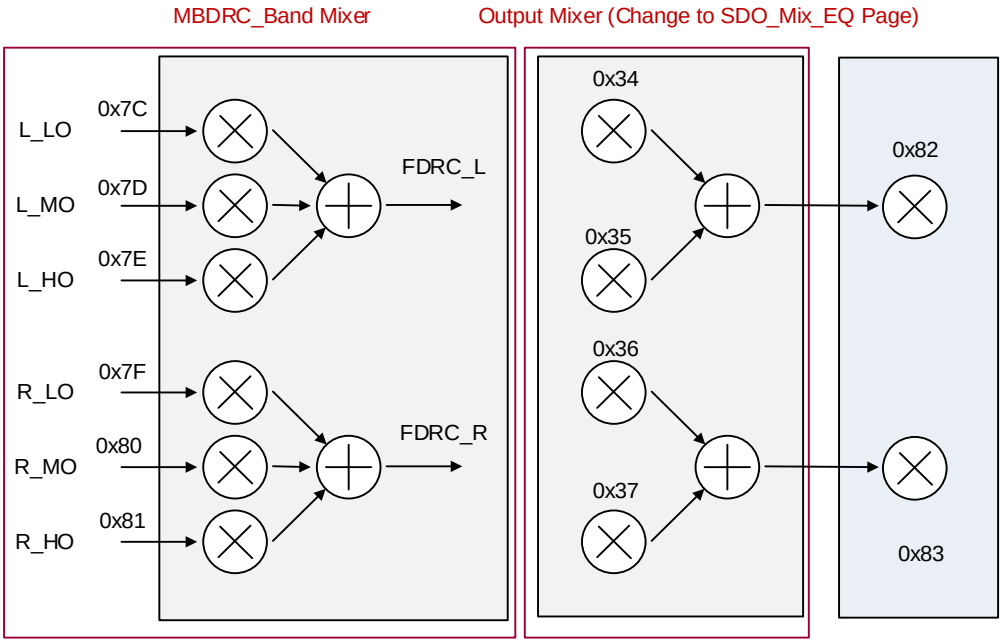
Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x0F.
2	0x0C	4	MBDRC_EQ_LINK	Write coefficient option for MBDRC EQ 0: L/R independent 1: L/R write the same data (default)

17.21.2 DRC_EQ Coefficient Control Flow

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	100: DSP signal process (DRC) → Select this page to control the below coefficient.
2	0x3A to 0x6B	31:0	HB_CH1_BQ1_B0	High Band Ch1 BQ1 B0
		. . .		
		31:0	LB_CH2_BQ2_A2	Low Band Ch2 BQ2 A2

17.22 MBDRC/Output Mixer (Change to DRC Page)

Block Diagram and Description



Note: Output Mixer only available when MRDRC using same coefficient.

17.22.1 MBDRC/Band Mixer/Output Control Flow

Step	Address	BITS	Name	Description
1	0x0A	2:0	REG_PAGE_SEL	100: DSP signal process (DRC) → Select this page to control the below coefficient.
	0x7C	31:0	CH1_OUT_MIX_L	Ch1 L band output mixer
	0x7D	31:0	CH1_OUT_MIX_M	Ch1 M band output mixer
	0x7E	31:0	CH1_OUT_MIX_H	Ch1 H band output mixer
	0x7F	31:0	CH2_OUT_MIX_L	Ch2 L band output mixer
	0x80	31:0	CH2_OUT_MIX_M	Ch2 M band output mixer
	0x81	31:0	CH2_OUT_MIX_H	Ch2 H band output mixer
2	0x0A	2:0	REG_PAGE_SEL	011: DSP signal process (IN/OUT MIXER SDO MIXER/EQ) → Select this page to control the below coefficient.
	0x34	31:0	CH1_OUT_MIX_0	Ch1 1 output Mixer 0 Note 1: Default signal flow is from CH1_OUT_MIX_0 Note 2: Change to SDO_Mix_Page to control output mixer coefficient
	0x35	31:0	CH1_OUT_MIX_1	Ch1 1 output Mixer 1 Note: Change to SDO_Mix_Page to control output mixer coefficient
	0x36	31:0	CH2_OUT_MIX_0	Ch2 1 output Mixer 0 Note: Change to SDO_Mix_Page to control output mixer coefficient

Step	Address	BITS	Name	Description
	0x37	31:0	CH2_OUT_MIX_1	Ch2 1 output Mixer 1 Note: • Default signal flow is from CH2_OUT_MIX_1 • Change to SDO_Mix_Page to control output mixer coefficient.

17.22.2 Output/MBDRC Mixer Gain Setting

Address	BITS	Name	Equation
0x7C to 0x81 For Band Mixer 0x34 to 0x37 for Output Mixer	31:0	mix_1[31:0] mix_0[31:0]	Equation: 20Log (Dec / 67108864) Range: 24dB (0X3F654E69) to Mute (0x00000000) Example: 6dB, Gain = 20Log (133899787 / 67108864) = 6dB Hex = 0x7FB260B Dec = 133899787

Gain	Dec	Hex
6dB	133899787	0X7FB260B
. . .	. . .	. . .
0	67108864	0X04000000
. . .	. . .	. . .

17.22.3 Mixer Gain Inverse Setting

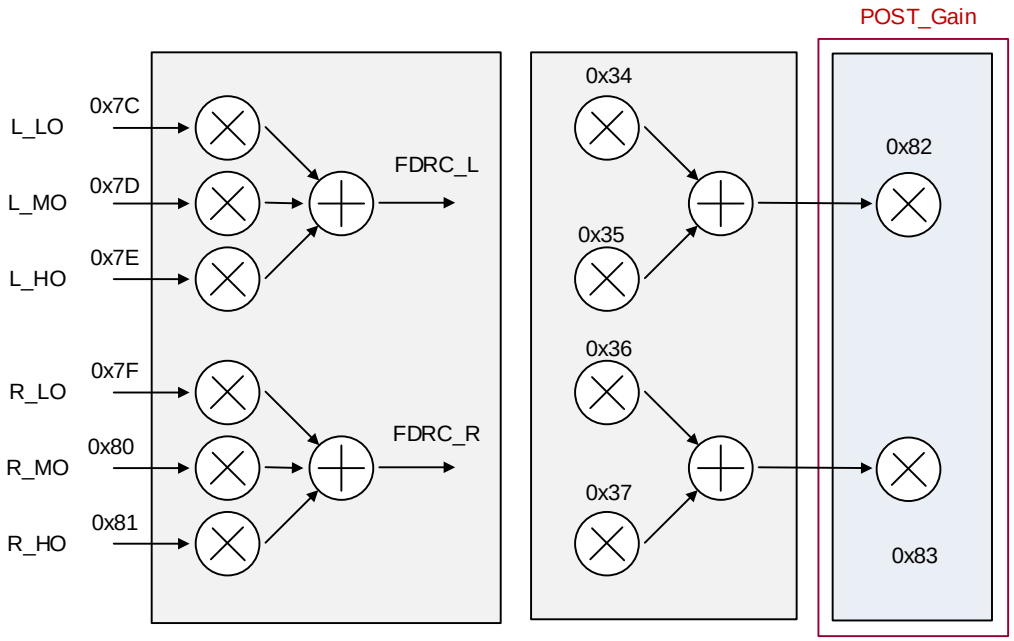
Address	BITS	Name	Equation
0x7C to 0x81 For Band Mixer 0x34 to 0x37 for Output Mixer	31:0	mix_1[31:0] mix_0[31:0]	Equation: 20Log (Dec / 67108864) Range: 24dB (0X3F654E69) to Mute (0x00000000) Example: 6dB, Gain = 20Log (133899787 / 67108864) = 6dB Hex = 0xF804D9F5 Dec = –133899787

Gain	Dec	Hex
6dB	–133899787	0X F804D9F5
. . .	. . .	. . .
0	–67108864	0XFC000007
. . .	. . .	. . .

17.23 Post-Gain (Change to DRC Page)

Block Diagram and Description

→ The gain stage after output mixer



17.23.1 Post Gain Control Flow

Address	BITS	Name	Equation
0x0A	2:0	REG_PAGE_SEL	100: DSP signal process (DRC) → Select this page to control the below coefficient.
0x82	31:0	Ch1_POST_SCALE	Equation: 10^(((Gain/20)) + LOG(2^26)) Range: 24dB (0xFFC09AB197) to Mute (0xFFFFFFFD61) Example: 6dB, Hex = 0xF804D9F5 Dec = –133899787 Gain = 20Log (255 / 128) = 6dB
0x83	31:0	Ch2_POST_SCALE	

Gain	Dec	Hex
6dB	–133899787	0x F804D9F5
. . .	. . .	. . .
0dB	–67108864	0xFC000000
. . .	. . .	. . .

17.24 Volume Ramp

00: 4.33ms from mute to 0dB (0.5dB/20.83μs) (default)

01: 8.66ms from mute to 0dB (0.25dB/20.83μs)

10: 17.33ms from mute to 0dB (0.125dB/20.83μs).

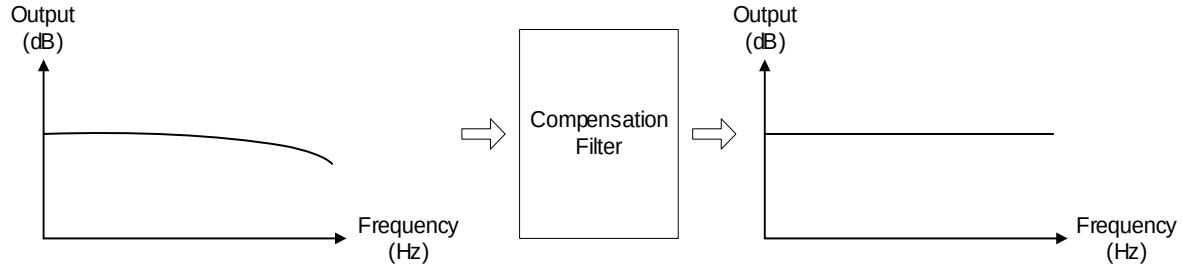
11: 34.65ms from mute to 0dB (0.0625dB/20.83μs).

Address	BITS	Name	Description
0x32	13:12	VOL_RAMP_MODE[13:12]	00: 4.33ms from mute to 0dB (0.5dB/20.83μs) (default) 01: 8.66ms from mute to 0dB (0.25dB/20.83μs) 10: 17.33ms from mute to 0dB (0.125dB/20.83μs) 11: 34.65ms from mute to 0dB (0.0625dB/20.83μs)

Note 23. The ramp time is fixed, it will not be affected by the sampling rate.

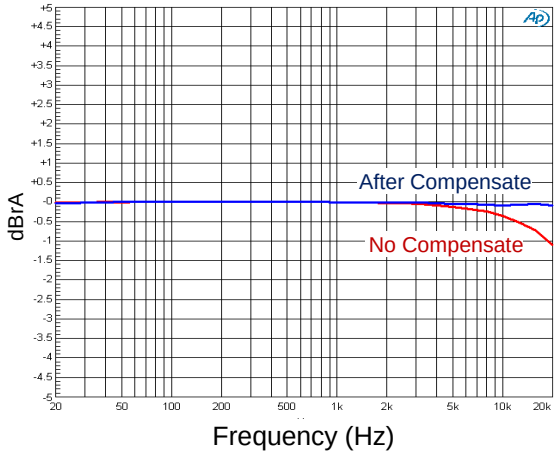
17.25 Compensate Filter

Compensation filter is aimed to compensate internal gain from DAC, this filter can also compensate the frequency response affected by LC filter. The recommended setting will be based on different application circuits to fit the curve.



Compensate Description	Equation
Compensate	y[n] = B3* x [n-6] + B2* x [n-5] + B1* x [n-4] + B0* x [n-3] + B1* x [n-2] + B2* x [n-1] + B3* x [n] B0, B1, B2, B3: Compensate coefficient N: Input signal when applied

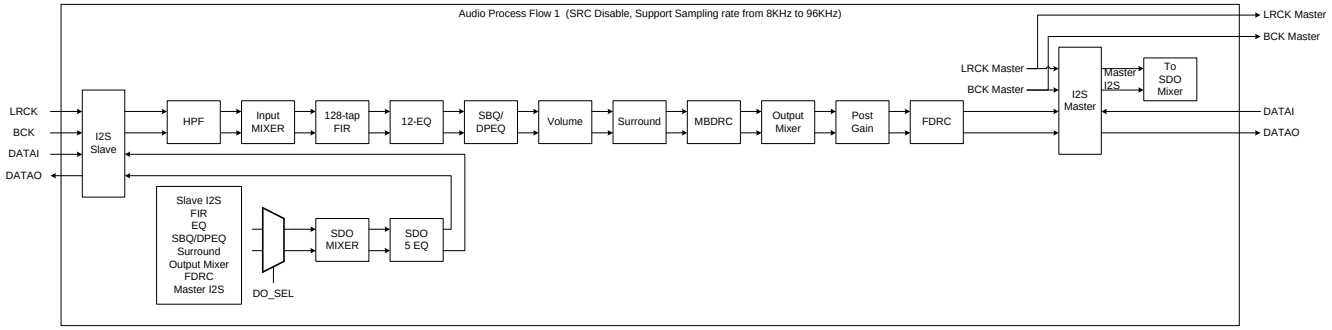
Address	BITS	Name	Description
0x06	6	COMP_EN	1: Compensation filter enable 0: Compensation filter disable (default)
0x3A	16:0	COMP_B0	Compensate B0, B1, B2, and B3 coefficient
0x3B	16:0	COMP_B1	
0x3C	16:0	COMP_B2	
0x3D	16:0	COMP_B3	



17.26 Data Output (Control Page)

Block Diagram and Description

→ The RT9125H has SDO output which can configure signal output after processor.
→ The SDO output consist output mixer, and 5 Bi-Quad, which can be used for sub-woofer application.



17.26.1 SDO Control Function

Address	BITS	Name	Description
0x0A	2:0	REG_PAGE_SEL	000: sys ctrl → Select this page to control the 0x03
0x03	7:4	SDO_SEL	0000: No output (default) 0001: I^2S interface 0010: 128-tap FIR 0011: EQ BQ 0100: Smooth BQ/ DPEQ 0101: Spatializer/CCS 0110: Output Mixer 0111: Final DRC Others: No output

17.26.2 SDO Output Mixer Control (Change to SDO_Mixer Control)

Address	BITS	Name	Description
0x0A	2:0	REG_PAGE_SEL	011: DSP signal process (IN/OUT MIXER SDO MIXER/EQ) → Select this page to control the 0x38, 0x39, 0x3A, and 0x3B.
0x38	31:0	SDO_CH1_IN_MIX_0	Ch1 SDO output mixer 0 Note: Default signal is from Ch1 SDO output mixer 0
0x39	31:0	SDO_CH1_IN_MIX_1	Ch1 SDO output mixer 1
0x3A	31:0	SDO_CH2_IN_MIX_0	Ch2 SDO output mixer 0
0x3B	31:0	SDO_CH2_IN_MIX_1	Ch2 SDO output mixer 1 Note: Default signal is from Ch2 SDO output mixer 1

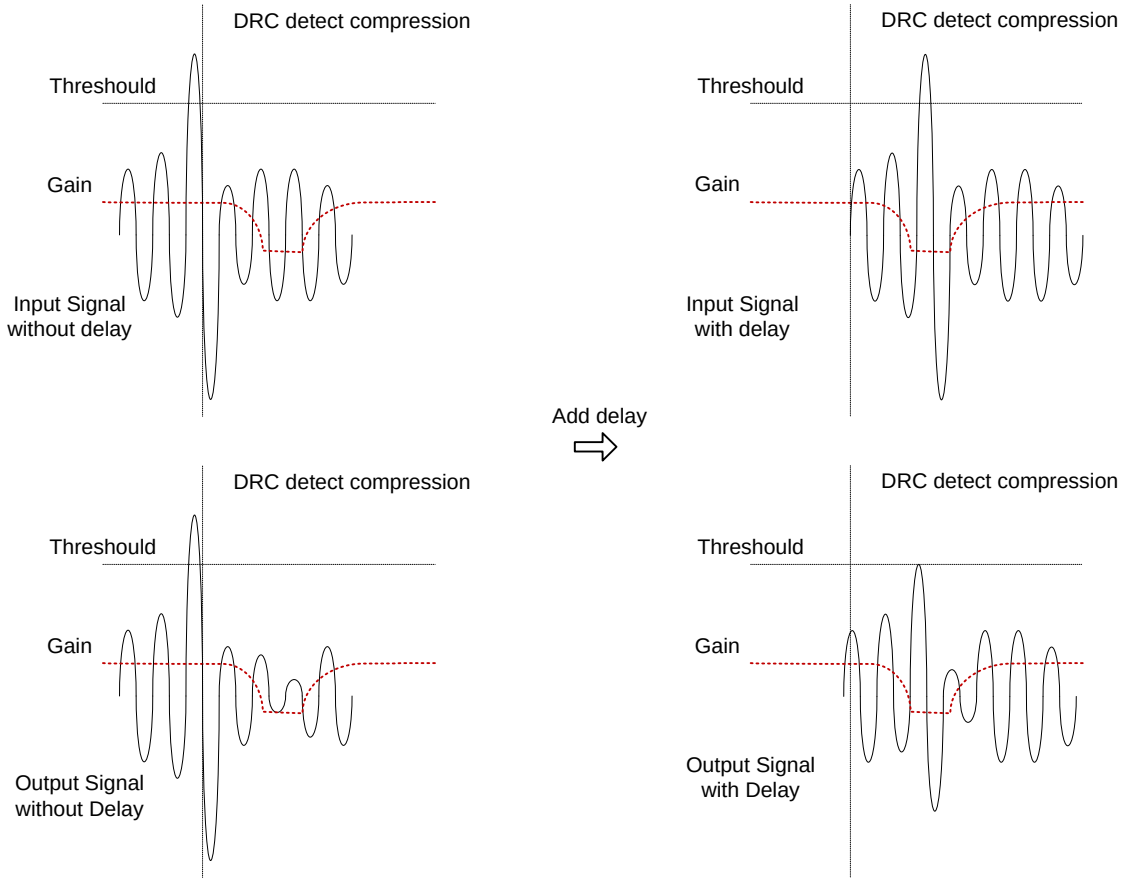
17.26.3 SDO EQ Coefficient

Address	BITS	Name	Description
0x0A	2:0	REG_PAGE_SEL	011: DSP signal process (IN/OUT MIXER SDO MIXER/EQ) → Select this page to control the below EQ coefficient.
0x3C	31:0	SDO1_BQ1_B0	Ch1 SDO BQ 1 coefficient BO
. . .			
0x6D	31:0	SDO2_BQ5_A1	Ch2 SDO BQ 5 coefficient A1

DRC4 is final stage of DRC. It can be configured as the final DRC to limit the output power. (Change to DRC Page)

Block Diagram and Description

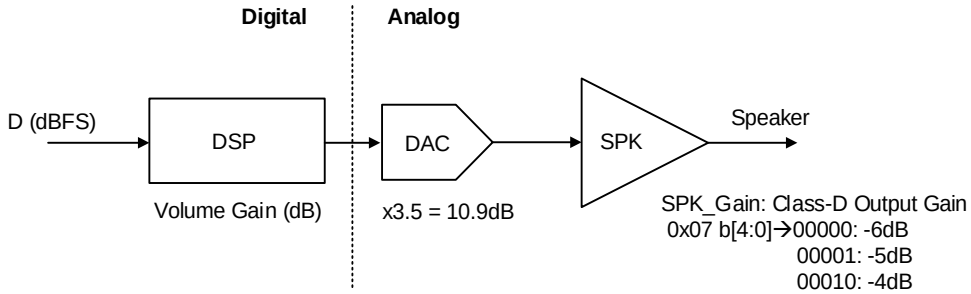
→ Make the audio output signal lately.



Delay = (DRC4_Delay) * 1 / Sample rate

Address	BITS	Name	Description
0x0A	2:0	REG_PAGE_SEL	100: DSP signal process (DRC) → Select this page to control the below coefficient.
0xB4	7:0	DRC4_DELAY	DRC4_DELAY → DRC 4 delay for channel 1
0xB5	7:0	DRC4_DELAY 2	DRC4_DELAY 2 → DRC 4 delay for channel 2

17.27 Amplification Gain



Address	BITS	Name	Description
0x07	4:0	D_SPK_GAIN[4:0]	Class-D output gain 00000: –6dB 00001: –5dB 00010: –4dB 00011: –3dB 00100: –2dB 00101: –1dB 00110: 0dB 00111: 1dB 01000: 2dB 01001: 3dB 01010: 4dB 01011: 5dB 01100: 6dB 01101: 7dB 01110: 8dB 01111: 9dB 10000: 10dB 10001: 11dB 10010: 12dB 10011: 13dB (default) 10100: 14dB 10101: 15dB 10110: 6dB 10111: 17dB 11000 ~ 11111: No setting

17.28 Master Volume Gain

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0x20</td><td>10:0</td><td>MS_VOL[10:0]</td><td>Equation: 24dB - (Dec x 0.0625)
Range: 24dB (0X000) to mute (0x7ff)
Example: 10dB, Hex = 0xE0
Dec = 224
Gain = 24dB - (224 x 0.0625) = 10dB
<table><tr><th>Gain</th><th>Dec</th><th>Hex</th></tr><tr><td>24dB</td><td>0</td><td>0x00</td></tr><tr><td>10dB</td><td>224</td><td>0XE0</td></tr><tr><td>.
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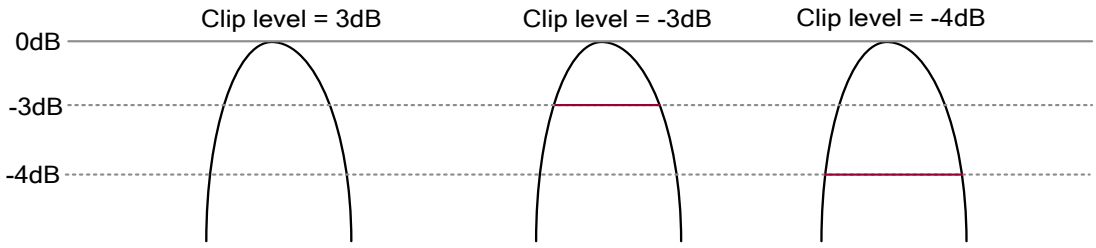
</table>

17.29 Hard Clip Function

To clip the signal with different threshold, operate in time domain.



Address	BITS	Name	Description
0x06	0	HARD_CLIP_EN	0: Disable hard clip (default) 1: Enable hard clip
0x27	10:0	HARD_CLIP_TH[10:0]	Hard clip threshold for hard clip, when threshold > 0, there is no any clipping effect happened. 11'h180: 0dB 0.0625db per step Note: Due to there is –2dB at digital filter, so hard clipping only works when threshold < –2dB.

17.30 PBTL Function

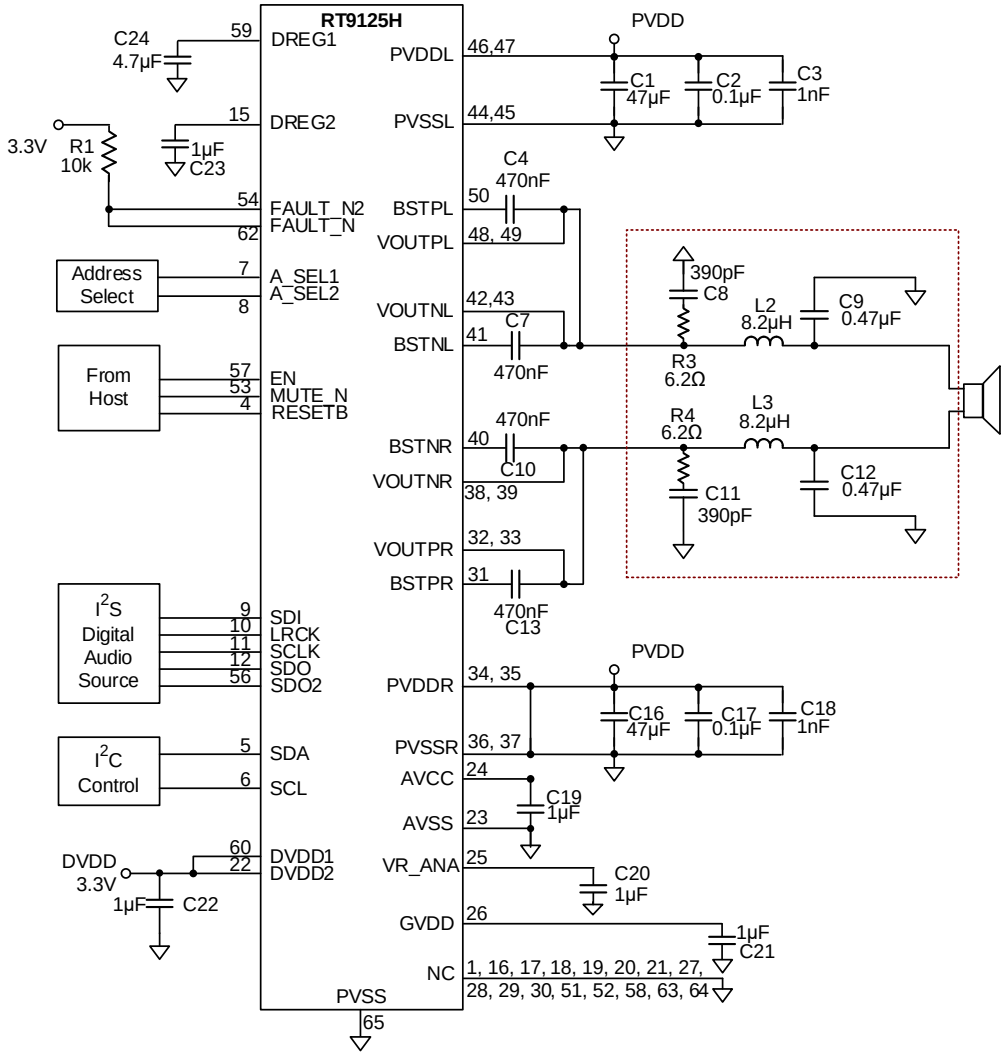
It can be configured by the hardware, and also need to change the software setting

The input signal can be configured by the input mixer, from register 0x30 to configure the input signal. The default signal for the PBTL is from 0x30 L channel signal.

Address	BITS	Name	Description
0x05	4	D_PBTL	0 : BTL (default) 1 : PBTL

Address	BITS	Name	Description
0x30	16:0	CH1_IN_MIX_0	u[23:17], mix_0[16:0] u : Unused
0x31	16:0	CH1_IN_MIX_1	u[23:17], mix_1[16:0] u : Unused

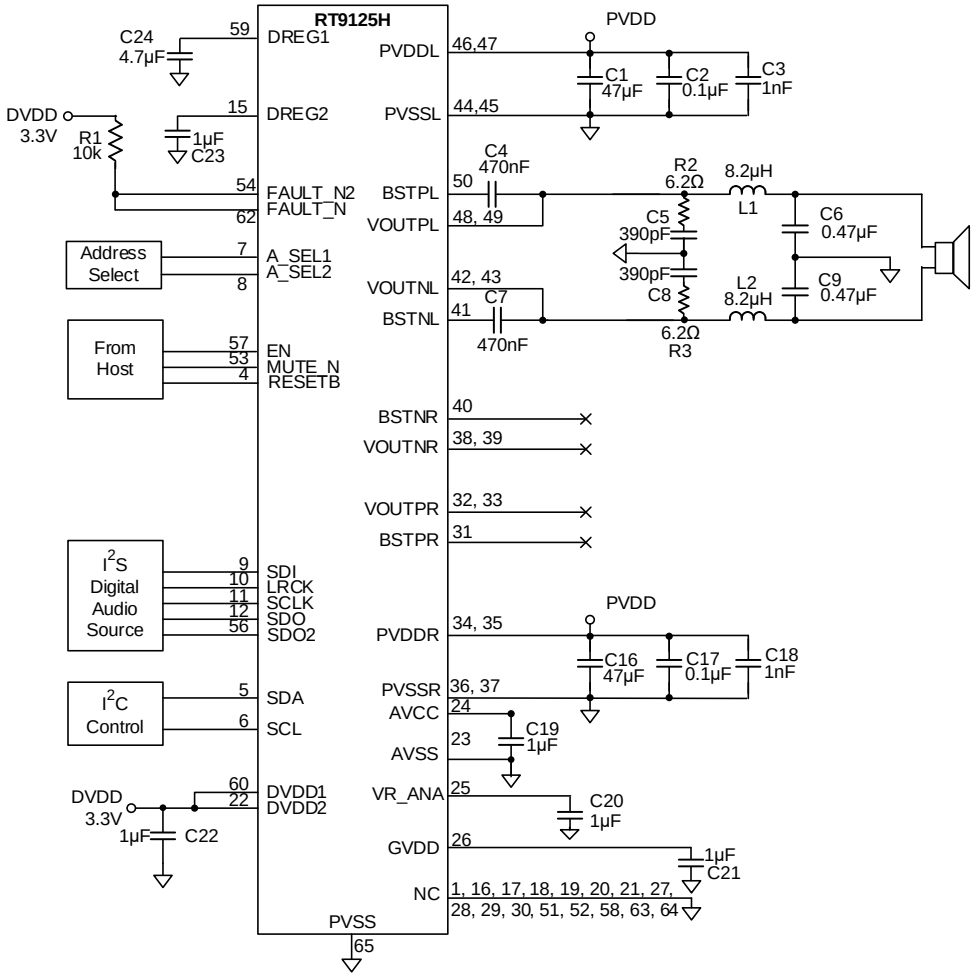
17.30.1 Mono PBTL Application Circuit

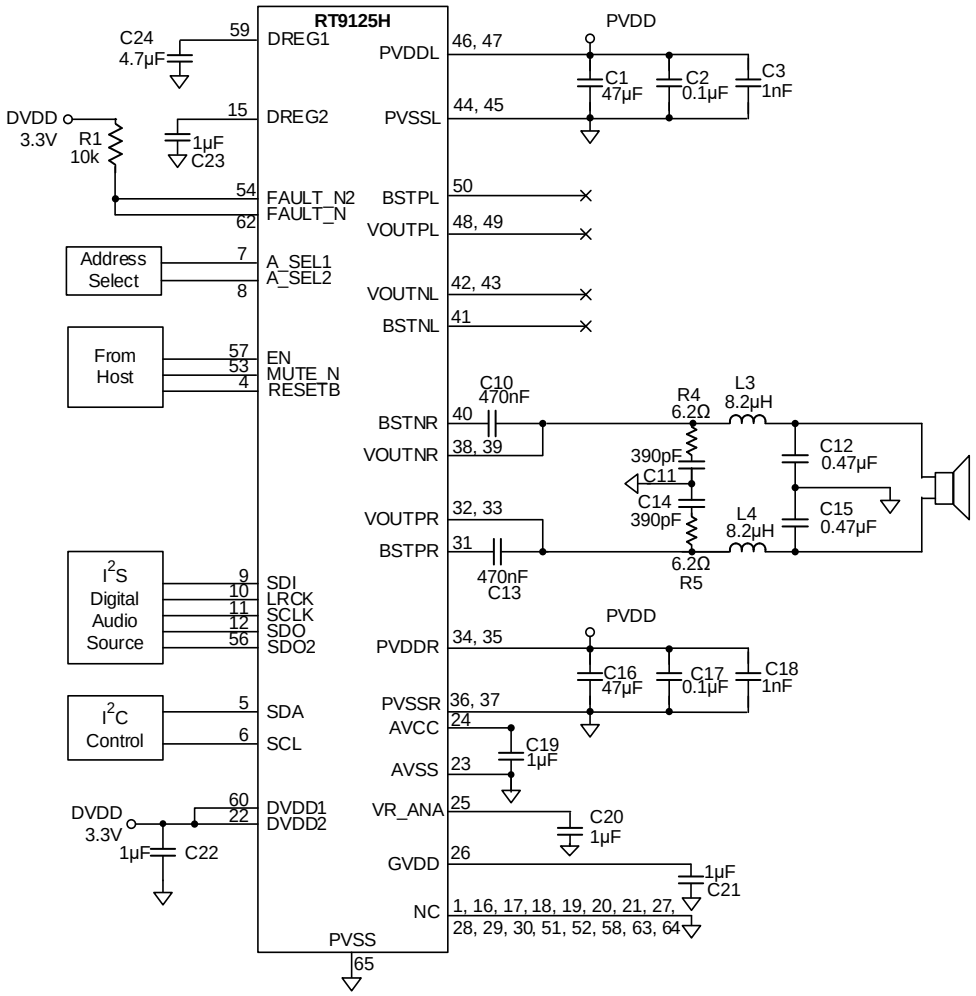


17.30.2 Mono Configuration

To use the mono configuration, it can be configured by register setting.

Address	BITS	Name	Description
0x15	7	D_RLPF_EN	DAC RCH LPF enable 0: Force off 1: Follow sequence (default)
	6	D_LLPF_EN	DAC LCH LPF enable 0: Force off 1: Follow sequence (default)
	5	D_EN_RCH_PWR	RCH PWR stage enable 0: Force off 1: Follow sequence (default)
	4	D_EN_LCH_PWR	LCH PWR stage enable 0: Force off 1: Follow sequence (default)
	3	D_RDAC_EN	DAC RCH enable 0: Force off 1: Follow sequence (default)
	2	D_LDAC_EN	DAC LCH enable 0: Force off 1: Follow sequence (default)
	1	D_EN_MD_RCH	MD RCH enable 0: Force off 1: Follow sequence (default)
	0	D_EN_MD_LCH	MD LCH enable 0: Force off 1: Follow sequence (default)

Mono Configuration	Example
Use Left Channel	Set the Bit[7], Bit[5], Bit[3], Bit[1] to Zero, others keep 1 

Mono Configuration	Example
Use Right Channel	Set the Bit[6], Bit[4], Bit[2], Bit[0] to Zero, others keep 1 

18 Operation

18.1 Error Reporting

The FAULT_N, and FAULT_N2 pin is for reporting error status. The FAULT_N, and FAULT_N2 go to low when protection happens. This pin is open-drain configuration, a pull-up resistor is needed.

18.2 Clock Detection

The RT9125H can accept SCLK to be as 32fs, 48fs and 64fs and support only a 1xfs LRCK. The internal oscillator will check SCLK input constantly. If clock is lost, the RT9125H will shut down the power stage automatically.

18.3 Volume Control

The RT9125H has master volume MS_VOL and each channel volume CH1_VOL, CH2_VOL control. The step of each volume is 0.0625dB per step, from 24dB to mute. CH1 and CH2 also have each mute control, CH1_MUTE and CH2_MUTE.

18.4 Overvoltage Protection

The RT9125H monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin rises above the overvoltage threshold, 28V (minimum), the OVP circuit turns off the output immediately and operates in auto-recovery mode, or the latch mode can also be configured in operation.

18.5 Over-Temperature Protection

The over-temperature protection function will turn off the power MOSFET when the junction temperature exceeds 150°C (minimum). Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation, or the latch mode can also be configured in operation.

18.6 Dynamic Range Enhancement

The dynamic range enhancement enhances the dynamic range for the application. It will optimize the noise during operation.

18.7 Built-In Anti-POP Function

An internal soft-start function controls the duty ramp-up rate of the output PWM voltage to minimize the POP noise during start-up. Similarly, when power shuts down, the duty also ramp-down to eliminate the POP noise. This function also acts when the PWDN_N pin turns ON/OFF.

18.8 Overcurrent Protection

The RT9125H provides OCP function to prevent the device from damages during overload or short-circuit conditions.

The current function is detected by an internal sensing circuit. Once when the inductor short to each other and to GND, the OCP function is designed to operate the latch mode.

18.9 Undervoltage Protection

The RT9125H monitors the voltage on PVDD voltage threshold. When the voltage on the PVDDL/R pin falls below the undervoltage threshold, 4V (which can be programmable), the UVP circuit turns off the output immediately, or the latch mode can be configured in operation.

18.10 OLD/SLD Function

The RT9125H adapt the over load detection and short load detection, which can be used to detect the speaker terminal is short or open.

18.11 CRC Check Function

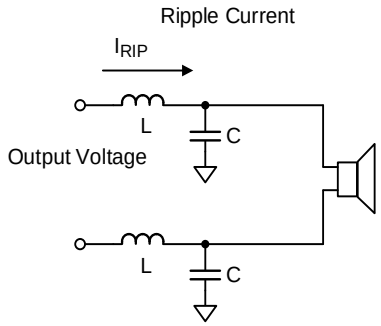
The RT9125H adapt the CRC checksum function which can check the register coefficient.

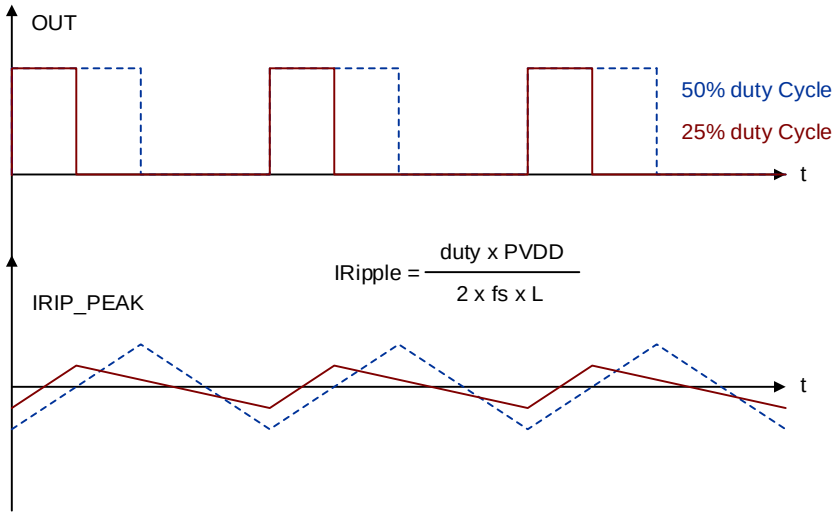
18.12 Multi signal path option

The RT9125H adapt the 2 signal path which can be configured by different application.

18.13 CMH Common Mode Hopping Mode

The RTQ9125H build-in Common Mode Hopping (CMH) mode to reduce pulse width at small signal, inductor current ripple is reduced, and hence light load efficiency is improved.





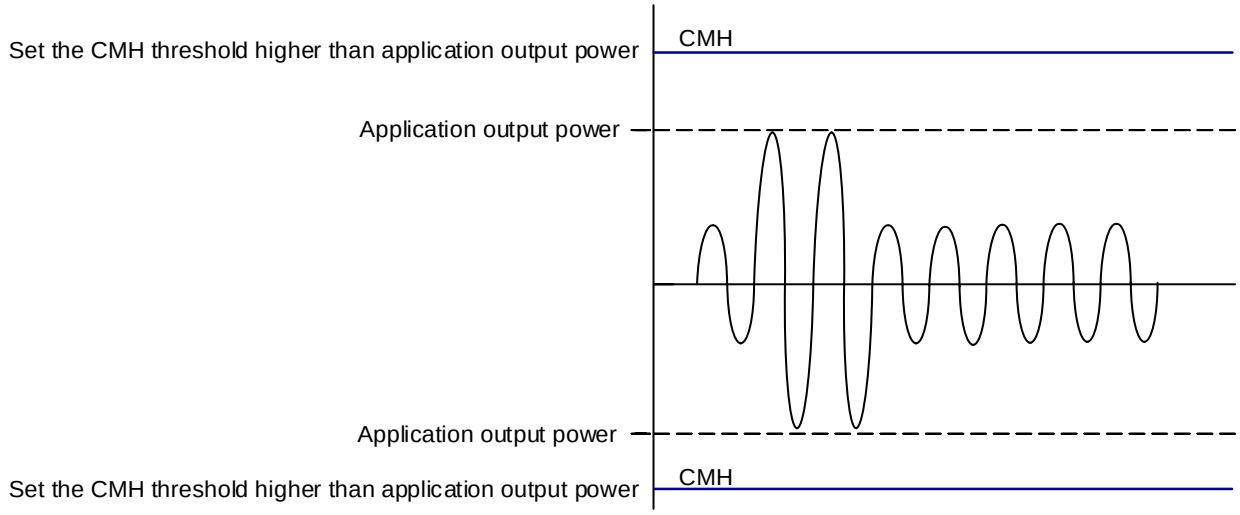


Figure 3. Current Ripple with CMH

Address	BITS	Name	Equation
0x94	7:0	D_CMH_TH [7:0]	CMH threshold: 20*log10(CMH_TH/2^8) + 2dB Output power: $10^{(D+Vol\_Gain)}/20$ x 3.5 x Output_Gain (Vp) Use the output power to calculate the CMH threshold. Note: • If application output power is 12W, please set the CMH threshold higher than 12W, like 13W, 14W, or 15W. By set register 0x94. • For the CMH threshold, recommended threshold not over 11Vp for 4W. • For 6W, recommended not over 12.2Vp.

18.14 Spread Spectrum

There are two methods, one is spread spectrum frequency, the other is added noise to triangular modulation.

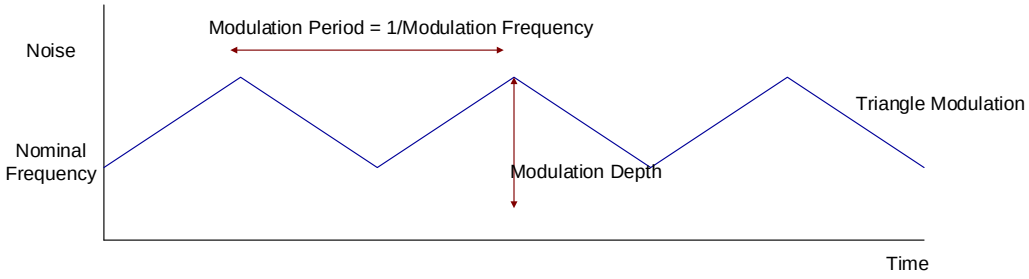


Figure 4. Current Ripple with CMH

Address	BITS	Name	Description
0x09	7	D_FSS_EN	Spread spectrum enable 0: Disable (default) 1: Enable
	6	PWM_MODEWHITE	Noise select 0: pink noise (default) 1: white noise
	5	PWM_SELCOEF	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4
	4	PWM_NOISE_EN	Add noise to TRI_GEN 0: disable (default) 1: enable
	3:2	D_NOISE_AMP	Nosie amplitude for SSC 00: 5.78% (default) 01: 11.55% 10: 17.33% 11: 23.1%
	1:0	D_FSS_AMP	Spread spectrum frequency variation amplitude 00: 16.60% 01: 33.19% (default) 10: 33.19% 11: 49.79%

18.15 PWM Phase Change

The RT9125H has channel to channel phase control function. Channel 1 is used as a reference for other channels, and channel 2 output PWM phase can be shifted from 0 to 315 degree, each step 45 degree.

Address	BITS	Name	Description
0x07	7:5	D_PWM_PHASE	PWM output phase select 000: 0 (default) 001: 45 010: 90 011: 135 100: 180 101: 225 110: 270 111: 315

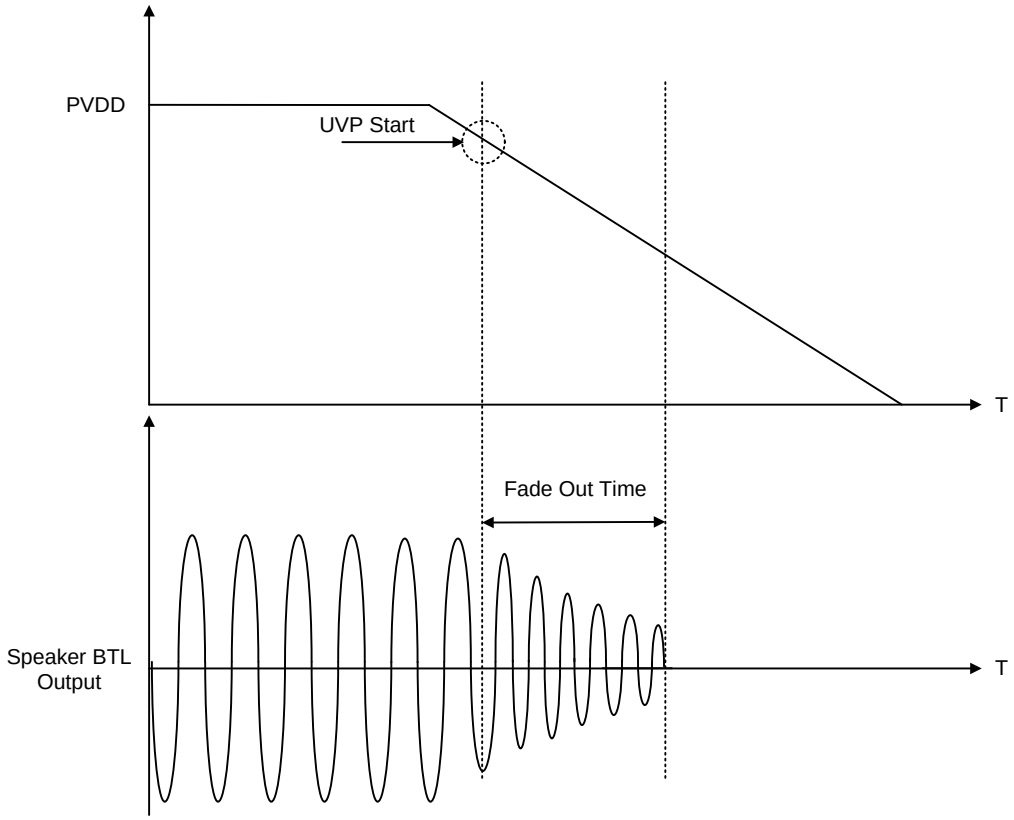
18.16 UVP Speaker Fade Out Function

The RT9125H has UVP fade function, which is used for the when suddenly AC pull off.

Block Diagram and Description

UVP voltage selection for PVDD

The UVP voltage can programmable. Once PVDD voltage drops below the preset value, the RT9125H will ramp down signal to turn off the speaker



Note: There is no relation between the VOL_RAMP and UVP RAMP.

Address	BITS	Name	Description
0x6C	2:0	D_UVP_PVDD_SEL[2:0]	Select UVP level for PVDD power domain 000: 4.1V (default) 001: 6V 010: 8.5V 011: 9.5V 100: 10.9V 101: 12.7V 110: 15.4V 111: 20V
0x71	1	D_OV_FAULT_RAMP	PVDD OVP protection behavior 0: HZ_PROT directly 1: Power off sequence (default)

19 Application Information

(Note 24)

19.1 I²C Bus Specification

The RT9125H supports the I²C protocol via the input ports SCL and SDA. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the others as the slave. The master always starts the transfer and provides the serial clock for synchronization. The RT9125H is always a slave device in all of its communications. It can operate at up to 400kB/s.

19.2 Communication Protocol

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition. START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer. STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the RT9125H and the bus master. During the data input, the RT9125H samples the SDA signal on the rising edge of clock SCL. For correct device operation, the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

19.3 Boost Capacitor Selection

For the large power output, and low frequency, the boost capacitor can be chosen from 0.47μF to 1μF. Refer to Table 1 for Reference value.

Table 1. Boost Capacitor Select Table

Test Condition	Capacitor Value
PVDD = 24V, R = 8Ω, Output Power > 2x25W, 20Hz, BTL Mode	1μF
PVDD = 24V, R = 4Ω, Output Power < 2x20W, 20Hz, BTL Mode	0.47μF
PVDD = 24V, R = 4Ω, Output Power > 60W, 20Hz, PBTL Mode	1μF
PVDD = 24V, R = 8Ω, Output Power > 35W, 20Hz, PBTL Mode	1μF

19.4 Device Addressing

The RT9125H supports 16 I²C slave ID addresses, which can be configured by using different resister (20% tolerance). Refer to Table 2 for the address configuration.

Table 2. Address Select Table

SEL_1	SEL_2	Address
High	High	0x15
High	Low	0x11
Low	High	0x14
Low	Low	0x10
High+600k	High	0x17
High+600k	Low	0x13
Low+600k	High	0x16
Low+600k	Low	0x12
High	High+600k	0x1d
High	Low+600k	0x19
High+600k	High+600k	0x1f
High+600k	Low+600k	0x1b
Low	High+600k	0x1c
Low	Low+600k	0x18
Low+600k	High+600k	0x1e
Low+600k	Low+600k	0x1a

19.5 LC Filter Selection

For the different PWM switching and to avoid large current ripple, refer to Table 3 to select suitable LC combination.

Table 3. LC Filter Selection Table

PWM	Inductor	Capacitor Value
384kHz	10μH to 8.2μH	0.68μF to 0.47μF
768kHz	4.7μF	0.47μF to 0.22μF

19.6 I²C Write Control

Following the START condition, the master sends a device select code with the RW bit set to 0. The RT9125H acknowledges this and the writes for the byte of internal address. After receiving the internal byte address, the RT9125H again responds with an acknowledgement.

19.7 I²C Read Control

Following the START condition the master sends a device select code with the RW bit set to 1. The RT9125H acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

19.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a RLQFP-64L 10x10 (PP) package, the thermal resistance, θ_{JA}, is 55.24°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (150°C - 25°C) / (55.24°C/W) = 2.26W for a RLQFP-64L 10x10 (PP) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

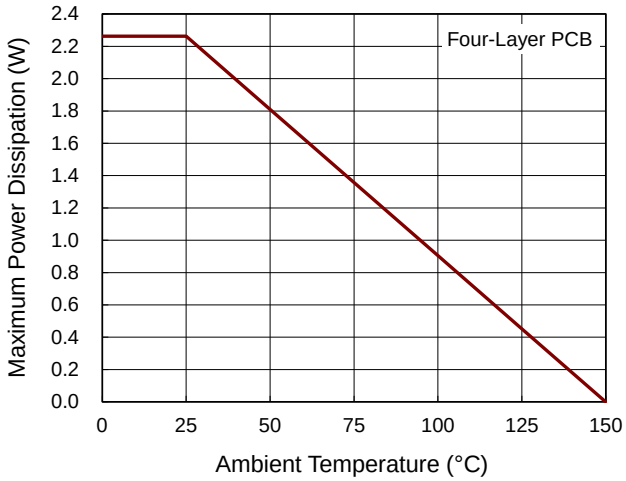
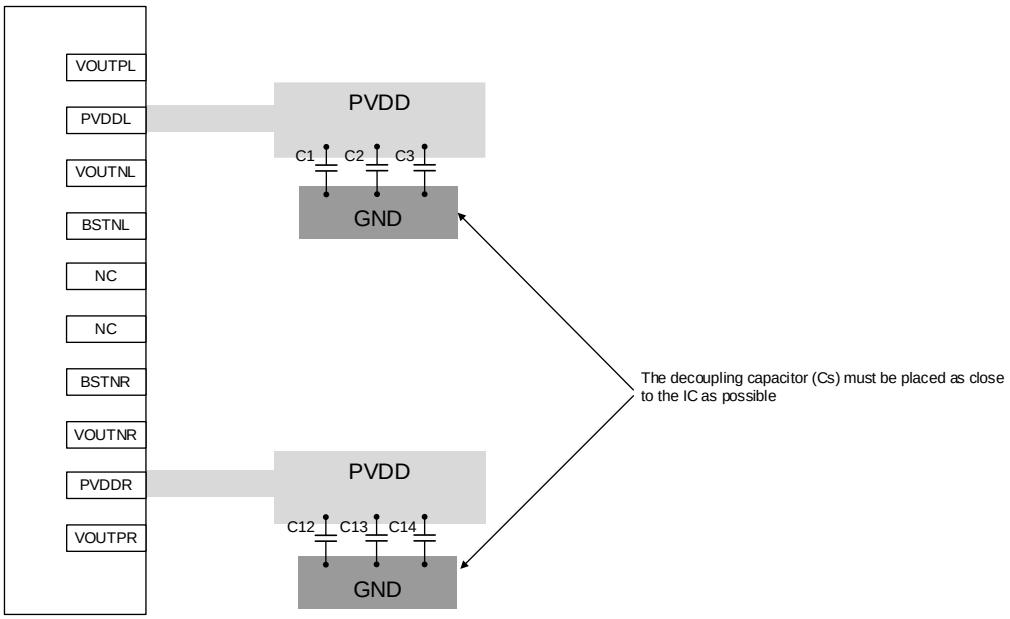


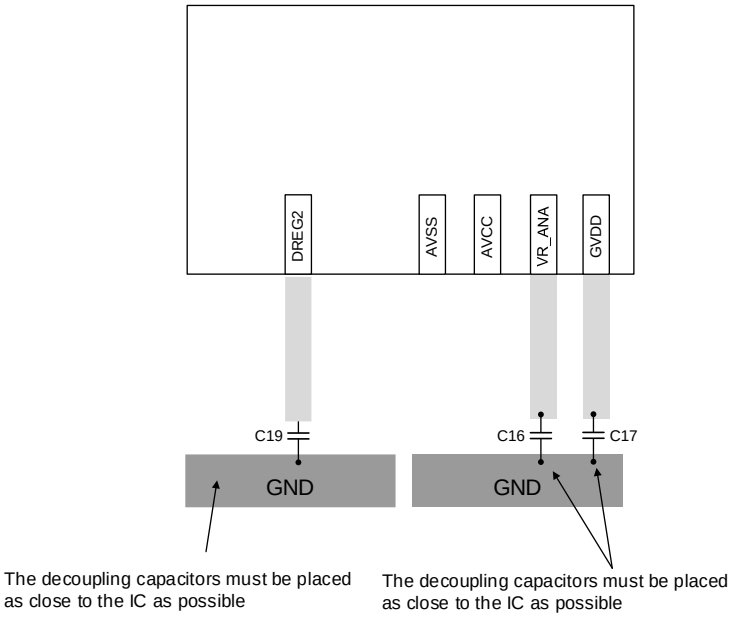
Figure 5. Derating Curve of Maximum Power Dissipation

19.9 Layout Guide

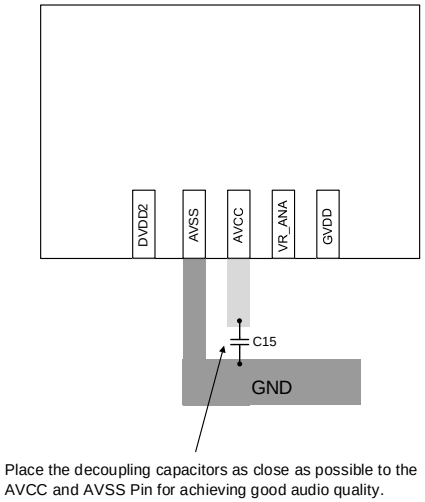
Place the decoupling capacitors as close as possible to the PVCC and GND, then use shortest trace to link these capacitors, and use more vias for GND link to GND layer to reduce parasitic inductance and resistance. The trace width is 30mil at least.



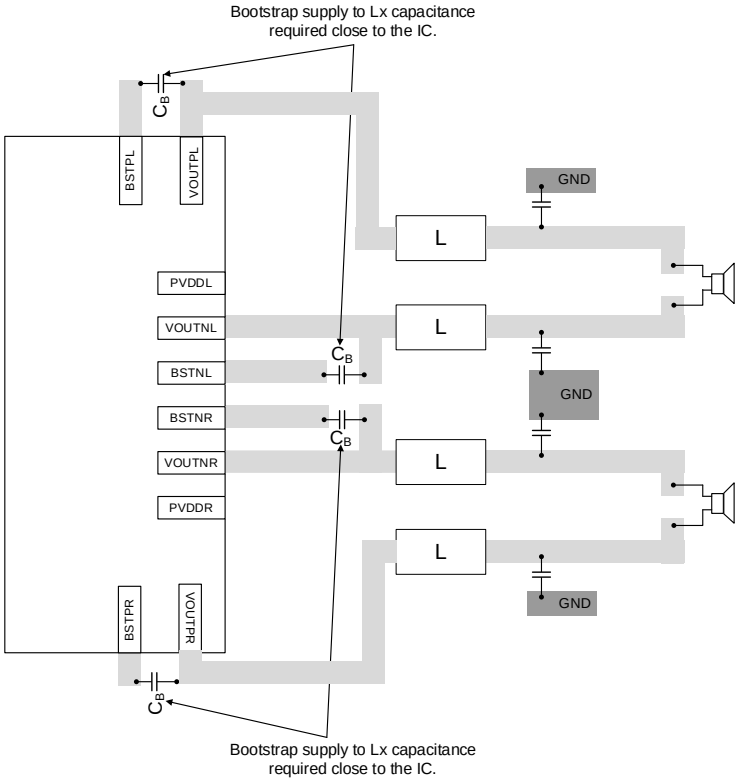
The DREG2 VR_ANA and GVDD decoupling capacitors must be placed as close to the IC as possible.



Place the decoupling capacitors as close as possible to the AVCC and AVSS Pin for achieving good audio quality, the trace width of AVCC is 30mil at least.



The traces of VOUTPL VOUTNL VOUTPR and VOUTNR should be kept as equal width and length respectively, and Bootstrap supply to Lx capacitance is required to be close to the IC.



If possible, coplanar ground fill on both sides for differential pair of speaker out shielding.

Note 24. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

20 Functional Register Description

The register description which is described as prohibit is not allow to be set.

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
Control Page (Digital Portion)								
0x00	1	VERSION	7:4	0	4	0000	RO	D_VERSION_IED
0x01	1	I2S_CLK_FMT	7:4	5	4	0101	RW	Sampling rate (manual setting or report) If 0x04 bit 4 SR_DET_EN = 1, SR_MODE report sampling rate detection result. 0000: 8kHz 0001: 12kHz 0010: 16kHz 0011: 24kHz 0100: 32kHz 0101: 44.1/48kHz (default) 0110: 88.2/96kHz 0111: 192kHz Others: Sampling rate error report
			3:0	2	4	0010	RW	BCK OSR mode (manual setting or report) If 0x04 bit 4 SR_DET_EN = 1, BCK_MODE report BCK OSR detection result. 0000: BCK = 32fs 0001: BCK = 48fs 0010: BCK = 64fs (default) 0011: BCK = 96fs 0100: BCK = 128fs 0101: BCK = 192fs 0110: BCK = 256fs 0111: BCK = 384fs 1000: BCK = 512fs Others: BCK mode error report

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x02	1	I2S_DATA_FMT	7	0	1	0	RW	I²S data out launch edge selection 0: BCK_RX_EDGE = 0, launch with falling edge; BCK_RX_EDGE = 1, launch with rising edge (default) 1: BCK_RX_EDGE = 0, launch with rising edge; BCK_RX_EDGE = 1, launch with falling edge
			6	0	1	0	RW	0: RX @BCK rising edge and TX @BCK falling edge (default) 1: RX @BCK falling edge and TX @BCK rising edge
			5:4	2	2	10	RW	Audio bits for signal process 00: 16 bits 01: 20 bits 10: 24 bits (default) 11: 32 bits
			3	1	1	1	RW	TDM or DSPM offset selection 0: Without offset (DSPMB) 1: 1 bit clock offset (DSPMA) (default)
			2:0	0	3	000	RW	I²S format selection 000: I²S (default) 001: Left Justify 010: Right Justify 011: DSP mode 100: EIAJ Others: TDM mode

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x03	1	I2S_DIO_SEL	7:4	0	4	0000	RW	0000: No output (default) 0001: I^2S interface 0010: 128-tap FIR 0011: EQ BQ 0100: Smooth BQ/ DPEQ 0101: Spatializer/CCS 0110: Output Mixer 0111: Final DRC Others: No output
			3:2	0	2	00	RW	00: SDIN-L to LCH (default) 01: SDIN-R to LCH 1X: 0 to LCH
			1:0	1	2	01	RW	00: SDIN-L to RCH 01: SDIN-R to RCH (default) 1X: 0 to RCH
0x04	1	TDM_RX_L	5:0	0	6	000000	RW	TDM start transmitting location select for L channel 000000: Start from 0+offset (default) 000001: Start from 8+offset 000010: Start from 16+offset 000011: Start from 24+offset … 111101: Start from 488+offest 111110: Start from 496+offset 111111: Start from 504+offset

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x05	1	TDM_RX_R	5:0	4	6	000100	RW	TDM start transmitting location select for R channel 000000: Start from 0+offset 000001: Start from 8+offset 000010: Start from 16+offset 000011: Start from 24+offset (default) … 111101: Start from 488+offest 111110: Start from 496+offset 111111: Start from 504+offset
0x06	1	TDM_TX_L	5:0	0	6	000000	RW	TDM start receiving location select for L channel 000000: Start from 0+offset (default) 000001: Start from 8+offset 000010: Start from 16+offset 000011: Start from 24+offset … 111101: Start from 488+offest 111110: Start from 496+offset 111111: Start from 504+offset
0x07	1	TDM_TX_R	5:0	4	6	000100	RW	TDM start receiving location select for R channel 000000: Start from 0+offset 000001: Start from 8+offset 000010: Start from 16+offset 000011: Start from 24+offset (default) … 111101: Start from 488+offest 111110: Start from 496+offset 111111: Start from 504+offset

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x08	1	SYS_CTRL	7	1	1	1	RW	Silence detection enable 0: Disable 1: Enable (default)
			6	1	1	1	RW	Sampling rate and BCK OSR mode detection enable bit 0: Disable, manual set SR mode and BCK mode 1: Enable (default)
			5	1	1	1	RW	Sampling rate converter enable internal process with 88.2k/96kHz sampling rate (support input fs = 32kHz, 44.1k/48kHz) 0: Disable 1: Enable (default)
			4	0	1	0	RW	DRC compress mode selection 0: Compress jointly (2.0) (default) 1: Compress independently (1.1)
			3	0	1	0	RW	DRC predict gain enable 0: Disable (default) 1: Enable
			2	1	1	1	RW	I^2S Master Clock generator enable 0: Bypass I^2S slave clock to I^2S master I^2S master format = I^2S when I^2S slave set as I^2S/LJ/RJ I^2S master format = DSPM_A when I^2S slave set as DSPM/TDM 1: Enable clock generator (default) I^2S master format fix as I^2S with 64fs
			1:0	0	2	00	RW	DSP control 2'b00: amp off (default) 2'b01: amp on 2'b10: Force entry silence mode 2'b11: mute

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x09	1	PROCESS_FLOW_SEL	7:6	2	2	10	RW	Digital process flow selection 00: HPF → MIX → FIR → EQ → SBQ/DPEQ → VOL → Surround → MBDRC → Post Gain → FDRC 01: HPF → MIX → EQ → FIR → SBQ/DPEQ → VOL → Surround → MBDRC → Post Gain → FDRC 10: FIR → HPF → MIX → EQ → SBQ/DPEQ → VOL → Surround → MBDRC → Post Gain → FDRC (default)
			3:2	2	2	10	RO	Digital process flow 00: HPF → MIX -> FIR → EQ → SBQ/DPEQ → VOL → Surround → MBDRC → Post Gain → FDRC 01: HPF → MIX -> EQ → FIR → SBQ/DPEQ → VOL → Surround → MBDRC → Post Gain → FDRC 10: FIR → HPF → MIX → EQ → SBQ/DPEQ → VOL → Surround -> MBDRC → Post Gain → FDRC (default)
0x0A	1	REG_PAGE_SEL	2:0	0	3	000	RW	register page select for 0x30 to 0xFF 000: sys ctrl (default) 001: DSP signal process (EQ) 010: DSP signal process (SBQ/DPEQ) 011: DSP signal process (INOUT MIXER SDO MIXER/EQ) 100: DSP signal process (DRC) 101: DSP signal process (FIR) Others: N/A

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x0B	1	SW_RST	7	0	1	0	WO	Prohibited
			1:0	0	2	00	RW	FAULTB pin type selection 00: Interrupt = output low, normal = floating (default) 01: Interrupt = output high, normal = floating 10: Interrupt = output low, normal = output high 11: Interrupt = output high, normal = output low
0x0C	1	DSP_EQ_OPT	7	1	1	1	RW	Write coefficient option for EQ 0: L/R independent 1: L/R write the same data (default)
			6	1	1	1	RW	Write coefficient option for SMEQ/DPEQ 0: L/R independent 1: L/R write the same data (default)
			5	1	1	1	RW	Write coefficient option for SURROUND EQ 0: L/R independent 1: L/R write the same data (default)
			4	1	1	1	RW	Write coefficient option for MBDRC EQ 0: L/R independent 1: L/R write the same data (default)
			3	1	1	1	RW	Write coefficient option for SDO EQ 0: L/R independent 1: L/R write the same data (default)
			2	0	1	0	RW	FIR coefficient option when SSRC enable @ 32kHz/44.1kHz/48kHz 0: Embedded low pass coefficient (default) 1: Manual write coefficient

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
			1	1	1	1	RW	DRC AT/RT hysteresis enable 0: Disable 1: Enable (default)
			0	1	1	1	RW	MBDRC EQ order select 0: 2nd order 1: 4th order (default)
0x0D	1	DSP_BLK_EN	7	1	1	1	RW	DSP_HPF_EN 0: Bypass 1: Enable (default)
			6	0	1	0	RW	FIR_EN 0: Bypass (default) 1: Enable
			5	0	1	0	RW	EQ_EN 0: Bypass (default) 1: Enable
			4	0	1	0	RW	SDO_EQ_EN 0: Bypass (default) 1: Enable
			3	0	1	0	RW	SMEQ_DPEQ_EN 0: Bypass (default) 1: Enable
			2	0	1	0	RW	SMEQ DPEQ select 0: Smooth EQ (default) 1: Dynamic EQ
			1	0	1	0	RW	SURROUND_EN 0: Bypass (default) 1: Enable
			0	0	1	0	RW	Surround select 0: Spatialize (default) 1: CCS

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x0E	1	DSP_DRC_OPT	7	1	1	1	RW	1: Peak mode (default) 0: RMS mode
			6	1	1	1	RW	1: Peak mode (default) 0: RMS mode
			5	1	1	1	RW	1: Peak mode (default) 0: RMS mode
			4	1	1	1	RW	1: Peak mode (default) 0: RMS mode
			2	1	1	1	RW	0: Normal mode 1: Output 0 (default)
			1	1	1	1	RW	0: Normal mode 1: Output 0 (default)
			0	0	1	0	RW	0: Normal mode (default) 1: Output 0

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x0F	1	DSP_DRC_EN	7	0	1	0	RW	0: DRC4 enable (Final DRC) (default) 1: DRC4 disable (Final DRC)
			6	0	1	0	RW	0: DRC3 enable (H band) (default) 1: DRC3 disable (H band)
			5	0	1	0	RW	0: DRC2 enable (M band) (default) 1: DRC2 disable (M band)
			4	0	1	0	RW	0: DRC1 enable (L_band) (default) 1: DRC1 disable (L_band)
			3	0	1	0	RW	1: DRC4 Noise Gate enable 0: DRC4 Noise Gate disable (default)
			2	0	1	0	RW	1: DRC3 Noise Gate enable 0: DRC3 Noise Gate disable (default)
			1	0	1	0	RW	1: DRC2 Noise Gate enable 0: DRC2 Noise Gate disable (default)
			0	0	1	0	RW	1: DRC1 Noise Gate enable 0: DRC1 Noise Gate disable (default)
0x10	1	INT_CTRL0	1	0	1	0	RW	LRCK/BCK error 0: Normal (default) 1: Fault (write 1 to clear)
0x12	1	ASEL_ERR	1	0	1	0	W1C	I^2C slave address pin detection error 0: Normal (default) 1: Error
			0	0	1	0	W1C	I^2C slave address pin detection error 0: Normal (default) 1: Error
0x13	1	CRC_REG	7:0	0	8	00000000	RO	CRC8 for register set
0x14	1	CRC_MEM	7:0	0	8	00000000	RO	CRC8 for memory set

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x30	1	SBQ_CTRL	6:4	7	3	111	RW	SBQ smooth time select 000: 8 samples 001: 16 samples 010: 32 samples 011: 64 samples 100: 128 samples 101: 256 samples 110: 512 samples 111: 1024 samples (default)
			3	1	1	1	RO	Report status of smooth transition (after TS), 1 = done
			1:0	0	2	00	RWC	Trigger smooth BQ coefficients update: When non-zero value is written, smooth transition is triggered. After transition is done, this register automatically goes back to 00. Before transition done, any new write to this register is invalid 00: No update (default) 01: SBQ_BK1 to SBQ13, SBQ_BK2 to SBQ14 10: SBQ_BK1 to SBQ15, SBQ_BK2 to SBQ16 11: SBQ_BK1 to SBQ17, SBQ_BK2 to SBQ18
0x31	1	DRC_INPUT_SEL	3:2	0	2	00	RW	MBDRC input select for L channel 00: Surround L Channel (default) 01: Surround R Channel 1X: Surround (L+R) / 2
			1:0	1	2	01	RW	MBDRC input select for R channel 00: Surround L Channel 01: Surround R Channel (default) 1X: Surround (L+R) / 2

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x32	2	MS_VOL_CTRL	14	0	1	0	RW	Skip volume ramp 0: Ramp with ramp mode option (default) 1: Skip volume ramp
			13:12	0	2	00	RW	Volume slew step control 00: 4.33ms from mute to 0dB (0.5dB/20.83μs) 01: 8.66ms from mute to 0dB (0.25dB/20.83μs) (default) 10: 17.33ms from mute to 0dB (0.125dB/20.83μs) 11: 34.65ms from mute to 0dB (0.0625dB/20.83μs)
			10:0	180	11	001_10000000	RW	Master volume control 11'h000: 24dB 11'h180: 0dB 11'h7FF: mute (default) 0.0625dB per step
0x34	2	DSP_CH_L_VOL_ADJ	10:0	180	11	001_10000000	RW	LCH volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step
0x36	2	DSP_CH_R_VOL_ADJ	10:0	180	11	001_10000000	RW	RCH volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x38	1	SIL_OPT	5:4	3	2	11	RW	Silence detection threshold selection (only one threshold for 8bit) 00: –72dB (16bit)/–96dB (20bit)/–120dB (24bit)/–144dB (32bit) 01: –78dB (16bit)/–102dB (20bit)/–126dB (24bit)/–150dB (32bit) 10: –84dB (16bit)/–108dB (20bit)/–132dB (24bit)/–156dB (32bit) 11: –90dB (default) (16bit)/–114dB (20bit)/–138dB (24bit)/–166dB (32bit)
			2:0	2	3	010	RW	Silence mode hold time selection 000: 1ms 001: 20ms 010: 40ms (default) 011: 80ms 100: 160ms 101: 320ms 110: 640ms 111: 1.28s
MBDRC_Surround Page								
0x30	4	SURROUND_BQ0_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	LB_CH1_BQ1
0x31	4	SURROUND_BQ0_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ1
0x32	4	SURROUND_BQ0_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ1
0x33	4	SURROUND_BQ0_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ1
0x34	4	SURROUND_BQ0_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ1
0x35	4	SURROUND_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	LB_CH1_BQ2

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x36	4	SURROUND_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ2
0x37	4	SURROUND_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ2
0x38	4	SURROUND_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ2
0x39	4	SURROUND_BQ1_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ2
0x3A	4	HB_CH1_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	HB_CH1_BQ1_B0
0x3B	4	HB_CH1_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH1_BQ1_B1
0x3C	4	HB_CH1_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH1_BQ1_B2
0x3D	4	HB_CH1_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH1_BQ1_A1
0x3E	4	HB_CH1_BQ1_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH1_BQ1_A2
0x3F	4	HB_CH1_BQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	HB_CH1_BQ2_B0
0x40	4	HB_CH1_BQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH1_BQ2_B1
0x41	4	HB_CH1_BQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH1_BQ2_B2
0x42	4	HB_CH1_BQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH1_BQ2_A1
0x43	4	HB_CH1_BQ2_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH1_BQ2_A2
0x44	4	MB_CH1_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	MB_CH1_BQ1_B0
0x45	4	MB_CH1_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	MB_CH1_BQ1_B1

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x46	4	MB_CH1_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	MB_CH1_BQ1_B2
0x47	4	MB_CH1_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	MB_CH1_BQ1_A1
0x48	4	MB_CH1_BQ1_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	MB_CH1_BQ1_A2
0x49	4	LB_CH1_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	LB_CH1_BQ1_B0
0x4A	4	LB_CH1_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ1_B1
0x4B	4	LB_CH1_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ1_B2
0x4C	4	LB_CH1_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ1_A1
0x4D	4	LB_CH1_BQ1_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ1_A2
0x4E	4	LB_CH1_BQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	LB_CH1_BQ2_B0
0x4F	4	LB_CH1_BQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ2_B1
0x50	4	LB_CH1_BQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ2_B2
0x51	4	LB_CH1_BQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ2_A1
0x52	4	LB_CH1_BQ2_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH1_BQ2_A2
0x53	4	HB_CH2_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	HB_CH2_BQ1_B0
0x54	4	HB_CH2_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH2_BQ1_B1
0x55	4	HB_CH2_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH2_BQ1_B2

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x56	4	HB_CH2_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH2_BQ1_A1
0x57	4	HB_CH2_BQ1_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH2_BQ1_A2
0x58	4	HB_CH2_BQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	HB_CH2_BQ2_B0
0x59	4	HB_CH2_BQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH2_BQ2_B1
0x5A	4	HB_CH2_BQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH2_BQ2_B2
0x5B	4	HB_CH2_BQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH2_BQ2_A1
0x5C	4	HB_CH2_BQ2_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	HB_CH2_BQ2_A2
0x5D	4	MB_CH2_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	MB_CH2_BQ1_B0
0x5E	4	MB_CH2_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	MB_CH2_BQ1_B1
0x5F	4	MB_CH2_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	MB_CH2_BQ1_B2
0x60	4	MB_CH2_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	MB_CH2_BQ1_A1
0x61	4	MB_CH2_BQ1_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	MB_CH2_BQ1_A2
0x62	4	LB_CH2_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	LB_CH2_BQ1_B0
0x63	4	LB_CH2_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH2_BQ1_B1
0x64	4	LB_CH2_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH2_BQ1_B2
0x65	4	LB_CH2_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH2_BQ1_A1

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x66	4	LB_CH2_BQ1_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH2_BQ1_A2
0x67	4	LB_CH2_BQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	LB_CH2_BQ2_B0
0x68	4	LB_CH2_BQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH2_BQ2_B1
0x69	4	LB_CH2_BQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH2_BQ2_B2
0x6A	4	LB_CH2_BQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH2_BQ2_A1
0x6B	4	LB_CH2_BQ2_A2	31:0	0	32	00000000_00000000_00000000_00000000	RW	LB_CH2_BQ2_A2
0x6C	4	DRC1_RMS_AE	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC1 RMS AE
0x6D	4	DRC1_RMS_1-AE	31:0	0	32	00000000_00000000_00000000_00000000	RW	DRC1 RMS 1-AE
0x6E	4	DRC1_GAIN_AA	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC1 GAIN AA
0x6F	4	DRC1_GAIN_AD	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC1 GAIN AD
0x70	4	DRC2_RMS_AE	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC2 RMS AE
0x71	4	DRC2_RMS_1-AE	31:0	0	32	00000000_00000000_00000000_00000000	RW	DRC2 RMS 1-AE
0x72	4	DRC2_GAIN_AA	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC2 GAIN AA
0x73	4	DRC2_GAIN_AD	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC2 GAIN AD
0x74	4	DRC3_RMS_AE	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC3 RMS AE
0x75	4	DRC3_RMS_1-AE	31:0	0	32	00000000_00000000_00000000_00000000	RW	DRC3 RMS 1-AE

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x76	4	DRC3_GAIN_AA	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC3 GAIN AA
0x77	4	DRC3_GAIN_AD	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC3 GAIN AD
0x78	4	DRC4_AE	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC4 AE
0x79	4	DRC4_1-AE	31:0	0	32	00000000_00000000_00000000_00000000	RW	DRC4 1-AE
0x7A	4	DRC4_AA	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC4 AA
0x7B	4	DRC4_AD	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC4 AD
0x7C	4	CH1_OUT_MIX_L	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_OUT_MIX_L
0x7D	4	CH1_OUT_MIX_M	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_OUT_MIX_M
0x7E	4	CH1_OUT_MIX_H	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_OUT_MIX_H
0x7F	4	CH2_OUT_MIX_L	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_OUT_MIX_L
0x80	4	CH2_OUT_MIX_M	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_OUT_MIX_M
0x81	4	CH2_OUT_MIX_H	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_OUT_MIX_H
0x82	4	CH1_POST_GAIN	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_POST_GAIN
0x83	4	CH2_POST_GAIN	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_POST_GAIN
0x84	4	DRC1_RMS_AE_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC1_RMS_AE_2
0x85	4	DRC1_RMS_1-AE_2	31:0	0	32	00000000_00000000_00000000_00000000	RW	DRC1_RMS_1_AE_2

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x86	4	DRC1_GAIN_AA_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC1_GAIN_AA_2
0x87	4	DRC1_GAIN_AD_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC1_GAIN_AD_2
0x88	4	DRC2_RMS_AE_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC2_RMS_AE_2
0x89	4	DRC2_RMS_1-AE_2	31:0	0	32	00000000_00000000_00000000_00000000	RW	DRC2_RMS_1_AE_2
0x8A	4	DRC2_GAIN_AA_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC2_GAIN_AA_2
0x8B	4	DRC2_GAIN_AD_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC2_GAIN_AD_2
0x8C	4	DRC3_RMS_AE_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC3_RMS_AE_2
0x8D	4	DRC3_RMS_1-AE_2	31:0	0	32	00000000_00000000_00000000_00000000	RW	DRC3_RMS_1_AE_2
0x8E	4	DRC3_GAIN_AA_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC3_GAIN_AA_2
0x8F	4	DRC3_GAIN_AD_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC3_GAIN_AD_2
0x90	4	DRC4_AE_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC4_AE_2
0x91	4	DRC4_1-AE_2	31:0	0	32	00000000_00000000_00000000_00000000	RW	DRC4_1_AE_2
0x92	4	DRC4_AA_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC4_AA_2
0x93	4	DRC4_AD_2	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	DRC4_AD_2
0x94	1	DRC1_K	7:0	80	8	10000000	RW	DRC1_K
0x95	1	DRC2_K	7:0	80	8	10000000	RW	DRC2_K
0x96	1	DRC3_K	7:0	80	8	10000000	RW	DRC3-K
0x97	1	DRC4_K	7:0	80	8	10000000	RW	DRC4_K
0x98	2	DRC1_T	10:0	0	11	000_00000000	RW	DRC1_T

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x99	2	DRC2_T	10:0	0	11	000_00000000	RW	DRC2_T
0x9A	2	DRC3_T	10:0	0	11	000_00000000	RW	DRC3-T
0x9B	2	DRC4_T	10:0	0	11	000_00000000	RW	DRC4_T
0x9C	2	DRC1_N_T	10:0	640	11	110_01000000	RW	DRC1_N_T
0x9D	2	DRC2_N_T	10:0	640	11	110_01000000	RW	DRC2_N_T
0x9E	2	DRC3_N_T	10:0	640	11	110_01000000	RW	DRC3_N_T
0x9F	2	DRC4_N_T	10:0	640	11	110_01000000	RW	DRC4_N_T
0xA0	2	DRC1_O	10:0	180	11	001_10000000	RW	DRC1_O
0xA1	2	DRC2_O	10:0	180	11	001_10000000	RW	DRC2_O
0xA2	2	DRC3_O	10:0	180	11	001_10000000	RW	DRC3-O
0xA3	2	DRC4_O	10:0	180	11	001_10000000	RW	DRC4_O
0xA4	1	DRC1_K_2	7:0	80	8	10000000	RW	DRC1_K
0xA5	1	DRC2_K_2	7:0	80	8	10000000	RW	DRC2_K
0xA6	1	DRC3_K_2	7:0	80	8	10000000	RW	DRC3-K
0xA7	1	DRC4_K_2	7:0	80	8	10000000	RW	DRC4_K
0xA8	2	DRC1_T_2	10:0	0	11	000_00000000	RW	DRC1_T
0xA9	2	DRC2_T_2	10:0	0	11	000_00000000	RW	DRC2_T
0xAA	2	DRC3_T_2	10:0	0	11	000_00000000	RW	DRC3-T
0xAB	2	DRC4_T_2	10:0	0	11	000_00000000	RW	DRC4_T
0xAC	2	DRC1_N_T_2	10:0	640	11	110_01000000	RW	DRC1_N_T
0xAD	2	DRC2_N_T_2	10:0	640	11	110_01000000	RW	DRC2_N_T
0xAE	2	DRC3_N_T_2	10:0	640	11	110_01000000	RW	DRC3_N_T
0xAF	2	DRC4_N_T_2	10:0	640	11	110_01000000	RW	DRC4_N_T
0xB0	2	DRC1_O_2	10:0	180	11	001_10000000	RW	DRC1_O
0xB1	2	DRC2_O_2	10:0	180	11	001_10000000	RW	DRC2_O
0xB2	2	DRC3_O_2	10:0	180	11	001_10000000	RW	DRC3-O
0xB3	2	DRC4_O_2	10:0	180	11	001_10000000	RW	DRC4_O
0xB4	1	DRC4_DELAY	7:0	FF	8	11111111	RW	DRC4_DELAY
0xB5	1	DRC4_DELAY_2	7:0	FF	8	11111111	RW	DRC4_DELAY_2
EQ Page								
0x30	4	CH1_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ1

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x31	4	CH1_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ1
0x32	4	CH1_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ1
0x33	4	CH1_BQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ1
0x34	4	CH1_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ1
0x35	4	CH1_BQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ2
0x36	4	CH1_BQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ2
0x37	4	CH1_BQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ2
0x38	4	CH1_BQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ2
0x39	4	CH1_BQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ2
0x3A	4	CH1_BQ3_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ3
0x3B	4	CH1_BQ3_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ3
0x3C	4	CH1_BQ3_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ3
0x3D	4	CH1_BQ3_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ3
0x3E	4	CH1_BQ3_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ3
0x3F	4	CH1_BQ4_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ4
0x40	4	CH1_BQ4_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ4

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x41	4	CH1_BQ4_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ4
0x42	4	CH1_BQ4_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ4
0x43	4	CH1_BQ4_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ4
0x44	4	CH1_BQ5_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ5
0x45	4	CH1_BQ5_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ5
0x46	4	CH1_BQ5_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ5
0x47	4	CH1_BQ5_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ5
0x48	4	CH1_BQ5_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ5
0x49	4	CH1_BQ6_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ6
0x4A	4	CH1_BQ6_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ6
0x4B	4	CH1_BQ6_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ6
0x4C	4	CH1_BQ6_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ6
0x4D	4	CH1_BQ6_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ6
0x4E	4	CH1_BQ7_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ7
0x4F	4	CH1_BQ7_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ7
0x50	4	CH1_BQ7_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ7

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x51	4	CH1_BQ7_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ7
0x52	4	CH1_BQ7_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ7
0x53	4	CH1_BQ8_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ8
0x54	4	CH1_BQ8_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ8
0x55	4	CH1_BQ8_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ8
0x56	4	CH1_BQ8_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ8
0x57	4	CH1_BQ8_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ8
0x58	4	CH1_BQ9_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ9
0x59	4	CH1_BQ9_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ9
0x5A	4	CH1_BQ9_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ9
0x5B	4	CH1_BQ9_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ9
0x5C	4	CH1_BQ9_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ9
0x5D	4	CH1_BQ10_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ10
0x5E	4	CH1_BQ10_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ10
0x5F	4	CH1_BQ10_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ10
0x60	4	CH1_BQ10_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ10

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x61	4	CH1_BQ10_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ10
0x62	4	CH1_BQ11_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ11
0x63	4	CH1_BQ11_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ11
0x64	4	CH1_BQ11_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ11
0x65	4	CH1_BQ11_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ11
0x66	4	CH1_BQ11_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ11
0x67	4	CH1_BQ12_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_BQ12
0x68	4	CH1_BQ12_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ12
0x69	4	CH1_BQ12_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ12
0x6A	4	CH1_BQ12_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ12
0x6B	4	CH1_BQ12_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_BQ12
0x6C	4	CH2_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ1
0x6D	4	CH2_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ1
0x6E	4	CH2_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ1
0x6F	4	CH2_BQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ1
0x70	4	CH2_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ1

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x71	4	CH2_BQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ2
0x72	4	CH2_BQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ2
0x73	4	CH2_BQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ2
0x74	4	CH2_BQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ2
0x75	4	CH2_BQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ2
0x76	4	CH2_BQ3_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ3
0x77	4	CH2_BQ3_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ3
0x78	4	CH2_BQ3_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ3
0x79	4	CH2_BQ3_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ3
0x7A	4	CH2_BQ3_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ3
0x7B	4	CH2_BQ4_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ4
0x7C	4	CH2_BQ4_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ4
0x7D	4	CH2_BQ4_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ4
0x7E	4	CH2_BQ4_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ4
0x7F	4	CH2_BQ4_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ4
0x80	4	CH2_BQ5_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ5

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x81	4	CH2_BQ5_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ5
0x82	4	CH2_BQ5_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ5
0x83	4	CH2_BQ5_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ5
0x84	4	CH2_BQ5_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ5
0x85	4	CH2_BQ6_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ6
0x86	4	CH2_BQ6_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ6
0x87	4	CH2_BQ6_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ6
0x88	4	CH2_BQ6_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ6
0x89	4	CH2_BQ6_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ6
0x8A	4	CH2_BQ7_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ7
0x8B	4	CH2_BQ7_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ7
0x8C	4	CH2_BQ7_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ7
0x8D	4	CH2_BQ7_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ7
0x8E	4	CH2_BQ7_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ7
0x8F	4	CH2_BQ8_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ8
0x90	4	CH2_BQ8_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ8

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x91	4	CH2_BQ8_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ8
0x92	4	CH2_BQ8_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ8
0x93	4	CH2_BQ8_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ8
0x94	4	CH2_BQ9_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ9
0x95	4	CH2_BQ9_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ9
0x96	4	CH2_BQ9_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ9
0x97	4	CH2_BQ9_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ9
0x98	4	CH2_BQ9_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ9
0x99	4	CH2_BQ10_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ10
0x9A	4	CH2_BQ10_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ10
0x9B	4	CH2_BQ10_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ10
0x9C	4	CH2_BQ10_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ10
0x9D	4	CH2_BQ10_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ10
0x9E	4	CH2_BQ11_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ11
0x9F	4	CH2_BQ11_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ11
0xA0	4	CH2_BQ11_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ11

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0xA1	4	CH2_BQ11_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ11
0xA2	4	CH2_BQ11_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ11
0xA3	4	CH2_BQ12_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_BQ12
0xA4	4	CH2_BQ12_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ12
0xA5	4	CH2_BQ12_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ12
0xA6	4	CH2_BQ12_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ12
0xA7	4	CH2_BQ12_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_BQ12
SDO_Mix_Page								
0x30	4	CH1_IN_MIX_0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_IN_MIX_0
0x31	4	CH1_IN_MIX_1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_IN_MIX_1
0x32	4	CH2_IN_MIX_0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_IN_MIX_0
0x33	4	CH2_IN_MIX_1	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_IN_MIX_1
0x34	4	CH1_OUT_MIX_0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_OUT_MIX_1
0x35	4	CH1_OUT_MIX_1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_OUT_MIX_0
0x36	4	CH2_OUT_MIX_0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_OUT_MIX_1
0x37	4	CH2_OUT_MIX_1	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_OUT_MIX_0
0x38	4	SDO_CH1_IN_MIX_0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH1_IN_MIX_1

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x39	4	SDO_CH1_IN_MIX_1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_IN_MIX_0
0x3A	4	SDO_CH2_IN_MIX_0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_IN_MIX_1
0x3B	4	SDO_CH2_IN_MIX_1	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH2_IN_MIX_0
0x3C	4	SDO_CH1_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH1_BQ1
0x3D	4	SDO_CH1_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ1
0x3E	4	SDO_CH1_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ1
0x3F	4	SDO_CH1_BQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ1
0x40	4	SDO_CH1_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ1
0x41	4	SDO_CH1_BQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH1_BQ2
0x42	4	SDO_CH1_BQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ2
0x43	4	SDO_CH1_BQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ2
0x44	4	SDO_CH1_BQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ2
0x45	4	SDO_CH1_BQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ2
0x46	4	SDO_CH1_BQ3_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH1_BQ3
0x47	4	SDO_CH1_BQ3_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ3
0x48	4	SDO_CH1_BQ3_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ3

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x49	4	SDO_CH1_BQ3_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ3
0x4A	4	SDO_CH1_BQ3_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ3
0x4B	4	SDO_CH1_BQ4_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH1_BQ4
0x4C	4	SDO_CH1_BQ4_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ4
0x4D	4	SDO_CH1_BQ4_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ4
0x4E	4	SDO_CH1_BQ4_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ4
0x4F	4	SDO_CH1_BQ4_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ4
0x50	4	SDO_CH1_BQ5_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH1_BQ5
0x51	4	SDO_CH1_BQ5_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ5
0x52	4	SDO_CH1_BQ5_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ5
0x53	4	SDO_CH1_BQ5_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ5
0x54	4	SDO_CH1_BQ5_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH1_BQ5
0x55	4	SDO_CH2_BQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH2_BQ1
0x56	4	SDO_CH2_BQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ1
0x57	4	SDO_CH2_BQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ1
0x58	4	SDO_CH2_BQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ1

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x59	4	SDO_CH2_BQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ1
0x5A	4	SDO_CH2_BQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH2_BQ2
0x5B	4	SDO_CH2_BQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ2
0x5C	4	SDO_CH2_BQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ2
0x5D	4	SDO_CH2_BQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ2
0x5E	4	SDO_CH2_BQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ2
0x5F	4	SDO_CH2_BQ3_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH2_BQ3
0x60	4	SDO_CH2_BQ3_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ3
0x61	4	SDO_CH2_BQ3_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ3
0x62	4	SDO_CH2_BQ3_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ3
0x63	4	SDO_CH2_BQ3_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ3
0x64	4	SDO_CH2_BQ4_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH2_BQ4
0x65	4	SDO_CH2_BQ4_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ4
0x66	4	SDO_CH2_BQ4_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ4
0x67	4	SDO_CH2_BQ4_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ4
0x68	4	SDO_CH2_BQ4_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ4

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x69	4	SDO_CH2_BQ5_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	SDO_CH2_BQ5
0x6A	4	SDO_CH2_BQ5_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ5
0x6B	4	SDO_CH2_BQ5_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ5
0x6C	4	SDO_CH2_BQ5_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ5
0x6D	4	SDO_CH2_BQ5_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	SDO_CH2_BQ5
SBQ_DPEQ_Page								
0x30	4	CH1_SBQ13_DPEQ_HBQ0_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_SBQ13_DPEQ_HBQ0_B0
0x31	4	CH1_SBQ13_DPEQ_HBQ0_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ13_DPEQ_HBQ0_B1
0x32	4	CH1_SBQ13_DPEQ_HBQ0_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ13_DPEQ_HBQ0_B2
0x33	4	CH1_SBQ13_DPEQ_HBQ0_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ13_DPEQ_HBQ0_A0
0x34	4	CH1_SBQ13_DPEQ_HBQ0_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ13_DPEQ_HBQ0_A1
0x35	4	CH1_SBQ14_DPEQ_HBQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_SBQ14_DPEQ_HBQ1_B0
0x36	4	CH1_SBQ14_DPEQ_HBQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ14_DPEQ_HBQ1_B1
0x37	4	CH1_SBQ14_DPEQ_HBQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ14_DPEQ_HBQ1_B2
0x38	4	CH1_SBQ14_DPEQ_HBQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ14_DPEQ_HBQ1_A0
0x39	4	CH1_SBQ14_DPEQ_HBQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ14_DPEQ_HBQ1_A1
0x3A	4	CH1_SBQ15_DPEQ_LBQ0_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_SBQ15_DPEQ_LBQ0_B0

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x3B	4	CH1_SBQ15_DPEQ_LBQ0_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ15_DPEQ_LBQ0_B1
0x3C	4	CH1_SBQ15_DPEQ_LBQ0_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ15_DPEQ_LBQ0_B2
0x3D	4	CH1_SBQ15_DPEQ_LBQ0_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ15_DPEQ_LBQ0_A0
0x3E	4	CH1_SBQ15_DPEQ_LBQ0_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ15_DPEQ_LBQ0_A1
0x3F	4	CH1_SBQ16_DPEQ_LBQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_SBQ16_DPEQ_LBQ1_B0
0x40	4	CH1_SBQ16_DPEQ_LBQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ16_DPEQ_LBQ1_B1
0x41	4	CH1_SBQ16_DPEQ_LBQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ16_DPEQ_LBQ1_B2
0x42	4	CH1_SBQ16_DPEQ_LBQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ16_DPEQ_LBQ1_A0
0x43	4	CH1_SBQ16_DPEQ_LBQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ16_DPEQ_LBQ1_A1
0x44	4	CH1_SBQ17_DPEQ_SBQ0_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_SBQ17_DPEQ_SBQ0_B0
0x45	4	CH1_SBQ17_DPEQ_SBQ0_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ17_DPEQ_SBQ0_B1
0x46	4	CH1_SBQ17_DPEQ_SBQ0_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ17_DPEQ_SBQ0_B2
0x47	4	CH1_SBQ17_DPEQ_SBQ0_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ17_DPEQ_SBQ0_A0
0x48	4	CH1_SBQ17_DPEQ_SBQ0_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ17_DPEQ_SBQ0_A1
0x49	4	CH1_SBQ18_DPEQ_SBQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_SBQ18_DPEQ_SBQ1_B0
0x4A	4	CH1_SBQ18_DPEQ_SBQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ18_DPEQ_SBQ1_B1

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x4B	4	CH1_SBQ18_DPEQ_SBQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ18_DPEQ_SBQ1_B2
0x4C	4	CH1_SBQ18_DPEQ_SBQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ18_DPEQ_SBQ1_A0
0x4D	4	CH1_SBQ18_DPEQ_SBQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ18_DPEQ_SBQ1_A1
0x4E	4	CH1_SBQ_BK1_DPEQ_HBQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_SBQ_BK1_DPEQ_HBQ2_B0
0x4F	4	CH1_SBQ_BK1_DPEQ_HBQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ_BK1_DPEQ_HBQ2_B1
0x50	4	CH1_SBQ_BK1_DPEQ_HBQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ_BK1_DPEQ_HBQ2_B2
0x51	4	CH1_SBQ_BK1_DPEQ_HBQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ_BK1_DPEQ_HBQ2_A0
0x52	4	CH1_SBQ_BK1_DPEQ_HBQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ_BK1_DPEQ_HBQ2_A1
0x53	4	CH1_SBQ_BK2_DPEQ_LBQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_SBQ_BK2_DPEQ_LBQ2_B0
0x54	4	CH1_SBQ_BK2_DPEQ_LBQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ_BK2_DPEQ_LBQ2_B1
0x55	4	CH1_SBQ_BK2_DPEQ_LBQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ_BK2_DPEQ_LBQ2_B2
0x56	4	CH1_SBQ_BK2_DPEQ_LBQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ_BK2_DPEQ_LBQ2_A0
0x57	4	CH1_SBQ_BK2_DPEQ_LBQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_SBQ_BK2_DPEQ_LBQ2_A1
0x58	4	CH1_DPEQ_SBQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_DPEQ_SBQ2_B0
0x59	4	CH1_DPEQ_SBQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_DPEQ_SBQ2_B1
0x5A	4	CH1_DPEQ_SBQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_DPEQ_SBQ2_B2

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x5B	4	CH1_DPEQ_SBQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_DPEQ_SBQ2_A0
0x5C	4	CH1_DPEQ_SBQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH1_DPEQ_SBQ2_A1
0x5D	4	CH2_SBQ13_DPEQ_HBQ0_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_SBQ13_DPEQ_HBQ0_B0
0x5E	4	CH2_SBQ13_DPEQ_HBQ0_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ13_DPEQ_HBQ0_B1
0x5F	4	CH2_SBQ13_DPEQ_HBQ0_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ13_DPEQ_HBQ0_B2
0x60	4	CH2_SBQ13_DPEQ_HBQ0_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ13_DPEQ_HBQ0_A0
0x61	4	CH2_SBQ13_DPEQ_HBQ0_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ13_DPEQ_HBQ0_A1
0x62	4	CH2_SBQ14_DPEQ_HBQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_SBQ14_DPEQ_HBQ1_B0
0x63	4	CH2_SBQ14_DPEQ_HBQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ14_DPEQ_HBQ1_B1
0x64	4	CH2_SBQ14_DPEQ_HBQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ14_DPEQ_HBQ1_B2
0x65	4	CH2_SBQ14_DPEQ_HBQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ14_DPEQ_HBQ1_A0
0x66	4	CH2_SBQ14_DPEQ_HBQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ14_DPEQ_HBQ1_A1
0x67	4	CH2_SBQ15_DPEQ_LBQ0_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_SBQ15_DPEQ_LBQ0_B0
0x68	4	CH2_SBQ15_DPEQ_LBQ0_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ15_DPEQ_LBQ0_B1
0x69	4	CH2_SBQ15_DPEQ_LBQ0_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ15_DPEQ_LBQ0_B2
0x6A	4	CH2_SBQ15_DPEQ_LBQ0_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ15_DPEQ_LBQ0_A0

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x6B	4	CH2_SBQ15_DPEQ_LBQ0_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ15_DPEQ_LBQ0_A1
0x6C	4	CH2_SBQ16_DPEQ_LBQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_SBQ16_DPEQ_LBQ1_B0
0x6D	4	CH2_SBQ16_DPEQ_LBQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ16_DPEQ_LBQ1_B1
0x6E	4	CH2_SBQ16_DPEQ_LBQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ16_DPEQ_LBQ1_B2
0x6F	4	CH2_SBQ16_DPEQ_LBQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ16_DPEQ_LBQ1_A0
0x70	4	CH2_SBQ16_DPEQ_LBQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ16_DPEQ_LBQ1_A1
0x71	4	CH2_SBQ17_DPEQ_SBQ0_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_SBQ17_DPEQ_SBQ0_B0
0x72	4	CH2_SBQ17_DPEQ_SBQ0_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ17_DPEQ_SBQ0_B1
0x73	4	CH2_SBQ17_DPEQ_SBQ0_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ17_DPEQ_SBQ0_B2
0x74	4	CH2_SBQ17_DPEQ_SBQ0_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ17_DPEQ_SBQ0_A0
0x75	4	CH2_SBQ17_DPEQ_SBQ0_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ17_DPEQ_SBQ0_A1
0x76	4	CH2_SBQ18_DPEQ_SBQ1_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_SBQ18_DPEQ_SBQ1_B0
0x77	4	CH2_SBQ18_DPEQ_SBQ1_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ18_DPEQ_SBQ1_B1
0x78	4	CH2_SBQ18_DPEQ_SBQ1_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ18_DPEQ_SBQ1_B2
0x79	4	CH2_SBQ18_DPEQ_SBQ1_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ18_DPEQ_SBQ1_A0
0x7A	4	CH2_SBQ18_DPEQ_SBQ1_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ18_DPEQ_SBQ1_A1

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x7B	4	CH2_SBQ_BK1_DPEQ_HBQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_SBQ_BK1_DPEQ_HBQ2_B0
0x7C	4	CH2_SBQ_BK1_DPEQ_HBQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ_BK1_DPEQ_HBQ2_B1
0x7D	4	CH2_SBQ_BK1_DPEQ_HBQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ_BK1_DPEQ_HBQ2_B2
0x7E	4	CH2_SBQ_BK1_DPEQ_HBQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ_BK1_DPEQ_HBQ2_A0
0x7F	4	CH2_SBQ_BK1_DPEQ_HBQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ_BK1_DPEQ_HBQ2_A1
0x80	4	CH2_SBQ_BK2_DPEQ_LBQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_SBQ_BK2_DPEQ_LBQ2_B0
0x81	4	CH2_SBQ_BK2_DPEQ_LBQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ_BK2_DPEQ_LBQ2_B1
0x82	4	CH2_SBQ_BK2_DPEQ_LBQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ_BK2_DPEQ_LBQ2_B2
0x83	4	CH2_SBQ_BK2_DPEQ_LBQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ_BK2_DPEQ_LBQ2_A0
0x84	4	CH2_SBQ_BK2_DPEQ_LBQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_SBQ_BK2_DPEQ_LBQ2_A1
0x85	4	CH2_DPEQ_SBQ2_B0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_DPEQ_SBQ2_B0
0x86	4	CH2_DPEQ_SBQ2_B1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_DPEQ_SBQ2_B1
0x87	4	CH2_DPEQ_SBQ2_B2	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_DPEQ_SBQ2_B2
0x88	4	CH2_DPEQ_SBQ2_A0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_DPEQ_SBQ2_A0
0x89	4	CH2_DPEQ_SBQ2_A1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_DPEQ_SBQ2_A1
0x8A	4	CH1_ALPHA_0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH1_ALPHA_0

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x8B	4	CH1_ OEMGA_0	31:0	0	32	00000000_00000000 _00000000_00000000	RW	CH1_OEMGA_0
0x8C	4	CH1_THR1 _0	10:0	7B0	11	111_10110000	RW	8.3 format Default = –10dB
0x8D	4	CH1_THR2 _0	10:0	710	11	111_00010000	RW	8.3 format Default = –30dB
0x8E	4	CH1_DIF_ THR_N_0	31:0	00333333	32	00000000_00110011 _00110011_00110011	RW	Default = 0.05dB
0x8F	4	CH1_AT_0	31:0	04000000	32	00000100_00000000 _00000000_00000000	RW	CH1_AT_0
0x90	4	CH1_RT_0	31:0	0	32	00000000_00000000 _00000000_00000000	RW	CH1_RT_0
0x91	4	CH1_ ALPHA_1	31:0	04000000	32	00000100_00000000 _00000000_00000000	RW	CH1_ALPHA_1
0x92	4	CH1_ OEMGA_1	31:0	0	32	00000000_00000000 _00000000_00000000	RW	CH1_OEMGA_1
0x93	4	CH1_THR1 _1	31:0	7B0	32	01111011_01111011 _01111011_10110000	RW	8.3 format Default = –10dB
0x94	4	CH1_THR2 _1	31:0	710	32	01110001_01110001 _01110001_00010000	RW	8.3 format Default = –30dB
0x95	4	CH1_DIF_ THR_N_1	31:0	00333333	32	00000000_00110011 _00110011_00110011	RW	CH1_DIF_THR_N_1
0x96	4	CH1_AT_1	31:0	04000000	32	00000100_00000000 _00000000_00000000	RW	CH1_AT_1
0x97	4	CH1_RT_1	31:0	0	32	00000000_00000000 _00000000_00000000	RW	CH1_RT_1
0x98	4	CH2_ALPH A_0	31:0	04000000	32	00000100_00000000 _00000000_00000000	RW	CH2_ALPHA_0
0x99	4	CH2_ OEMGA_0	31:0	0	32	00000000_00000000 _00000000_00000000	RW	CH2_OEMGA_0
0x9A	4	CH2_THR1 _0	31:0	7B0	32	01111011_01111011 _01111011_10110000	RW	8.3 format Default = –10dB
0x9B	4	CH2_THR2 _0	31:0	710	32	01110001_01110001 _01110001_00010000	RW	8.3 format Default = –30dB

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x9C	4	CH2_DIF_THR_N_0	31:0	00333333	32	00000000_00110011_00110011_00110011	RW	CH2_DIF_THR_N_0
0x9D	4	CH2_AT_0	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_AT_0
0x9E	4	CH2_RT_0	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_RT_0
0x9F	4	CH2_ALPHA_1	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_ALPHA_1
0xA0	4	CH2_OEMGA_1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_OEMGA_1
0xA1	4	CH2_THR1_1	10:0	7B0	11	111_10110000	RW	8.3 format Default = –10dB
0xA2	4	CH2_THR2_1	10:0	710	11	111_00010000	RW	8.3 format Default = –30dB
0xA3	4	CH2_DIF_THR_N_1	31:0	00333333	32	00000000_00110011_00110011_00110011	RW	Default = 0.05dB
0xA4	4	CH2_AT_1	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	CH2_AT_1
0xA5	4	CH2_RT_1	31:0	0	32	00000000_00000000_00000000_00000000	RW	CH2_RT_1
FIR_Page								
0x30	4	FIR_TAP1	31:0	04000000	32	00000100_00000000_00000000_00000000	RW	FIR_TAP1
0x31	4	FIR_TAP2	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP2
0x32	4	FIR_TAP3	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP3
0x33	4	FIR_TAP4	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP4
0x34	4	FIR_TAP5	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP5
0x35	4	FIR_TAP6	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP6

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x36	4	FIR_TAP7	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP7
0x37	4	FIR_TAP8	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP8
0x38	4	FIR_TAP9	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP9
0x39	4	FIR_TAP10	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP10
0x3A	4	FIR_TAP11	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP11
0x3B	4	FIR_TAP12	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP12
0x3C	4	FIR_TAP13	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP13
0x3D	4	FIR_TAP14	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP14
0x3E	4	FIR_TAP15	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP15
0x3F	4	FIR_TAP16	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP16
0x40	4	FIR_TAP17	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP17
0x41	4	FIR_TAP18	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP18
0x42	4	FIR_TAP19	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP19
0x43	4	FIR_TAP20	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP20
0x44	4	FIR_TAP21	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP21
0x45	4	FIR_TAP22	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP22

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x46	4	FIR_TAP23	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP23
0x47	4	FIR_TAP24	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP24
0x48	4	FIR_TAP25	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP25
0x49	4	FIR_TAP26	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP26
0x4A	4	FIR_TAP27	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP27
0x4B	4	FIR_TAP28	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP28
0x4C	4	FIR_TAP29	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP29
0x4D	4	FIR_TAP30	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP30
0x4E	4	FIR_TAP31	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP31
0x4F	4	FIR_TAP32	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP32
0x50	4	FIR_TAP33	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP33
0x51	4	FIR_TAP34	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP34
0x52	4	FIR_TAP35	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP35
0x53	4	FIR_TAP36	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP36
0x54	4	FIR_TAP37	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP37
0x55	4	FIR_TAP38	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP38

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x56	4	FIR_TAP39	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP39
0x57	4	FIR_TAP40	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP40
0x58	4	FIR_TAP41	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP41
0x59	4	FIR_TAP42	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP42
0x5A	4	FIR_TAP43	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP43
0x5B	4	FIR_TAP44	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP44
0x5C	4	FIR_TAP45	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP45
0x5D	4	FIR_TAP46	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP46
0x5E	4	FIR_TAP47	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP47
0x5F	4	FIR_TAP48	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP48
0x60	4	FIR_TAP49	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP49
0x61	4	FIR_TAP50	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP50
0x62	4	FIR_TAP51	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP51
0x63	4	FIR_TAP52	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP52
0x64	4	FIR_TAP53	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP53
0x65	4	FIR_TAP54	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP54

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x66	4	FIR_TAP55	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP55
0x67	4	FIR_TAP56	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP56
0x68	4	FIR_TAP57	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP57
0x69	4	FIR_TAP58	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP58
0x6A	4	FIR_TAP59	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP59
0x6B	4	FIR_TAP60	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP60
0x6C	4	FIR_TAP61	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP61
0x6D	4	FIR_TAP62	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP62
0x6E	4	FIR_TAP63	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP63
0x6F	4	FIR_TAP64	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP64
0x70	4	FIR_TAP65	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP65
0x71	4	FIR_TAP66	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP66
0x72	4	FIR_TAP67	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP67
0x73	4	FIR_TAP68	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP68
0x74	4	FIR_TAP69	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP69
0x75	4	FIR_TAP70	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP70

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x76	4	FIR_TAP71	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP71
0x77	4	FIR_TAP72	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP72
0x78	4	FIR_TAP73	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP73
0x79	4	FIR_TAP74	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP74
0x7A	4	FIR_TAP75	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP75
0x7B	4	FIR_TAP76	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP76
0x7C	4	FIR_TAP77	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP77
0x7D	4	FIR_TAP78	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP78
0x7E	4	FIR_TAP79	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP79
0x7F	4	FIR_TAP80	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP80
0x80	4	FIR_TAP81	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP81
0x81	4	FIR_TAP82	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP82
0x82	4	FIR_TAP83	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP83
0x83	4	FIR_TAP84	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP84
0x84	4	FIR_TAP85	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP85
0x85	4	FIR_TAP86	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP86

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x86	4	FIR_TAP87	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP87
0x87	4	FIR_TAP88	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP88
0x88	4	FIR_TAP89	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP89
0x89	4	FIR_TAP90	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP90
0x8A	4	FIR_TAP91	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP91
0x8B	4	FIR_TAP92	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP92
0x8C	4	FIR_TAP93	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP93
0x8D	4	FIR_TAP94	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP94
0x8E	4	FIR_TAP95	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP95
0x8F	4	FIR_TAP96	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP96
0x90	4	FIR_TAP97	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP97
0x91	4	FIR_TAP98	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP98
0x92	4	FIR_TAP99	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP99
0x93	4	FIR_TAP100	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP100
0x94	4	FIR_TAP101	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP101
0x95	4	FIR_TAP102	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP102

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x96	4	FIR_TAP103	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP103
0x97	4	FIR_TAP104	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP104
0x98	4	FIR_TAP105	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP105
0x99	4	FIR_TAP106	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP106
0x9A	4	FIR_TAP107	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP107
0x9B	4	FIR_TAP108	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP108
0x9C	4	FIR_TAP109	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP109
0x9D	4	FIR_TAP110	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP110
0x9E	4	FIR_TAP111	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP111
0x9F	4	FIR_TAP112	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP112
0xA0	4	FIR_TAP113	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP113
0xA1	4	FIR_TAP114	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP114
0xA2	4	FIR_TAP115	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP115
0xA3	4	FIR_TAP116	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP116
0xA4	4	FIR_TAP117	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP117
0xA5	4	FIR_TAP118	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP118

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0xA6	4	FIR_TAP119	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP119
0xA7	4	FIR_TAP120	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP120
0xA8	4	FIR_TAP121	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP121
0xA9	4	FIR_TAP122	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP122
0xAA	4	FIR_TAP123	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP123
0xAB	4	FIR_TAP124	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP124
0xAC	4	FIR_TAP125	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP125
0xAD	4	FIR_TAP126	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP126
0xAE	4	FIR_TAP127	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP127
0xAF	4	FIR_TAP128	31:0	00000000	32	00000000_00000000_00000000_00000000	RW	FIR_TAP128

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
Analog Portion								
0x00	2	DEV_ID	15:0	5140	16	01010001_01000000	RO	PRODUCT_ID
0x01	1	I2S_CLK_FMT	7:4	5	4	0101	RW	Sampling rate report 0000: 8kHz 0001: 11.025/12kHz 0010: 16kHz 0011: 22.05/24kHz 0100: 32KHz 0101: 44.1/48kHz (default) 0110: 88.2/96kHz 0111: 192kHz Others: Reserved
			3:0	2	4	0010	RW	BCK mode report 0000: BCK = 32fs 0001: BCK = 48fs 0010: BCK = 64fs (default) 0011: BCK = 96fs 0100: BCK = 128fs 0101: BCK = 192fs 0110: BCK = 256fs 0111: BCK = 384fs 1000: BCK = 512fs Others: Reserved

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x02	1	I2S_DATA_FMT	7	0	1	0	RW	I²S data data out launch edge selection 0: BCK_RX_EDGE = 0, launch with falling edge; BCK_RX_EDGE = 1, launch with rising edge (default) 1: BCK_RX_EDGE = 0, launch with rising edge; BCK_RX_EDGE = 1, launch with falling edge
			6	0	1	0	RW	0: RX @BCK rising edge and TX @BCK falling edge (default) 1: RX @BCK falling edge and TX @BCK rising edge
			5:4	2	2	10	RW	Audio bits for signal process 00: 16bits 01: 20bits 10: 24bits (default) 11: 32bits
			3	1	1	1	RW	TDM or DSPM offset selection 0: Without offset (DSPMB) 1: 1bit clock offset (DSPMA) (default)
			2:0	0	3	000	RW	I²S format selection 000: I²S (default) 001: Left Justify 010: Right Justify 011: DSP mode 100: EIAJ Others: TDM mode

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x03	1	SIL_CTRL	7	1	1	1	RW	Silence detection enable 0: Disable 1: Enable (default)
			5:4	3	2	11	RW	Silence detection threshold selection (only one threshold for 8-bit) 00: –72dB (16bit)/–96dB (20bit)/–120 dB (24bit)/–144dB (32bit) 01: –78dB (16bit)/–102dB (20bit)/–126dB (24bit)/–150dB (32bit) 10: –84dB (16bit)/–108dB (20bit)/–132dB (24bit)/–156dB (32bit) 11: –90dB (default) (16bit)/–114dB (20bit)/–138dB (24bit)/–166dB (32bit)
			2:0	2	3	010	RW	Silence mode hold time selection 000: 1ms 001: 20ms 010: 40ms (default) 011: 80ms 100: 160ms 101: 320ms 110: 640ms 111: 1.28s
0x04	1	SDIO_SEL	5:4	0	2	00	RW	00: No output (default) 01: Interface output 10: Final output 11: Peak level detect result
			3:2	0	2	00	RW	00: SDIN-L to CH1 (default) 01: SDIN-R to CH1 1X: 0 to CH1
			1:0	1	2	01	RW	00: SDIN-L to CH2 01: SDIN-R to CH2 (default) 1X: 0 to CH2

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x05	1	SYS_CTL	7	1	1	1	RW	Sampling rate detection enable bit detect sampling rate and BCK mode 0: Disable, manual set 0x01 SR mode and BCK mode 1: Enable (default)
			6	0	1	0	RW	DRE offset calibration enable 0: Disable (default) 1: Enable
			5	0	1	0	RW	Reserved for new feature 0: BTL mode (default) 1: CMH mode
			4	0	1	0	RW	0: BTL (default) 1: PBTL
			3:2	1	2	01	RW	VTRI frequency 00: 400kHz 01: 800kHz (default) 10: None 11: None
			1:0	0	2	00	RW	AMP control 00: amp off (default) 01: amp on 10: Force entry silence mode 11: mute

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x06	1	BLK_EN	6	0	1	0	RW	0: Compensation filter disable (default) 1: Compensation filter enable (not available in 96k and 192kHz sampling rate)
			5	1	1	1	RW	0: High-Pass filter disable 1: High-Pass filter enable (default)
			4	0	1	0	RW	Thermal foldback control enable 0: Disable 1: Enable (default)
			3	1	1	1	RW	DRC mode selection 0: RMS mode 1: Peak mode (default)
			2	0	1	0	RW	DRC enable 0: Disable (default) 1: Enable
			1	0	1	0	RW	DRC noise gate enable 0: Disable (default) 1: Enable
			0	0	1	0	RW	Hard clip enable 0: Disable (default) 1: Enable

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x07	1	ANA_OUT_CTRL	7:5	0	3	000	RW	PWM output phase select 000: 0 (default) 001: 45 010: 90 011: 135 100: 180 101: 225 110: 270 111: 315
			4:0	13	5	10011	RW	Class-D output gain, 5'h00: –6dB 5'h01: –5dB 5'h02: –4dB 5'h03: –3dB 5'h04: –2dB 5'h05: –1dB 5'h06: 0dB 5'h07: 1dB 5'h08: 2dB 5'h09: 3dB 5'h0A: 4dB 5'h0B: 5dB 5'h0C: 6dB 5'h0D: 7dB 5'h0E: 8dB 5'h0F: 9dB 5'h10: 10dB 5'h11: 11dB 5'h12: 12dB 5'h13: 13dB (default) 5'h14: 14dB 5'h15: 15dB 5'h16: 16dB 5'h17: 17dB 11000 ~ 11111: No setting

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x08	1	OLSL_CTRL	7	0	1	0	RW	Reserved
			5	0	1	0	RO	Open/Short load detection finish 0: Not enable or under detection (default) 1: Finish
			4	0	1	0	RW	Open/Short load detection enable 0: Disable (default) 1: Enable
			3	0	1	0	RO	Open load report for channel L 0: Normal (default) 1: Open
			2	0	1	0	RO	Open load report for channel R 0: Normal (default) 1: Open
			1	0	1	0	RO	Short load report for channel L 0: Normal (default) 1: Short
			0	0	1	0	RO	Short load report for channel R 0: Normal (default) 1: Short

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x09	1	PWM_SS_OPT	7	0	1	0	RW	Spread spectrum enable 0: Disable (default) 1: Enable
			6	0	1	0	RW	Noise select 0: Pink noise (default) 1: White noise
			5	0	1	0	RW	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4
			4	0	1	0	RW	Add noise to TRI_GEN 0: Disable (default) 1: Enable
			3:2	0	2	00	RW	Nosie amplitude for SSC 00: 5.78% (default) 01: 11.55% 10: 17.33% 11: 23.1%
			1:0	1	2	01	RW	Spread spectrum frequency variation amplitude 00: 16.60% 01: 33.19% (default) 10: 33.19% 11: 49.79%

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x0A	1	RAMP_CTRL	5	0	1	0	RW	0: Unmute (default) 1: CH2 soft mute
			4	0	1	0	RW	0: Unmute (default) 1: CH1 soft mute
			3	0	1	0	RW	0: Not skip ramp (default) 1: Skip volume ramp
			1:0	1	2	01	RW	Volume slew step control 00: 4.33ms from mute to 0dB (0.5dB/20.83μs) 01: 8.66ms from mute to 0dB (0.25dB/20.83μs) (default) 10: 17.33ms from mute to 0dB (0.125dB/20.83μs) 11: 34.65ms from mute to 0dB (0.0625dB/20.83μs)
0x0B	1	TFC_CTRL	7	0	1	0	RO	Reserved
			6	0	1	0	RO	Reserved
			5:4	0	2	00	RW	Thermal foldback active threshold 00: Temp 110°C (default) 01: Temp 120°C 10: Temp 130°C 11: Temp 140°C
			3:2	0	2	00	RW	Thermal foldback attack/release rate 00: 0.0625dB/25ms (default) 01: 0.0625dB/50ms 10: 0.0625dB/100ms 11: 0.0625dB/200ms
			1:0	0	2	00	RW	Thermal foldback attack/release rate 00: 0.0625dB/50ms (default) 01: 0.0625dB/100ms 10: 0.0625dB/200ms 11: 0.0625dB/400ms

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x0C	1	TDM_RX_LOC_L	5:0	0	6	000000	RW	TDM start reviving location select for left channel 00000: Start from 0+offset (default) 00001: Start from 8+offset … 11100: Start from 488+offest 11101: Start from 496+offset 11110: Not available 11111: Not available
0x0D	1	TDM_RX_LOC_R	5:0	3	6	000011	RW	TDM start reviving location select for left channel 00000: Start from 0+offset 00001: Start from 8+offset … 11100: Start from 488+offest 11101: Start from 496+offset 11110: Not available 11111: Not available
0x0E	1	TDM_TX_LOC_L	5:0	0	6	000000	RW	TDM start transmitting location select for left channel 00000: Start from 0+offset (default) 00001: Start from 8+offset … 11100: Start from 488+offest 11101: Start from 496+offset 11110: Not available 11111: Not available

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x0F	1	TDM_TX_LOC_R	5:0	3	6	000011	RW	TDM start transmitting location select for right channel 00000: Start from 0+offset 00001: Start from 8+offset … 11100: Start from 488+offest 11101: Start from 496+offset 11110: Not available 11111: Not available
0x10	1	ERR_RPT	7	0	1	0	W1C	Reserved
			6	0	1	0	W1C	DC flag report 0: No DC error (default) 1: DC error
			5	0	1	0	W1C	0: No SCLK error (default) 1: SCLK error, write 1 to clear flag
			4	0	1	0	W1C	0: No LRCK clock error (default) 1: LRCK clock error, write0 to clear flag
			3	0	1	0	W1C	0: No OC error (default) 1: OC, write 1 to clear flag
			2	0	1	0	W1C	0: No OV error (default) 1: OV, write 1 to clear flag
			1	0	1	0	W1C	0: No OT error (default) 1: OT, write 1 to clear flag
			0	0	1	0	W1C	0: No UV error (default) 1: UV, write 1 to clear flag

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x11	1	ERR_MASK	6	0	1	0	RW	Fault mask for DC error 0: Not mask (default) 1: Mask
			5	1	1	1	RW	Fault mask for 0x02 SCLK error 0: Not mask 1: Mask (default)
			4	1	1	1	RW	Fault mask for 0x02 LRCK error 0: Not mask 1: Mask (default)
			3	0	1	0	RW	Fault mask for 0x02 OC error 0: Not mask (default) 1: Mask
			2	0	1	0	RW	Fault mask for 0x02 OV error 0: Not mask (default) 1: Mask
			1	0	1	0	RW	Fault mask for 0x02 OT error 0: Not mask (default) 1: Mask
			0	0	1	0	RW	Fault mask for 0x02 UV error 0: Not mask (default) 1: Mask
0x12	1	ERR_TYPE	3	1	1	1	RW	OCP fault behavior type select. 0: Auto-recovery (default) 1: Latch
			2	0	1	0	RW	OVP fault behavior type select. 0: Auto-recovery (default) 1: Latch
			1	0	1	0	RW	OTP fault behavior type select. 0: Auto-recovery (default) 1: Latch
			0	0	1	0	RW	UVP fault behavior type select. 0: Auto-recovery (default) 1: Latch

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x13	1	FAULT_CTRL	3:0	2	4	0010	RW	Power stage auto-recovery time 0010: 299ms (default) 0011: 449ms 0100: 598ms 0101: 748ms 0110: 898ms 0111: 1047ms 1000: 1197ms 1001: 1346ms 101X: 1496ms 11XX: 1496ms
0x14	1	DC_PORT_OPT	3:2	2	2	10	RW	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%
			1	0	1	0	RW	Detection time 0: 342ms (default) 1: 684ms
			0	1	1	1	RW	DC protection enable 0: Disable 1: Enable (default)

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x15	1	ANA_PWR_CTRL1	7	1	1	1	RW	Enable DAC RCH LPF 0: Disable 1: Enable (default)
			6	1	1	1	RW	Enable DAC LCH LPF 0: Disable 1: Enable (default)
			5	1	1	1	RW	RCH PWR stage enable 0: Disable 1: Enable (default)
			4	1	1	1	RW	LCH PWR stage enable 0: Disable 1: Enable (default)
			3	1	1	1	RW	Enable DAC_RCH 0: Disable 1: Enable (default)
			2	1	1	1	RW	Enable DAC LCH 0: Disable 1: Enable (default)
			1	1	1	1	RW	MD RCH enable 0: Force off 1: Follow sequence (default)
			0	1	1	1	RW	MD LCH enable 0: Force off 1: Follow sequence (default)
0x16	1	ANA_PWR_CTRL2	5	0	1	0	RW	Reserved
			4	0	1	0	RW	Reserved
			3	0	1	0	RW	Reserved
			2	0	1	0	RW	Reserved
			1	0	1	0	RW	Reserved
			0	0	1	0	RW	Reserved
0x20	2	Master Volume	10:0	7FF	11	111_11111111	RW	Master volume control 11'h000: 24dB 11'h180: 0dB 11'h7FF: mute (default) 0.0625dB per step
0x21	2	Ch1 Volume	10:0	180	11	001_10000000	RW	CH1 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step

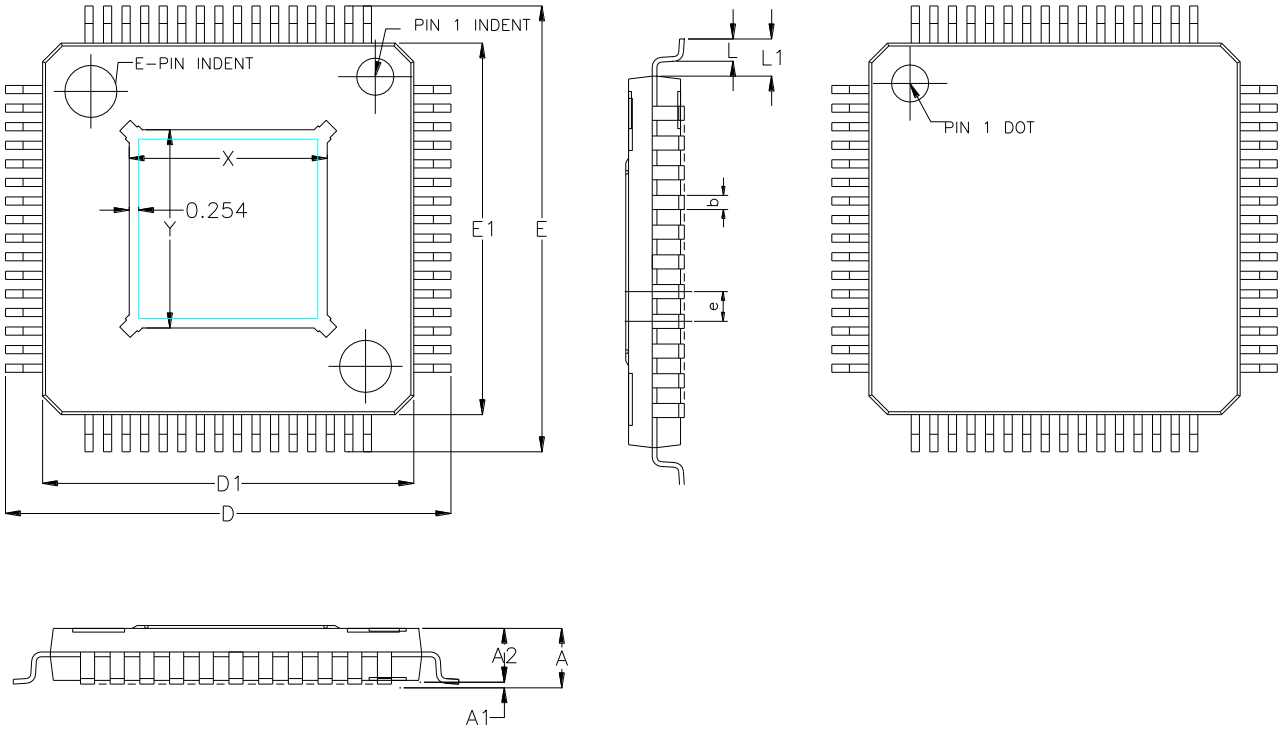
Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x22	2	Ch2 Volume	10:0	180	11	001_10000000	RW	CH2 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step
0x23	2	DRCThreshold	10:0	0	11	000_00000000	RW	DRC threshold 11'h000: 0dB (default) 11'h180: –24dB 11'h67E: –103.875dB 11'h67F to 11'h7FF: Not available 0.0625dB per step
0x24	2	DRC Ratio	7:0	80	8	10000000	RW	DRC compress ratio 8'h00: No compression 8'h80 to 8'hFF: Full compression 1/128 per step
0x25	2	DRC Make Up Gain	10:0	180	11	001_10000000	RW	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: –103.9375dB 0.0625dB per step
0x26	2	DRC Noise Gate	10:0	640	11	110_01000000	RW	Noise gate threshold 11'h000: 0dB 11'h180: –24dB 11'h640: –100dB (default) 11'h67E: –103.875dB 11'h67F to 11'h7FF: Not available 0.0625dB per step
0x27	2	Hard Clipping Threshold	10:0	180	11	001_10000000	RW	Hard clip threshold when HARD_CLIP_EN = 1 >0dB is not allowable for hard clip threshold setting 11'h180: 0dB (default) 0.0625db per step
0x28	2	Volume control for open load detection	10:0	23E	11	010_00111110	RW	Volume control for open load detection 11'h000: 24dB 11'h180: 0dB 11'h23E: –11.875dB (default) 11'h7FF: mute 0.0625dB per step

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x29	2	Volume control for short load detection	10:0	310	11	011_00010000	RW	Volume control for short load detection 11'h000: 24dB 11'h180: 0dB 11'h310: −25dB (default) 11'h7FF: mute 0.0625dB per step
0x30	3	CH1_IN_MIX_0	16:0	08000	17	0_10000000_00000000	RW	CH1_IN_MIX_0
0x31	3	CH1_IN_MIX_1	16:0	0	17	0_00000000_00000000	RW	CH1_IN_MIX_1
0x32	3	CH2_IN_MIX_0	16:0	0	17	0_00000000_00000000	RW	CH2_IN_MIX_0
0x33	3	CH2_IN_MIX_1	16:0	08000	17	0_10000000_00000000	RW	CH2_IN_MIX_1
0x34	3	DRC_AE	16:0	08000	17	0_10000000_00000000	RW	DRC_AE
0x35	3	DRC_1-AE	16:0	0	17	0_00000000_00000000	RW	DRC_1-AE
0x36	3	DRC_AD	16:0	08000	17	0_10000000_00000000	RW	DRC_AD
0x37	3	DRC_AA	16:0	08000	17	0_10000000_00000000	RW	DRC_AA
0x38	3	RMS_RPT_AE	16:0	08000	17	0_10000000_00000000	RW	RMS_RPT_AE
0x3A	3	Compensation filter coefficient B0	16:0	08000	17	0_10000000_00000000	RW	Compensation filter coefficient B0
0x3B	3	Compensation filter coefficient B1	16:0	0	17	0_00000000_00000000	RW	Compensation filter coefficient B1
0x3C	3	Compensation filter coefficient B2	16:0	0	17	0_00000000_00000000	RW	Compensation filter coefficient B2
0x3D	3	Compensation filter coefficient B3	16:0	0	17	0_00000000_00000000	RW	Compensation filter coefficient B3
0x3E	4	CH1_RMS_RPT	31:0	0	32	00000000_00000000_00000000_00000000	RO	Prohibited
0x3F	4	CH2_RMS_RPT	31:0	0	32	00000000_00000000_00000000_00000000	RO	Prohibited

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x40	1	SW_RESET	7	0	1	0	WO	Prohibited
0x6C	1	UVP_OPT	7	1	1	1	RW	Prohibited
			6	1	1	1	RW	0: Disable 1: Enable (default)
			5:4	01	2	01	RW	Adjust UVP threshold for detecting DVDD = 3.3V Rising: 11: 2.7V 10: 2.6V 01: 2.5V (default) 00: 1.48 (= VR_DIG) Falling: 11: 2.8V 10: 2.7V 01: 2.6V (default) 00: 1.55 (= VR_DIG)
			2:0	000	2	000	RW	Select UVP level for PVDD power domain 000: 4.1V (default) 001: 6V 010: 8.5V 011: 9.5V 100: 10.9V 101: 12.7V 110: 15.4V 111: 20V
0x71	1	FAULT_ RAMP_OPT	1	1	1	1	RW	PVDD UVP protection behavior 0: HZ_PROT directly 1: Power-off sequence (default)

Addr	Length	RegName	Bit	Hex Default	Bit Number	Default	Type	Description
0x94	1	CMH_TH	7:0	45	8	01000101	RW	threshold of CMH to BD mode modulation 8'h00: DRE_TH (CMH switch with DRE) Others: 20*log10(CMH_TH/2^10)dB 8'h45: –23.43dB (Po= 0.5W) 8'h78: –18.66dB (Po= 1.5W) 8'h8A: –17.41 (Po=2W) (Po is based on SPK Gain = 18db, RL = 6Ω)

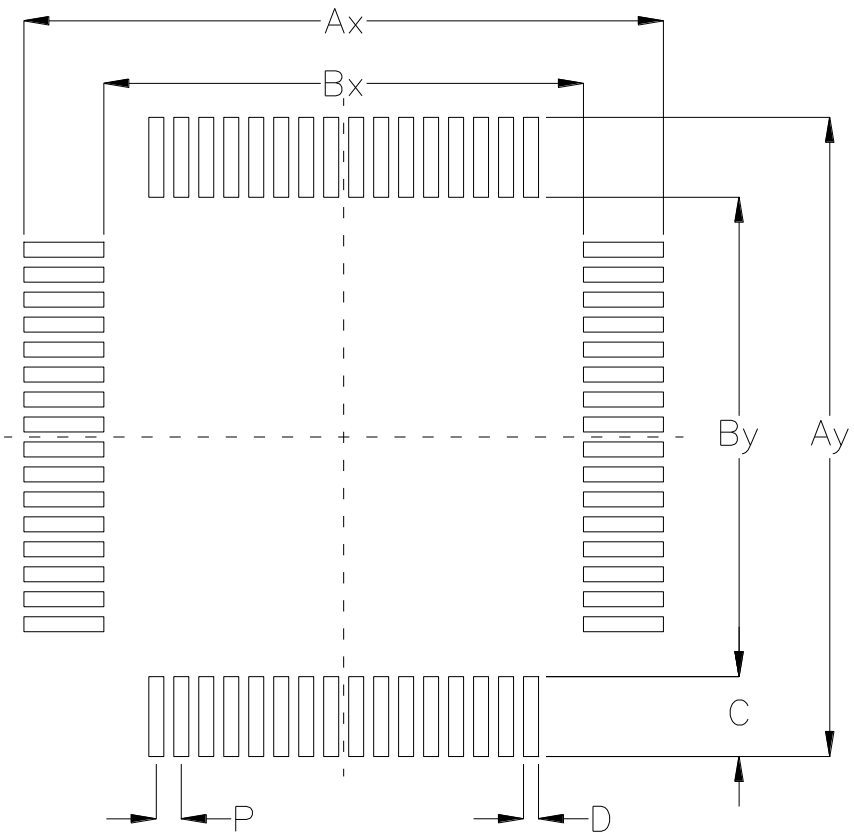
21 Outline Dimension



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	normal	Max	Min	normal	Max
A	1.400	1.500	1.600	0.055	0.059	0.063
A1	0.050	0.100	0.150	0.002	0.004	0.006
A2	1.350	1.400	1.450	0.053	0.055	0.057
b	0.170	0.220	0.270	0.007	0.009	0.011
C	0.090	0.150	0.200	0.004	0.006	0.008
D	11.800	12.000	12.200	0.465	0.472	0.480
E	11.800	12.000	12.200	0.465	0.472	0.480
D1	9.900	10.000	10.100	0.390	0.394	0.398
E1	9.900	10.000	10.100	0.390	0.394	0.398
X	4.675	5.334	5.434	0.184	0.210	0.214
Y	4.675	5.334	5.434	0.184	0.210	0.214
e	0.500			0.020		
L	0.450	0.600	0.750	0.018	0.024	0.030
L1	0.800	1.000	1.200	0.031	0.039	0.047

RLQFP-64L 10x10 (Exposed Pad) Plastic Package

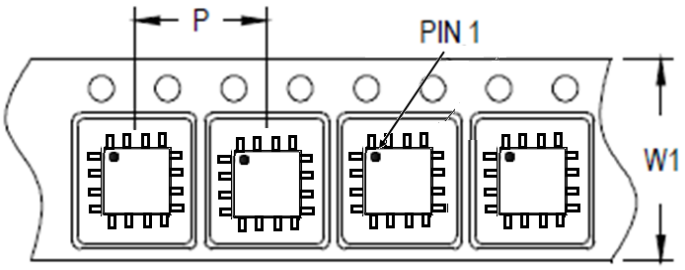
22 Footprint Information

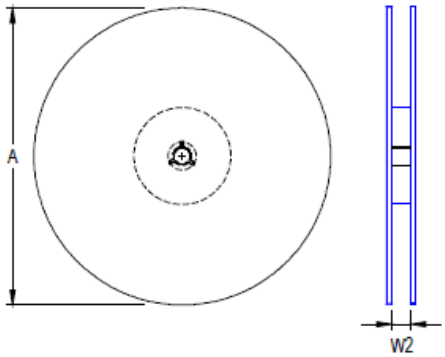


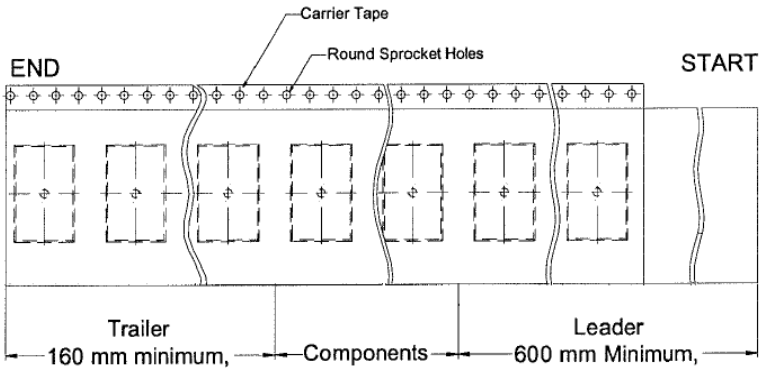
Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P	Ax	Ay	Bx	By	C	D	
RLQFP10x10-64(PP)	64	0.50	12.80	12.80	9.60	9.60	1.60	0.30	±0.05

23 Packing Information

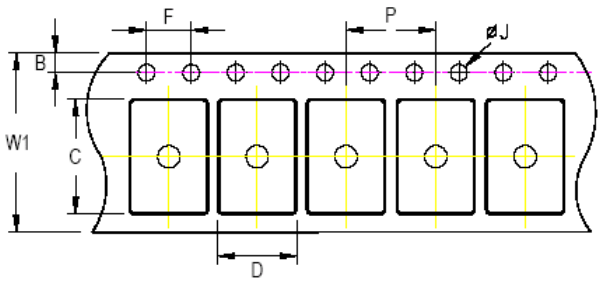
23.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
LQFP10x10	24	16	330	13	1,500	160	600	24.4/26.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 24mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
24mm	24.3mm	15.9mm	16.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	2.1mm	2.3mm	0.6mm

23.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Package \ Container	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
LQFP10x10	13”	1,500	Box G	1	1,500	Carton A	6	9,000

23.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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24 Datasheet Revision History

Version	Date	Description	Item
00	2025/3/7	Final	*Applications on page 1* - Updated applications *Ordering Information on page 1* *Absolute Maximum Ratings on page 8* - Updated the value of θJC(Top) and Note 5 *Electrical Characteristics on page 10* - Modified the value of Cross-Talk *Application Information on page 82, 86* - Modified Table 1 - Modified layout description