30W, Stereo, Ultra Low Noise, High-Efficiency, Inductor-Less, I²S General-Purpose Class-D Audio Amplifier with DRC Control

General Description

The RT9120S is a high efficiency, I²S-input, stereo channel audio power amplifier delivering maximum 2x30W into 8Ω BTL speaker loads. It can deliver over 94% power efficiency at 2x10W and eliminate the need for heatsink.

The built-in anti-pop functions can reduce the speaker's pop noise under all kind of scenarios. Built-in protection circuits can provide over-temperature, overcurrent, overvoltage, undervoltage protections and report error status.

The RT9120S is a 3-wired device receiving all clocks from external sources with standard I²S, Left-justified, Right-justified or TDM formats. It can support wide input sampling rate from 8kHz to 192kHz.

The RT9120S features one band DRC and flexible input mixer, and power clipping.

Ordering Information

RT9120S □□

- Package Type
  QV: VQFN-32L 5x5 (V-Type)
- Lead Plating System
  G: Green (Halogen Free and Pb Free)

Note:

Richtek products are:

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Wide Input Supply Range: 4.5V to 26.4V**
- **Support 1.8V, 3.3V I/O**
- **Configurable 4 Different IC Slave Address**
- **1x53W, 1.0 Mode (4Ω, 22V, THD + N = 1%)**
- **2x30W, 2.0 Mode (8Ω, 24V, THD + N = 1%)**
- **SNR Up to 113dB**
- **THD + N is 0.03% at 1W**
- **35μV Noise Floor**
- **Efficiency Up to 94% at 2x10W for 8Ω**
- **$R_{DS(ON)}$ Low to 90mΩ**
- **PWM Switching Frequency up to 1.536MHz**
- **Sampling Frequency from 8kHz to 192kHz**
- **Support TDM Format for Multi-Channel**
- **Built-In Anti-Pop Function**
- **Programmable Coefficients for DRC Filters**
- **Built-In DC Blocking Filters**
- **Built-in Thermal Fold Back control**
- **Protection Features: UVLO, OVP, OCP, OTP and DCP**
- **Inductor-Less Application**
- **VQFN-32L Thermally-Enhanced Package**
- **RoHS Compliant and Halogen Free**

Applications

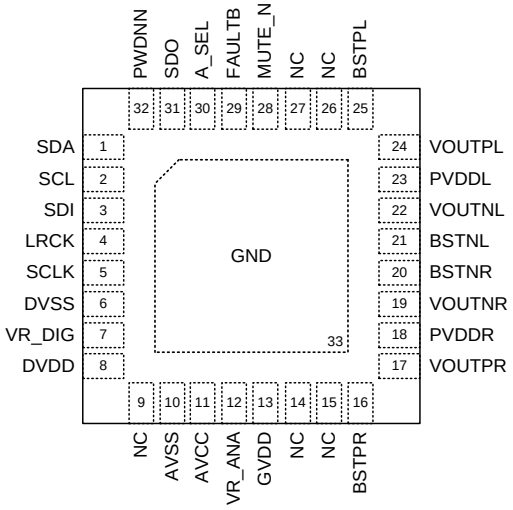
- LCD-TV
- Monitors
- Home Audio
- Amusement Equipment
- Electronic Music Equipment

Marking Information

RT9120SGQV: Product Code
YMDNN: Date Code

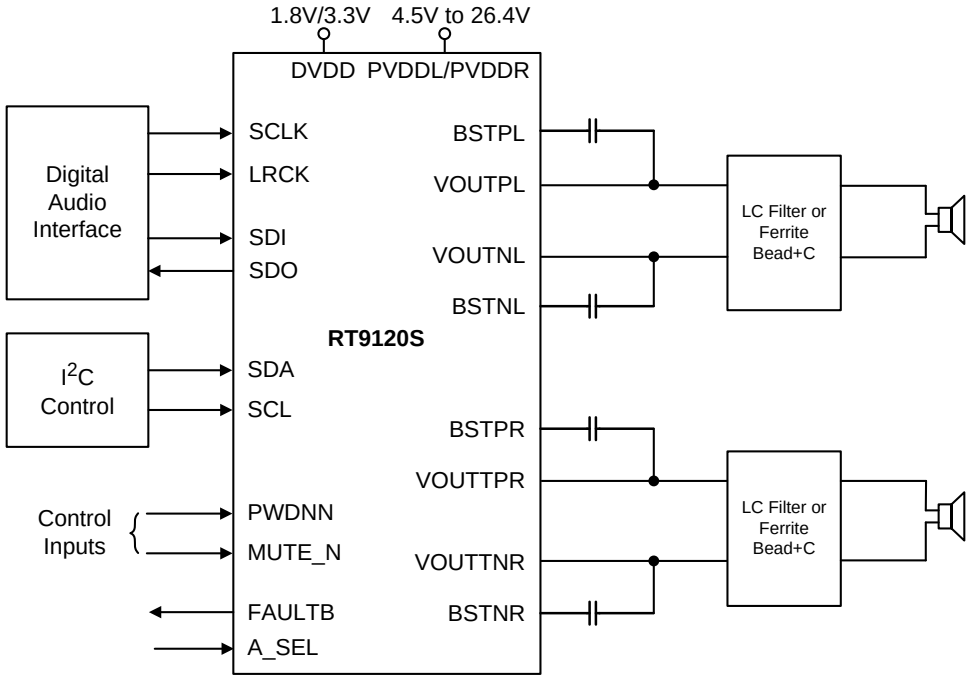
Pin Configuration

(TOP VIEW)



VQFN-32L 5x5

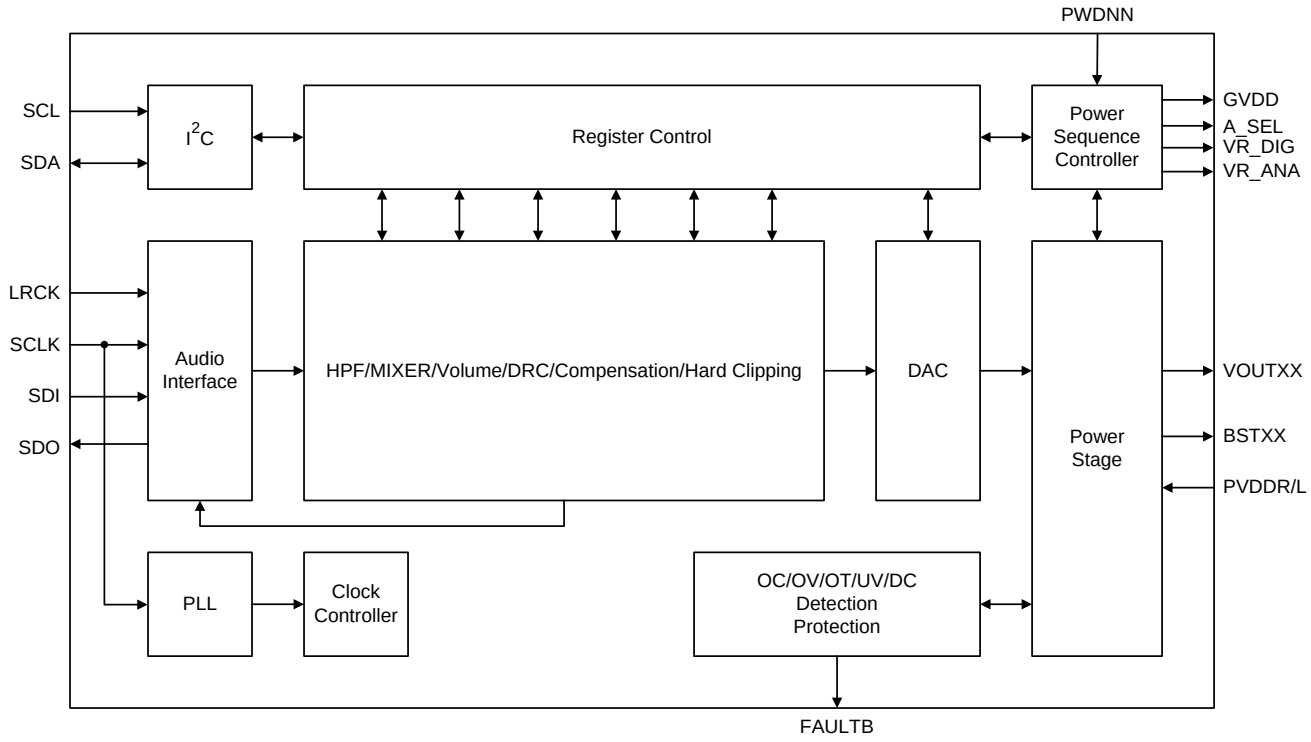
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	IO	Pin Function
1	SDA	DIO	I^2C data input/output.
2	SCL	DI	I^2C clock input.
3	SDI	DI	I^2S data input.
4	LRCK	DI	I^2S L/R clock input.
5	SCLK	DI	I^2S bit clock input.
6	DVSS	P	Ground for digital circuits.
7	VR_DIG	P	1.8V digital supply voltage generated by internal LDO. Noted: when DVDD is 1.8V, please connect DVDD to the VR_DIG.
8	DVDD	P	3.3V, 1.8V power supply for I/O.
9, 14, 15, 26, 27	NC	P	No internal connection. (For the layout, please tight to GND)
10	AVSS	P	Ground for analog circuits.
11	AVCC	P	26.4V power supply for analog circuits.
12	VR_ANA	P	Analog reference voltage.
13	GVDD	P	Internal power supply generated by LDO.
16	BSTPR	P	Bootstrap supply for VOUTPR.
17	VOUTPR	AO	Positive output of RCH.
18	PVDDR	P	26.4V power supply for RCH.
19	VOUTNR	AO	Negative output of RCH.
20	BSTNR	P	Bootstrap supply of VOUTNR.
21	BSTNL	P	Bootstrap supply for VOUTNL.
22	VOUTNL	AO	Negative output of LCH.
23	PVDDL	P	26.4V power supply for LCH.
24	VOUTPL	AO	Positive output of LCH.
25	BSTPL	P	Bootstrap supply for VOUTPL.
28	MUTE_N	DI	Mute pin.
29	FAULTB	DO	Fault indicator (low active).
30	A_SEL	DI	Slave address selection.
31	SDO	DO	I^2S data output.
32	PWDNN	DI	Power down pin, low active.
33 (Exposed Pad)	PVSS	P	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

Error Reporting

The FAULTB pin is for report error status. The FAULTB go to low when protection happen. This pin is open-drain configuration, need pull-up resistor.

Clock Detection

The RT9120S can accept SCLK to be as 32fs, 48fs and 64fs and support only a 1xfs LRCK. The internal oscillator will check SCLK input constantly. If clock is lost, the RT9120S will shut down the power stage automatically.

Volume Control

The RT9120S have master volume MS_VOL and each channel volume CH1_VOL, CH2_VOL control. The step of each volume is 0.0625dB per step, from 24dB to mute. CH1 and CH2 also have each mute control, CH1_MUTE and CH2_MUTE.

Built-In Anti-POP Function

An internal soft-start function controls the duty ramp-up rate of the output PWM voltage to minimize the POP noise during start-up. Similarly, when power shut-down, the duty also ramp-down to eliminate the POP noise. This function also acts when the PWDNN pin turns-ON/OFF.

Overcurrent Protection

The RT9120S provides OCP function to prevent the device from damages during overload or short-circuit conditions.

The current function is detected by an internal sensing circuit. Once when the inductor short to the each other and to GND the OCP function is design to operate the latch mode.

Undervoltage Protection

The RT9120S monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin falls below the undervoltage threshold, 4V (Which can be programmable.), the UVP circuit turns off the output immediately, or the latch mode can configure to use.

Overvoltage Protection

The RT9120S monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin rise behind the overvoltage threshold, 30V, the OVP circuit turns off the output immediately and operates in auto-recovery mode, or the latch mode can configure to use.

Over-Temperature Protection

The over-temperature protection function will turn off the power MOSFET when the junction temperature exceeds 150°C (minimum). Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation, or the latch mode can configure to use.

Dynamic Range Enhancement

The dynamic range enhancement which enhance the dynamic range for the application. It will optimize the noise when the operating.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, AVCC, PVDDL, PVDDR ---------- –0.3V to 32V
- Supply Voltage, DVDD ---------- –0.3V to 9V
- Speaker Amplifier Output Voltage, VOUTXX ---------- –0.3V to 32V
- BSTXX (Note 2) ---------- –0.3V to 36V
- SCL, SDA, FAULTB ---------- –0.3V to 6V
- LRCK, SCLK, SDI, MUTE_N, PWDNN, A_SEL ---------- –0.3V to DVDD + 0.5V
- GND to PVSS, DVSS and AVSS ---------- –0.3V to 0.3V
- VOUTPR, VOUTNR, VOUTPL, VOUTNL (Note 3) ---------- –10V to 37V
- SDO ---------- –0.3V to 9V
- VR_DIG ---------- –0.3V to 4V
- VR_ANA, GVDD ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-32L 5x5 ---------- 4.51W
- Package Thermal Resistance (Note 4)
  VQFN-32L 5x5, θ_{JA} ---------- 27.7°C/W
  VQFN-32L 5x5, $\theta_{JC(TOP)}$ ---------- 0.3°C/W
  VQFN-32L 5x5, $\theta_{JC(BOTTOM)}$ ---------- 0.7°C/W
- Package Thermal Resistance (4-Layer EVB)
  VQFN-32L 5x5, θ_{JA} ---------- 17.53°C/W
  VQFN-32L 5x5, $\theta_{JC(TOP)}$ ---------- 1.6°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 6)

- Supply Input Voltage, DVDD ---------- 3.0V to 3.6V
- Supply Input Voltage (For 1.8V I/O), DVDD, VR_DIG ---------- 1.62V to 1.98V
- Supply Input Voltage, PVDDL, PVDDR, AVCC ---------- 4.5V to 26.4V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 150°C

Electrical Characteristics

(PVDDL = PVDDR = AVCC = 12V, DVDD = 3.3V, R_L = 8Ω, T_A = 25°C, fsw = 384kHz, L = 10μH, C = 0.47μF, unless otherwise specified.) (Note 7)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
PWDNN	VIH: High-Level-Input Voltage	V_{IH}			DVDD x 0.7	--	--	V
	VIL: Low-Level-Input Voltage	V_{IL}			--	--	DVDD x 0.3	
FAULTB	VOL: Low-Level-Output Voltage	V_{OL}	I_{PULLUP} = 3mA		--	--	0.4	V
DVDD Quiescent Current (Normal Mode)		I_{Q_D}	PWDNN = 3.3V, for DVDD, no load, no LC filter		--	7.5	15	mA
DVDD Shut Down Current		I_{SD_D}	PWDNN = 0.8V, for DVDD, no load, no LC filter		--	--	15	μA
PVDDL/R + AVCC Quiescent Current (Normal Mode)		I_{Q_P}	PWDNN = 3.3V, switch 50% duty , no load, no LC filter		--	20	25	mA
PVDDL/R + AVCC Shut Down Current		I_{SD_P}	PWDNN = 0.8V, no load, no LC filter		--	--	20	μA
Drain-Source On-State Resistance		$R_{DS(ON)}$	PVDD = 12V, I_{OUT} = 500mA, T_J = 25°C	High-Side	--	90	--	mΩ
				Low-Side	--	85	--	
Speaker Gain Variation		$\Delta A_{V(SPK\_AMP)}$	Gain different between L and R channel		–0.5	--	0.5	dB
Startup Time from Shut Down		t_{ON}	Excluding volume ramp		--	80	--	ms
Shut Down Time from Enable		t_{OFF}	Excluding volume ramp		--	60	--	ms
PWM Switching Frequency		f_{SW}	384kHz mode		364.8	384	403.2	kHz
			768kHz mode		729.6	768	806.4	
			1536kHz mode		1459.2	1536	1612.8	
RMS Output Power		P_O	THD + N = 10%, (BTL), PVDD = 12V, RL = 8Ω		9	10	--	W
			THD + N = 1%, (BTL), PVDD = 24V, RL = 8Ω		28	30	--	
Total Harmonic Distortion + Noise		THD+N	P_O =1W (BTL)		--	0.03	0.1	%
Output Integrated Noise		Vn	20Hz to 20kHz, A-weighted		--	35	--	μV
Output Offset Voltage		V_{OS}	PVDD = 12V, disable DC Calibration		–6.5	--	6.5	mV
			PVDD = 12V, enable DC calibration		–5	--	5	
			PVDD = 24V, disable DC Calibration		–13	--	13	
			PVDD = 24V, enable DC calibration		–5	--	5	
Cross-Talk		X_{TALK}	Output power = 1W, none shielding choke		--	–75	--	dB
			Output power = 1W, with shielding choke		--	–100	--	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Signal-to-Noise Ratio		SNR	THD + N = 1%, PVDD = 24V	--	113	--	dB
Power Supply Rejection Ratio (On Going to Discuss)		PSRR	Frequency @ 1kHz	--	–75	--	dB
Dynamic Range		DR	Input level –60dBFS	--	108	--	dB
Efficiency		η	Output Power = 10W + 10W	--	94	--	%
Over-Temperature Protection		OTP	Guaranteed by design	150	160	175	°C
Thermal Hysteresis				--	30	--	°C
Overcurrent Protection		OCP	For the PWM is 384kHz	6	7	--	A
			For the PWM is 1.5MHz	5	--	--	
PVDDL/PVDDR Overvoltage		OVP		--	30	--	V
PVDDL/PVDDR Undervoltage (Programmable)		UVP		--	4	--	V
I^2C Interface Electrical Characteristics							
High-Level Input Voltage (Belongs to the internal 1.8V domain)		V_{IH}		VR_DIG x 0.7	--	--	V
Low-Level Input Voltage (Belong to the internal 1.8V domain)		V_{IL}		--	--	VR_DIG x 0.3	V
Digital Output Low (SDA)		V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency		f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition		t_{BUF}		1.3	--	--	µs
Hold Time After (Repeated) Start Condition		$t_{HD,STA}$		0.6	--	--	µs
Repeated Start Condition Setup Time		$t_{SU,STA}$		0.6	--	--	µs
Stop Condition Time		$t_{SU,STD}$		0.6	--	--	µs
Input Data Hold Time		$t_{HD,DAT(IN)}$		0	--	900	ns
Data Setup Time		$t_{SU,DAT}$		100	--	--	ns
Clock Low Period		t_{LOW}		1.3	--	--	µs
Clock High Period		t_{HIGH}		0.6	--	--	µs
Clock Data Fall Time		t_F		20	--	300	ns
Clock Data Rise Time		t_R		20	--	300	ns
Spike Suppression Time		t_{SP}		--	--	20	ns
I^2S Interface Electrical Characteristics							
High-Level Input Voltage		V_{IH}		2.5	--	--	V
Low-Level Input Voltage		V_{IL}		--	--	0.8	V
SDO	VOH: High-Level Output Voltage	V_{OH}		--	3.3	--	V
	VOL: Low-Level Output Voltage	V_{OL}		--	--	0.4	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
High-Level Input Voltage		V_{IH}	DVDD = 1.8V	1.4	--	--	V
Low-Level Input Voltage		V_{IL}	DVDD = 1.8V	--	--	0.5	V
SDO	VOH: High-Level Output Voltage	V_{OH}	DVDD = 1.8V	--	1.8	--	V
	VOL: Low-Level Output Voltage	V_{OL}	DVDD = 1.8V	--	--	0.2	
Frequency		f_{SCLKIN}		0.256	--	24.576	MHz
Setup Time, LRCK to SCLK Rising Edge		t_{su1}		10	--	--	ns
Hold Time, LRCK from SCLK Rising Edge		t_{h1}		10	--	--	ns
Setup Time, SDIN to SCLK Rising Edge		t_{su2}		10	--	--	ns
Hold Time, SDIN from SCLK Rising Edge		t_{h2}		10	--	--	ns
Rise/Fall Time for SCLK/LRCK		t_R/t_F		--	--	20	ns
I^2S Duty Cycle for Rising		%		40	--	60	%

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. The result is defined when the cross voltage between BST and VOUT is 5V.

Note 3. The switching terminal should be used within AC peak limits. Overshoot and undershoot must be less than 100ns.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four-layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is measured at the case top of the package. The result is including the bonding, GND, and real Die.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

Note 6. The device is not guaranteed to function outside its operating conditions.

Note 7. Measurements were made using the RT9120S_EVM board and Audio Precision System 2722 with AUX-0025 low-pass filter.

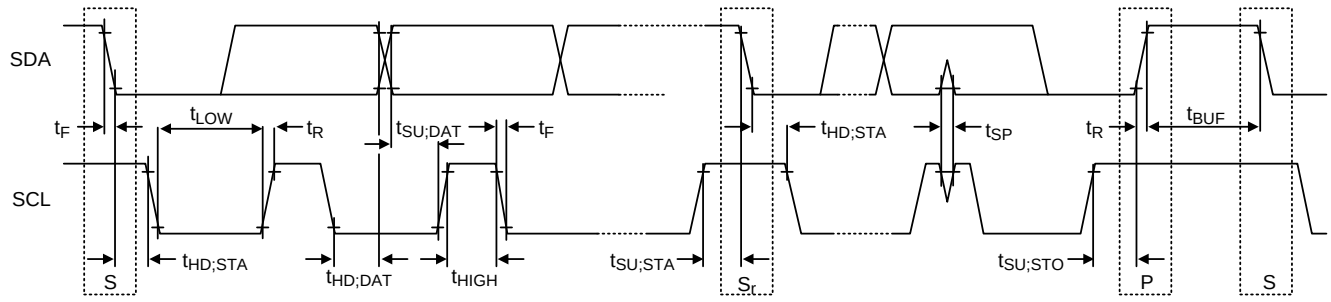


Figure 1. I^2C Interface Timing Diagram

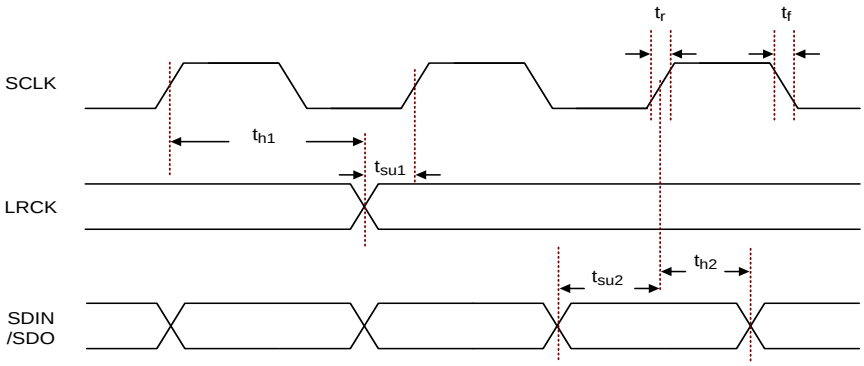
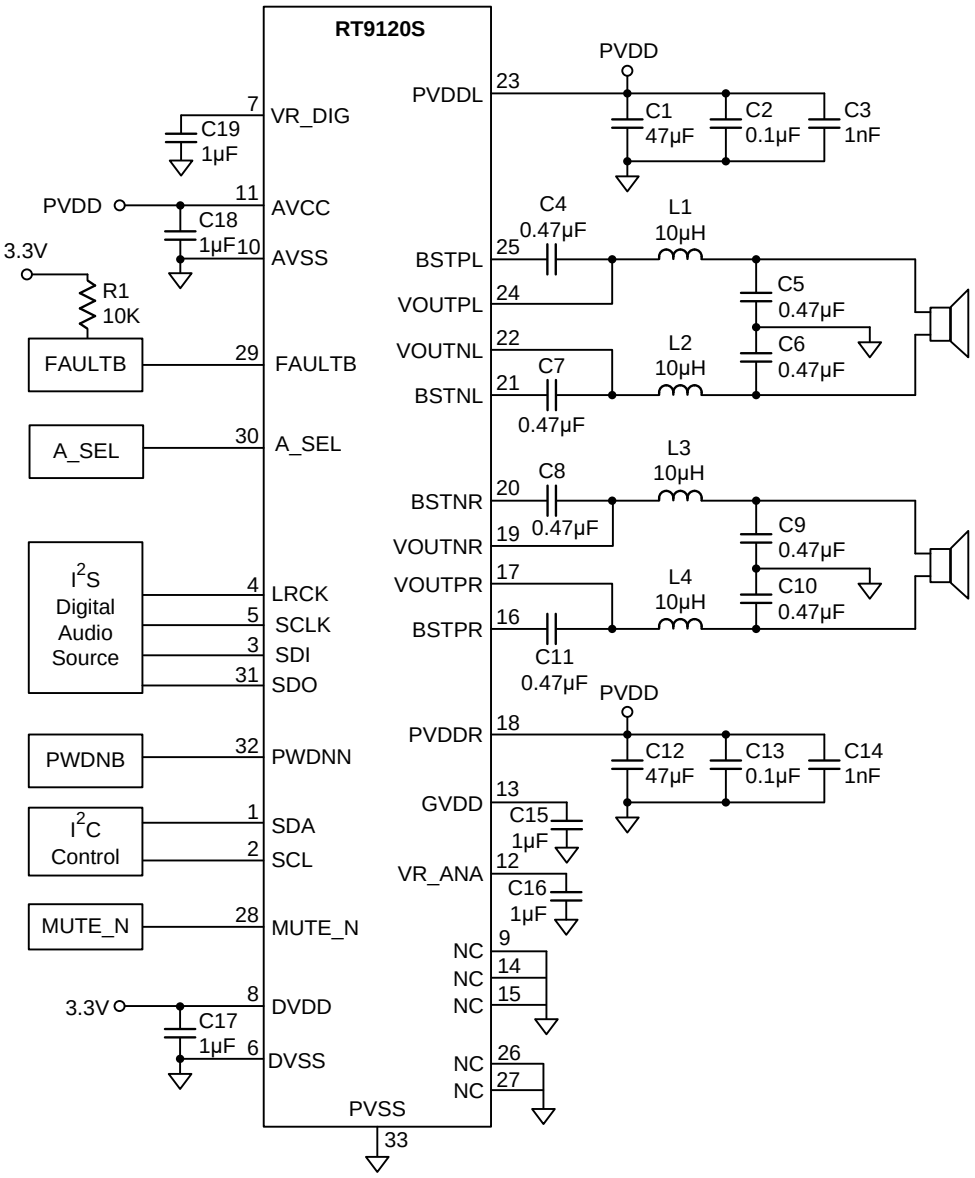


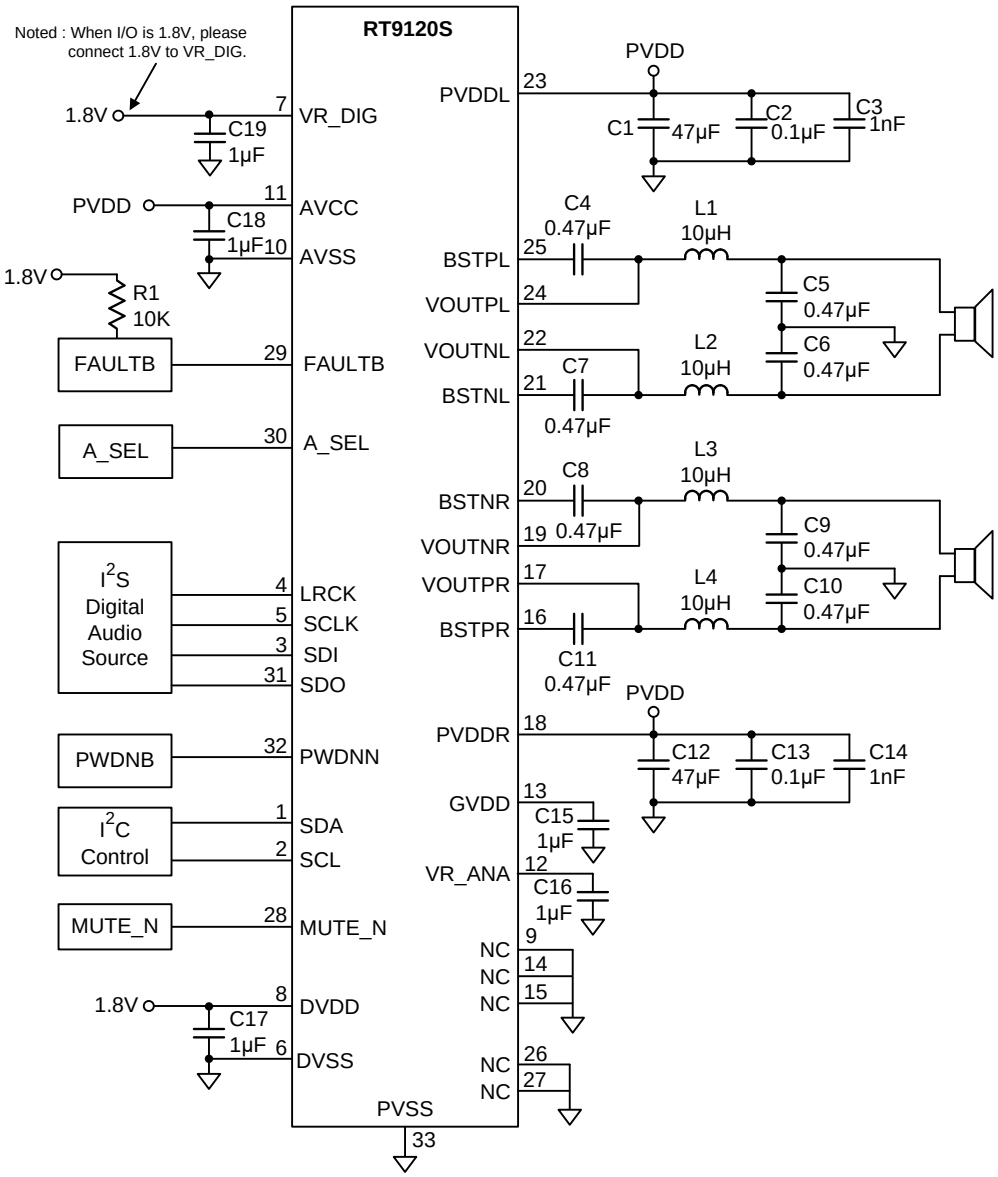
Figure 2. Timing Diagram of Slave Mode I^2S Interface

Typical Application Circuit

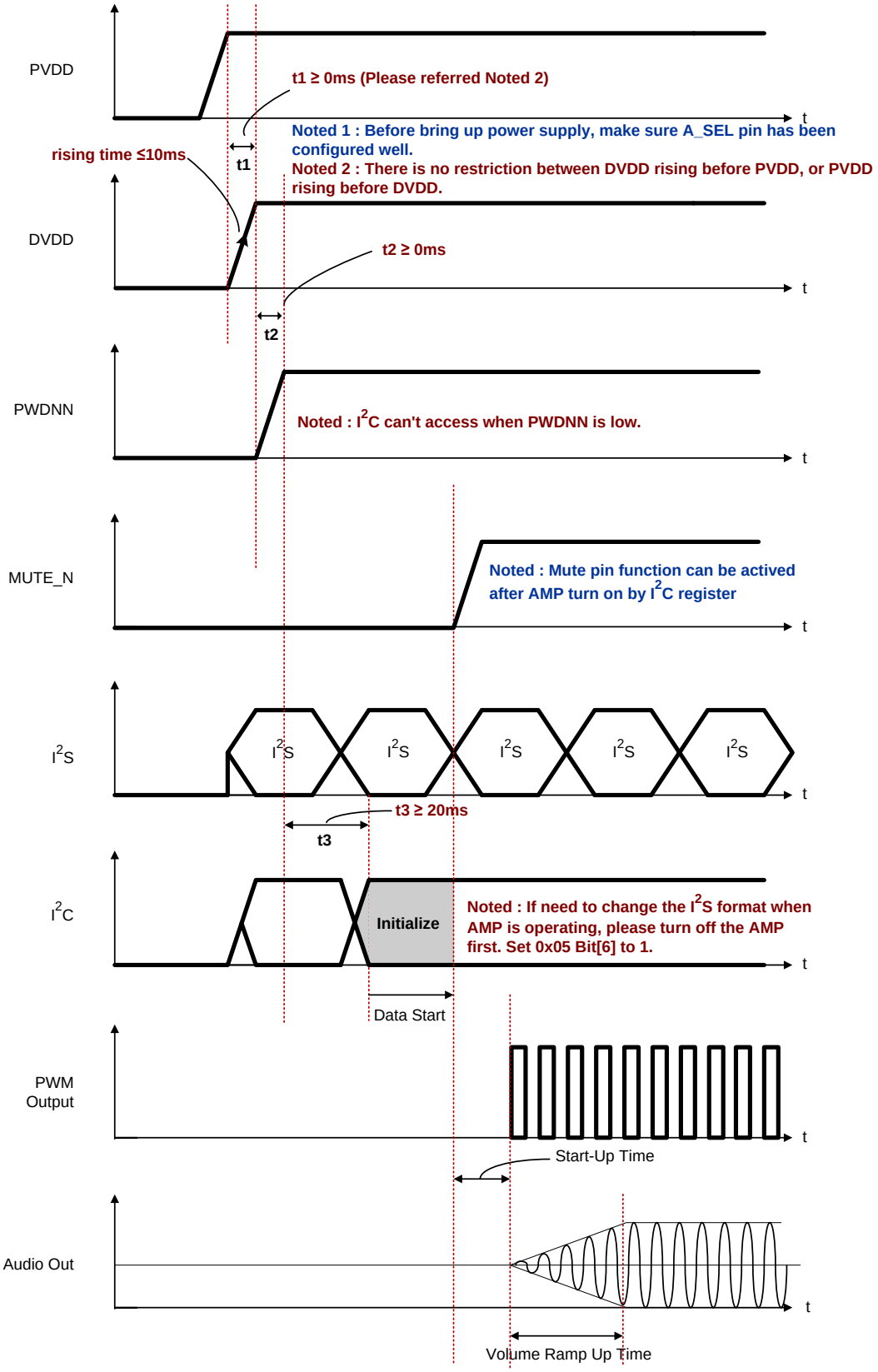
3.3V I/O Application



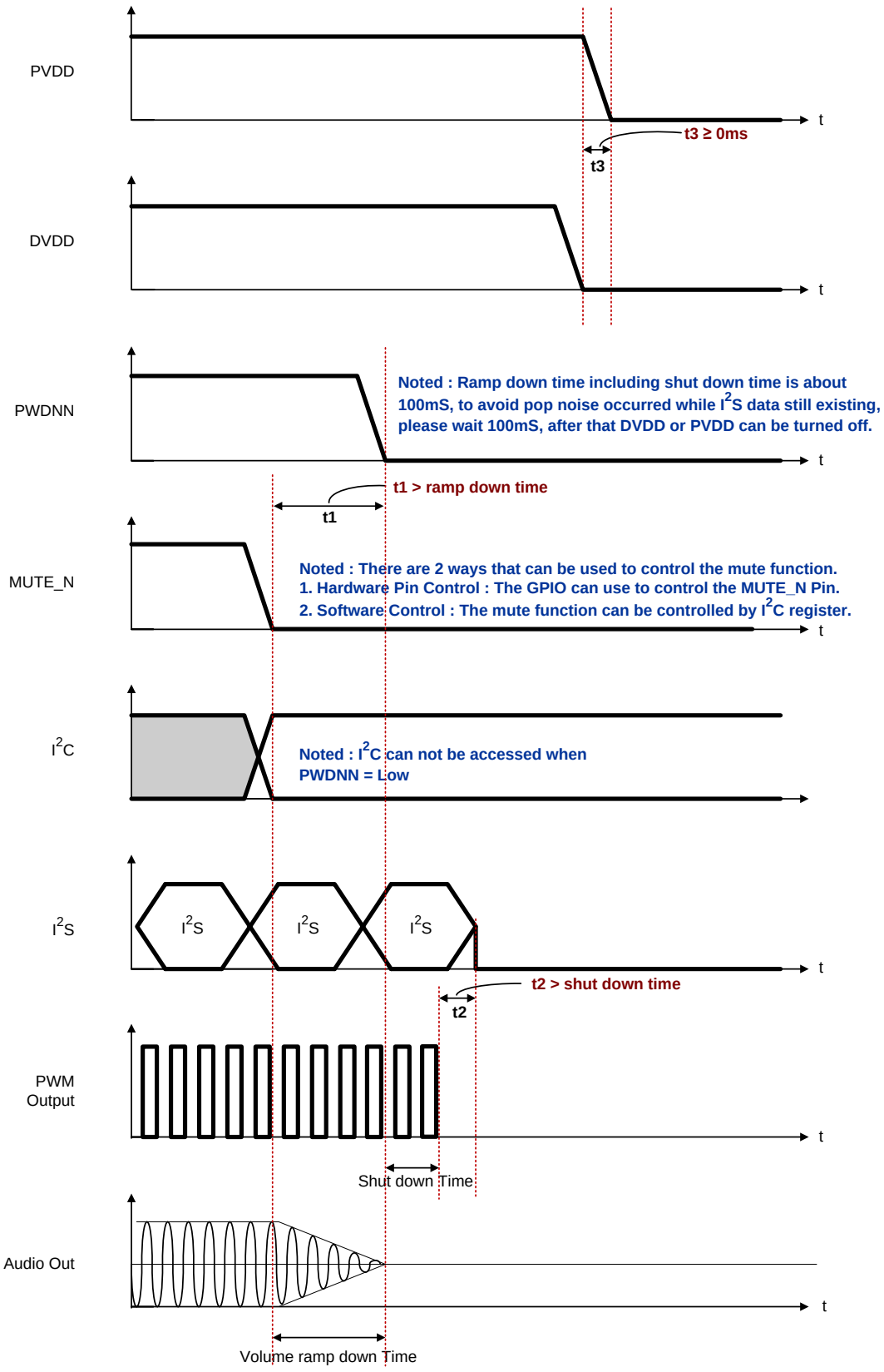
1.8V I/O Application



Power-On Sequence



Power-Off Sequence



Initial Sequence (BTL Mode, PWM = 384kHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x40	1	0x80	SW reset, if HW reset has been done (PWDNN set to low), there is no need to do the SW reset.	Initial setting
20ms delay					
2	0x63	1	0xDE	Internal setting	
3	0x07	1	0x37	Analog gain (Optional)	
4	0x65	1	0x66	Internal setting	
5	0x15	1	0x20	DC offset calibration enable. DC offset calibration disable. (There is no need to set 0x15 and 0x6E if DC offset calibration is disable)	
6	0x6E	1	0x19		
7	0x6C	1	0xC0	DVDD = 1.8V, set 0x6C to 0xC0. DVDD = 3.3V, no need to adjust.	
8	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
9	0x05	1	0x80	Amp turn on (PWM is 384kHz)	Amp turn on

Initial Sequence (BTL Mode, PWM = 768kHz, 1.5MHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x40	1	0x80	SW reset, if HW reset has been done (PWDNN set to low), there is no need to do the SW reset.	Initial setting
20ms delay					
2	0x63	1	0xDE	Internal setting	
3	0x07	1	0x37	Analog gain (Optional)	
4	0x65	1	0x11	Internal setting	
5	0x15	1	0x20	DC offset calibration DC offset calibration disable. (There is no need to set 0x15 and 0x6E if DC offset calibration is disable)	
6	0x6E	1	0x19		
7	0x6C	1	0xC0	DVDD = 1.8V, set 0x6C to 0xC0. DVDD = 3.3V, no need to adjust.	
8	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
9	0x05	1	0x88	Amp turn on (PWM is 768kHz)	Amp turn on
		1	0x8C	Amp turn on (PWM is 1.5MHz)	

Initial Sequence (PBTL Mode, PWM = 384kHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x40	1	0x80	SW reset, if HW reset has been done (PWDNN set to low), there is no need to do the SW reset.	Initial setting
20ms delay					
2	0x15	1	0x40	Internal setting	
3	0x64	1	0x39	Internal setting	
4	0x63	1	0xDE	Internal setting	
5	0x07	1	0x37	Analog gain (Optional)	
6	0x65	1	0x77	Internal setting	
7	0x15	1	0x60	DC offset calibration DC offset calibration disable. (Please set 0x15 to 0x40, and no need to set 0x6E)	
8	0x6E	1	0x19		
9	0x6C	1	0xC0	DVDD = 1.8V, set 0x6C to 0xC0. DVDD = 3.3V, no need to adjust.	
10	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
11	0x30	3	0x01, 0xC0, 0x07	Set input mixing = L/2+R/2 for mono mode	
12	0x31	3	0x01, 0xC0, 0x07		
13	0x05	1	0x90	Set to PBTL and Amp turn on (PWM is 384kHz)	Amp turn on

Initial Sequence (PBTL Mode, PWM = 768kHz, 1.5MHz)

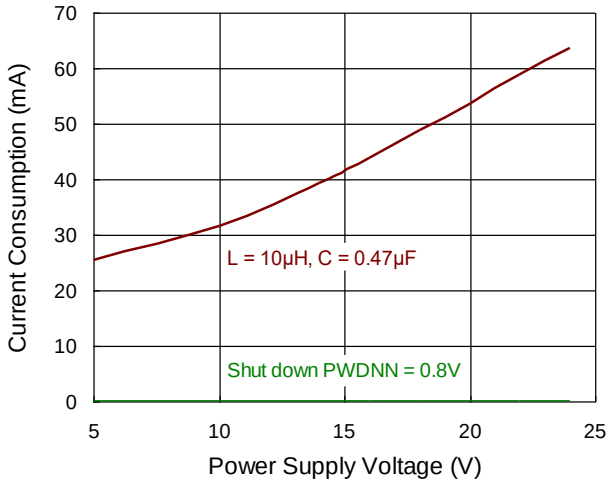
Sequence	reg_addr	reg_size	reg_value	Description	
1	0x40	1	0x80	SW reset, if HW reset has been done (PWDNN set to low), there is no need to do the SW reset.	Initial setting
20ms delay					
2	0x15	1	0x40	Internal setting	
3	0x64	1	0x39	Internal setting	
4	0x63	1	0xDE	Internal setting	
5	0x07	1	0x37	Analog gain (Optional)	
6	0x65	1	0x11	Internal setting	
7	0x15	1	0x60	DC offset calibration DC offset calibration disable. (Please set 0x15 to 0x40, and no need to set 0x6E)	
8	0x6E	1	0x19		
9	0x6C	1	0xC0	DVDD = 1.8V, set 0x6C to 0xC0. DVDD = 3.3V, no need to adjust.	
10	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
11	0x30	3	0x01, 0xC0, 0x07	Set input mixing = L/2+R/2 for mono mode	
12	0x31	3	0x01, 0xC0, 0x07		

Sequence	reg_addr	reg_size	reg_value	Description	
13	0x05	1	0x98	Set to PBTL and Amp turn on (PWM is 768kHz)	Amp turn on
		1	0x9C	Set to PBTL and Amp turn on (PWM is 1.5MHz)	

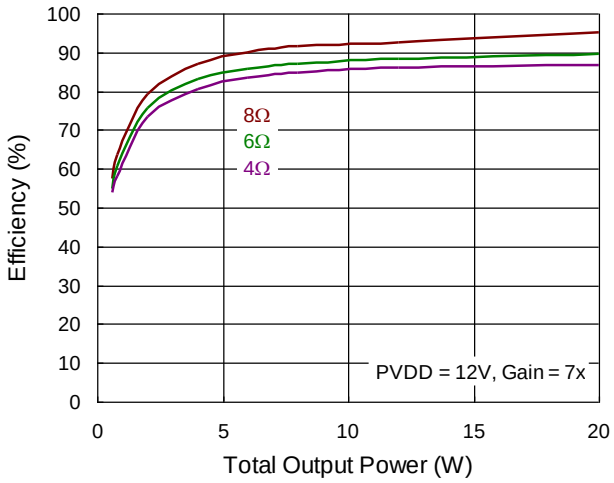
Typical Operating Characteristics

PWM = 384kHz

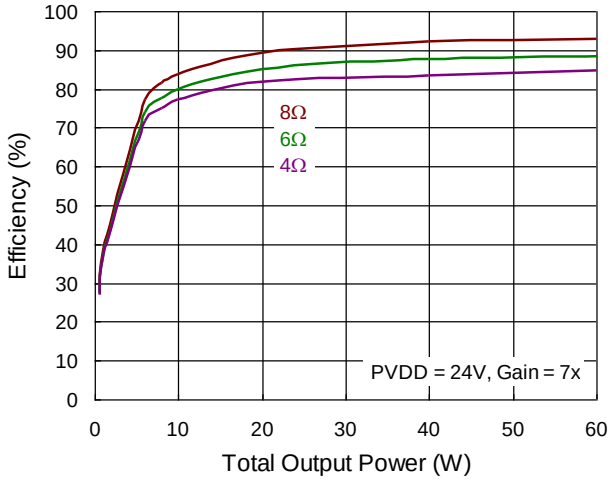
Current Consumption vs. Power Supply Voltage



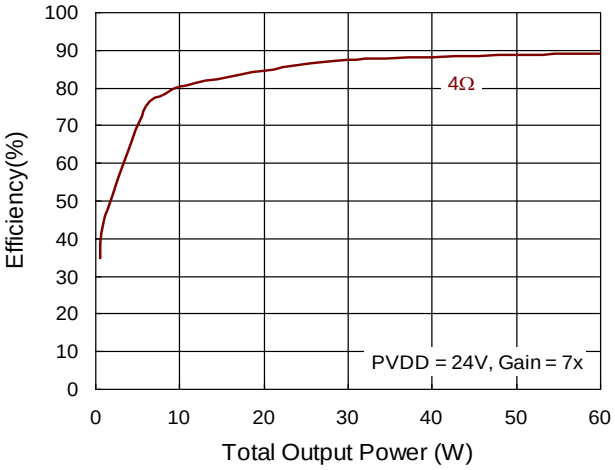
Efficiency vs. Total Output Power (BTL)



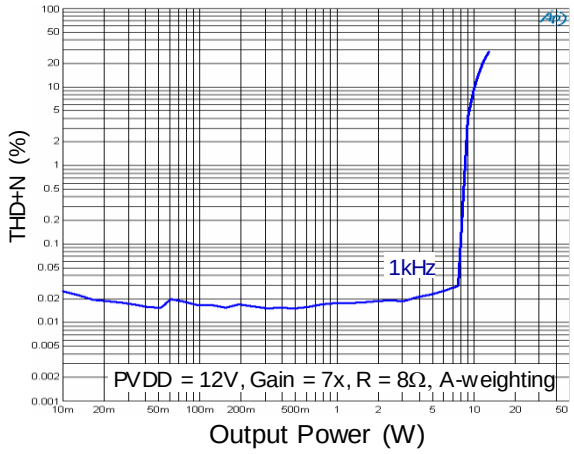
Efficiency vs. Total Output Power (BTL)



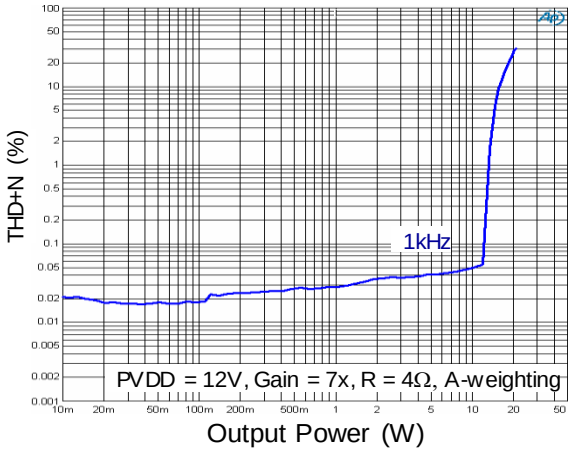
Efficiency vs. Total Output Power (PBTL)



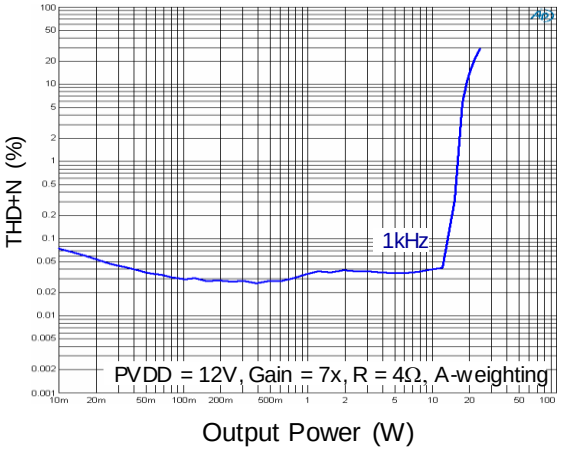
THD + N vs. Output Power (BTL)



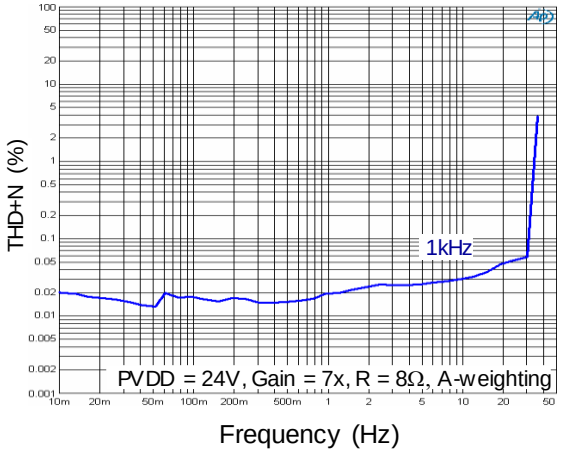
THD + N vs. Output Power (BTL)



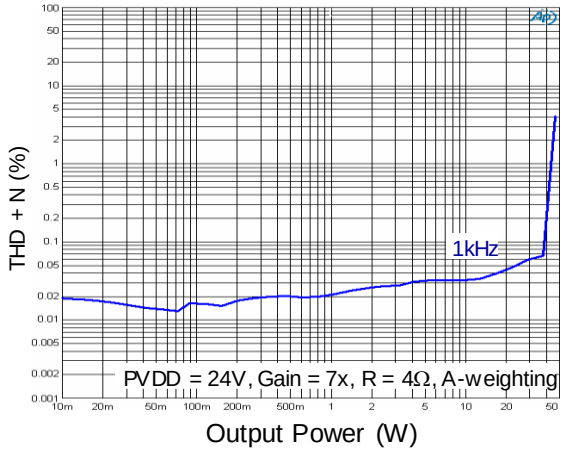
THD + N vs. Output Power (PBTL)



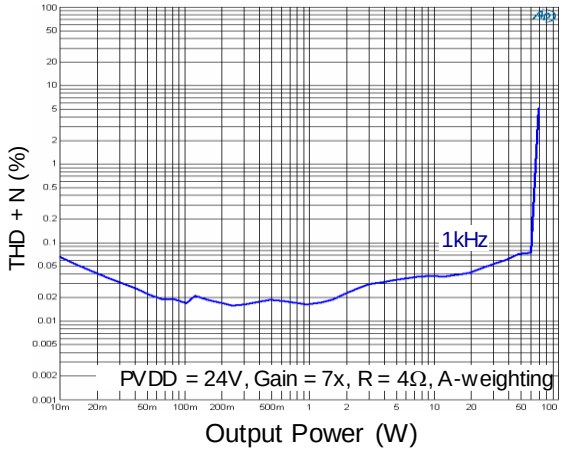
THD + N vs. Output Power (BTL)



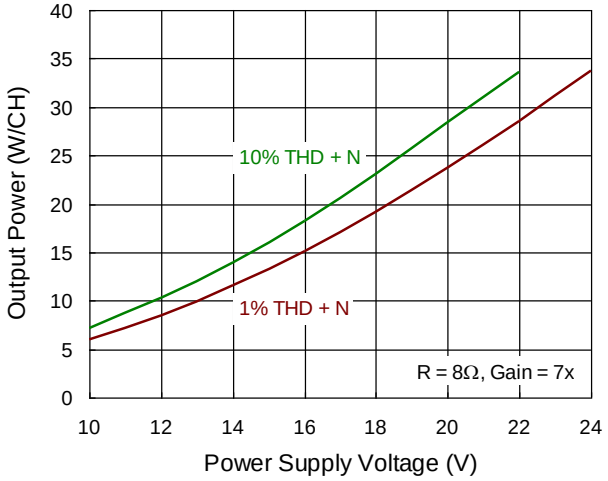
THD + N vs. Output Power (BTL)



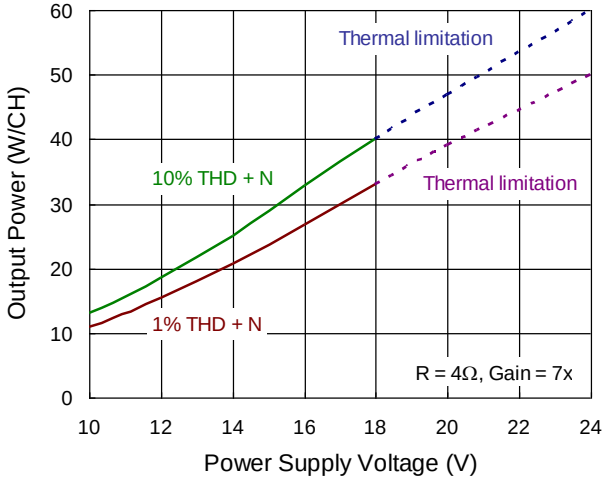
THD + N vs. Output Power (PBTL)



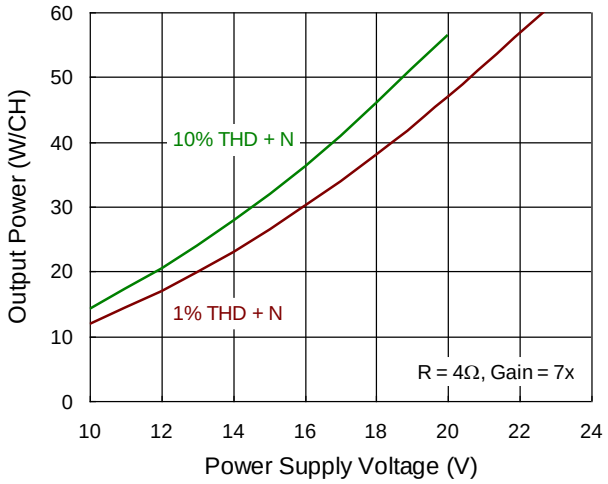
Output Power vs. Power Supply Voltage (BTL)



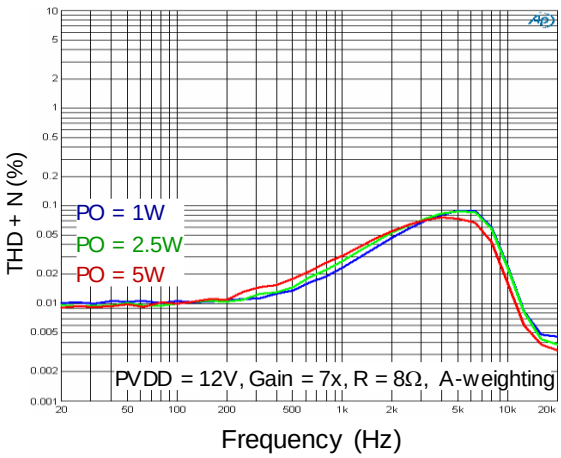
Output Power vs. Power Supply Voltage (BTL)



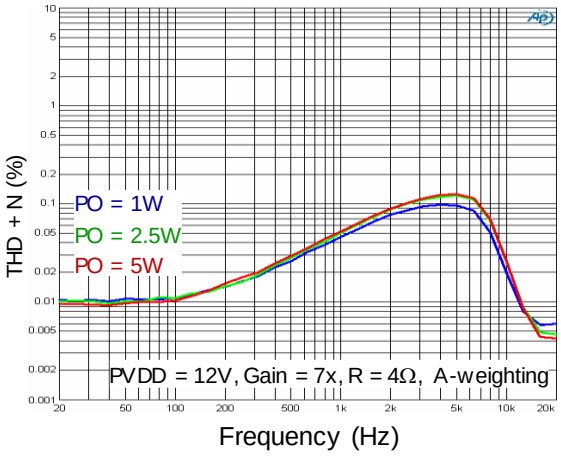
Output Power vs. Power Supply Voltage (PBTL)



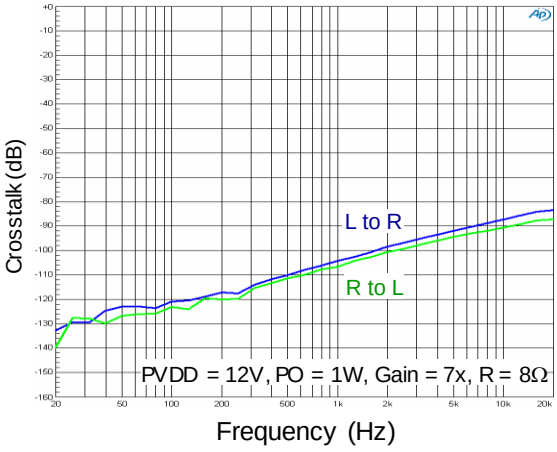
THD + N vs. Frequency (BTL)



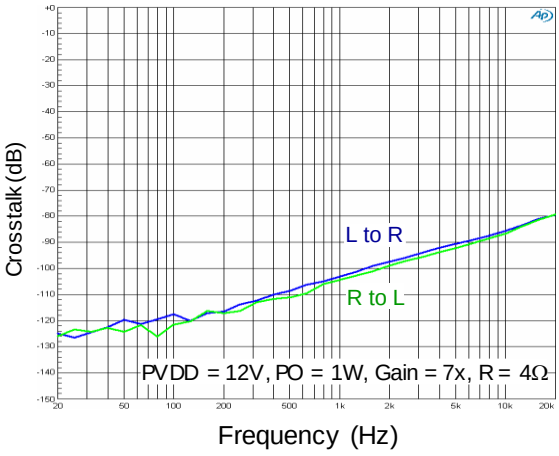
THD + N vs. Frequency (BTL)



Crosstalk vs. Frequency

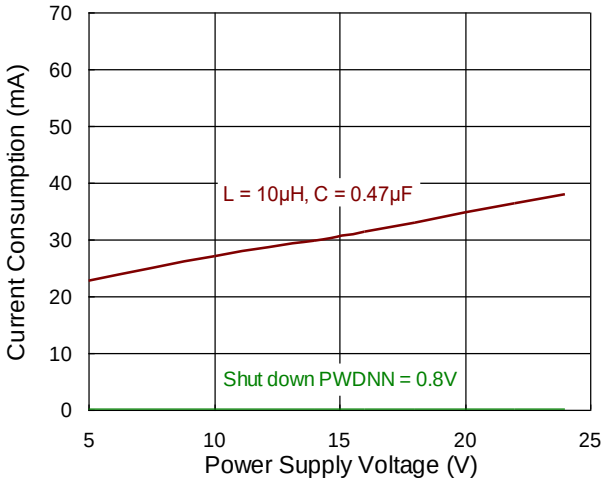


Crosstalk vs. Frequency

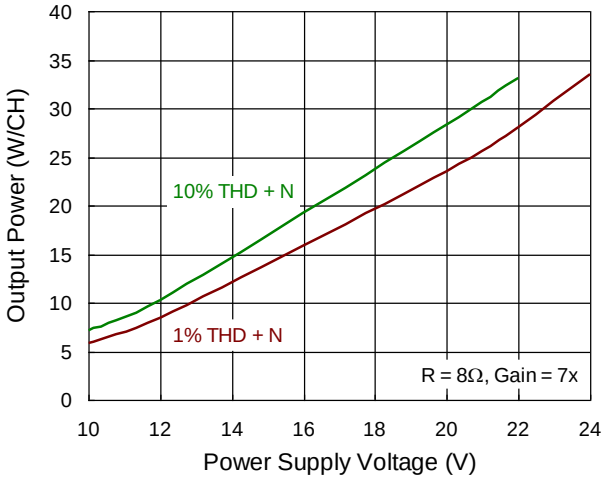


PWM = 768kHz

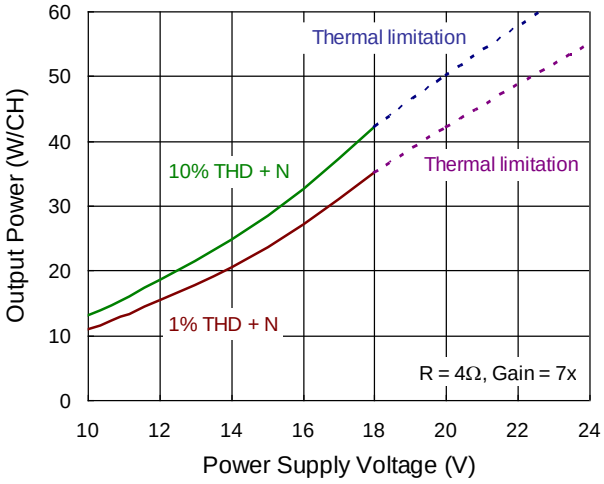
Current Consumption vs. Power Supply Voltage



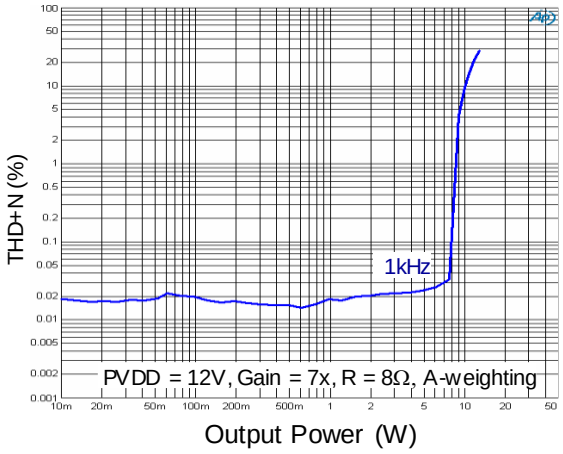
Output Power vs. Power Supply Voltage (BTL)



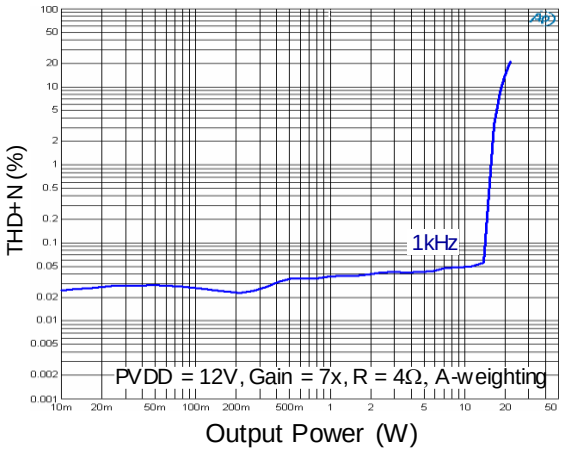
Output Power vs. Power Supply Voltage (BTL)



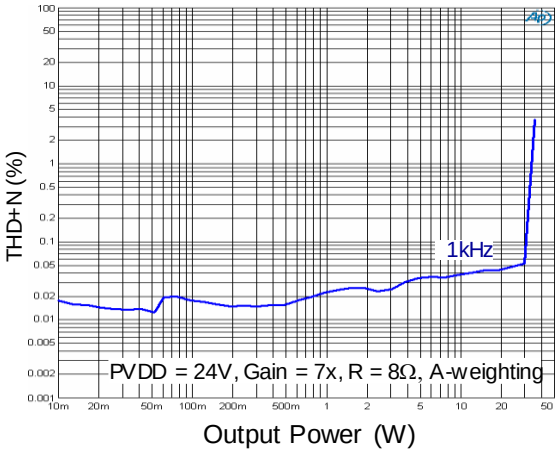
THD + N vs. Output Power (BTL)



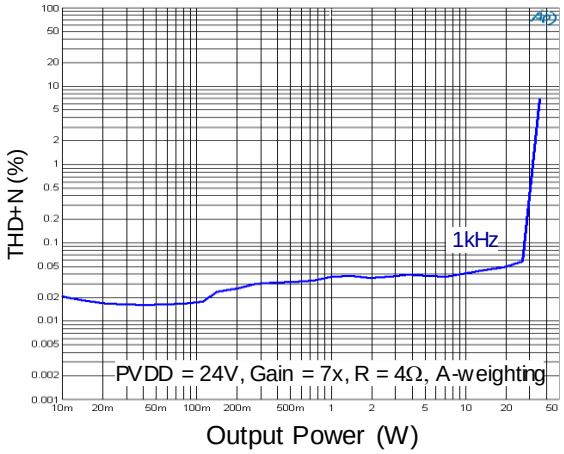
THD + N vs. Output Power (BTL)



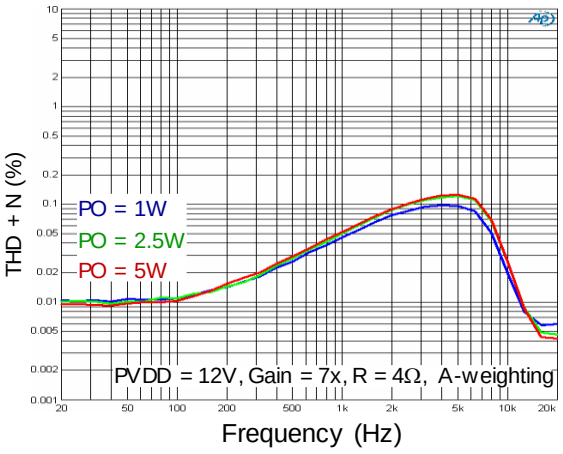
THD + N vs. Output Power (BTL)



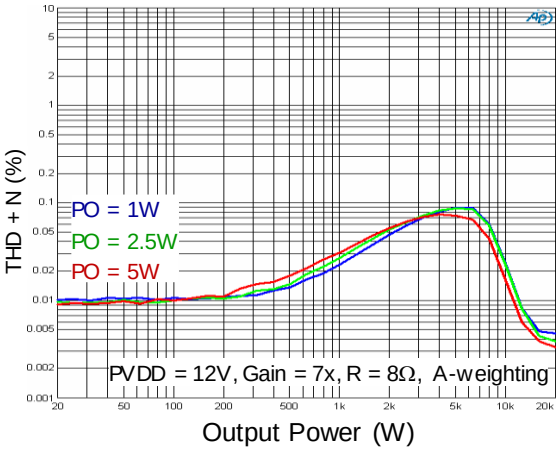
THD + N vs. Output Power (BTL)



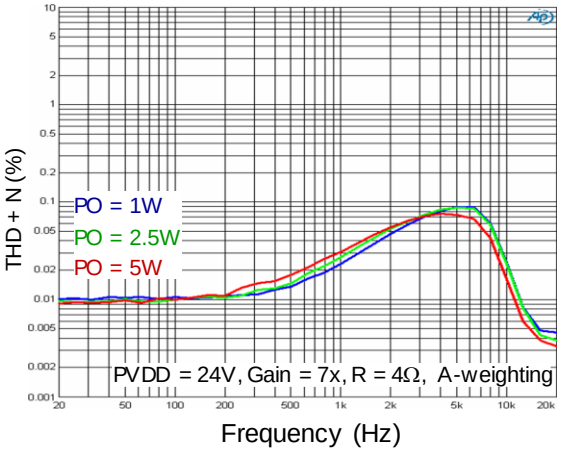
THD + N vs. Frequency (BTL)



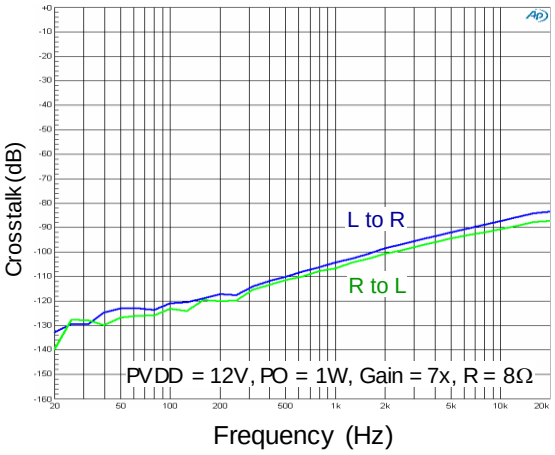
THD + N vs. Frequency (BTL)



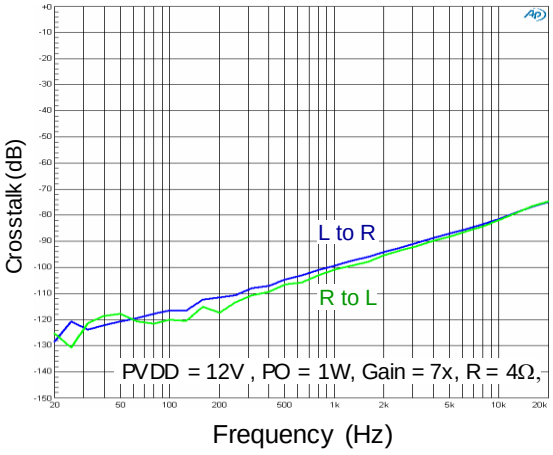
THD + N vs. Frequency (BTL)

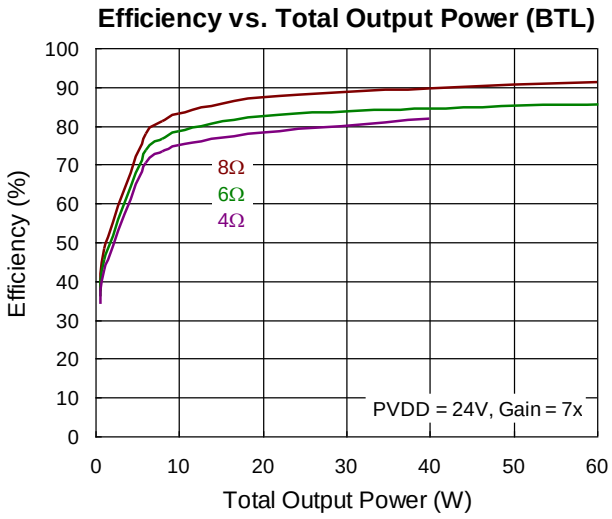


Crosstalk vs. Frequency



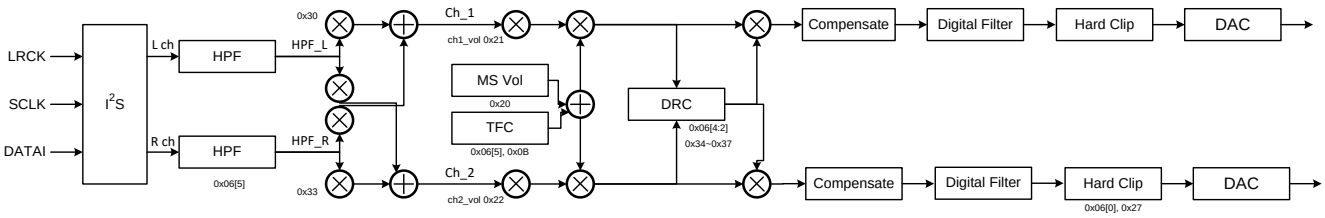
Crosstalk vs. Frequency





Noted: Measurements were made using the RT9120S_EVM board and Audio Precision System 2722 with AUX0025 low-pass filter. All measurements taken with 1kHz.

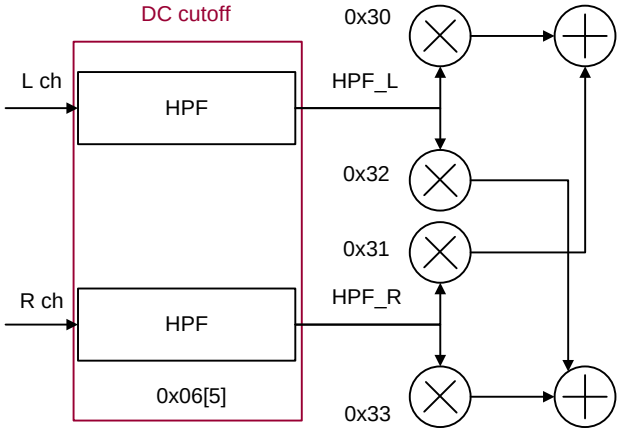
Signal Path



Input High Pass Filter

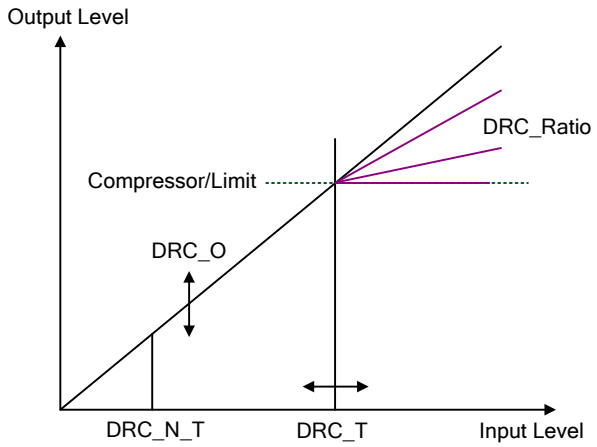
Block Diagram & Description

→There are DC-Cut filter for each output filter. The cut off frequency is 1.5Hz



Address	BITS	Name	Description
0x06	5	HPF_EN	0: Input high pass filter disable 1: Input high pass filter enable

DRC

DRC Description	Address	Description
DRC_T: Threshold	0x23	
DRC_RATIO: Compress ratio	0x24	
DRC_O: Make up gain	0x25	
DRC_N_T: Noise gate threshold	0x26	
Noise gate enable	0x06	

DRC Enable

Address	BITS	Name	Description
0x06	2	DRC_EN	0: DRC disable 1: DRC enable

DRC Noise Gate Enable

Address	BITS	Name	Description
0x06	1	DRC_N_EN	0: DRC Noise gate disable 1: DRC Noise gate enable

DRC Control

Address	BITS	Name	Description
0x23	10:0	DRC_TH[10:0]	TH[10:0], DRC Threshold
0x24	7:0	DRC_RATIO[7:0]	RATIO[7:0] DRC compression ratio
0x25	10:0	DRC_O[10:0]	O[10:0] DRC make up gain
0x26	10:0	DRC_N_T[10:0]	N_T[10:0] DRC Noise gate of the DRC

DRC Timing

Address	BITS	Name	Description
0x34	16:0	DRC_AE[16:0]	DRC_AE[16:0], DRC Energy estimator
0x35	16:0	DRC_1_AE[16:0]	DRC_1_AE[16:0], DRC Energy estimator (release) (Noted: When set to peak mode, this value need to adjust)
0x36	16:0	DRC_AD[16:0]	DRC_AD[16:0] DRC release time
0x37	16:0	DRC_AA[16:0]	DRC_AA[16:0] DRC attack time

DRC Timing Equation

<table>
<tr><th>DRC Description</th><th>Equation</th></tr>
<tr><td>AA/AE/AD/1-AE Timing Equation</td><td>
Equation: AA = $(1-e^{-2.2/(ta*fs)}) \times 2^{15}$
ta = AA/AD/AE timing,
f_S = sampling rate
Ex: ta = 0.15ms, f_S = 48k
AA = $(1-e^{-2.2/(0.00015*48000)}) \times 2^{15} = 8627.352$
DEC = 8627
HEX = 0x21B3

<table>
<tr><td>Threshold</td><td>T_Dec</td><td>T_Hex</td></tr>
<tr><td>0.15ms</td><td>8627</td><td>0x21B3</td></tr>
<tr><td>.
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<tr><td>400ms</td><td>3.75</td><td>0x3</td></tr>
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Noted: For the different Sampling Rate, the maximum timing will be

<table>
<tr><td>f_S (Sampling Rate)</td><td>Max Time (Unit: S)</td></tr>
<tr><td>192kHz</td><td>0.375</td></tr>
<tr><td>96kHz</td><td>0.750</td></tr>
<tr><td>48khz</td><td>1.500</td></tr>
<tr><td>32kHz</td><td>2.250</td></tr>
<tr><td>24kHz</td><td>3.000</td></tr>
<tr><td>16kHz</td><td>4.500</td></tr>
<tr><td>12kHz</td><td>6.000</td></tr>
<tr><td>8kHz</td><td>9.000</td></tr>
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<table>
<tr><th>DRC Description</th><th>Equation</th></tr>
<tr><td>DRC_T: Threshold</td><td>T is the threshold of the DRC
Equation: T = -(Threshold)/0.0625 (dB)
Ex: T = -10dB,
-(-10)/0.0625 = 160
T_Dec = 160
T_Hex = DEC2HEX (160) = 0xA0
<table><tr><th>Threshold</th><th>T_Dec</th><th>T_Hex</th></tr><tr><td>−10dB</td><td>160</td><td>0xA0</td></tr><tr><td>.
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<tr><td>DRC_Ratio: Compression Ratio</td><td>K is the compression ratio of the DRC
Equation: K_Hex = DEC2HEX (Ratio_Value)
EX: If compression Ratio is 50%
• The Ratio_Value is 128^0.5 = 64
• K_Dec = 64
• K_Hex = DEC2HEX (64) = 0x0040
• Noted: the maximum value for the full compression is 128
<table><tr><th>Ratio</th><th>K_Dec</th><th>K_Hex</th></tr><tr><td>Full Comp (100%)</td><td>128</td><td>0x0080</td></tr><tr><td>.
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.</td></tr><tr><td>50%</td><td>64</td><td>0x0040</td></tr><tr><td>.
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<tr><td>DRC_O: Make Up Gain</td><td>DRC_O is the offset of the DRC
Equation: DRC_O = (Offset-24)/0.0625
EX: Offset = 0dB
• Abs[(0-24/0.0625)] = 384
• DRC_O_Dec = 384
• DRC_O_Hex = DEC2HEX (384) = 0x0180
<table><tr><th>Offset</th><th>O_Dec</th><th>O_Hex</th></tr><tr><td>0dB</td><td>384</td><td>0x0180</td></tr><tr><td>.
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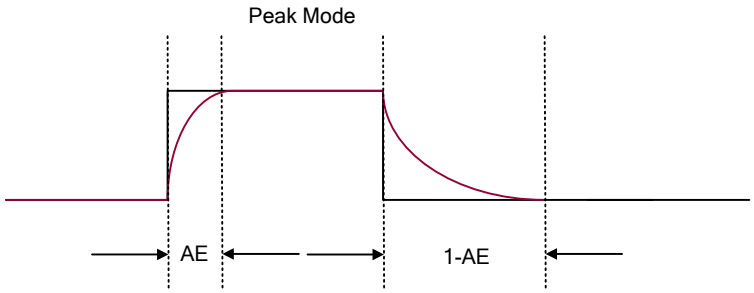
Peak Mode

Block Diagram & Description

→The detecting threshold using different calculated methods.

Peak mode: AE and 1-AE is independent

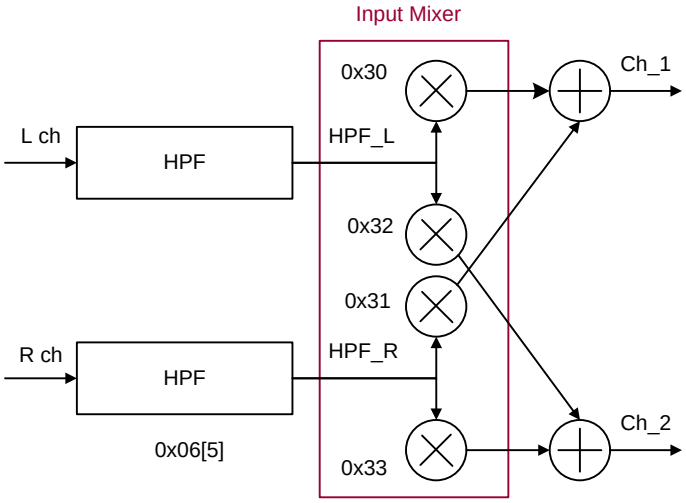


Address	BITS	Name	Description
0x06	3	DRC_PEAK	0: RMS mode 1: Peak mode Noted: the peak mode is recommended to use.

Input Mixer

Block Diagram & Description

→ Input mixer range is from mute to 6dB.



→Default setting is CH2_IN_MIX_1 is from HPF_R

→Default setting is CH1_IN_MIX_0 is from HPF_L

Address	BITS	Name	Description
0x30	23:0	CH1_IN_MIX_0	u[23:17], mix_0[16:0] u: Unused
0x31	23:0	CH1_IN_MIX_1	u[23:17], mix_1[16:0] u: Unused
0x32	23:0	CH2_IN_MIX_0	u[23:17], mix_0[16:0] u: Unused
0x33	23:0	CH2_IN_MIX_1	u[23:17], mix_1[16:0] u: Unused

Input Mixer Gain Setting

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0x30, 0x31,
0x32, 0x33,</td><td>16:0</td><td>mix_1[16:0], mix_0[16:0]</td><td>Equation: 20Log (Dec/32768)
Range: 6dB (0XFFFF) to Mute (0x00000000)
Ex: 6dB, Gain = 20Log (65535/32768) = 6dB
Hex = 0xFFFF
Dec = 65535
<table>
<tr><th>Gain</th><th>Dec</th><th>Hex</th></tr>
<tr><td>6dB</td><td>65535</td><td>0XFFFF</td></tr>
<tr><td>2dB</td><td>41252</td><td>0XA124</td></tr>
<tr><td>.
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<tr><td>0</td><td>32768</td><td>0X8000</td></tr>
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Mixer Inverse Phase Setting

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0x30, 0x31,
0x32, 0x33,</td><td>16:0</td><td>mix_1[16:0], mix_0[16:0]</td><td>Equation: Hex = DEC2HEX
Ex: Gain = 6dB,
Hex = 0x010000
Phase Inverse: Hex = DEC2HEX (–65535) = 0x010000
<table>
<tr><th>Gain</th><th>Dec</th><th>Hex</th></tr>
<tr><td>6dB</td><td>–65535</td><td>0X010000</td></tr>
<tr><td>4dB</td><td>–51791</td><td>0x013523</td></tr>
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<tr><td>0</td><td>–32768</td><td>0X018000</td></tr>
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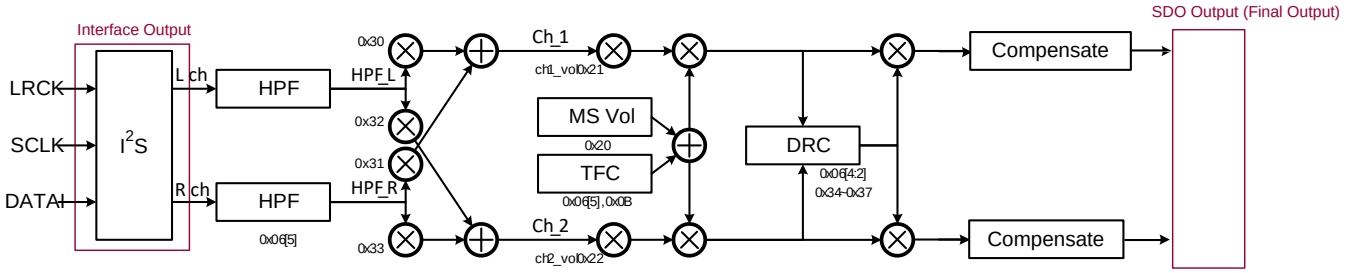
SDO Output Configure

Block Diagram & Description

→ The final stage of whole signal path is SDO output configure. It output the final level of each channel before digital filter. And output the I^2S data before the HPF.



Address	BITS	Name	Description
0x04	5:4	SDO_SEL[1:0]	00: Reserved 01: Interface output 10: Final output 11: Reserved

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

I²C Bus Specification

The RT9120S supports the I²C protocol via the input ports SCL and SDA. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The RT9120S is always a slave device in all of its communications. It can operate at up to 400kb/s. The RT9120S I²C interface is a slave only interface.

Communication Protocol

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition. START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer. STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the RT9120S and the bus master. During the data input, the RT9120S samples the SDA signal on the rising edge of clock SCL. For correct device operation, the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

Boost Capacitor Selection

For the large power output, and low frequency, the boost capacitor can be choose from 0.47μF to 1μF. Reference value can referred the below table:

Test Condition	Capacitor Value
PVDD = 24V, R = 8Ω, Output Power > 2x25W, 20Hz, BTL Mode.	1μF
PVDD = 24V, R = 4Ω, Output Power > 2x20W, 20Hz, BTL Mode.	0.47μF
PVDD = 24V, R = 4Ω, Output Power > 60W, 20Hz, PBTL Mode	1μF
PVDD = 24V, R = 8Ω, Output Power > 35W, 20Hz, PBTL Mode	1μF

Device Addressing

The RT9120S supports 4 different address setting. The default device address is 0011001 when A_SEL = DVDD, 0011000 when A_SEL = GND, 0011011 when A_SEL with 600kΩ resistor to DVDD and 0011010 when A_SEL with 600kΩ resistor to GND.

A_SEL	Device Address
DVDD	0011001
GND	0011000
With 600kΩ to DVDD	0011011
With 600kΩ to GND	0011010

I²C Write Control

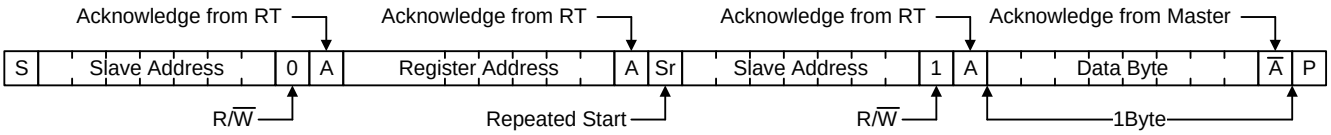
Following the START condition, the master sends a device select code with the RW bit set to 0. The RT9120S acknowledges this and the writes for the byte of internal address. After receiving the internal byte address, the RT9120S again responds with an acknowledgement.

I²C Read Control

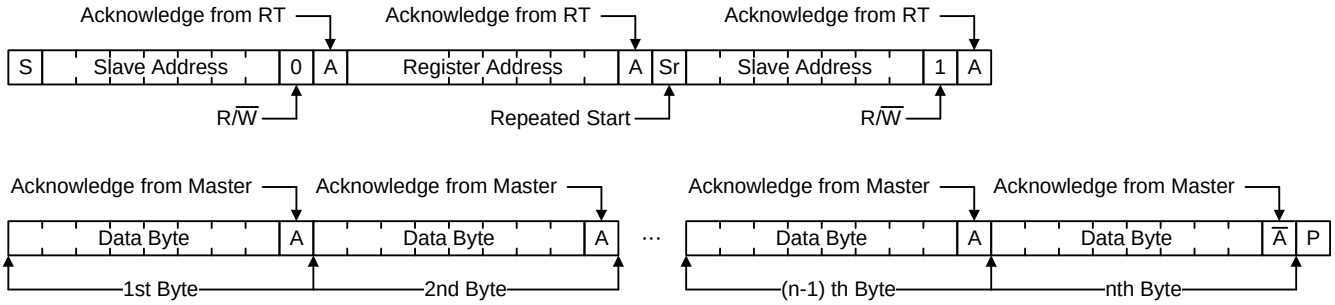
Following the START condition the master sends a device select code with the RW bit set to 1. The RT9120S acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

Read Function

■ Reading One Indexed Byte of Data from RT (With 1-Byte)

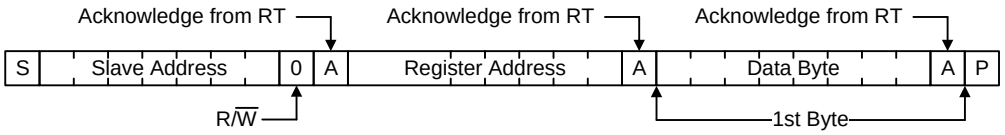


■ Reading n Indexed Words of Data from RT (With N-Byte)

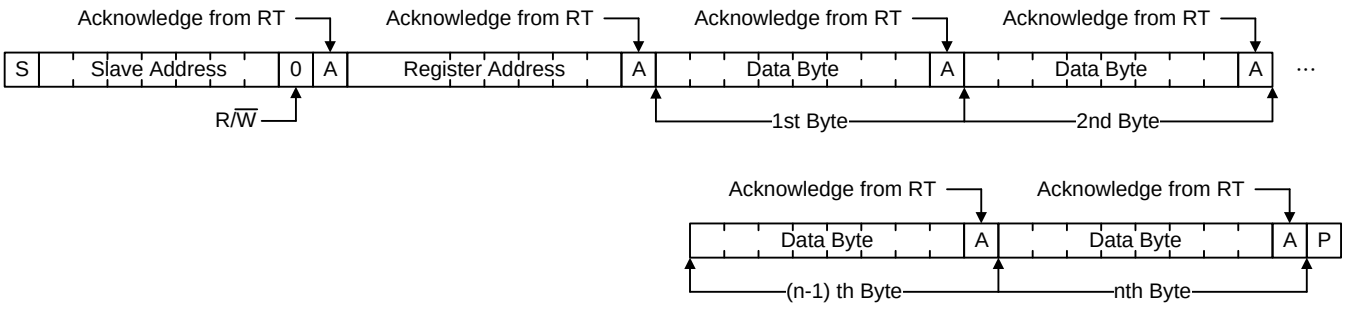


Write Function

■ Writing One Byte of Data to RT (With 1-Byte)

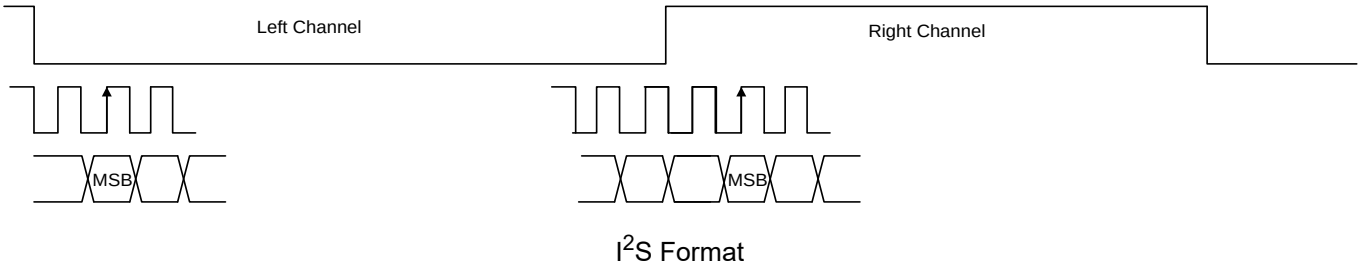


■ Writing n Bytes of Data to RT (With N-Byte)

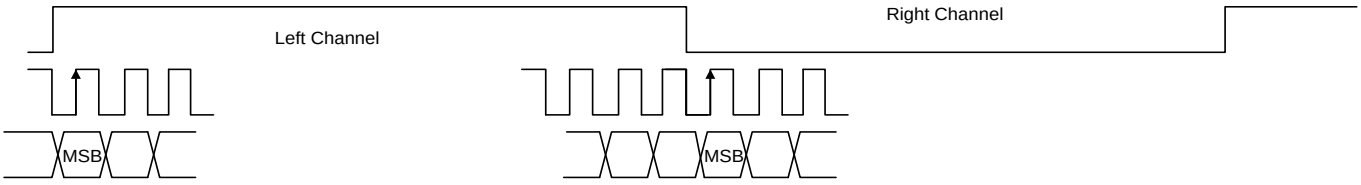


Audio Interface

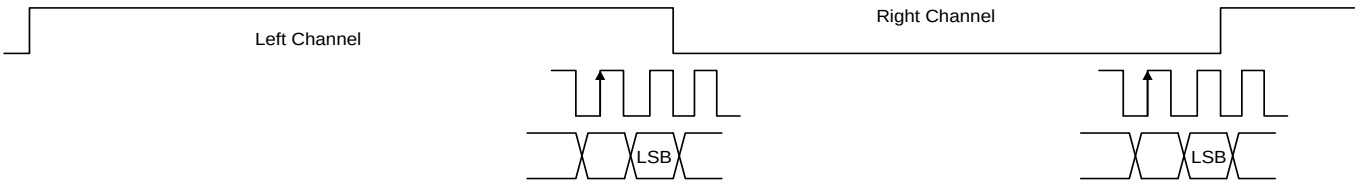
The RT9120S supports four kinds of audio interface, I^{2}S, Left justify, Right justify and TDM. Each kind of interface support 32bits, 24bits, 20bits, and 16 bits format. The timing diagram is shown below.



I^{2}S Format



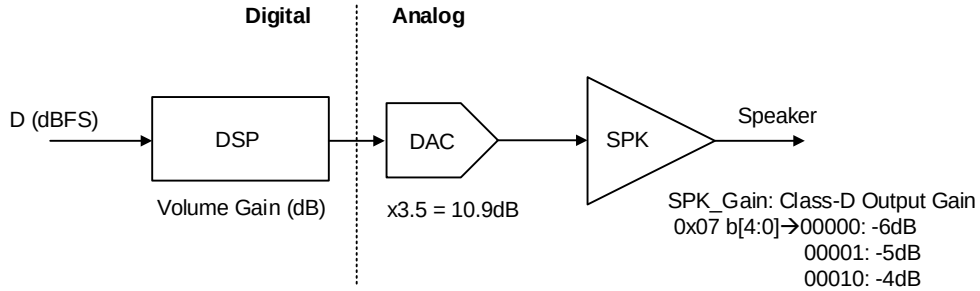
Left Justify



Right Justify

Address	BITS	Name	Description
0x02	3:2	AUD_FMT	00: I^{2}S (default) 01: Left Justify 10: Right Justify 11: DSP
	1:0	AUD_BITS	00: 16bits I^{2}S 01: 20bits I^{2}S 10: 24bits I^{2}S 11: 32bits I^{2}S (default)

Amplification Gain



SPK_Gain: Class-D Output Gain
0x07 b[4:0]→00000: -6dB
00001: -5dB
00010: -4dB
00011: -3dB
00100: -2dB
00101: -1dB
00110: 0dB
00111: 1dB
01000: 2dB
01001: 3dB
01010: 4dB
01011: 5dB
01100: 6dB
01101: 7dB
01110: 8dB
01111: 9dB
10000: 10dB
10001: 11dB
10010: 12dB
10011: 13dB
10100: 14dB
10101: 15dB
10110: 16dB
10111: 17dB

Output voltage calculation formula = $10^{(D+Vol\_Gain)/20}$ x 3.5 X Output_Gain (Vp)

Address	BITS	Name	Description
0x07	4:0	D_SPK_GAIN[4:0]	Class-D output gain 00000: −6dB 00001: −5dB 00010: −4dB 00011: −3dB 00100: −2dB 00101: −1dB 00110: 0dB 00111: 1dB 01000: 2dB 01001: 3dB 01010: 4dB 01011: 5dB 01100: 6dB 01101: 7dB 01110: 8dB 01111: 9dB 10000: 10dB 10001: 11dB 10010: 12dB 10011: 13dB (default) 10100: 14dB 10101: 15dB 10110: 16dB 10111: 17dB

Master Volume Gain

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0x20</td><td>10:0</td><td>MS_VOL[10:0]</td><td>Equation: 24dB - (Dec x 0.0625)
Range: 24dB (0X000) to mute (0x7ff)
Ex: 10dB, Hex = 0xE0
Dec = 224
Gain = 24dB - (224 x 0.0625) = 10dB
<table>
<tr><th>Gain</th><th>Dec</th><th>Hex</th></tr>
<tr><td>24dB</td><td>0</td><td>0x00</td></tr>
<tr><td>10dB</td><td>224</td><td>0XE0</td></tr>
<tr><td>.
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<tr><td>0dB</td><td>384</td><td>0x180</td></tr>
<tr><td>.
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</table>
</td></tr>
</table>

Volume Ramp

00: 1 step in every sample

01: mute → –40dB, every sample with 1 step. –40dB → 24dB, 2 sample with 1 step.

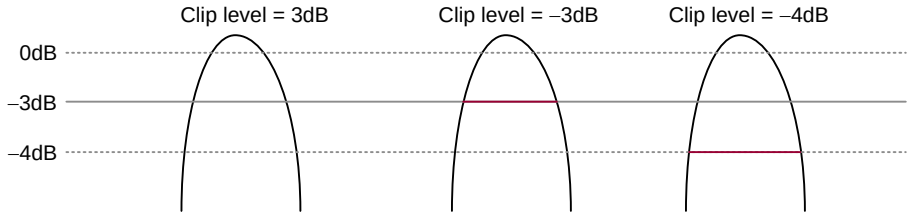
10: mute → –40dB, 2 sample with 1 step. –40dB → 24dB, 4 sample with 1 step.

Others: mute → –40dB, 4 sample with 1 step. –40dB → 24dB, 8 sample with 1 step.

Address	BITS	Name	Description
0x0A	1:0	VOL_RAMP_MODE[1:0]	00: 1 step in every sample 01: mute → –40dB, every sample with 1 step. –40dB → 24dB, 2 sample with 1 step. 10: mute → –40dB, 2 sample with 1 step. –40dB → 24dB, 4 sample with 1 step. Others: mute → –40dB, 4 sample with 1 step. –40dB → 24dB, 8 sample with 1 step.

Hard Clip Function

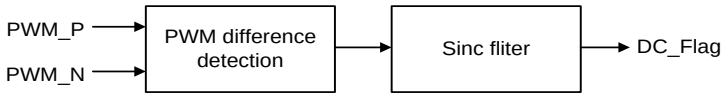
To clip the signal with different threshold, operate in time domain.



Address	BITS	Name	Description
0x06	0	HARD_CLIP_EN	0: Disable hard clip (default) 1: Enable hard clip
0x27	10:0	HARD_CLIP_TH[10:0]	Hard clip threshold for hard clip, when threshold > 0, there is no any clipping effect happened. 11'h180: 0dB 0.0625db per step Note: Due to there is –2dB at digital filter, so hard clipping only works when threshold < –2dB.

DC Protection Function

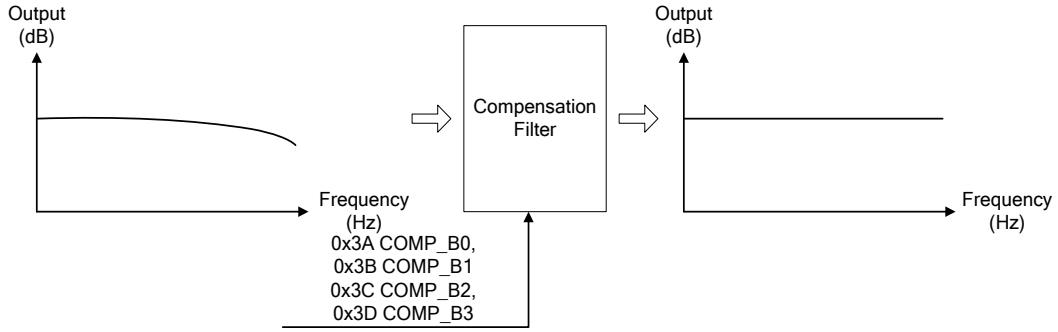
It is to use to protect the loudspeaker, when there are some DC exists at the output. The method is to detect DC at final stage (PWM), calculate the difference of the PWM and a Sinc filter to decide the DC level. The IC will shut down when detect the DC.



Address	BITS	Name	Description
0x14	7:4	Reserved	
	3:2	DC_TH[1:0]	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%
	1	DC_TIME_SEL	Detection time 0: 342ms (default) 1: 684ms
	0	DC_EN	0: DC Protection disable 1: DC protection enable (default)

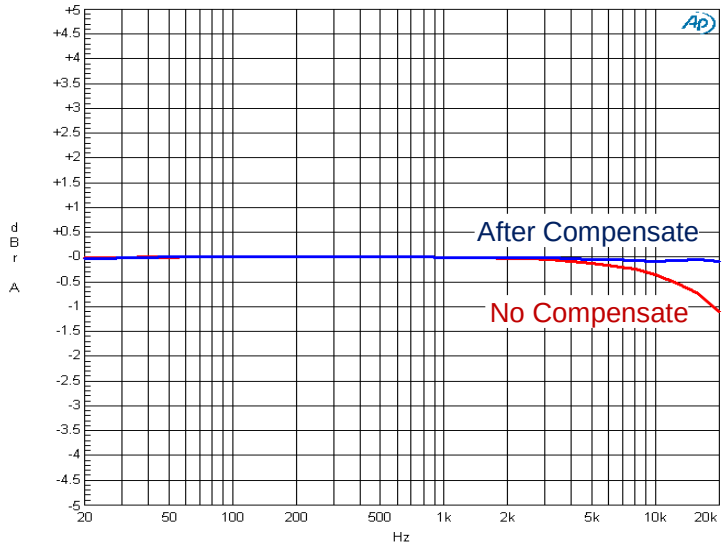
Compensate Filter

Compensation filter is purpose to compensate internal gain from DAC, this filter can also compensate the frequency response affected by LC filter, the recommended setting will base on different application circuit to fit the curve.



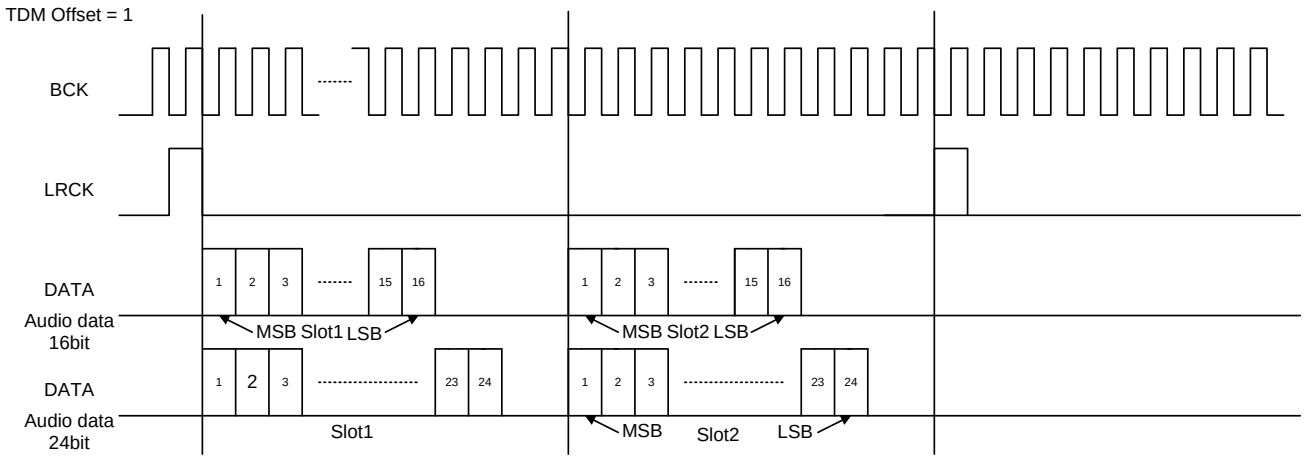
Compensate	Description									
Compensate	B0, B1, B2, B3: Compensate coefficient									
Gain										
Gain	0.1dB	0.2dB	0.3dB	0.4dB	0.5dB	0.6dB	0.7dB	0.8dB	0.9dB	1dB
Coefficient										
B3	00000	1FFFF	00003	00006	00005	00005	00004	00002	00002	00008
B2	0000E	0001E	00022	00026	0003A	00048	0005C	00073	00081	0007F
B1	1FFA1	1FF43	1FEDE	1FE79	1FE19	1FDB1	1FD51	1FCE9	1FC81	1FC14
B0	080A0	0813E	081FF	082C0	0835A	0840F	084A8	0854D	08602	086E0

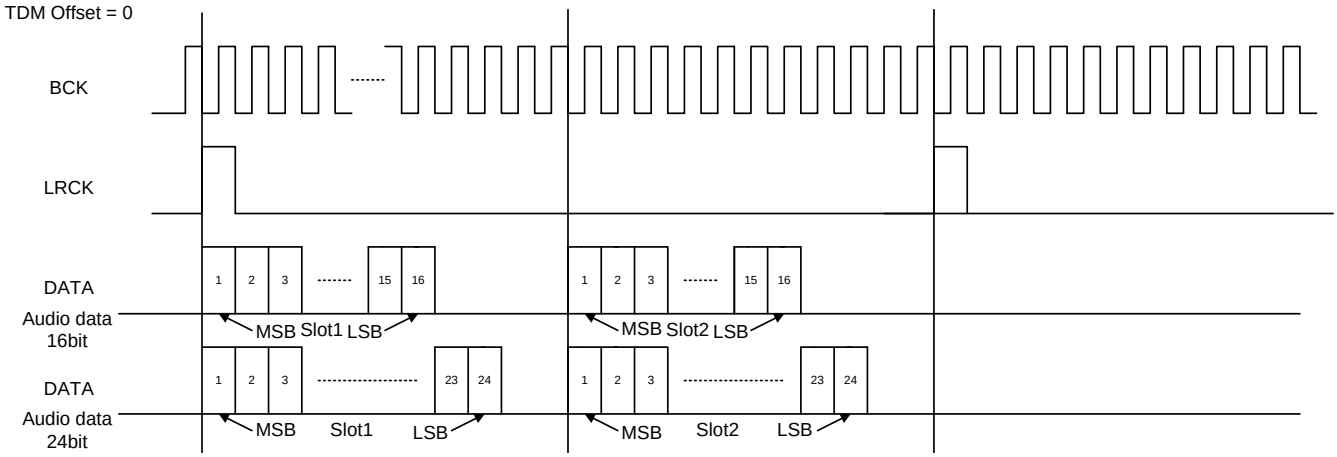
Address	BITS	Name	Description
0x06	6	COMP_EN	0: Compensation filter disable (default) 1: Compensation filter enable (Not available for 96kHz and 192kHz sampling rate)
0x3A	23:17	Reserved	Compensate B0 coefficient
	16:0	COMP_B0	
0x3B	23:17	Reserved	Compensate B1 coefficient
	16:0	COMP_B1	
0x3C	23:17	Reserved	Compensate B2 coefficient
	16:0	COMP_B2	
0x3D	23:17	Reserved	Compensate B3 coefficient
	16:0	COMP_B3	



TDM

RT9120S support TDM format, which maximum output can reach 16Ch.





Address	BITS	Name	Description
0xA0	7:3	Reserved	
	2	DATAO_PD	Prohibited
	1	TDM_OFFSET	TDM offset selection 0: Without offset 1: 1 bit clock offset (default)
	0	TDM_EN	0: TDM disable TDM application (default) 1: TDM enable
0xA1	7:6	Reserved	
	5:0	TDM_RX_LOC_L	TDM start receiving location select for left channel (reg*8 + offset) 000000: Start from 0+offset (default) 000001: Start from 8+offset … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available
0xA2	7:6	Reserved	
	5:0	TDM_RX_LOC_R	TDM start receiving location select for left channel (reg*8 + offset) 000000: Start from 0+offset 000001: Start from 8+offset … 000100: Start from 32+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available
0xA3	7:6	Reserved	
	5:0	TDM_TX_LOC_L	TDM start transmitting location select for left channel (reg*8 + offset) 000000: Start from 0+offset (default) 000001: Start from 8+offset … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available
0xA4	7:6	Reserved	
	5:0	TDM_TX_LOC_R	TDM start transmitting location select for right channel (reg*8 + offset) 000000: Start from 0+offset 000001: Start from 8+offset … 000100: Start from 32+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available

Example

1. Set the 0xA0, Bit[0] to 1
2. Set the 0x02, Bit[7:6] to 00
3. Use the below setting

Note 1: The RT9120S has SDO output, which can output the I^2S data and TDM data to SOC side for receiving use, so if the receiving not use, the 0xA3, and 0xA4 can keep the default setting.

Note 2: If SCLK (BCK) frequency is larger than the 10MHz, please set the 0x10 to 0x00 once the initial setting done.

If output is 16Ch, Sampling Rate is 48kHz								
Output Ch	**Ch1, Ch2**	**Ch3, Ch4**	**Ch5, Ch6**	**Ch7, Ch8**	**Ch9, Ch10**	**Ch11, Ch12**	**Ch13, Ch14**	**Ch15, Ch16**
0xA1	Set to 0x00	Set to 0x08	Set to 0x10	Set to 0x18	Set to 0x20	Set to 0x28	Set to 0x30	Set to 0x38
0xA2	Set to 0x04	Set to 0x0C	Set to 0x14	Set to 0x1C	Set to 0x24	Set to 0x2C	Set to 0x34	Set to 0x3C
0xA3	Set to 0x00	Set to 0x08	Set to 0x10	Set to 0x18	Set to 0x20	Set to 0x28	Set to 0x30	Set to 0x38
0xA4	Set to 0x04	Set to 0x0C	Set to 0x14	Set to 0x1C	Set to 0x24	Set to 0x2C	Set to 0x34	Set to 0x3C

If output is 8Ch, Sampling Rate is 96kHz				
Output Ch	**Ch1, Ch2**	**Ch3, Ch4**	**Ch5, Ch6**	**Ch7, Ch8**
0xA1	Set to 0x00	Set to 0x08	Set to 0x10	Set to 0x18
0xA2	Set to 0x04	Set to 0x0C	Set to 0x14	Set to 0x1C
0xA3	Set to 0x00	Set to 0x08	Set to 0x10	Set to 0x18
0xA4	Set to 0x04	Set to 0x0C	Set to 0x14	Set to 0x1C

If output is 4Ch, Sampling Rate is 192kHz		
Output Ch	**Ch1, Ch2**	**Ch3, Ch4**
0xA1	Set to 0x00	Set to 0x08
0xA2	Set to 0x04	Set to 0x0C
0xA3	Set to 0x00	Set to 0x08
0xA4	Set to 0x04	Set to 0x0C

PBTL Function

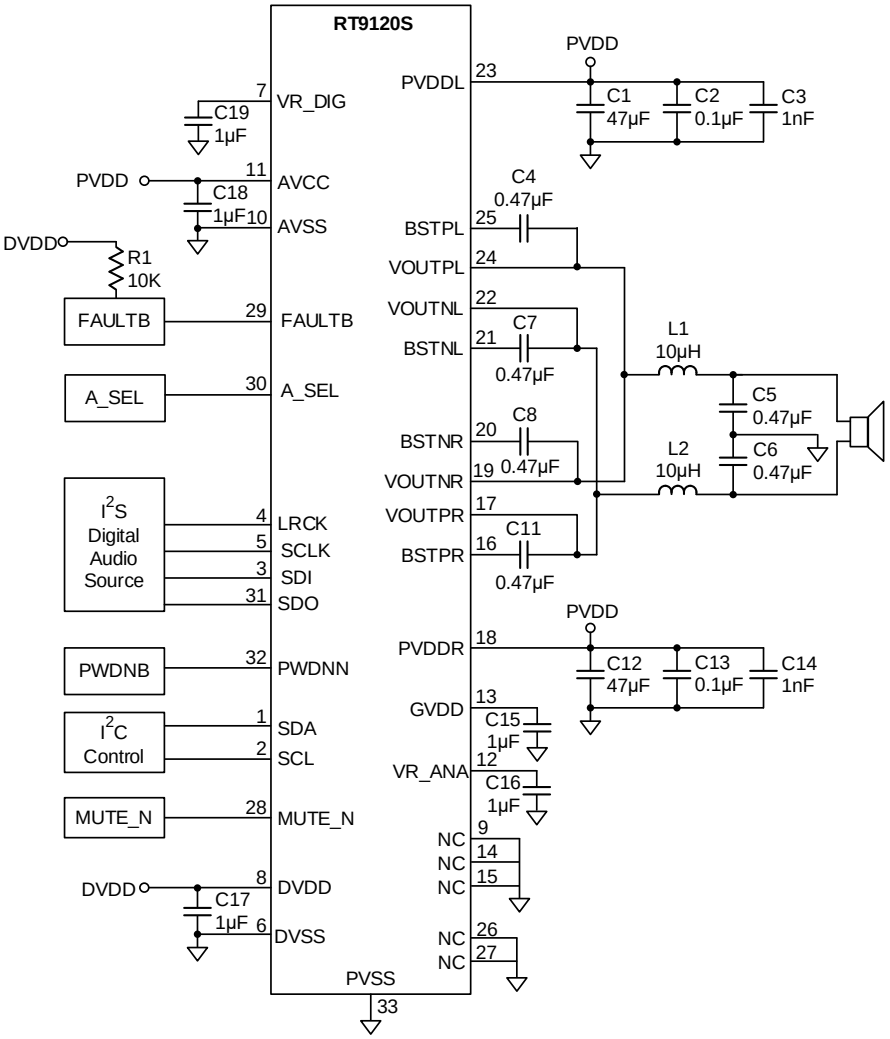
It can be configured by the hardware, and also need to change the software setting

The Input signal, can be configured by the input mixer, from register 0x30 to configure the input signal. The default signal for the PBTL is from 0x30 L channel signal.

Address	BITS	Name	Description
0x05	4	D_PBTL	0: BTL, 1: PBTL

Address	BITS	Name	Description
0x30	16:0	CH1_IN_MIX_0	u[23:17], mix_0[16:0] u: Unused
0x31	16:0	CH1_IN_MIX_1	u[23:17], mix_1[16:0] u: Unused

Mono PBTL Application Circuit

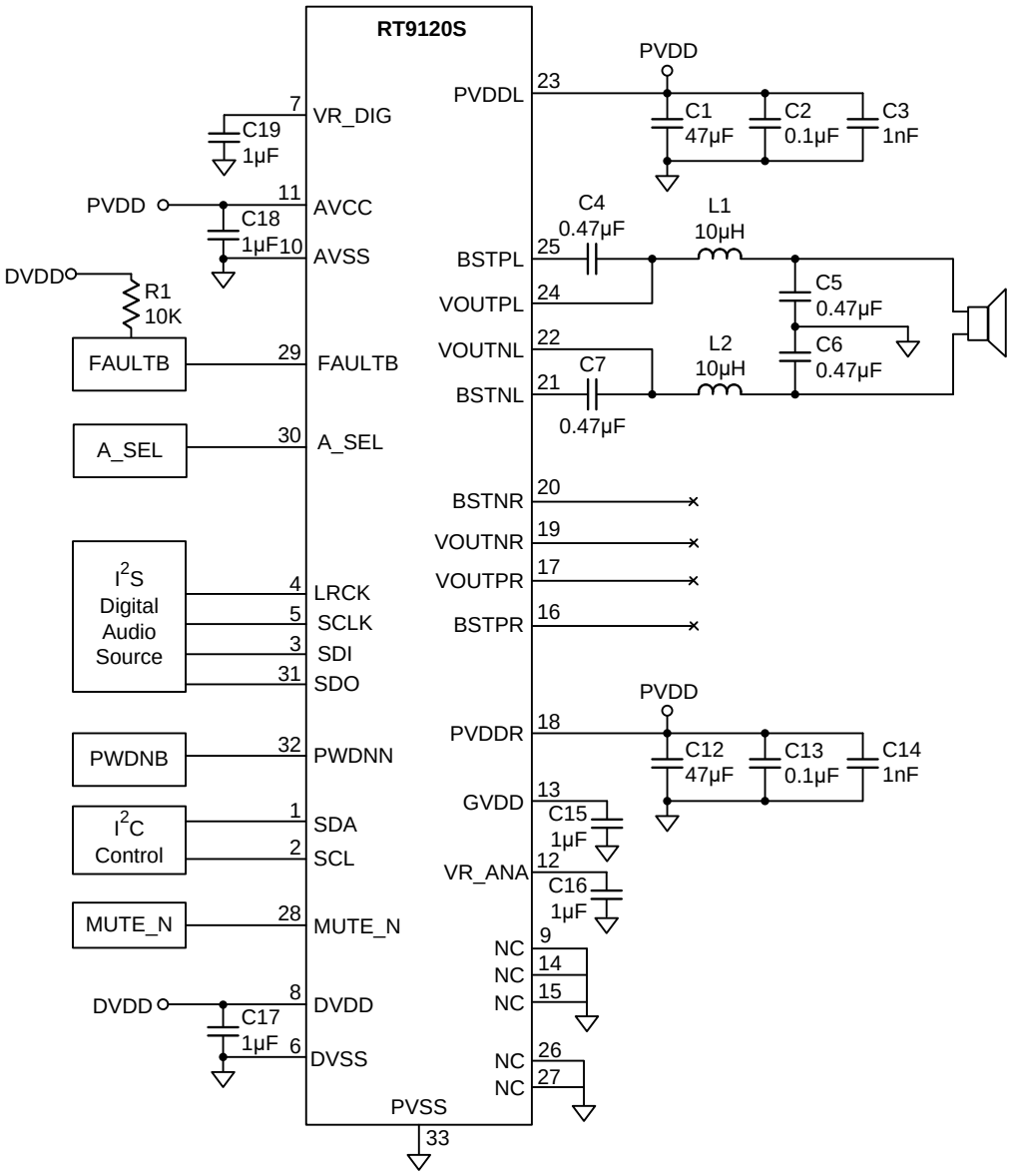


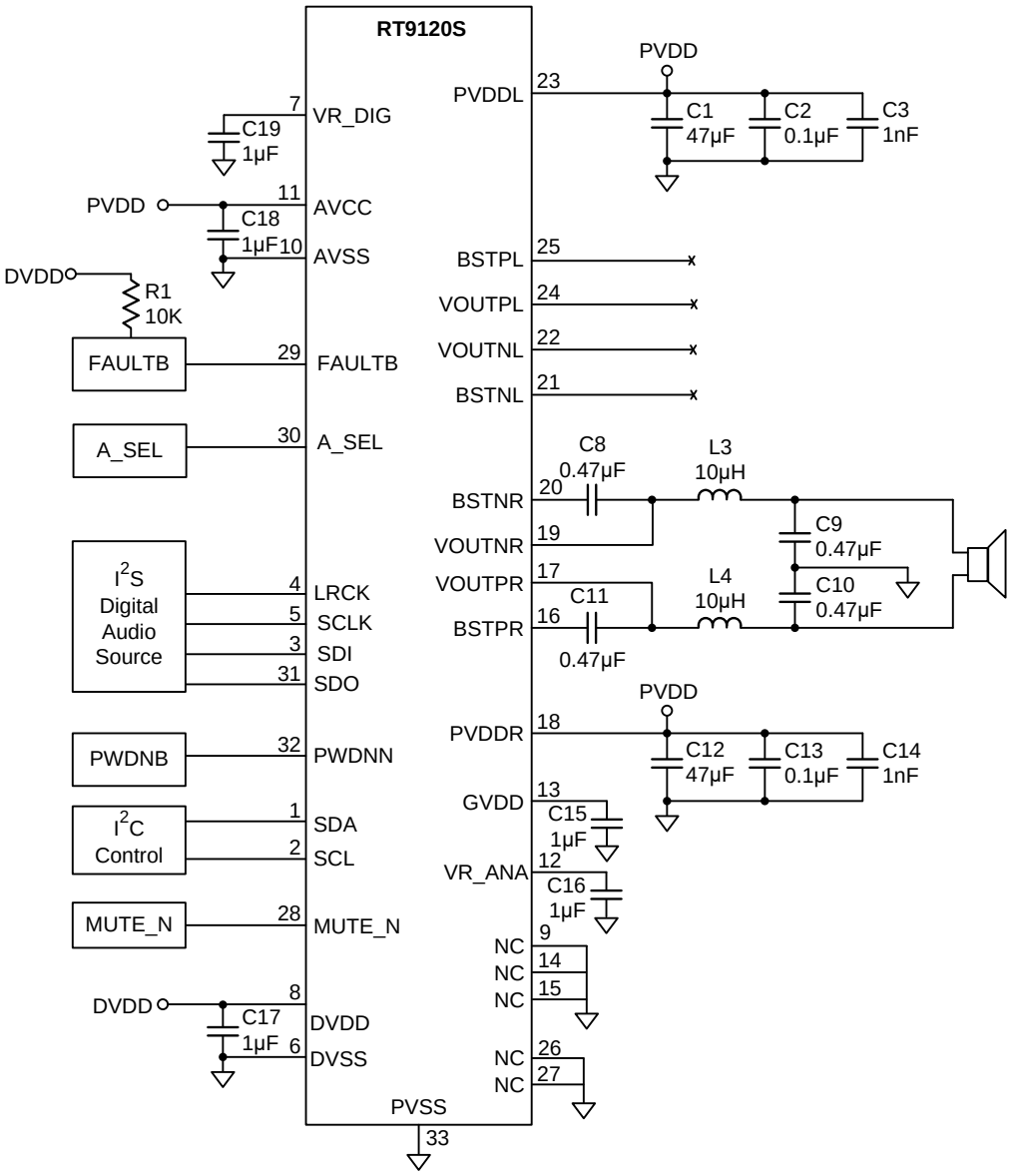
Mono Configuration

To use the mono configuration, It can be configured by register setting.

Address	BITS	Name	Description
0x08	7	D_LPFR_EN	Enable DAC RCH LPF 0: Disable 1: Enable (default)
	6	D_LPFL_EN	Enable DAC LCH LPF 0: Disable 1: enable (default)
	5	D_EN_RCH_PWR	RCH PWR stage enable 0: Disable 1: Enable (default)
	4	D_EN_LCH_PWR	LCH PWR stage enable 0: Disable 1: Enable (default)
	3	D_DAC_RCH_EN	Enable DAC_RCH 0: Disable 1: Enable (default)
	2	D_DAC_LCH_EN	Enable DAC LCH 0: Disable 1: enable (default)
	1	D_SPK_RCH_EN	Enable Class-D RCH SPK 0: Disable 1: Enable (default)
	0	D_SPK_LCH_EN	Enable Class-D LCH SPK 0: Disable 1: Enable (default)

Mono Configuration	Example
Use Left Channel	Set the Bit[7], Bit[5], Bit[3], Bit[1] to Zero, others keep 1



Mono Configuration	Example
Use Right Channel	Set the Bit[6], Bit[4], Bit[2], Bit[0] to Zero, others keep 1 

Protection Behavior

If the protection behavior happened, the IC will automated detect, the error condition can be checked by the register or FAULTB pin.

Protection Flag

Address	BITS	Name	Description
0x10	7	Reserved	
	6	DC_ERR	DC flag report 0: No DC error (default) 1: DC error
	5	SCLK_ERR	0: No SCLK error (default) 1: SCLK error, write 0 to clear flag
	4	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write0 to clear flag
	3	OC_ERR	0: No OC error (default) 1: OC, write 0 to clear flag
	2	OV_ERR	0: No OV error (default) 1: OV, write 0 to clear flag
	1	OT_ERR	0: No OT error (default) 1: OT, write 0 to clear flag
	0	UV_ERR	0: No UV error (default) 1: UV, write 0 to clear flag

Protection Type

Protection	Auto Recovery	Shutdown Amp (Latch Type)	Fault Pin Pull Low
DC Protection	No	Yes	Yes
SCLK ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[5]	Yes, but the MASK can be configured by the 0x11 bit[5]
LRCK ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[4]	Yes, but the MASK can be configured by the 0x11 bit[4]
OC ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[3]	Yes, but the MASK can be configured by the 0x11 bit[3]
OV ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[2]	Yes, but the MASK can be configured by the 0x11 bit[2]
OT ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[1]	Yes, but the MASK can be configured by the 0x11 bit[1]
UV ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[0]	Yes, but the MASK can be configured by the 0x11 bit[0]

When protection happened, there are 2 types of the protection behavior can be use.

1. Latch type: Will shut down the AMP directly.
2. Auto recovery type: The AMP will enter the auto recovery mode, until the protection behavior stop, the AMP will continued to work.
3. The DC protection only has the latch type.

Fault Behavior Type Select

If the protection behavior happened, the IC will automate detect, there are some error type can been configured by below list.

Address	BITS	Name	Description
0x12	5	SCLK_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch
	4	LRCK_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch
	3	OC_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery 1: Latch (default)
	2	OV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch
	1	OT_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch
	0	UV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch

Fault Mask

Address	BITS	Name	Description
0x11	5	SCLK_ERROR_mask	Fault mask for 0x10 SCLK error
	4	LRCK_ERROR_mask	Fault mask for 0x10 LRCK error
	3	OC_ERROR_mask	Fault mask for 0x10 OC error
	2	OV_ERROR_mask	Fault mask for 0x10 OV error
	1	OT_ERROR_mask	Fault mask for 0x10 OT error
	0	UV_ERROR_mask	Fault mask for 0x10 UV error

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-32L 5x5 package, the thermal resistance, θ_{JA}, is 27.7°C/W on a standard JEDEC 51-7 high effective- thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (150°C - 25°C) / (27.7°C/W) = 4.51W for a VQFN-32L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

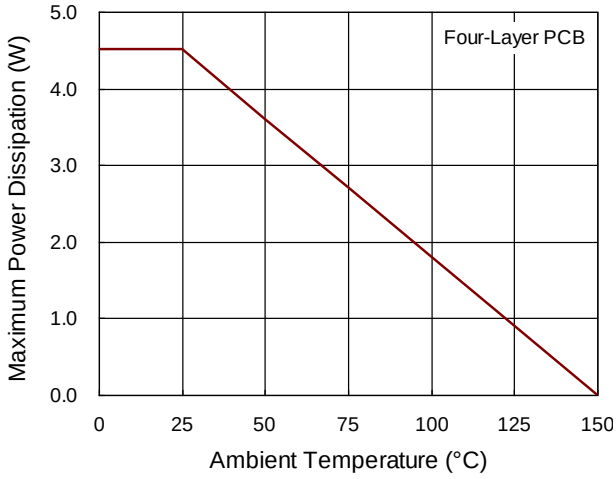
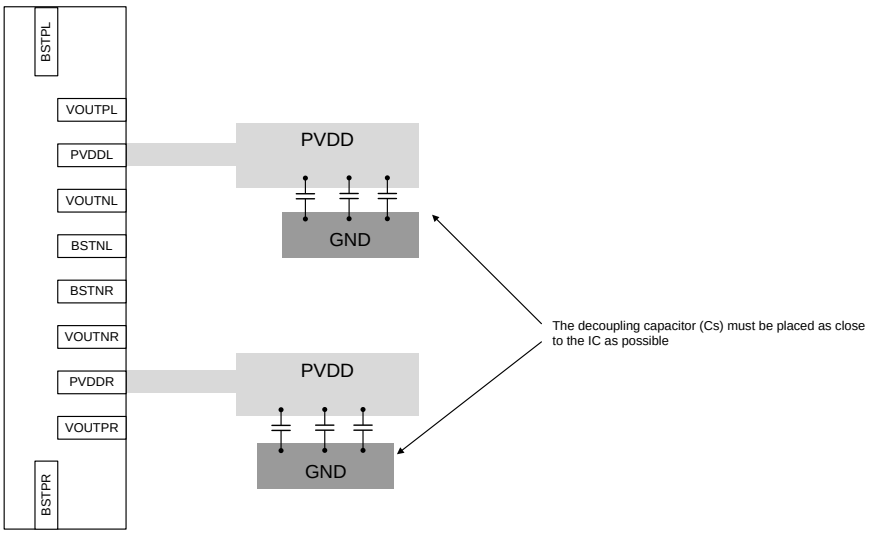


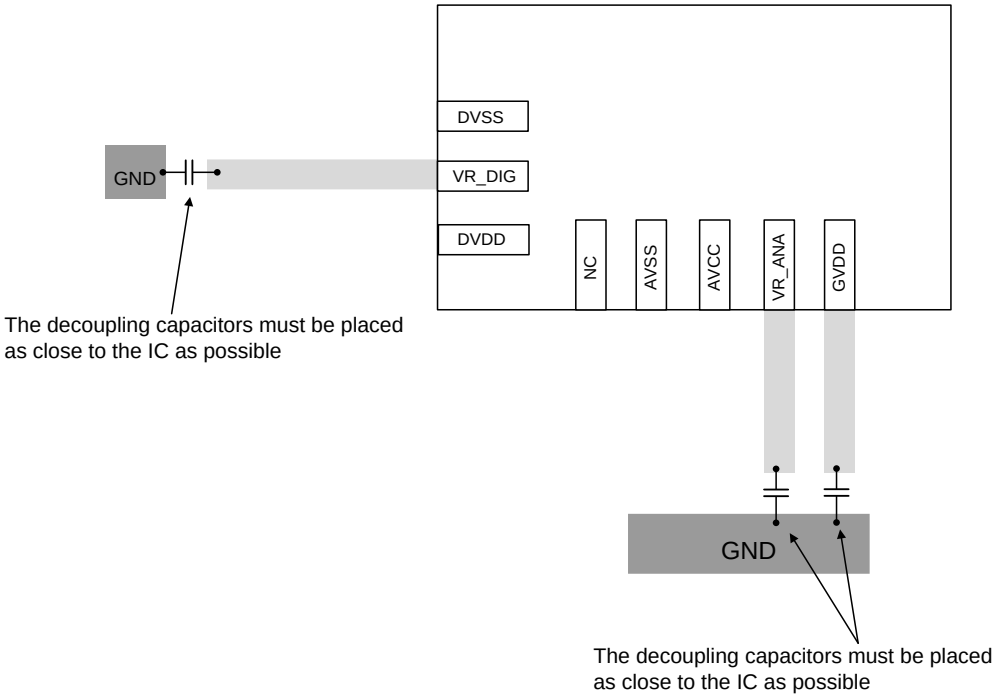
Figure 3. Derating Curve of Maximum Power Dissipation

Layout Guide

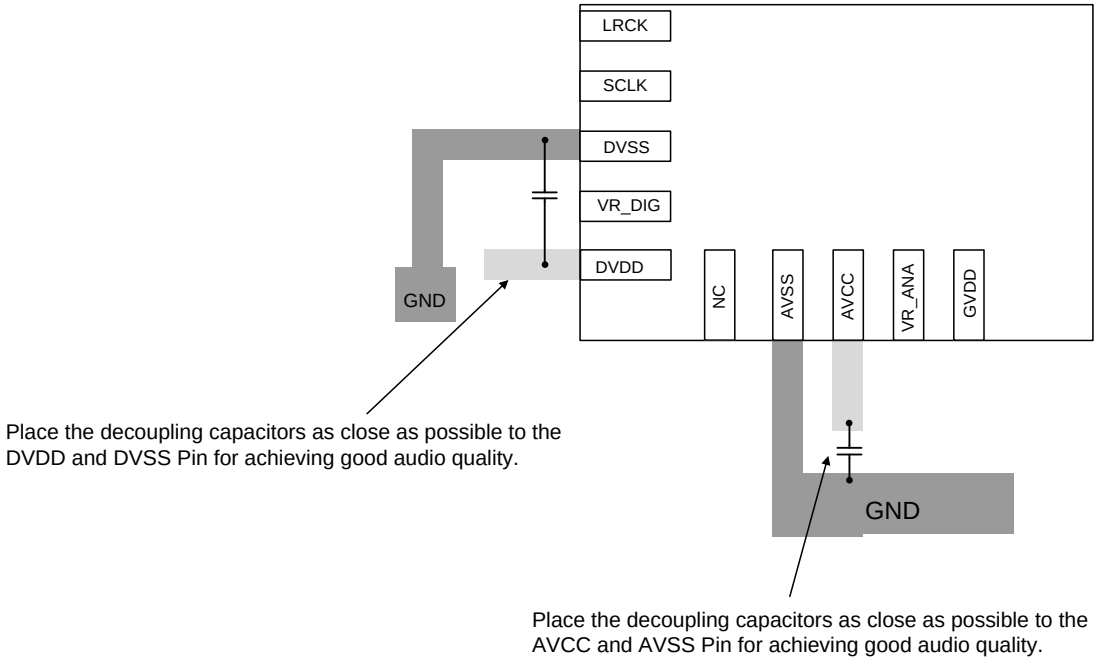
Place the decoupling capacitors as close as possible to the PVCC and GND, then use shortest trace to link these capacitors, and use more vias for GND link to GND layer to reduce parasitic inductance and resistance. The trace width is 30mil at least.



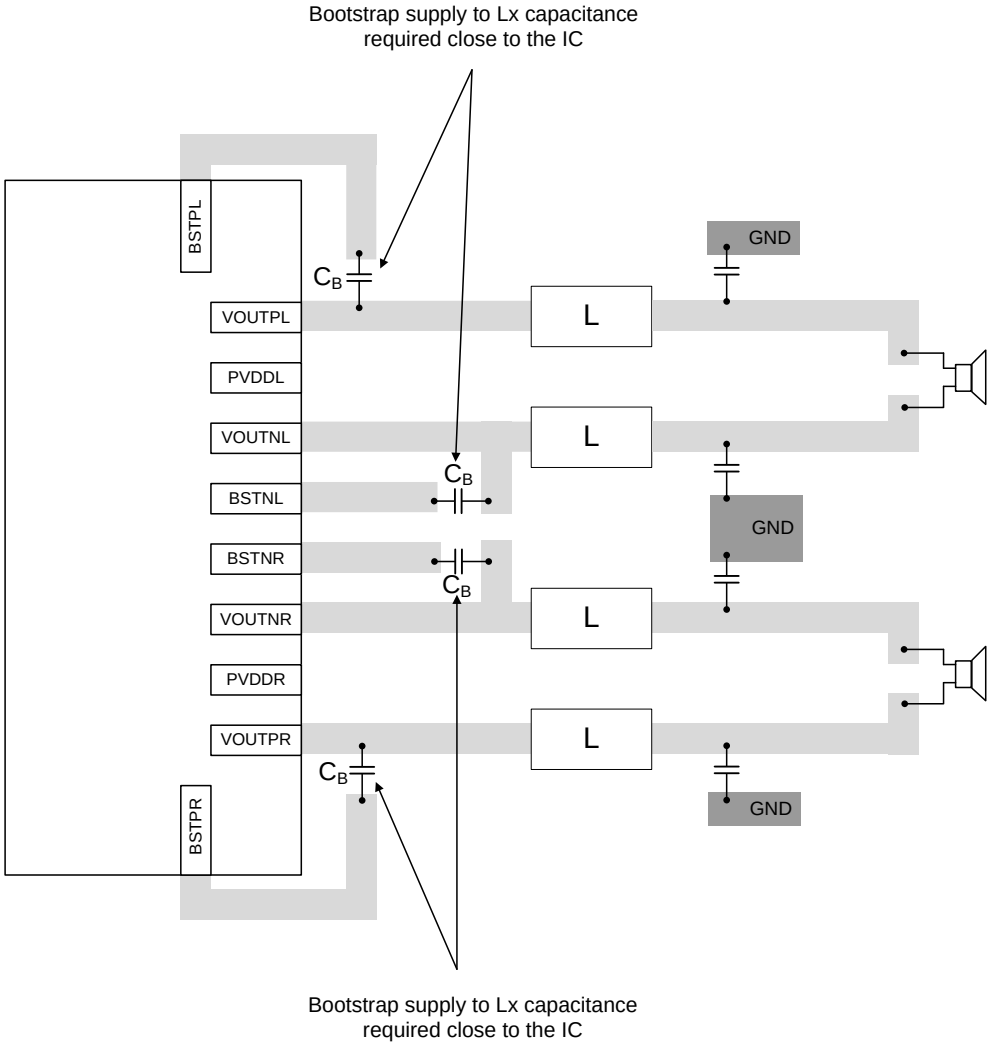
The VR_DIG, VR_ANA and GVDD decoupling capacitors must be placed as close to the IC as possible.



Place the decoupling capacitors as close as possible to the DVDD and DVSS Pin, AVCC and AVSS Pin for achieving good audio quality, the trace width of DVDD is 6mil at least and the trace width of AVCC is 30mil at least.



The traces of VOUTPL, VOUTNL, VOUTPR and VOUTNR should be kept equal width and length respectively, and Bootstrap supply to Lx capacitance required close to the IC.



If possible, coplanar ground fill on both sides for differential pair of speaker out shielding.

Register Map

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x00	2	DEV_ID	15:0	R	DEVICE_ID[15:0]		16'h4303
0x01	1	I2S_CLK_FMT	7:4	R/W	SR_MODE[2:0]	Sampling rate report 0000: 8kHz 0001: 11.025/12kHz 0010: 16kHz 0011: 22.05/24kHz 0100: 32kHz 0101: 44.1/48kHz (default) 0110: 88.2/96kHz 0111: 192kHz Others: Not supported/ SCLK loss/LRCK loss	4'b0101
			3:0	R/W	BCK_MODE[2:0]	BCK mode report 0000: BCK = 32fs 0001: BCK = 48fs 0010: BCK = 64fs (default) 0011: BCK = 96fs 0100: BCK = 128fs 0101: BCK = 192fs 0110: BCK = 256fs 0111: BCK = 384fs 1000: BCK = 512fs others: Reserved Note: For the 48fs, 96fs, 192fs, 384fs, 512fs, please set 0xF8 bit[6] to 0.	4'b0010

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x02	1	I2S_DATA_FMT	7:6	R/W	SCLK_DEG_SEL[1:0]	SCLK deglitch time selection 00: No deglitch 01: 1T sync 10: 2T deglitch 11: 3T deglitch (default)	2'b11
			5	R/W	SCLK_EDGE_SEL	0: RX @BCK rising edge & TX @BCK falling edge (default) 1: RX @BCK falling edge & TX @BCK rising edge	1'b0
			4	R/W	DSP_M_A_S	DSP mode A select, active with AUD_FMT = 2'b11 (DSP mode) 0: DSP mode A (default) 1: DSP mode B	1'b0
			3:2	R/W	AUD_FMT	00: I^2S (default) 01: Left Justify 10: Right Justify 11: DSP mode	2'b00
			1:0	R/W	AUD_BITS	00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits (default)	2'b11
0x04	1	SDIO_SEL	7	R	Reserved		1'b0
			6	R/W	Prohibit	Prohibited	1'b1
			5:4	R/W	SDO_SEL[1:0]	00: No output (default) 01: Interface output 10: Final output 11: Peak level detect result	2'b00
			3:2	R/W	CH1_SI[1:0]	00: SDIN-L to CH1 (default) 01: SDIN-R to CH1 1X: 0 to CH1	2'b00
			1:0	R/W	CH2_SI[1:0]	00: SDIN-L to CH2 01: SDIN-R to CH2 (default) 1X: 0 to CH2	2'b01

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x05	1	SYS_CTL	7	R/W	SR_AUTO_DET	Prohibited	1'b1
			6	R/W	SHUTDOWN	0: Turn on 1: Shut down (default)	1'b1
			5	R	Reserved		1'b0
			4	R/W	D_PBTL	0: BTL (default) 1: PBTL	1'b0
			3:2	R/W	D_SPK_VT_FREQ	PWM frequency 00: 384kHz 01: Reserved 10: 768kHz (default) 11: 1536kHz	2'b10
			1	R/W	DIS_A_SEL_PU	Prohibited	1'b0
			0	R/W	dSR_DIV_SEL	Prohibited	1'b0
0x06	1	DIG_BLK_EN	7	R/W	Reserved		1'b0
			6	R/W	COMP_EN	0: Compensation filter disable (default) 1: Compensation filter enable (not available in 96k & 192kHz Sampling Rate)	1'b0
			5	R/W	HPF_EN	0: High-Pass filter disable 1: High-Pass filter enable (default)	1'b1
			4	R/W	TFC_EN	Thermal fold back control enable 0: Disable (default) 1: Enable	1'b0
			3	R/W	DRC_PEAK	DRC mode selection 0: RMS mode 1: Peak mode (default)	1'b1
			2	R/W	DRC_EN	DRC enable 0: Disable (default) 1: Enable	1'b0
			1	R/W	DRC_N_EN	DRC noise gate enable 0: Disable (default) 1: Enable	1'b0
			0	R/W	HARD_CLIP_EN	Hard clip enable 0: Disable (default) 1: Enable	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x07	1	SPK_GAIN	7:6	R	Reserved		2'b00
			5	R/W	SPK_GAIN_SW_TO_EN	SPK gain switch @ zero crossing point, if the SPK gain change and no zero crossing point after 100ms, the gain will switch to the target gain when time out function is enable. 0: Disable 1: Enable (default)	1'b1
			4:0	R/W	D_SPK_GAIN[4:0]	Class-D output gain 00000: –6dB 00001: –5dB 00010: –4dB 00011: –3dB 00100: –2dB 00101: –1dB 00110: 0dB 00111: 1dB 01000: 2dB 01001: 3dB 01010: 4dB 01011: 5dB 01100: 6dB 01101: 7dB 01110: 8dB 01111: 9dB 10000: 10dB 10001: 11dB 10010: 12dB 10011: 13dB (default) 10100: 14dB 10101: 15dB 10110: 16dB 10111: 17dB	5'h13

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x08	1	INTER_PWR_CTRL	7	R/W	D_LPFR_EN	Enable DAC RCH LPF 0: Disable 1: Enable (default)	1'b1
			6	R/W	D_LPFL_EN	Enable DAC LCH LPF 0: Disable 1: Enable (default)	1'b1
			5	R/W	D_EN_RCH_PWR	RCH PWR stage enable 0: Disable 1: Enable (default)	1'b1
			4	R/W	D_EN_LCH_PWR	LCH PWR stage enable 0: Disable 1: Enable (default)	1'b1
			3	R/W	D_DAC_RCH_EN	Enable DAC_RCH 0: Disable 1: Enable (default)	1'b1
			2	R/W	D_DAC_LCH_EN	Enable DAC LCH 0: Disable 1: Enable (default)	1'b1
			1	R/W	D_SPK_RCH_EN	Enable Class-D RCH SPK 0: Disable 1: Enable (default)	1'b1
			0	R/W	D_SPK_LCH_EN	Enable Class-D LCH SPK 0: Disable 1: Enable (default)	1'b1
0x09	1	PWM_SS_OPT	7	R/W	D_FSS_EN	Spread spectrum enable 0: Disable (default) 1: Enable	1'b0
			6	R/W	PWM_MODEWHITE	Noise select 0: Pink noise (default) 1: White noise	1'b0
			5	R/W	PWM_SELCOEF	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4	1'b0
			4	R/W	PWM_NOISE_EN	Add noise to TRI_GEN 0: Disable (default) 1: Enable	1'b0
			3:2	R/W	D_NOISE_AMP[1:0]	Nosie amplitude for SSC	2'b00
			1:0	R/W	D_FSS_AMP[1:0]	Spread spectrum frequency variation amplitude 00: 20kHz 01: 40kHz (default) 10: 40kHz 11: 60kHz	2'b01

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x0A	1	VOL_RAMP	7:6	R	Reserved		2'b00
			5	R/W	CH2_MUTE	0: Unmute (default) 1: CH2 soft mute	1'b0
			4	R/W	CH1_MUTE	0: Unmute (default) 1: CH1 soft mute	1'b0
			3	R/W	SKIP_RAMP	Skip volume ramp	1'b0
			2	R	Reserved		1'b0
			1:0	R/W	VOL_RAMP_MODE [1:0]	Volume Slew step control 00: 1 step in every sample 01: mute → –40dB, every sample with1 step. –40dB → 24dB, 2 sample with 1 step. (default) 10: mute → –40dB, 2 sample with 1 step. –40dB → 24dB, 4 sample with 1 step. (default) Others: Mute → –40dB, 4 sample with 1 step. –40dB → 24dB, 8 sample with 1 step.	2'b01
0x0B	1	TFC_CTRL	7:6	R	Reserved	Prohibited	2'b00
			5	R	D_TFC_UPBOUN_FLAG	Prohibited	1'b0
			4	R	D_TFC_LOWBOUN_FLAG	Prohibited	1'b0
			3:2	R/W	TFC_TH	Thermal fold back active threshold 00: Temp 110°C (default) 01: Temp 120°C 10: Temp 130°C 11: Temp 140°C	2'b00
			1:0	R/W	TFC_RATE	Thermal fold back attack/release rate 00: 0.0625dB/50ms (default) 01: 0.0625dB/100ms 10: 0.0625dB/200ms 11: 0.0625dB/400ms	2'b00
0x0C	1	Reserved	7:0	R/W	Reserved	Prohibited	8'h30

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x10	1	ERR_RPT	7	R/W	ADS_ERR	Address R detection error 0: No R detect error (default) 1: R detect error, write 0 to clear flag	1'b0
			6	R	DC_ERR	DC flag report 0: No DC error (default) 1: DC error	1'b0
			5	R/W	SCLK_ERR	0: No SCLK error (default) 1: SCLK error, write 0 to clear flag	1'b0
			4	R/W	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write 0 to clear flag	1'b0
			3	R/W	OC_ERROR	0: No OC error (default) 1: OC, write 0 to clear flag	1'b0
			2	R/W	OV_ERROR	0: No OV error (default) 1: OV, write 0 to clear flag	1'b0
			1	R/W	OT_ERROR	0: No OT error (default) 1: OT, write 0 to clear flag	1'b0
			0	R/W	UV_ERROR	0: No UV error (default) 1: UV, write 0 to clear flag	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x11	1	ERR_MASK	7:6	R	Reserved	Prohibited	2'b00
			5	R/W	SCLK_ERROR_MASK	Fault mask for 0x10 SCLK error 0: Not mask 1: Mask (default)	1'b1
			4	R/W	LRCK_ERROR_MASK	Fault mask for 0x10 LRCK error 0: Not mask 1: Mask (default)	1'b1
			3	R/W	OC_ERROR_MASK	Fault mask for 0x10 OC error 0: Not mask (default) 1: Mask	1'b0
			2	R/W	OV_ERROR_MASK	Fault mask for 0x10 OV error 0: Not mask (default) 1: Mask	1'b0
			1	R/W	OT_ERROR_MASK	Fault mask for 0x10 OT error 0: Not mask (default) 1: Mask	1'b0
			0	R/W	UV_ERROR_MASK	Fault mask for 0x10 UV error 0: Not mask (default) 1: Mask	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x12	1	'ERR_TYPE	7:6	R	Reserved		2'b00
			5	R/W	SCLK_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch	1'b0
			4	R/W	LRCK_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch	1'b0
			3	R/W	OC_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery 1: Latch (default)	1'b1
			2	R/W	OV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch	1'b0
			1	R/W	OT_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch	1'b0
			0	R/W	UV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto recovery (default) 1: Latch	1'b0
0x13	1	AUTO_RCVRY	7:6	R	Reserved		2'b00
			5	R/W	FAULT_B_TYPE	0: Recovery type (default) 1: Latch type	1'b0
			4	R/W	PROT_PWR_PL_EN	Prohibited	1'b1
			3:0	R/W	RCVRY_TIME[3:0]	Power Stage auto recovery time 0010: 299ms (default) 0011: 449ms 0100: 598ms 0101: 748ms 0110: 898ms 0111: 1047ms 1000: 1197ms 1001: 1346ms 101X: 1496ms 11XX: 1496ms	4'b0010

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x14	1	DC_PROT	7:4	R	Reserved	Prohibited	4'b0000
			3:2	R/W	DC_TH[1:0]	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%	2'b10
			1	R/W	DC_TIME_SEL	Detection time 0: 342ms (default) 1: 684ms	1'b0
			0	R/W	DC_EN	DC protection enable 0: Disable 1: Enable (default)	1'b1
0x20	2	MS_VOL	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	MS_VOL[10:0]	Master volume control 11'h000: 24dB 11'h180: 0dB 11'h7FF: mute (default) 0.0625dB per step	11'h7FF
0x21	2	CH1_VOL	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	CH1_VOL[10:0]	CH1 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step	11'h180
0x22	2	CH2_VOL	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	CH2_VOL[10:0]	CH2 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step	11'h180
0x23	2	DRC_TH	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	DRC_TH	DRC threshold 11'h000: 0dB (default) 11'h180: −24dB 11'h67E: −103.875dB 11'h67F~11'h7FF: Not available 0.0625dB per step	11'h000
0x24	2	DRC_RATIO	15:8	R	Reserved	Prohibited	8'h00
			7:0	R/W	DRC_RATIO	DRC compress ratio 8'h00: No compression 8'h80~8'hFF: Full compression 1/128 per step	8'h80

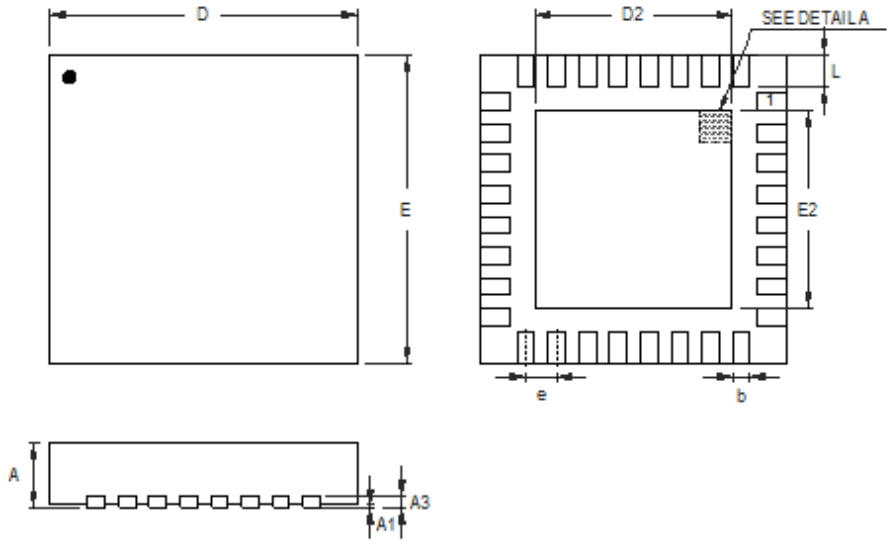
ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x25	2	DRC_OFFSET	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	DRC_OFFSET	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FE: −103.875dB 11'h7FF: Not available 0.0625dB per step	11'h180
0x26	2	DRC_NG_TH	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	DRC_NG_TH	Noise gate threshold 11'h000: 0dB 11'h180: −24dB 11'h640: −100dB (default) 11'h67E: −103.875dB 11'h67F~11'h7FF: Not available 0.0625dB per step	11'h640
0x27	2	HARD_CLIP_TH	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	HARD_CLIP_TH [10:0]	Hard Clip Threshold when HARD_CLIP_EN = 1 > 0dB is not allowable for hard clip threshold setting 11'h180: 0dB (default) 0.0625db per step	11'h180
0x30	3	CH1_IN_MIX_0	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH1_IN_MIX_0	CH1_IN_MIX_0	17’h08000
0x31	3	CH1_IN_MIX_1	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH1_IN_MIX_1	CH1_IN_MIX_1	17’h00000
0x32	3	CH2_IN_MIX_0	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH2_IN_MIX_0	CH2_IN_MIX_0	17’h00000
0x33	3	CH2_IN_MIX_1	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH2_IN_MIX_1	CH2_IN_MIX_1	17’h08000
0x34	3	DRC_AE	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_AE	DRC energy estimator	17’h08000
0x35	3	DRC_1-AE	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_1-AE	DRC energy estimator when releasing	17’h00000
0x36	3	DRC_AD	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_AD	DRC release time	17’h08000
0x37	3	DRC_AA	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_AA	DRC attack time	17’h08000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x38	3	RMS_RPT_AE	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	RMS_RPT_AE	Prohibited	17'h00000
0x3A	3	COMP_B0	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B0	Compensation filter coefficient B0	17'h08000
0x3B	3	COMP_B1	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B1	Compensation filter coefficient B1	17'h08000
0x3C	3	COMP_B2	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B2	Compensation filter coefficient B2	17'h00000
0x3D	3	COMP_B3	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B3	Compensation filter coefficient B3	17'h00000
0x3E	4	CH1_RMS_RPT	31:0	R	CH1_RMS_RPT[31:0]	Prohibited	32'h00000000
0x3F	4	CH2_RMS_RPT	31:0	R	CH2_RMS_RPT[31:0]	Prohibited	32'h00000000
0x40	1	SW_RESET	7	W	SF_RESET	Write 1 to trigger Software reset Need to wait 20ms for reset completion	1'b0
			6:0	R	Reserved	Prohibited	7'h00
0x6C	1	UVP_OPT	7	R	D_VCORE_OK	Prohibited	1'b1
			6	R/W	D_EN_DVDD_UV	Prohibited	1'b1
			5:4	R/W	D_UVP_DVDD_VTH [1:0]	Prohibited	2'b10
			3	R/W	D_UV_RAMP_DOWN	SPK UV protection behavior 0: HZ_PROT directly (default) 1: Power-off sequence	1'b0
			2:0	R/W	D_UVP_PVDD_SEL [2:0]	Select UVP level for PVDD power domain 000: 4V (default) 001: 6.1V 010: 8.7V 011: 11V 100: 12.8V 101: 15.2V 110: 20.3V 111: 21.2V	3'b000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xA0	1	AUD_TDM2	7:3	R	Reserved		5'b00000
			2	R/W	DATAO_PD	I Prohibited	1'b0
			1	R/W	TDM_OFFSET	TDM offset selection 0: Without offset 1: 1 bit clock offset (default)	1'b1
			0	R/W	TDM_EN	0: TDM disable TDM application (default) 1: TDM enable	1'b0
0xA1	1	TDM_RX_L	7:6	R	Reserved		2'b00
			5:0	R/W	TDM2_RX_LOC_L	TDM start receiving location select for left channel 00000: Start from 0 + offset (default) 00001: Start from 8 + offset … 11100: Start from 488 + offest 11101: Start from 496 + offset 11110: Not available 11111: Not available	6'b000000
0xA2	1	TDM_RX_R	7:6	R	Reserved		2'b00
			5:0	R/W	TDM2_RX_LOC_R	TDM start receiving location select for left channel 00000: Start from 0 + offset 00001: Start from 8 + offset … 000100: Start from 32+offset (default) … 11100: Start from 488 + offest 11101: Start from 496 + offset 11110: Not available 11111: Not available	6'b000100

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xA3	1	TDM_TX_L	7:6	R	Reserved		2'b00
			5:0	R/W	TDM2_TX_LOC_L	TDM start transmitting location select for left channel 00000: Start from 0 + offset (default) 00001: Start from 8 + offset … 11100: Start from 488 + offest 11101: Start from 496 + offset 11110: Not available 11111: Not available	6'b000000
0xA4	1	TDM_TX_R	7:6	R	Reserved		2'b00
			5:0	R/W	TDM2_TX_LOC_R	TDM start transmitting location select for right channel 00000: Start from 0+offset 00001: Start from 8+offset … 000100: Start from 32+offset (default) … 11100: Start from 488 + offest 11101: Start from 496 + offset 11110: Not available 11111: Not available	6'b000100

Outline Dimension



DETAIL A

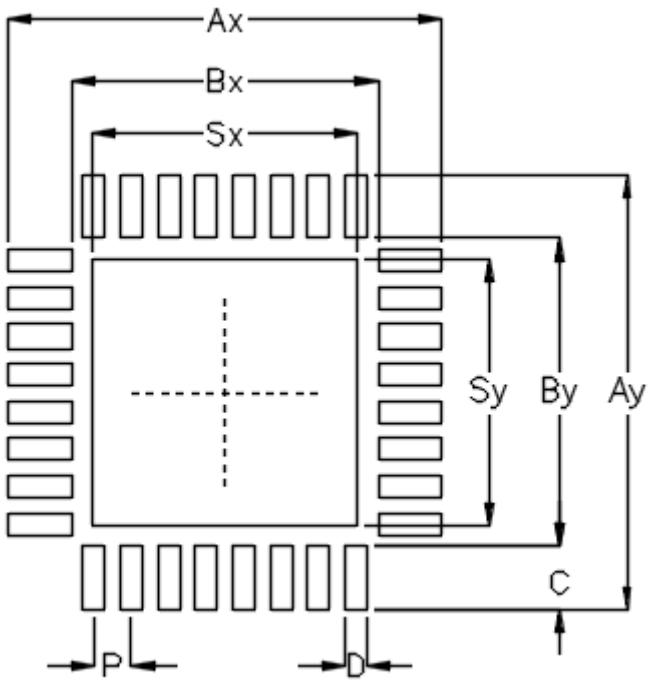
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 32L QFN 5x5 Package

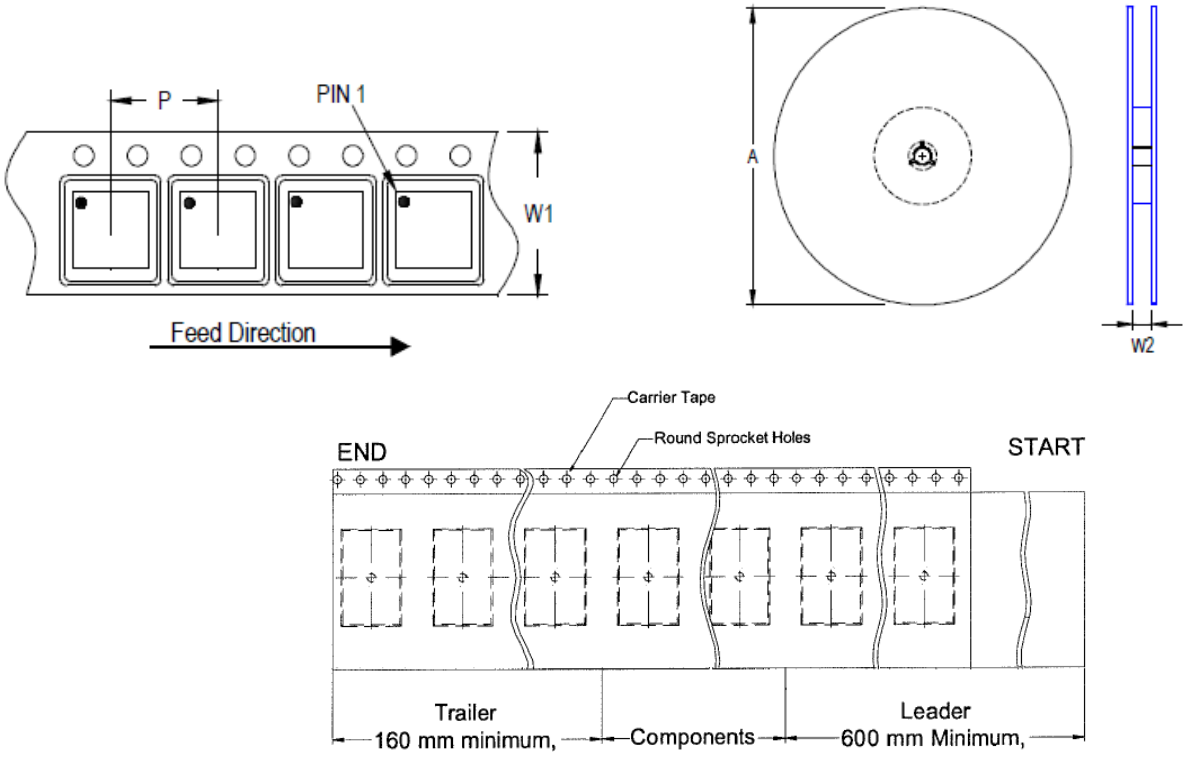
Footprint Information



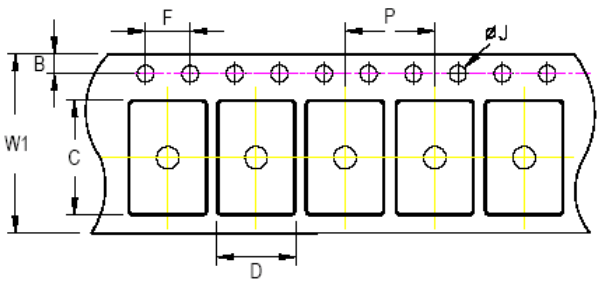
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-32	32	0.50	5.80	5.80	4.10	4.10	0.85	0.30	3.55	3.55	±0.05

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size.

The clearance between the components and

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 5x5	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2022/12/28	Final	Electrical Characteristics on P7 Initial Sequence on P15, 16