RICHTEK®

RT9120E

30W, Stereo, High-Efficiency, Inductor-Less, I²S General-Purpose Class-D Audio Amplifier with DRC Control

1 General Description

The RT9120E is a high efficiency, I²S-input, stereo channel audio power amplifier delivering maximum 2x30W into 8Ω BTL speaker loads. It can deliver over 94% power efficiency at 2x20W and eliminate the need for heatsink and implement CMH mode to reduce pulse width at small signal, inductor current ripple is reduced and hence light load efficiency is improved.

The built-in anti-pop functions can reduce the speaker's pop noise under all kind of scenarios. Built-in protection circuits can provide over-temperature, overcurrent, overvoltage, undervoltage protections and report error status.

The RT9120E is a 3-wired device receiving all clocks from external sources with standard I²S, Left-justified, Right-justified or TDM formats. It can support wide input sampling rate from 8kHz to 192kHz.

The RT9120E features one band DRC and flexible input mixer, and power clipping.

The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 85°C.

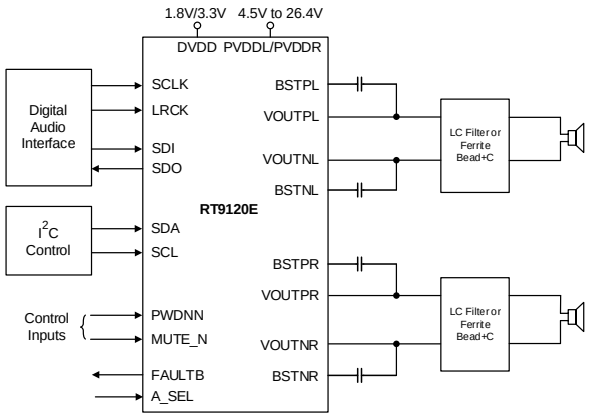
3 Features

- **CMH Mode for Lower Quiescent Current**
- **Wide Input Supply Range: 4.5V to 26.4V**
- **Support 1.8V and 3.3V I/O**
- **Configurable 4 Different IC Slave Address**
- **1x53W, 1.0 Mode (4Ω, 22V, THD + N = 1%)**
- **2x30W, 2.0 Mode (8Ω, 24V, THD + N = 1%)**
- **SNR Up to 113dB**
- **THD + N is 0.03% at 1W**
- **35μV Noise Floor**
- **Efficiency Up to 94% at 2x20W for 6Ω**
- **High Light Load Efficiency at CMH Mode**
- **$R_{DS(ON)}$ Low to 90mΩ**
- **Sampling Frequency from 8kHz to 192kHz**
- **Support TDM Format for Multi-Channel**
- **Built-In Anti-Pop Function**
- **Programmable Coefficients for DRC Filters**
- **Built-In DC Blocking Filters**
- **Built-In Thermal Fold Back control**
- **Protection Features: UVLO, OVP, OCP, OTP, and DCP**
- **Inductor-Less Application**
- **VQFN-32L Thermally-Enhanced Package**

2 Applications

- Wireless, Bluetooth Speakers
- Soundbars, Notebooks, PC Speakers
- Home Audio

4 Simplified Application Circuit



5 Ordering Information

RT9120E□-□□□□

Packing
A: Standard

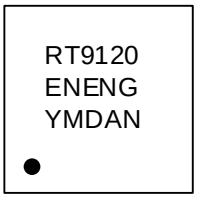
Trim Code

Package Type(1)
N: VQFN-32L 5x5 (V-Type)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information



RT9120ENENG: Product Code
YMDAN: Date Code

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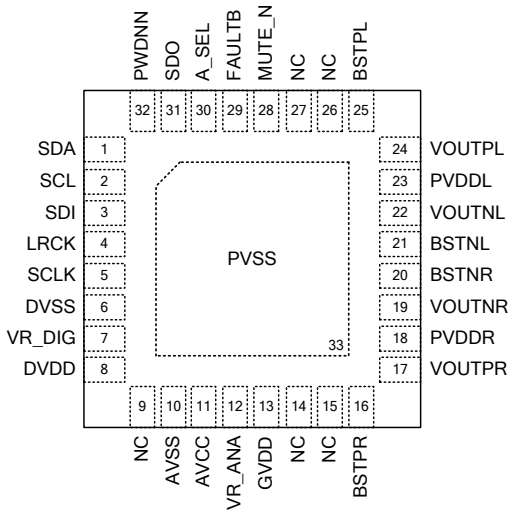
7 Pin Configuration

(TOP VIEW)



VQFN-32L 5x5

8 Functional Pin Description

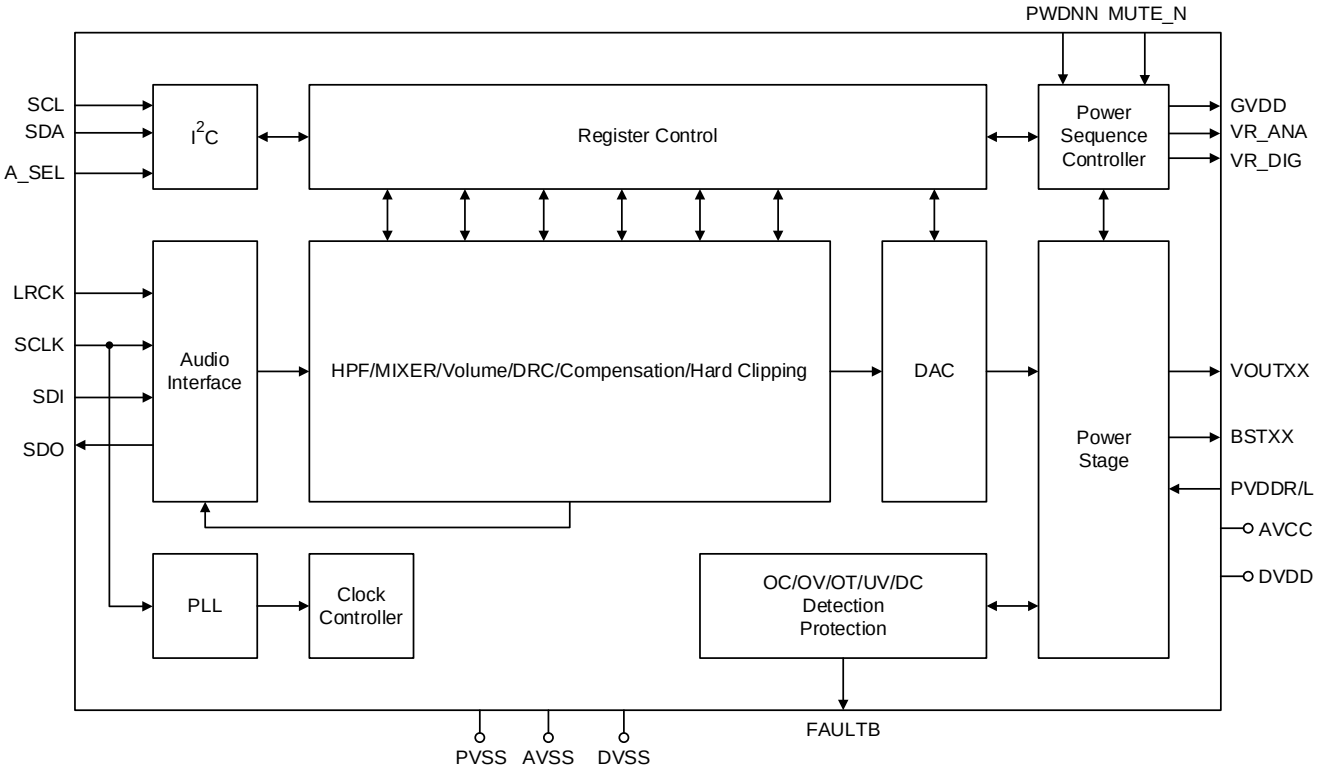
Pin No.	Pin Name	IO	Pin Function
1	SDA	DIO	I^2C data input/output.
2	SCL	DI	I^2C clock input.
3	SDI	DI	I^2S data input.
4	LRCK	DI	I^2S L/R clock input.
5	SCLK	DI	I^2S bit clock input.
6	DVSS	P	Ground for digital circuits.
7	VR_DIG	P	1.8V digital supply voltage generated by internal LDO. Note: when DVDD is 1.8V, connect DVDD to the VR_DIG.
8	DVDD	P	3.3V, 1.8V power supply for I/O.
9, 14, 15, 26, 27	NC	P	No internal connection. (For the layout, tie to GND)
10	AVSS	P	Ground for analog circuits.
11	AVCC	P	26.4V power supply for analog circuits.
12	VR_ANA	P	Analog reference voltage.
13	GVDD	P	Internal power supply generated by LDO.
16	BSTPR	P	Bootstrap supply for VOUTPR.
17	VOUTPR	AO	Positive output of RCH.
18	PVDDR	P	26.4V power supply for RCH.
19	VOUTNR	AO	Negative output of RCH.
20	BSTNR	P	Bootstrap supply of VOUTNR.

Pin No.	Pin Name	IO	Pin Function
21	BSTNL	P	Bootstrap supply for VOUTNL.
22	VOUTNL	AO	Negative output of LCH.
23	PVDDL	P	26.4V power supply for LCH.
24	VOUTPL	AO	Positive output of LCH.
25	BSTPL	P	Bootstrap supply for VOUTPL.
28	MUTE_N	DI	Mute pin.
29	FAULTB	DO	Fault indicator (low active).
30	A_SEL	DI	Slave address selection.
31	SDO	DO	I^2S data output.
32	PWDNN	DI	Power down pin, low active.
33 (Exposed Pad)	PVSS	P	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

8.1 IO Type Definition

- P: Power Pin
- DI: Digital Input Pin
- DO: Digital Output Pin
- DIO: Digital Input and Output Pin
- AO: Analog Output Pin

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, AVCC, PVDDL, PVDDR ---------- –0.3V to 32V
- Supply Voltage, DVDD ---------- –0.3V to 9V
- Speaker Amplifier Output Voltage, VOUTXX ---------- –0.3V to 32V
- BSTXX (Note 3) ---------- –0.3V to 36V
- SCL, SDA, FAULTB ---------- –0.3V to 6V
- LRCK, SCLK, SDI, MUTE_N, PWDNN, A_SEL ---------- –0.3V to DVDD + 0.5V
- GND to PVSS, DVSS and AVSS ---------- –0.3V to 0.3V
- VOUTPR, VOUTNR, VOUTPL, VOUTNL (Note 4) ---------- –10V to 37V
- SDO ---------- –0.3V to 9V
- VR_DIG ---------- –0.3V to 4V
- VR_ANA, GVDD ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  VQFN-32L 5x5 ---------- 4.51W
- Package Thermal Resistance (Note 5)

  VQFN-32L 5x5, θ_{JA} ---------- 27.7°C/W

  VQFN-32L 5x5, $\theta_{JC(TOP)}$ ---------- 0.3°C/W

  VQFN-32L 5x5, $\theta_{JC(BOTTOM)}$ ---------- 0.7°C/W
- Package Thermal Resistance (4-Layer EVB)

  VQFN-32L 5x5, θ_{JA} ---------- 17.53°C/W

  VQFN-32L 5x5, $\theta_{JC(TOP)}$ ---------- 1.6°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 6)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. The result is defined when the cross voltage between BST and VOUT is 5V.

Note 4. The switching terminal should be used within AC peak limits. Overshoot and undershoot must be less than 100ns.

Note 5. θ_{JA} is simulated in the natural convection at T_A = 25°C on a high effective four-layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is simulated at the case top of the package. The result is including the bonding, GND, and real Die.

Note 6. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 7)

- Supply Input Voltage, DVDD ---------- 3.0V to 3.6V
- Supply Input Voltage (For 1.8V I/O), DVDD, VR_DIG (Note 8) ---------- 1.74V to 1.98V
- Supply Input Voltage, PVDDL, PVDDR, AVCC ---------- 4.5V to 26.4V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 150°C

Note 7. The device is not guaranteed to function outside its operating conditions.

Note 8. In 1.8V I/O application, 1.8V is needed to be supplied from an external voltage source to DVDD and VR_DIG.

12 Electrical Characteristics

(PVDDL = PVDDR = AVCC = 12.7V, DVDD = 3.3V, R_L = 6Ω, T_A = 25°C, fsw = 384kHz, L = 10μH, C = 0.47μF, unless otherwise specified.) (Note 9)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
PWDNN High-Level Input Voltage	V_{IH}			DVDD x 0.7	--	--	V
PWDNN Low-Level Input Voltage	V_{IL}			--	--	DVDD x 0.3	V
FAULTB Low-Level Output Voltage	V_{OL}	I_{PULLUP} = 3mA		--	--	0.4	V
DVDD Quiescent Current (Normal Mode)	I_{DVDD}	PWDNN = 3.3V, for DVDD		--	8.5	--	mA
DVDD Shutdown Current	I_{DVDD_STBY}	PWDNN = 0V, no load, no LC filter		--	5	15	μA
PVDDL/R+AVCC Quiescent Current (CMH Mode)	I_{Q_P}	EN = 3.3V, switch 25% duty, no load, no LC filter, PWM = 384kHz		--	20	--	mA
PVDDL/R+AVCC Quiescent Current (CMH Mode)	I_{Q_P}	EN = 3.3V, switch 25% duty, L = 8.2μH, C = 0.47μF, PWM = 384kHz		--	20	--	mA
PVDDL/R+AVCC Quiescent Current (CMH Mode)	I_{Q_P}	EN = 3.3V, switch 25% duty, L = 6.8μH, C = 0.22μF, PWM = 768kHz		--	20	30	mA
PVDDL/R + AVCC Shutdown Current	I_{SD_P}	PWDNN = 0V, no load, no LC filter		--	10	20	μA
Drain-Source On-State Resistance	$R_{DS(ON)}$	PVDD = 12V, I_{OUT} = 500mA, T_J = 25°C	High-Side	--	90	--	mΩ
			Low-Side	--	85	--	
AMP Gain Variation	$\Delta A_{V(SPK\_AMP)}$	AMP to AMP gain difference		–0.5	--	0.5	dB
Speaker Gain Variation	$\Delta A_{V(L/R\ Ch)}$	L/R channel gain difference		--	--	0.4	dB
Startup Time from Shutdown	t_{ON}	Timing between from 0x05 bit [1:0] set to 01 to the PWM output		--	45	--	ms
Volume Ramp Up		Ramp up time is depends on the page 49 0x0A setting. Note: Default setting is 0x0A set to 01		4.33	--	34.65	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Shutdown Time from PWDNN Set to Low	t_{OFF}	Timing between from PWDNN set to low to the PWM stop output	--	--	200	us
Volume Ramp Up Down Time		Ramp down time is depends on the page 49 0x0A setting. Note: Default setting is 0x0A set to 01	4.33	--	34.65	ms
PWM Switching Frequency	f_{SW}	384kHz mode	--	384	--	kHz
		768kHz mode	--	768	--	
RMS Output Power	P_O	THD + N = 10%, (BTL), PVDD = 18V, R_L = 6Ω	--	27	--	W
		THD + N = 1%, (BTL), PVDD = 18V, R_L = 6Ω	--	23	--	
Total Harmonic Distortion + Noise	THD+N	P_O =1W (BTL)	--	0.03	--	%
Output Integrated Noise	Vn	20Hz to 20kHz, A-weighted	--	35	--	μV
Output Offset Voltage	V_{OS}	PVDD = 12V	–6.5	--	6.5	mV
		PVDD = 24V	–6.5	--	6.5	
Cross-Talk	X_{TALK}	Output power = 1W, 1kHz with non-shielding choke	--	–75	--	dB
		Output power = 1W, 1kHz with shielding choke	--	–100	--	
Signal-to-Noise Ratio	SNR	PVDD = 24V, 1% THD + N, R_L = 4Ω	--	113	--	dB
Power Supply Rejection Ratio	PSRR	Frequency @ 1kHz with 200mVpp ripple	--	75	--	dB
Dynamic Range	DR	Input level –60dBFS	--	113	--	dB
Efficiency	η	PVDD = 18V, output power = 20W + 20W, load = 6Ω	--	94	--	%
		PVDD = 18V, output power = 1.25W + 1.25W, load = 6Ω (CMH mode)	--	70	--	
Over-Temperature Protection	OTP	Guaranteed by design	150	160	175	°C
Thermal Hysteresis			--	20	--	°C
Overcurrent Protection	OCP		6	7	--	A
PVDDL/PVDDR Overvoltage Protection	OVP		28	--	30	V
PVDDL/PVDDR Undervoltage Protection	UVP	Note: PVDD UVP can be programmed, the UVP threshold can be set from 4V to 20V. Refer to page 46 for detailed setting.	3.9	4	--	V
OLD	OLD		16	--	--	Ω
SLD	SLD		--	--	2	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PVDD Range (Note 10)	V	BTL, R = 4Ω (Note 11)	--	--	21	V
		BTL, R ≥ 5Ω (Note 11)	--	--	26.4	
		PBTL, R = 2Ω	--	--	21	
		PBTL, R ≥ 3Ω	--	--	26.4	
I²C Interface Electrical Characteristics						
High-Level Input Voltage (Belongs to the Internal 1.8V Domain)	V_{IH}		DVDD x 0.7	--	--	V
Low-Level Input Voltage (Belong to the Internal 1.8V Domain)	V_{IL}		--	--	DVDD x 0.3	V
Digital Output Low (SDA)	V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency	f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3	--	--	µs
Hold Time After (Repeated) Start Condition	$t_{HD;STA}$		0.6	--	--	µs
Repeated Start Condition Setup Time	$t_{SU;STA}$		0.6	--	--	µs
Stop Condition Time	$t_{SU;STD}$		0.6	--	--	µs
Input Data Hold Time	$t_{HD;DAT(IN)}$		0	--	900	ns
Data Setup Time	$t_{SU;DAT}$		100	--	--	ns
Clock Low Period	t_{LOW}		1.3	--	--	µs
Clock High Period	t_{HIGH}		0.6	--	--	µs
Clock Data Fall Time	t_F		20	--	300	ns
Clock Data Rise Time	t_R		20	--	300	ns
Spike Suppression Time	t_{SP}		--	--	20	ns
Slave Mode I²S Interface Electrical Characteristics						
High-Level Input Voltage	V_{IH}		DVDD x 0.7	--	--	V
Low-Level Input Voltage	V_{IL}		--	--	DVDD x 0.3	V
SDO High-Level Output Voltage	V_{OH}	--	DVDD x 0.7	--	--	V
SDO Low-Level Output Voltage	V_{OL}	--	--	0.4	--	V
High-Level Input Voltage	V_{IH}	DVDD = 1.8V	1.4	--	--	V
Low-Level Input Voltage	V_{IL}	DVDD = 1.8V	--	--	0.5	V
SDO High-Level Output Voltage	V_{OH}	--	DVDD x 0.7	--	--	
SDO Low-Level Output Voltage	V_{OL}	--	--	0.2	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Frequency	f_{SCLKIN}		1.024	--	12.288	MHz
Setup Time, LRCK to SCLK Rising Edge	t_{su1}		10	--	--	ns
Hold Time, LRCK from SCLK Rising Edge	t_{h1}		10	--	--	ns
Setup Time, SDIN to SCLK Rising Edge	t_{su2}		10	--	--	ns
Hold Time, SDIN from SCLK Rising Edge	t_{h2}		10	--	--	ns
Rise/Fall Time for SCLK/LRCK	t_{RS}/t_{FS}		--	--	10	ns
I^2S Duty Cycle	%		40	--	60	%

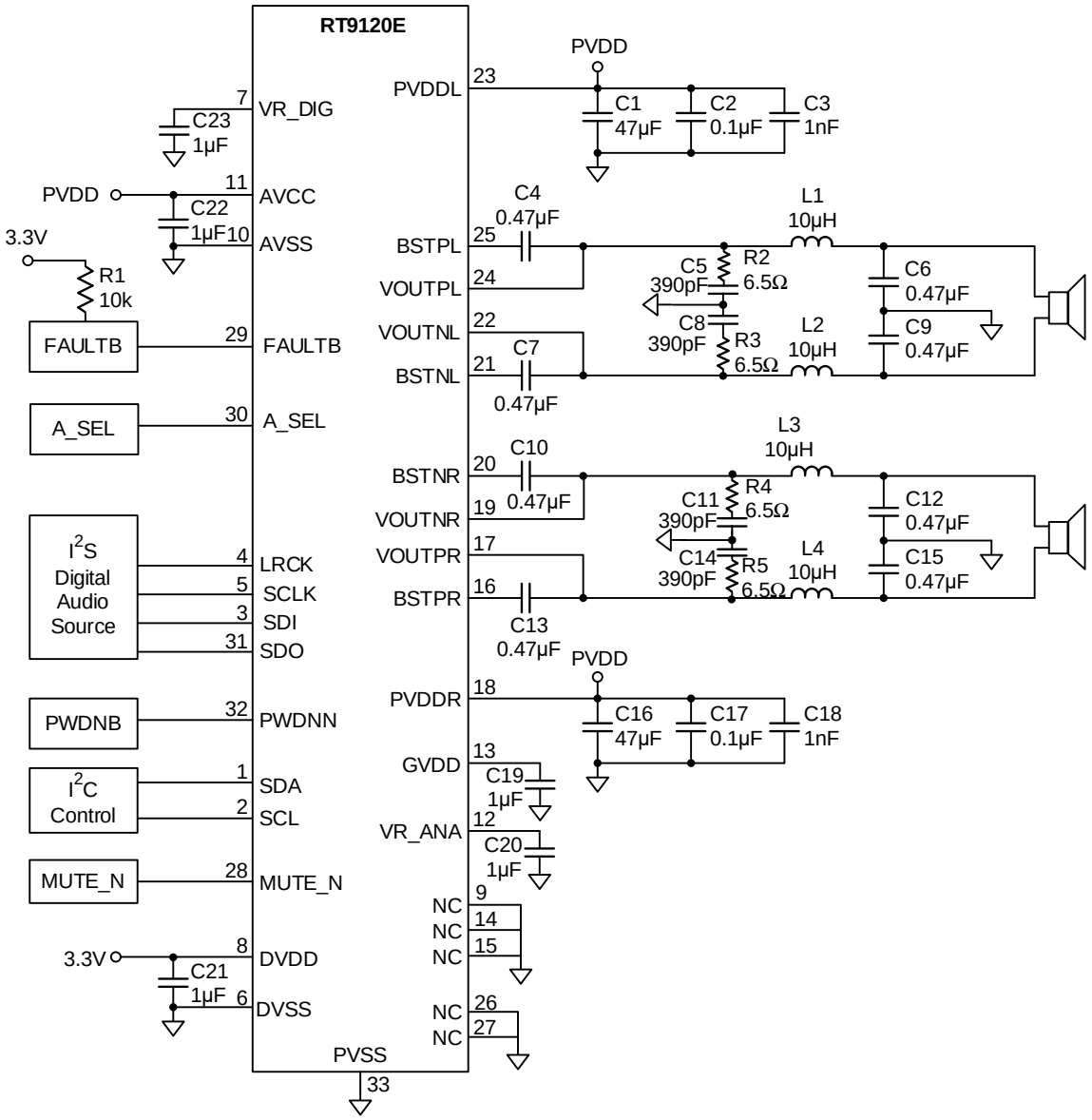
Note 9. Measurements were made using the RT9120E_EVM board and Audio Precision System 2722 with AUX-0025 low-pass filter.

Note 10. If the maximum output power not exceed the OCP value, there is no need to consider the minimum load.

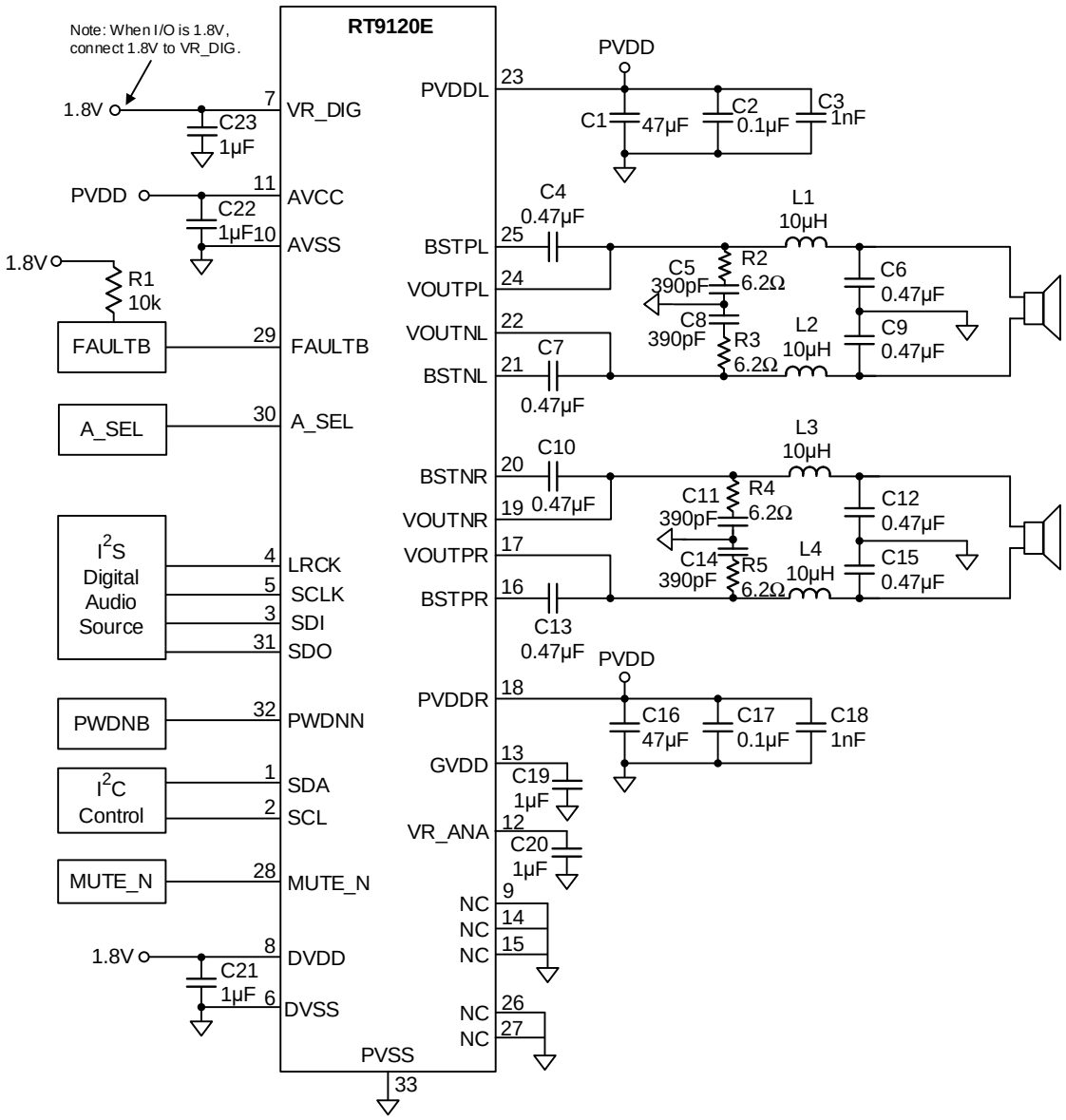
Note 11. Add snubber if output power is over 15W for 4Ω, or 25W for 6Ω. Snubber circuit refers to page 12 to page 15.

13 Typical Application Circuit

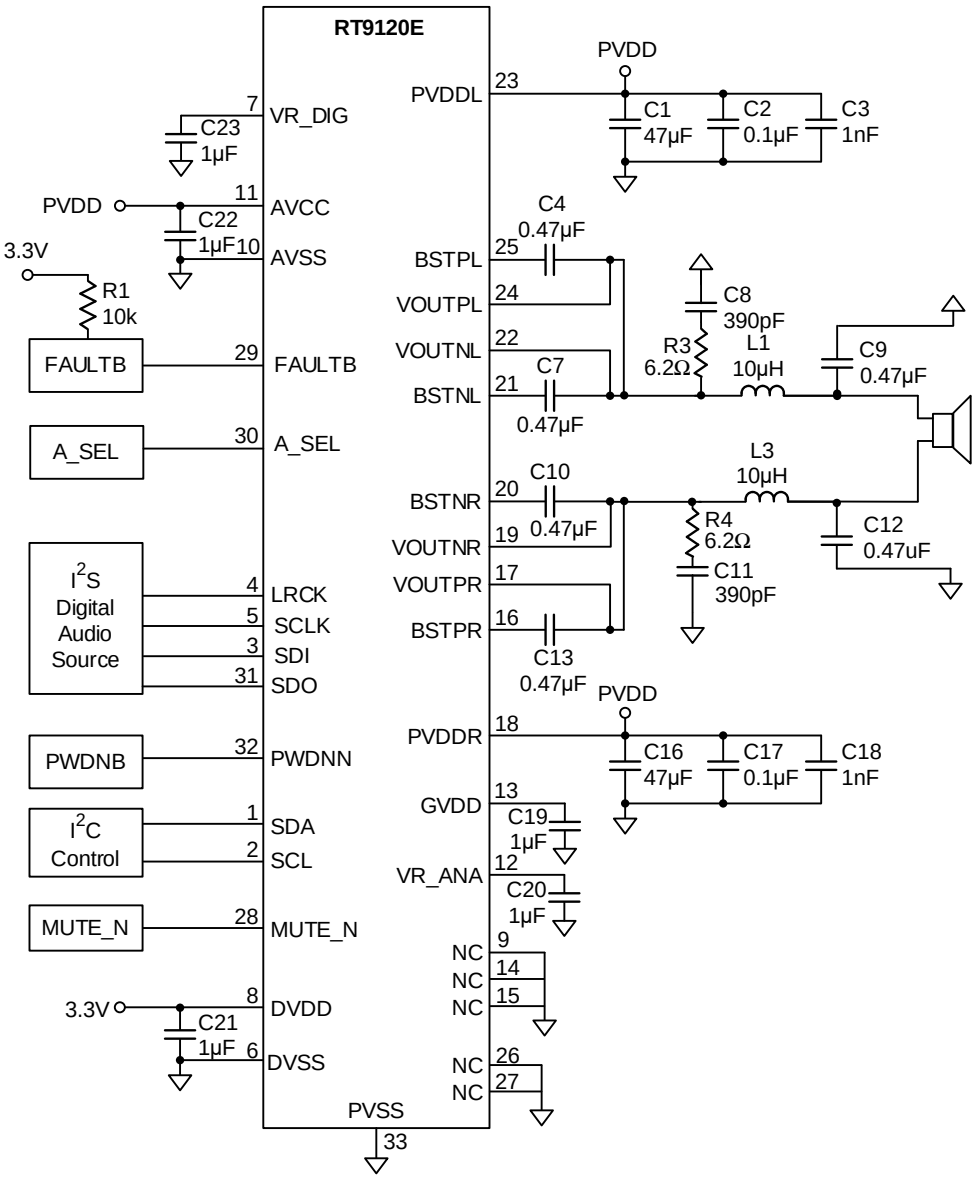
13.1 3.3V I/O Application (BTL)



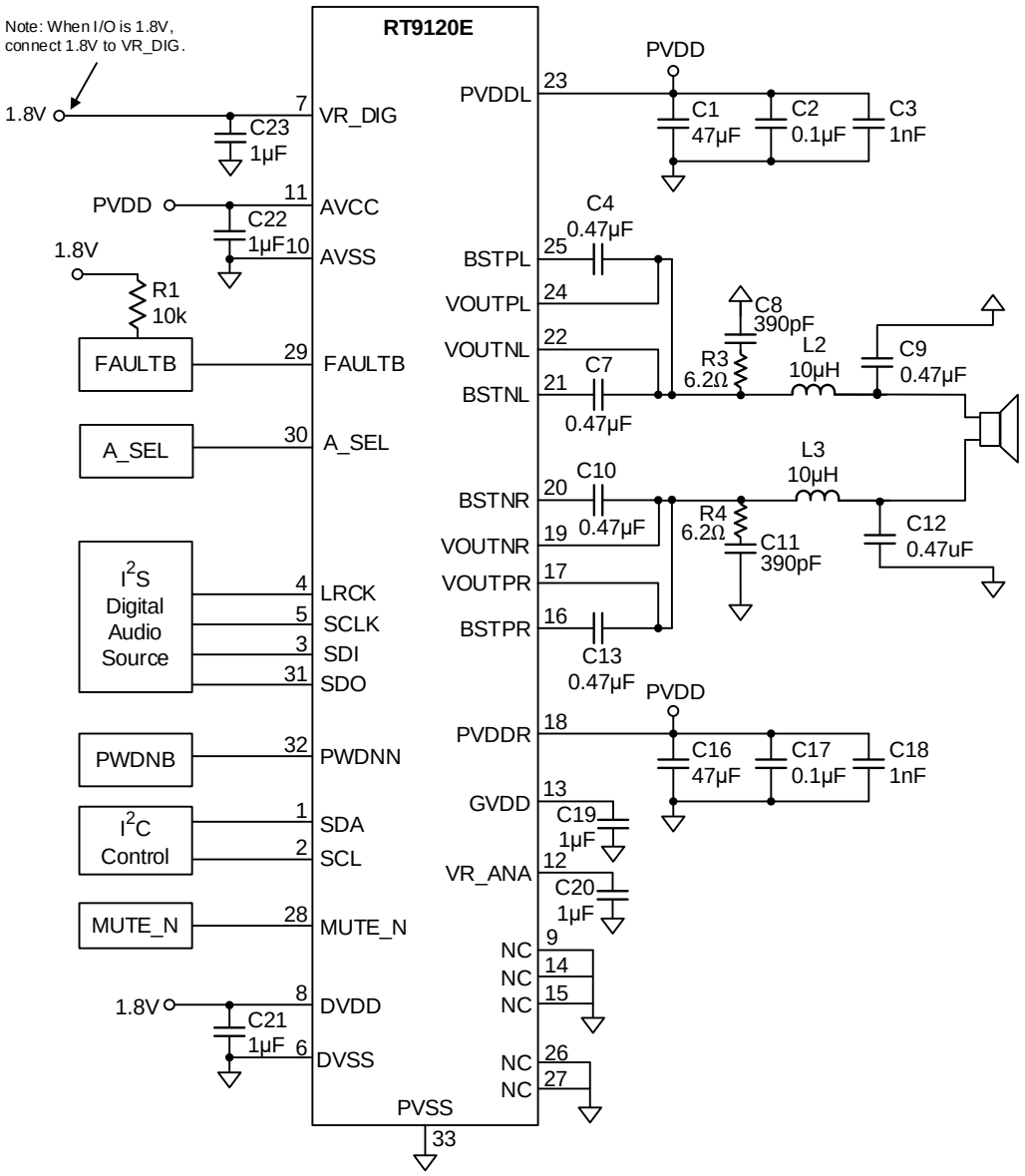
13.2 1.8V I/O Application (BTL)



13.3 3.3V I/O Application (PBTL)



13.4 1.8V I/O Application (PBTL)



14 Timing Diagram

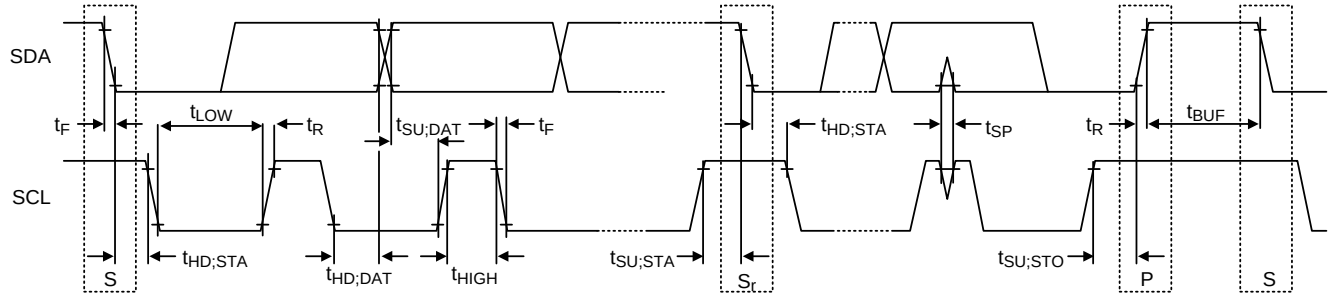


Figure 1. I²C Interface Timing Diagram

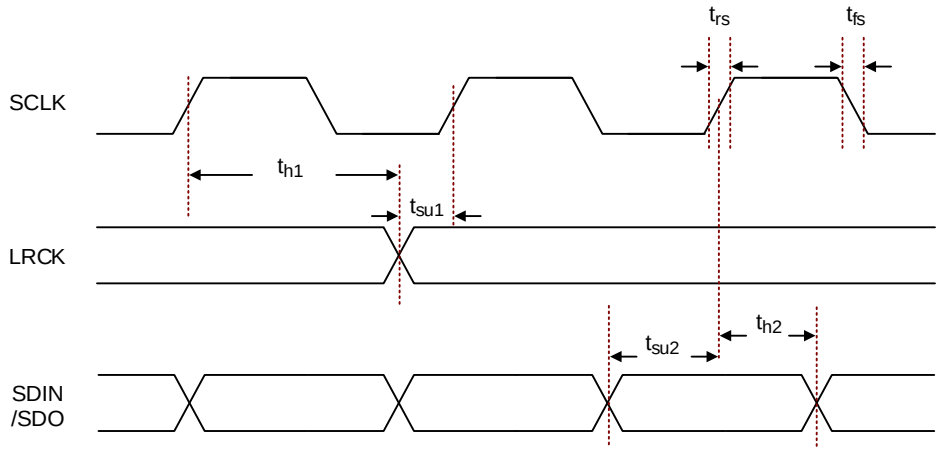
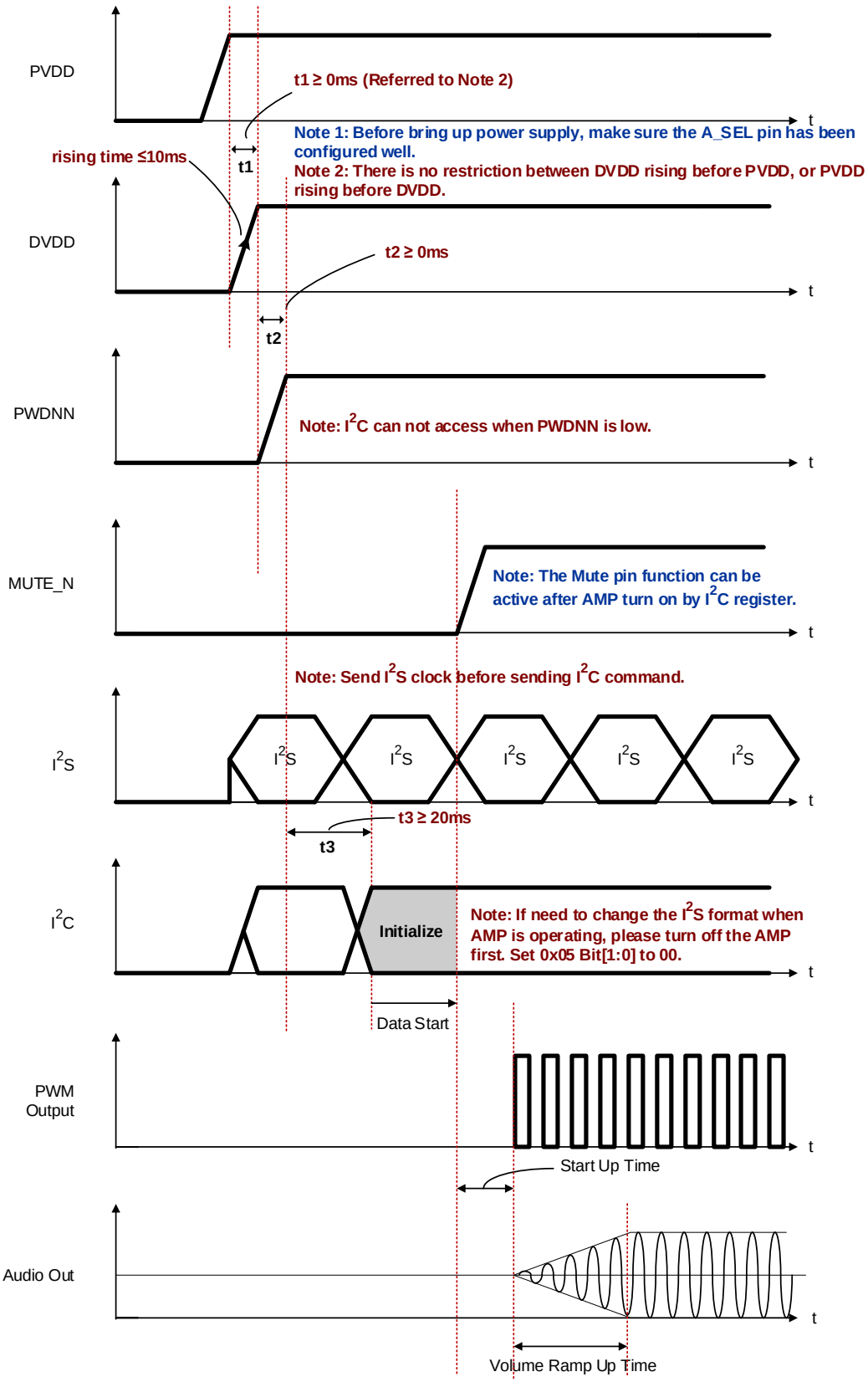


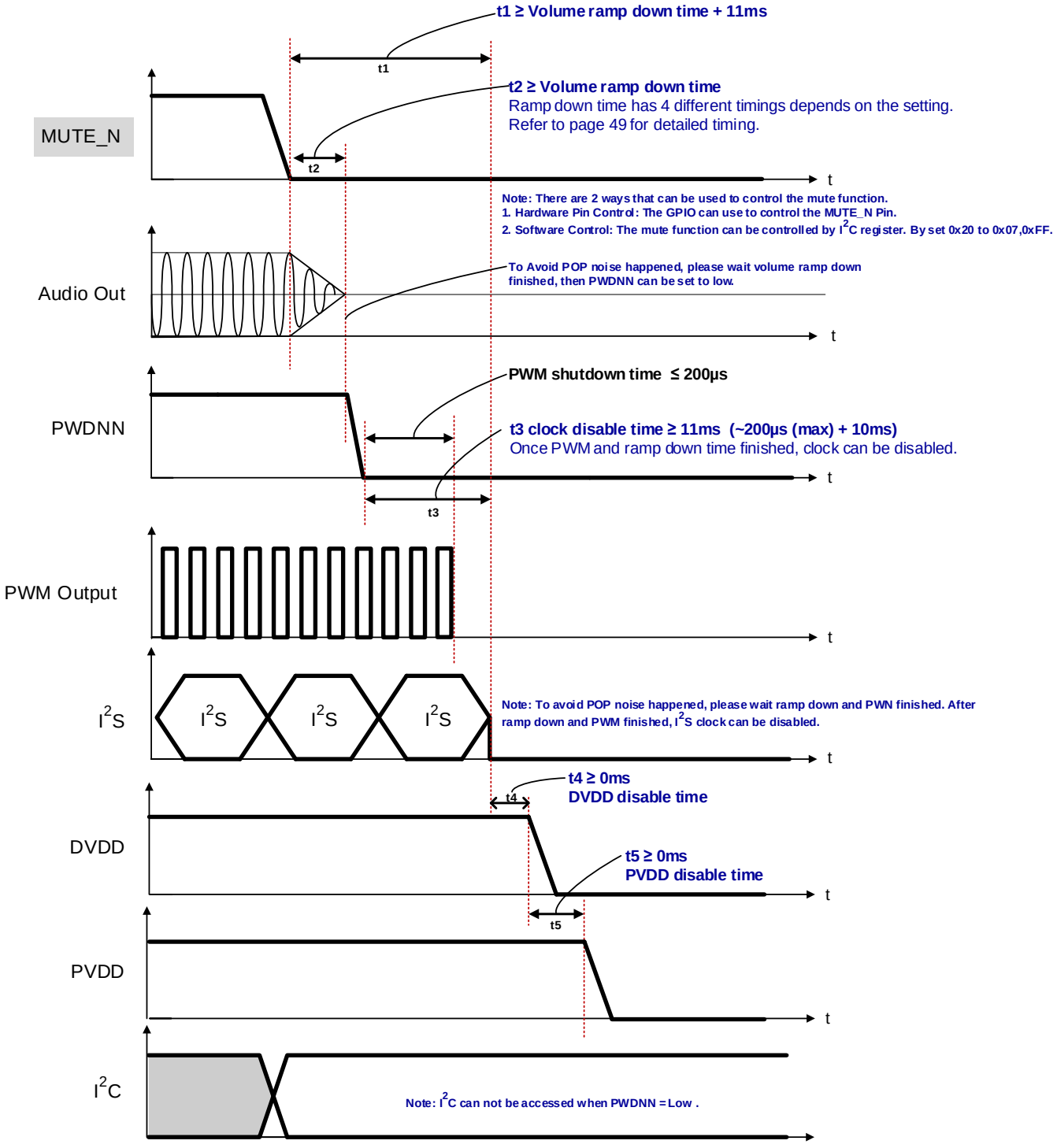
Figure 2. Timing Diagram of Slave Mode I²S Interface

14.1 Power-On Sequence



14.2 Power-Off Sequence (1)

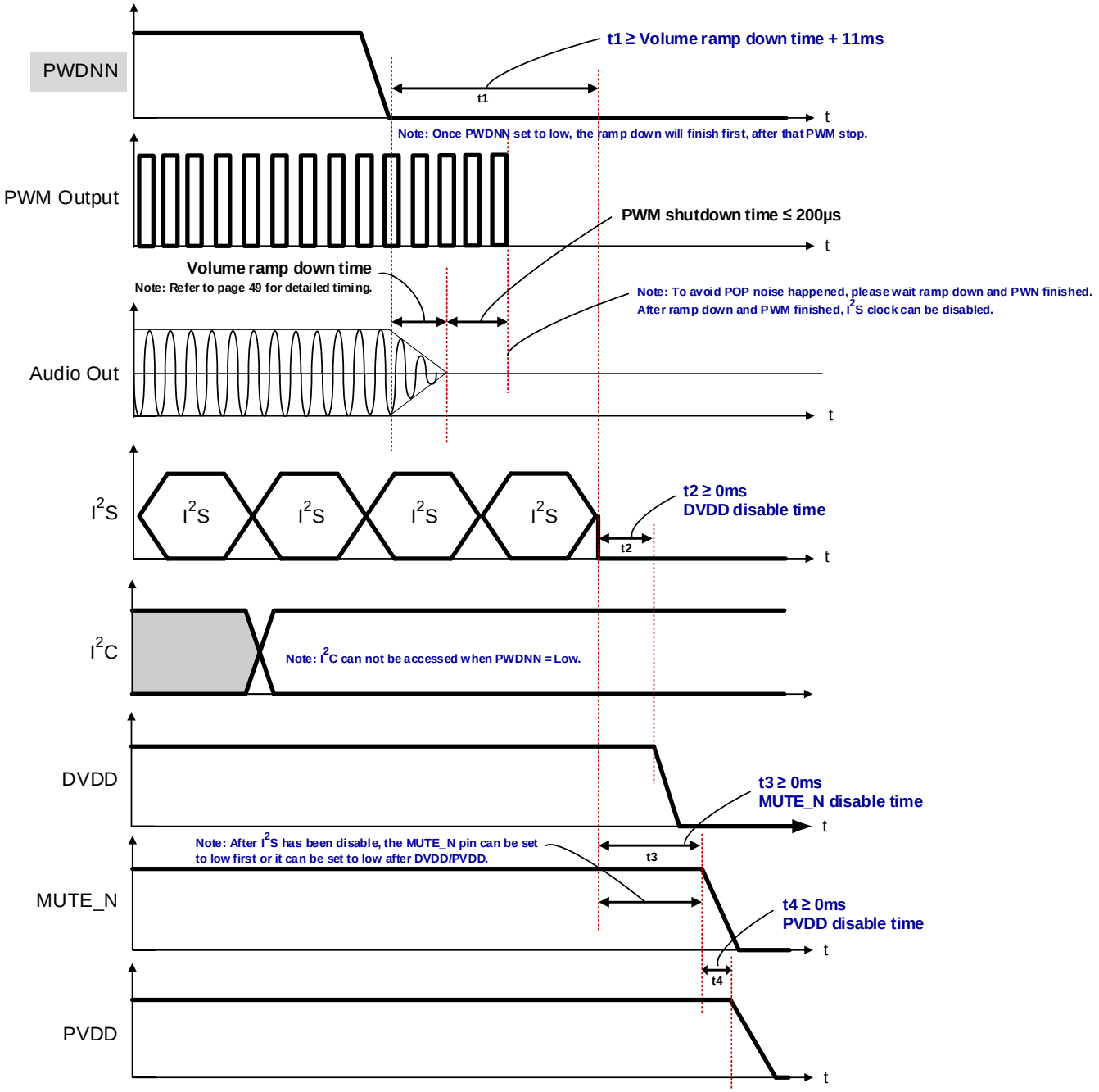
Control flow is: MUTE_N → Ramp down finished → EN → PWM → I²S Clock → DVDD/PVDD



Note 12. Exactly follow up the t1 to t5 timing sequence. Any violate the t1 to t5 timing sequence is not allowable. For the AC off, also follow up the t1 to t5 sequence.

14.3 Power-Off Sequence (2)

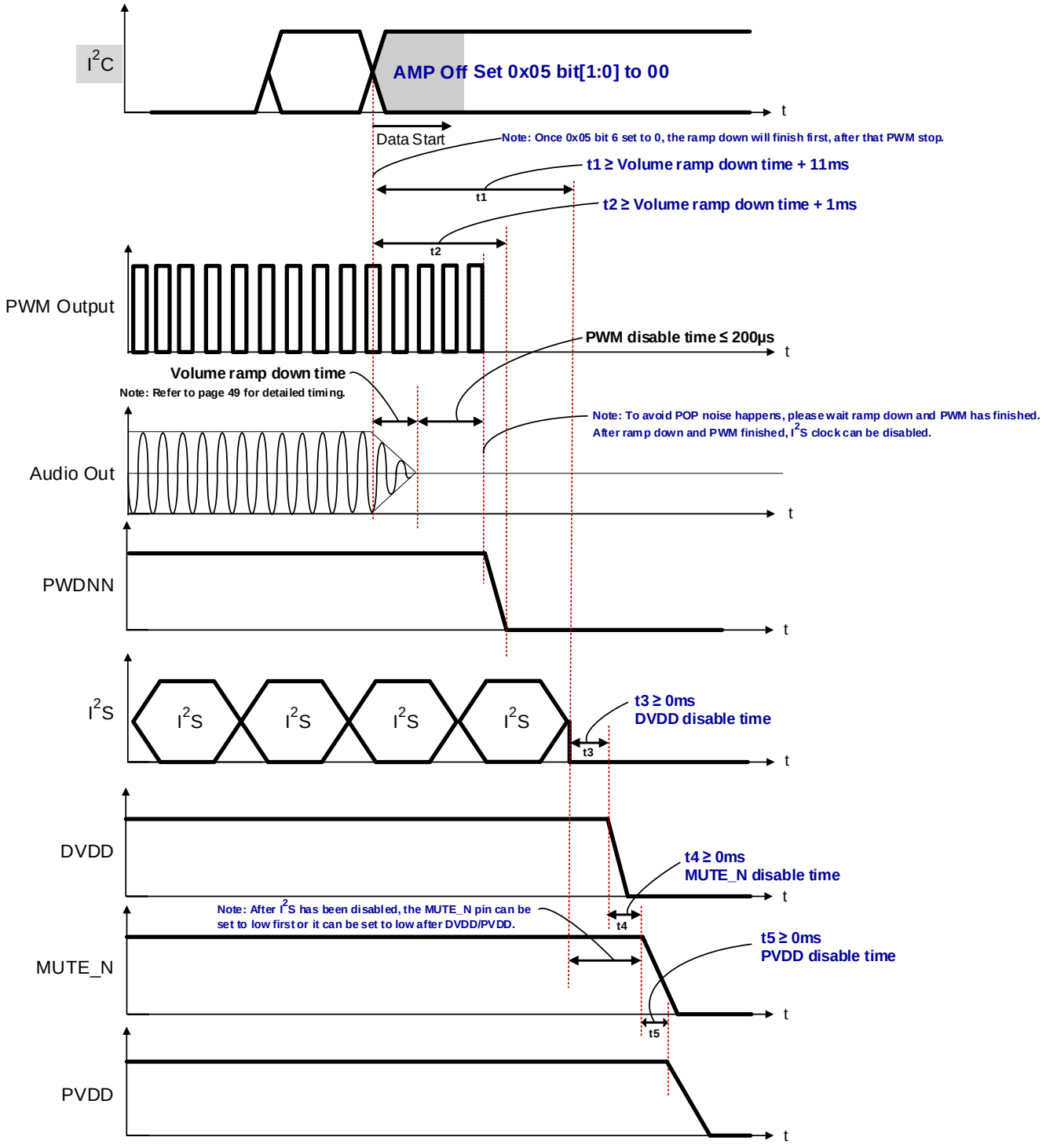
Control flow is: PWDNN → Ramp down and PWM finished → I²S Clock → DVDD/PVDD



Note 13. Exactly follow up the t1 to t4 timing sequence. Any violate the t1 to t4 timing sequence is not allowable. For the AC off, also follow up the t1 to t4 sequence.

14.4 Power-Off Sequence (3)

Control flow is: By using I²C to set AMP off → Ramp down finished → I²S Clock → DVDD/PVDD



Note 14. Exactly follow up the t1 to t5 timing sequence. Any violate the t1 to t5 timing sequence is not allowable. For the AC off, also follow up the t1 to t5 sequence.

14.5 Initial Sequence (BTL Mode)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x64	1	0xA9	Internal setting	
2	0x07	1	0x17	Analog gain (optional)	
3	0x65	1	0x33	Internal setting	
4	0x95	1	0xD0	Internal setting	
5	0x94	1	0x65	CMH threshold	
6	0x6C	1	0xC0	DVDD = 1.8V, Set 0x6C to 0xC0. DVDD = 3.3V, Keep default value.	
7	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
8	0x05	1	0xE1	Amp turn on (PWM is 384kHz)	Amp turn on
9	0x05	1	0xE5	Amp turn on (PWM is 768kHz)	Amp turn on

14.6 Initial Sequence (PBTL Mode)

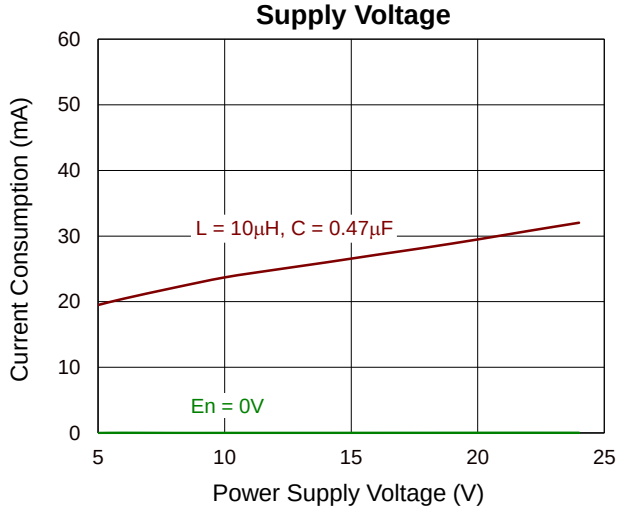
Sequence	reg_addr	reg_size	reg_value	Description	
1	0x64	1	0xA9	Internal setting	
2	0x07	1	0x17	Analog gain (optional)	
3	0x65	1	0x33	Internal setting	
4	0x95	1	0xD0	Internal setting	
5	0x94	1	0x6C	CMH threshold	
6	0x6C	1	0xC0	DVDD = 1.8V, Set 0x6C to 0xC0. DVDD = 3.3V, Keep default value.	
7	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
8	0x30	3	0x01, 0xC0, 0x07	Set input mixing = L/2+R/2 for mono mode	
9	0x31	3	0x01, 0xC0, 0x07		
10	0x05	1	0xF1	Set to PBTL and Amp turn on (PWM is 384kHz)	Amp turn on
11	0x05	1	0xF5	Set to PBTL and Amp turn on (PWM is 768kHz)	Amp turn on

15 Typical Operating Characteristics

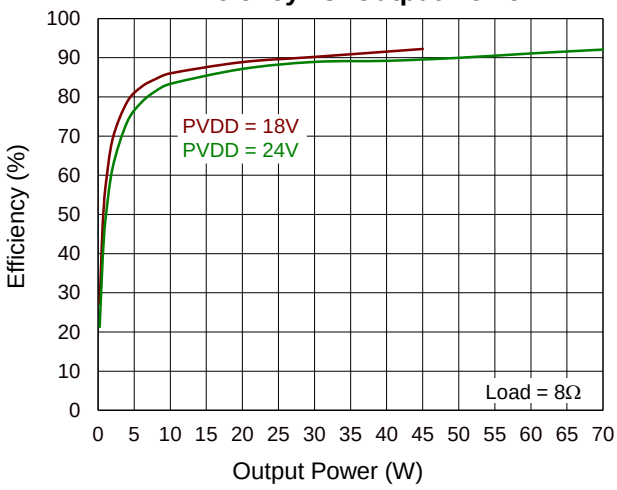
15.1 Bridge-Tied Load (BTL)

PWM = 768kHz

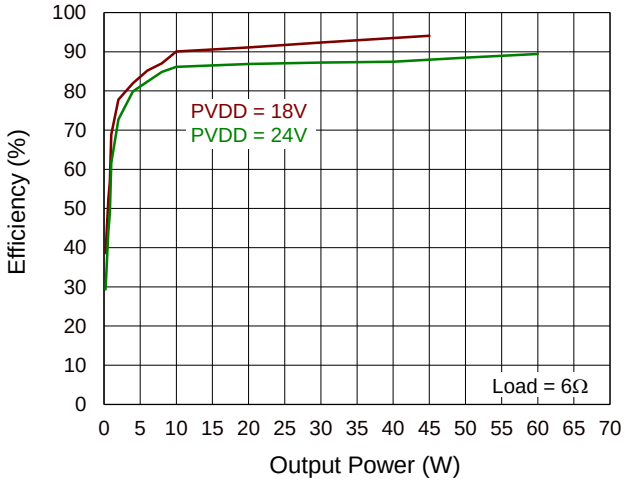
Current Consumption vs. Power Supply Voltage



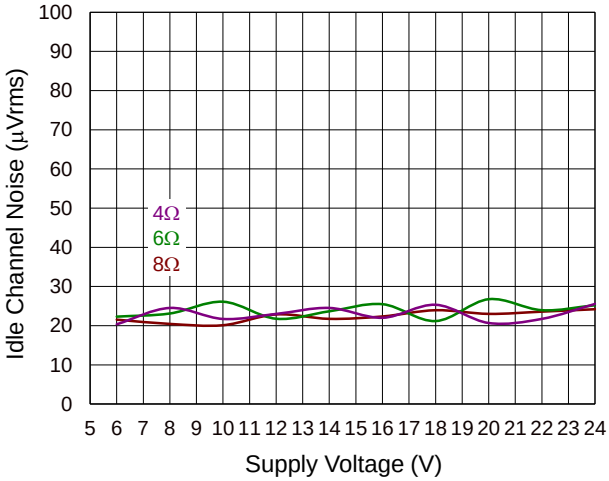
Efficiency vs. Output Power



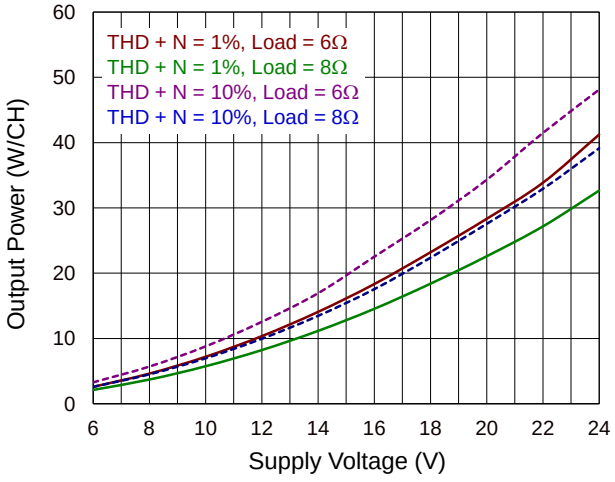
Efficiency vs. Output Power



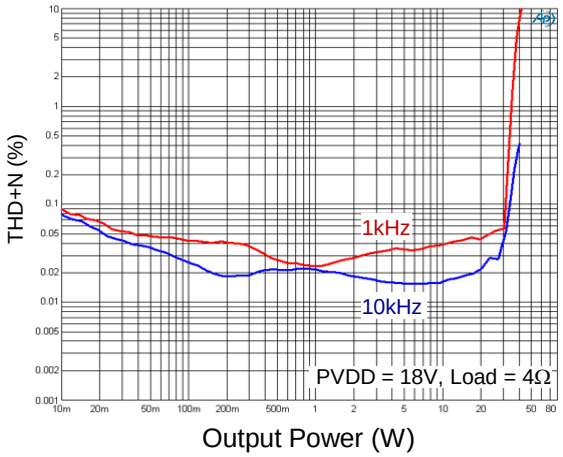
Idle Channel Noise vs. Supply Voltage



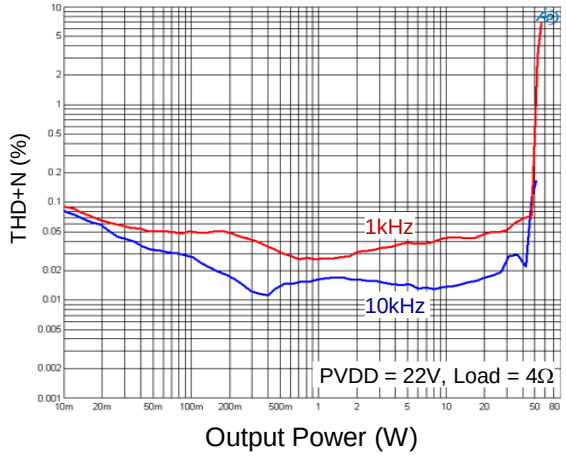
Output Power vs. Supply Voltage



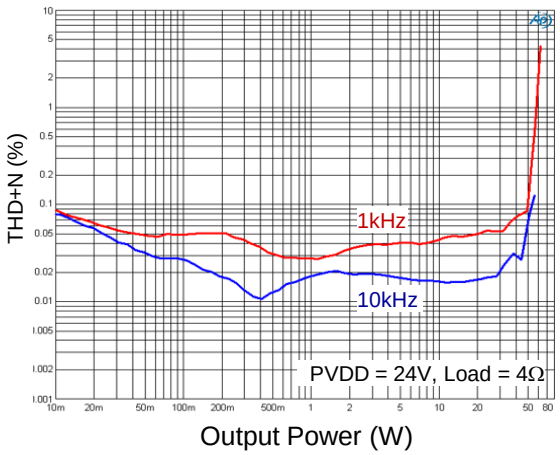
THD + N vs. Output Power (BTL)



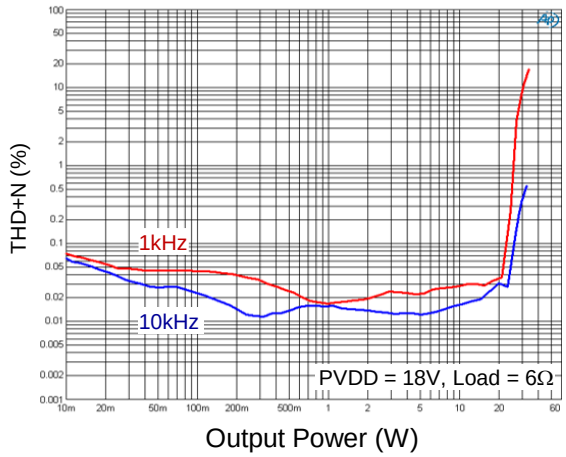
THD + N vs. Output Power (BTL)



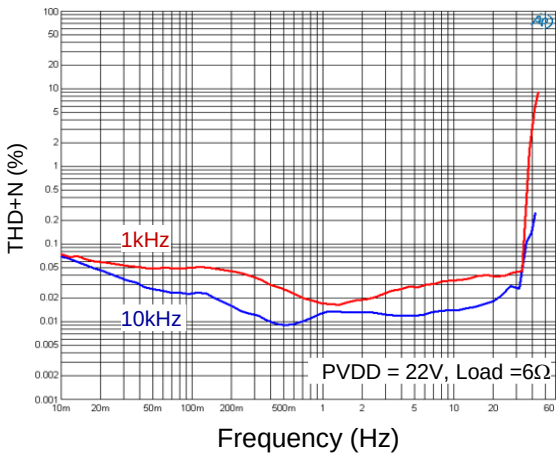
THD + N vs. Output Power (BTL)



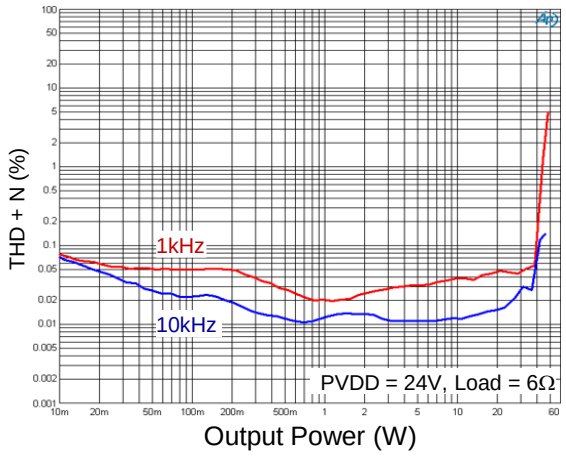
THD + N vs. Output Power (BTL)



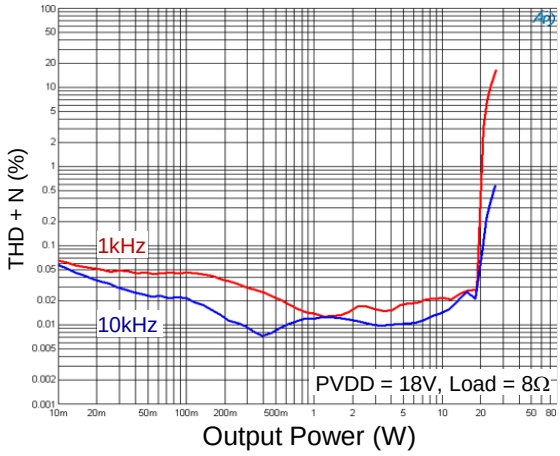
THD + N vs. Output Power (BTL)



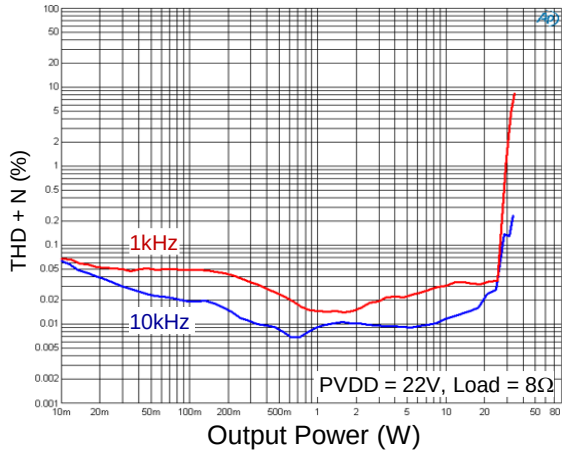
THD + N vs. Output Power (BTL)



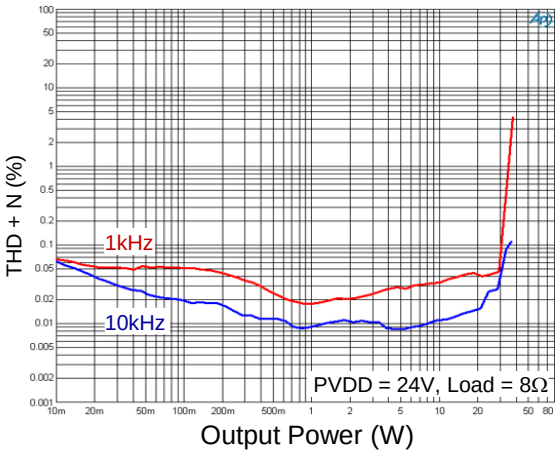
THD + N vs. Output Power (PBTL)



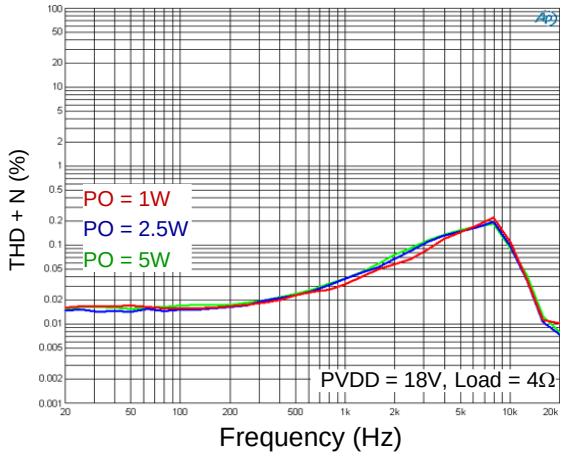
THD + N vs. Output Power (BTL)



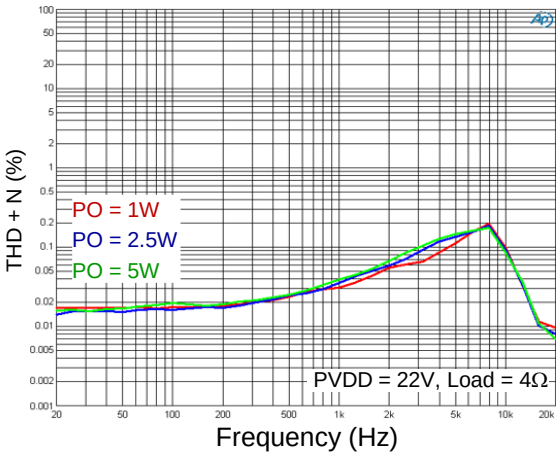
THD + N vs. Output Power (BTL)



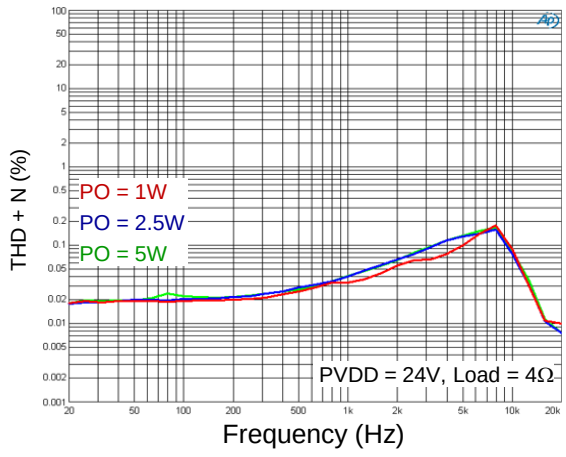
THD + N vs. Frequency (BTL)



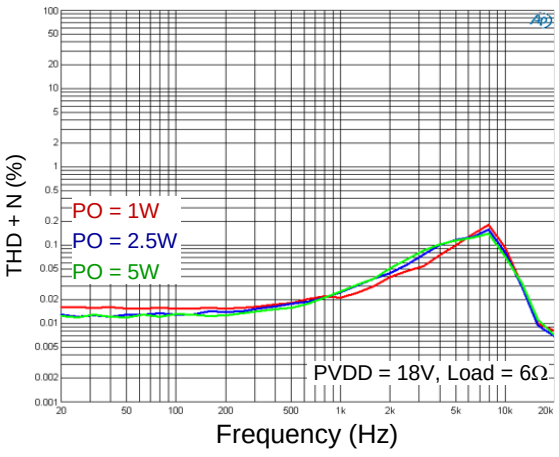
THD + N vs. Frequency (BTL)



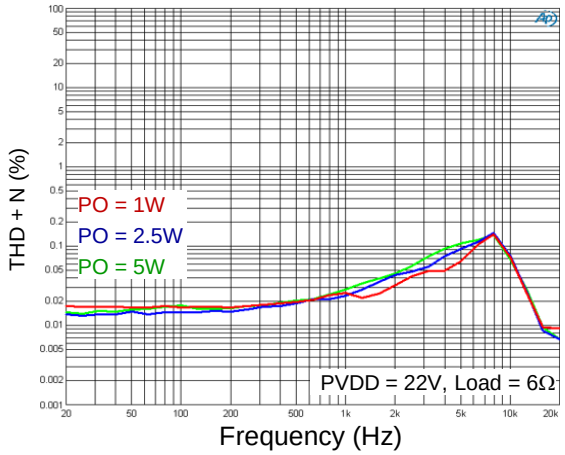
THD + N vs. Frequency (BTL)



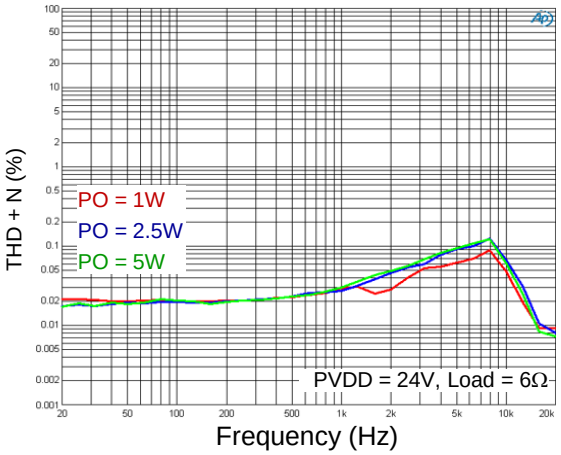
THD + N vs. Frequency (BTL)



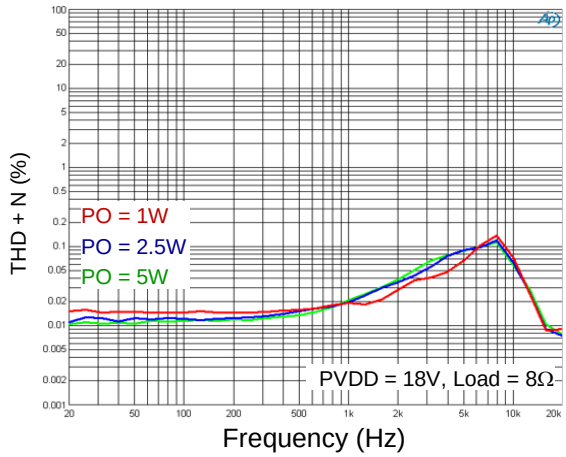
THD + N vs. Frequency (BTL)



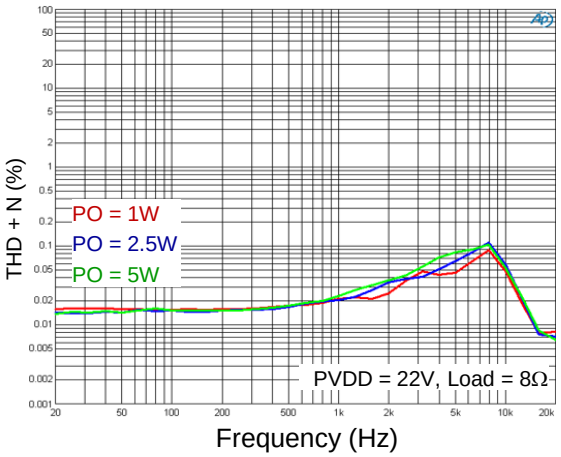
THD + N vs. Frequency (BTL)



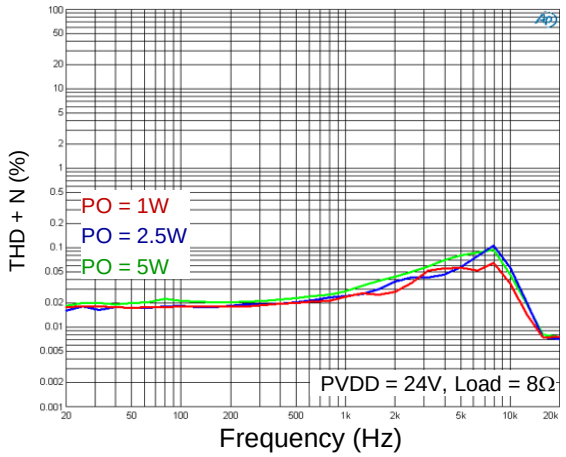
THD + N vs. Frequency (BTL)



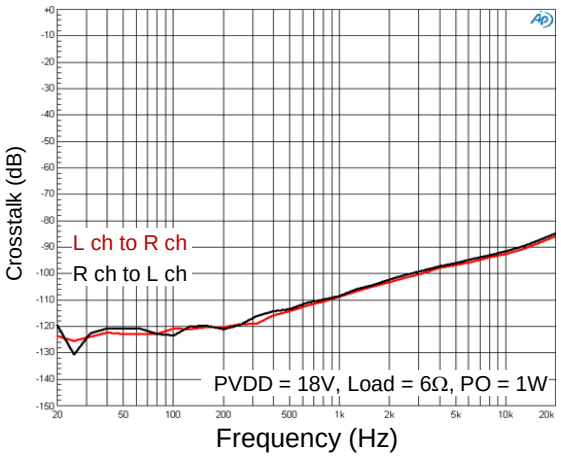
THD + N vs. Frequency (BTL)



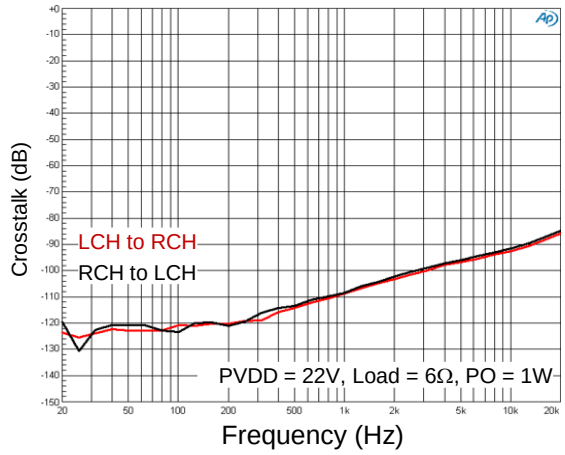
THD + N vs. Frequency (BTL)



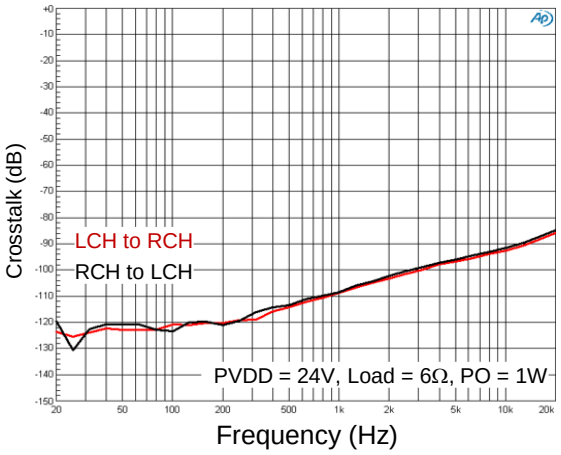
Crosstalk vs. Frequency (BTL)



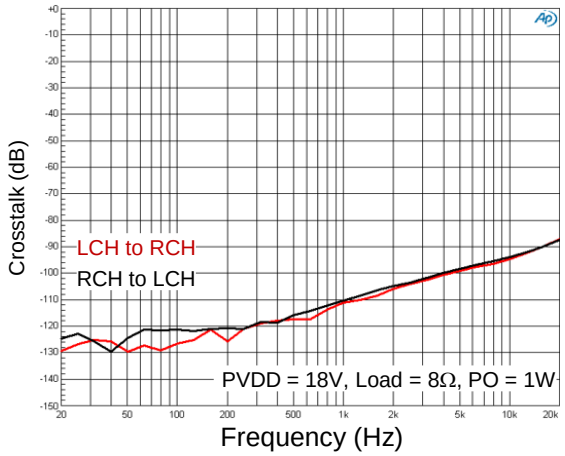
Crosstalk vs. Frequency (BTL)



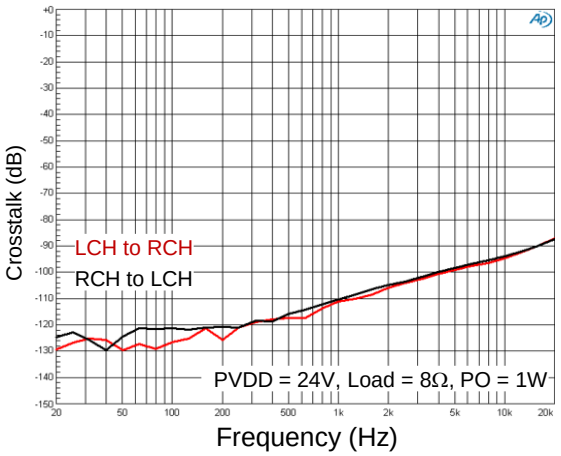
Crosstalk vs. Frequency (BTL)



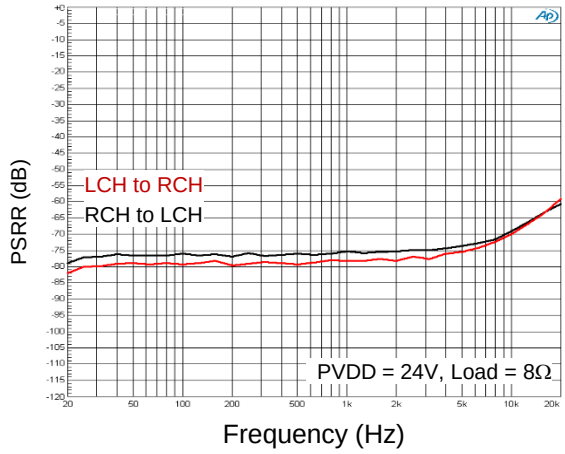
Crosstalk vs. Frequency (BTL)



Crosstalk vs. Frequency (BTL)



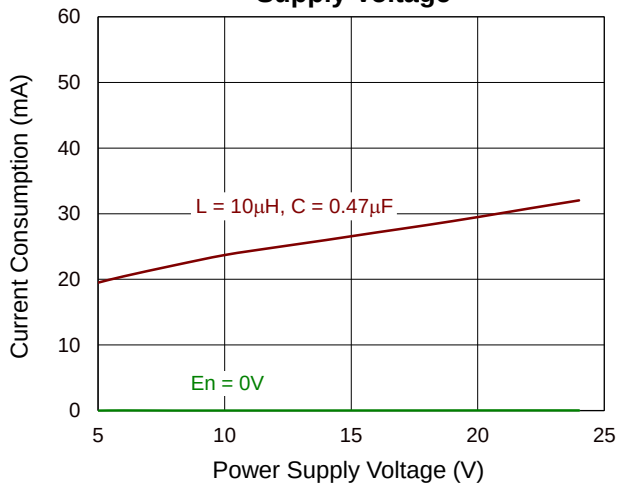
PSRR vs. Frequency (BTL)



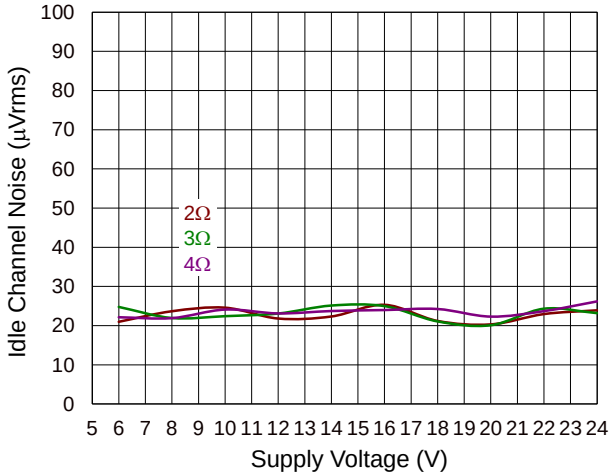
15.2 Parallel Bridge-Tied Load (PBTL)

PWM = 768kHz

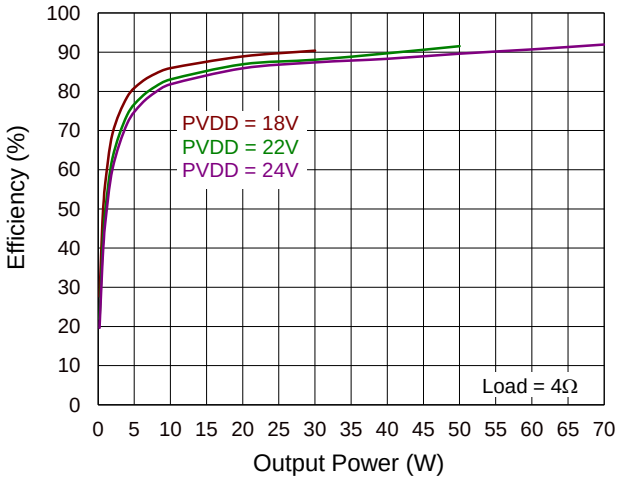
Current Consumption vs. Power Supply Voltage



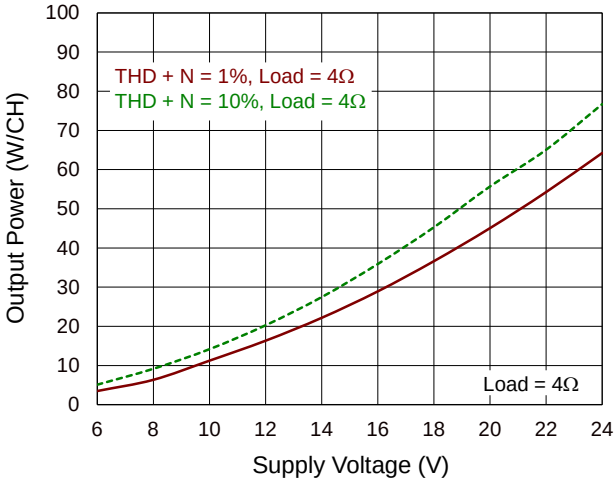
Idle Channel Noise vs. Supply Voltage



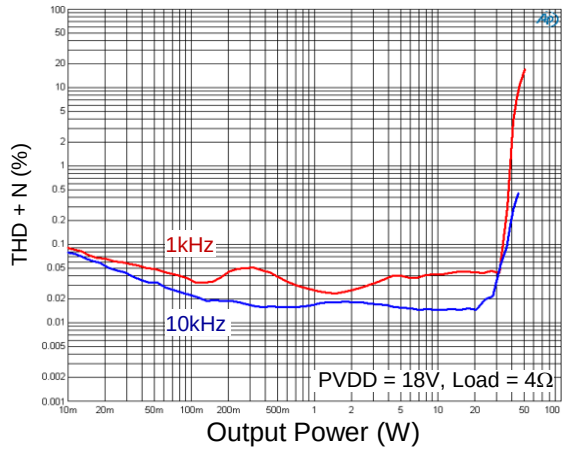
Efficiency vs. Output Power



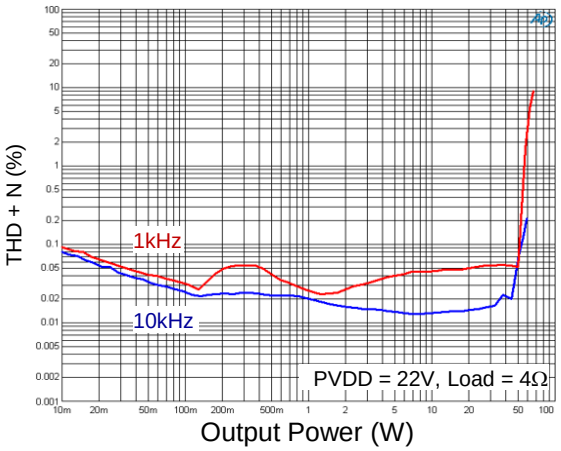
Output Power vs. Supply Voltage



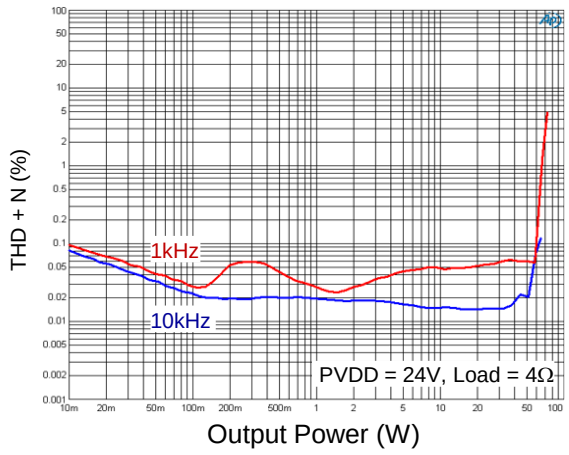
THD + N vs. Output Power (PBTL)



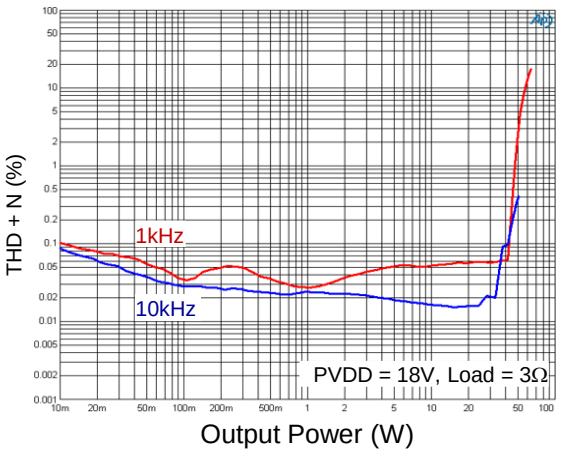
THD + N vs. Output Power (PBTL)



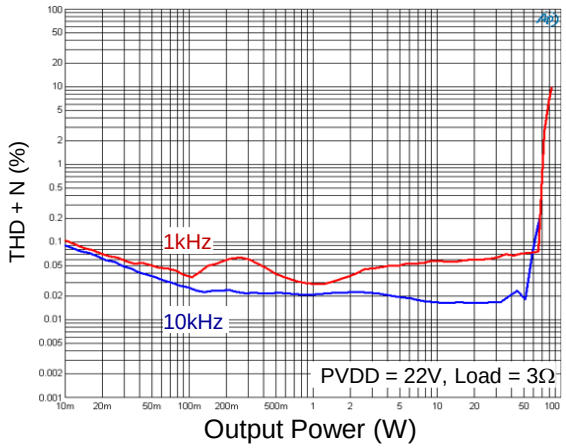
THD + N vs. Output Power (PBTL)



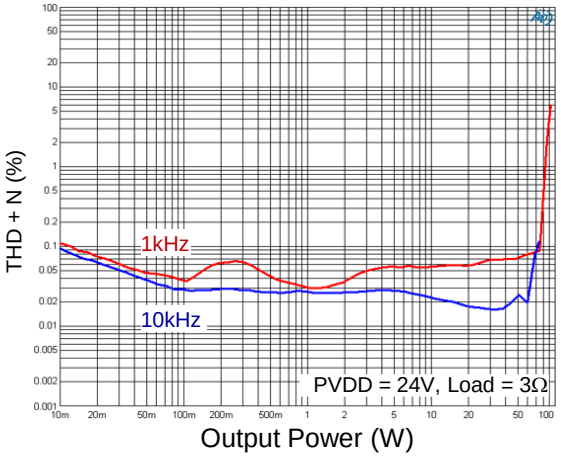
THD + N vs. Output Power (PBTL)



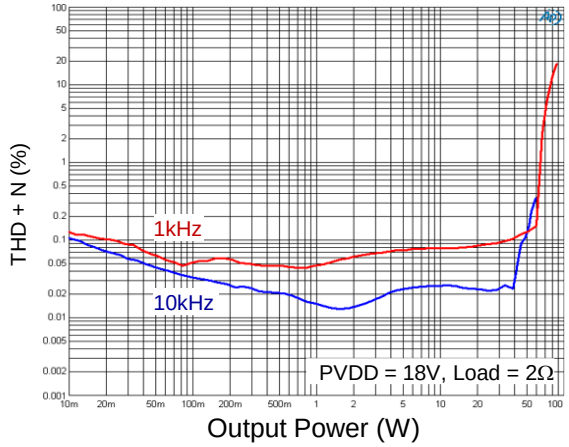
THD + N vs. Output Power (PBTL)



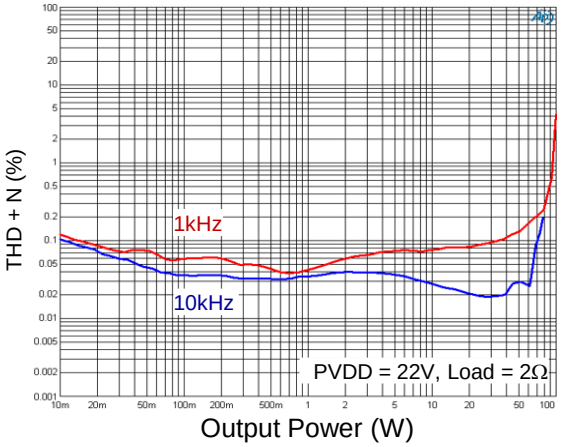
THD + N vs. Output Power (PBTL)



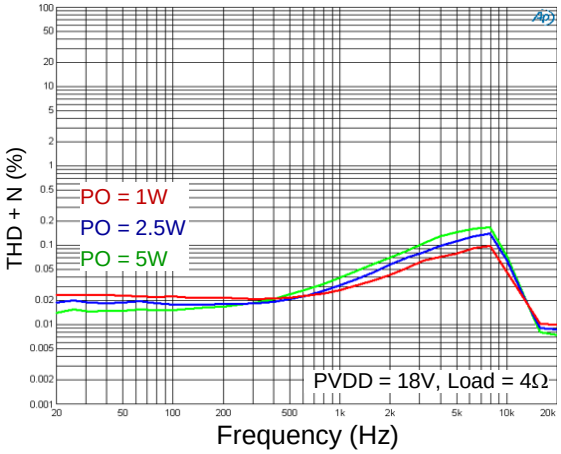
THD + N vs. Output Power (PBTL)



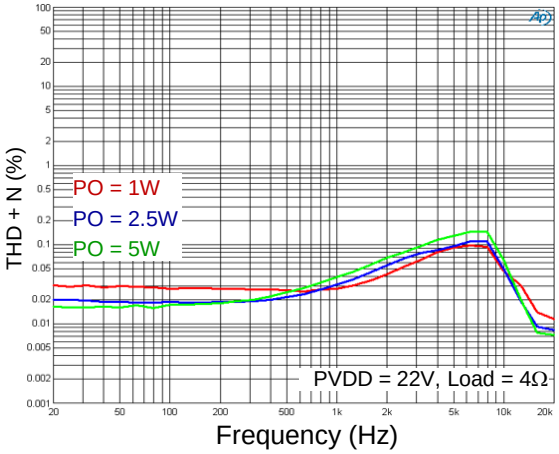
THD + N vs. Output Power (PBTL)



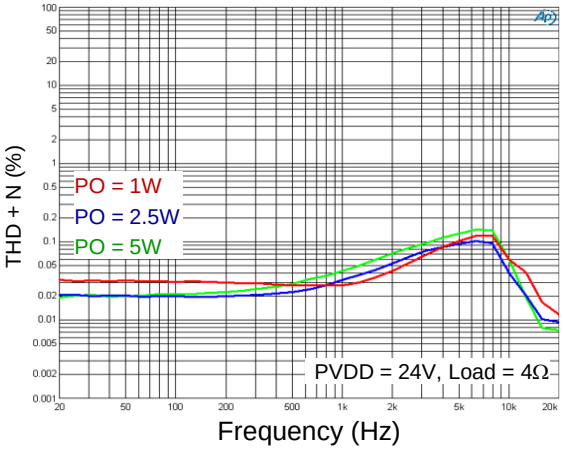
THD + N vs. Frequency (PBTL)



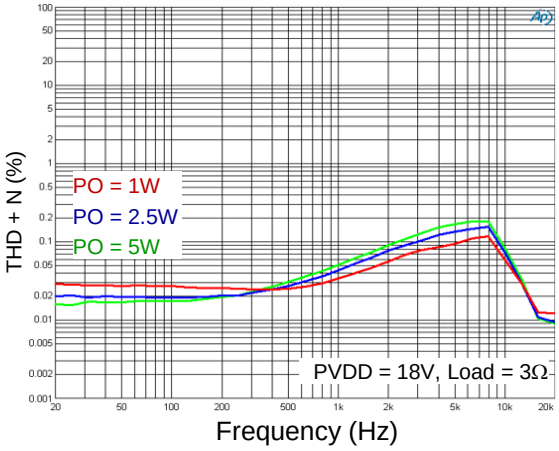
THD + N vs. Frequency (PBTL)



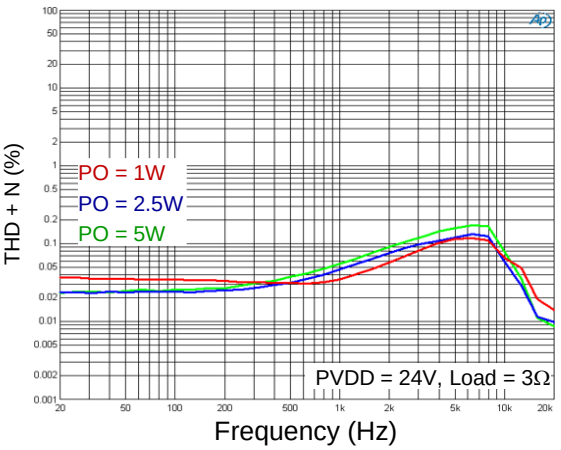
THD + N vs. Frequency (PBTL)



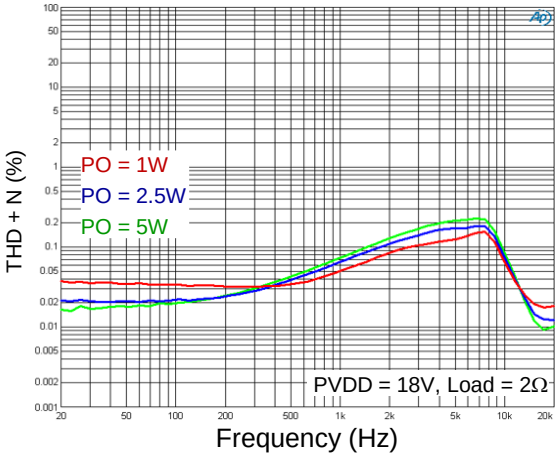
THD + N vs. Frequency (PBTL)



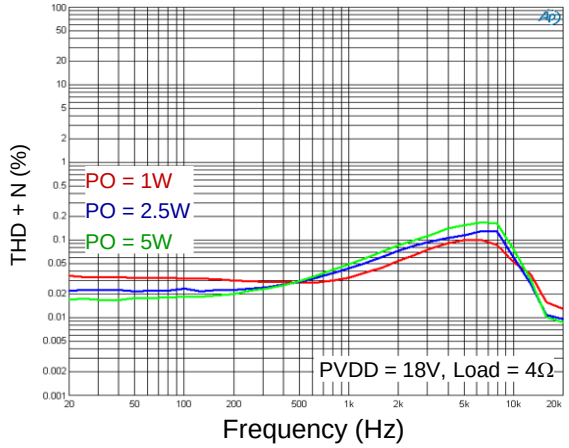
THD + N vs. Frequency (PBTL)



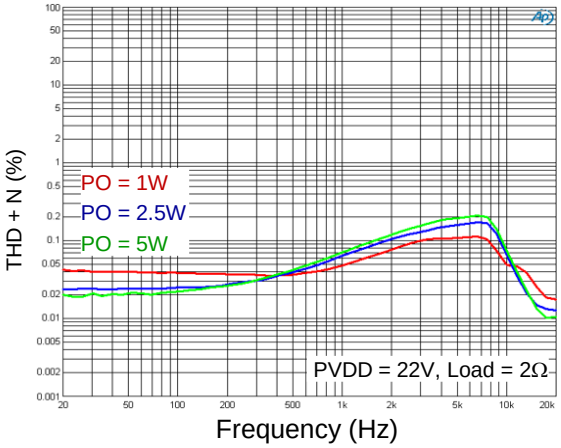
THD + N vs. Frequency (PBTL)



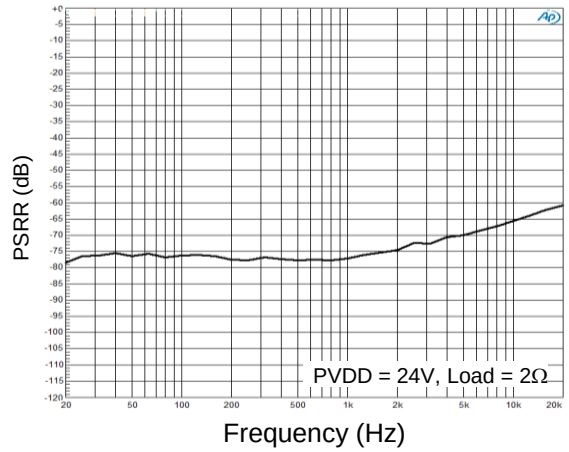
THD + N vs. Frequency (PBTL)



THD + N vs. Frequency (PBTL)



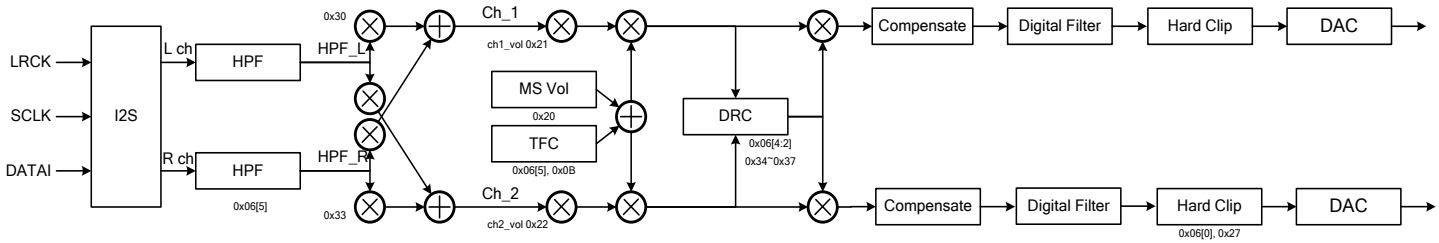
PSRR vs. Frequency (PBTL)



Note 15. Measurements were made using the RT9120E_EVM board and Audio Precision System 2722 with AUX0025 low-pass filter. All measurements taken with 1kHz.

Note 16. Measurements were made using the initial setting listed at page 21.

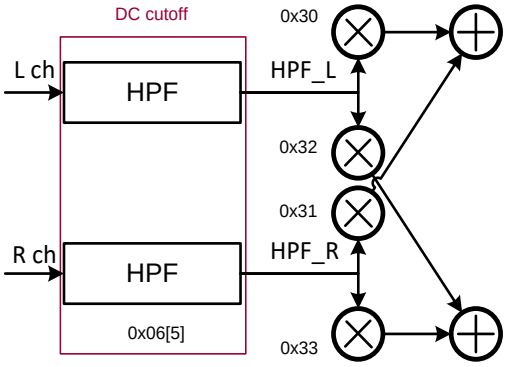
16 Signal Path



16.1 Input High Pass Filter

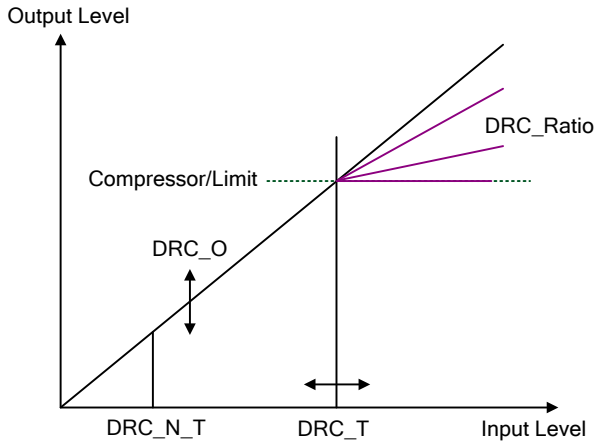
Block Diagram and Description

→There are DC-Cut filter for each output filter. The cut off frequency is 1.5Hz



Address	BITS	Name	Description
0x06	5	HPF_EN	0: Input high pass filter disable 1: Input high pass filter enable

16.2 DRC

DRC Description	Address	Description
DRC_T: Threshold	0x23	
DRC_RATIO: Compress ratio	0x24	
DRC_O: Make up gain	0x25	
DRC_N_T: Noise gate threshold	0x26	
Noise gate enable	0x06	

16.2.1 DRC Enable

Address	BITS	Name	Description
0x06	2	DRC_EN	0: DRC disable 1: DRC enable

16.2.2 DRC Noise Gate Enable

Address	BITS	Name	Description
0x06	1	DRC_N_EN	0: DRC Noise gate disable 1: DRC Noise gate enable

16.2.3 DRC Control

Address	BITS	Name	Description
0x23	10:0	DRC_TH[10:0]	TH[10:0], DRC threshold
0x24	7:0	DRC_RATIO[7:0]	RATIO[7:0] DRC compression ratio
0x25	10:0	DRC_O[10:0]	O[10:0] DRC make up gain
0x26	10:0	DRC_N_T[10:0]	N_T[10:0] DRC Noise gate of the DRC

16.2.4 DRC Timing

Address	BITS	Name	Description
0x34	16:0	DRC_AE[16:0]	DRC_AE[16:0], DRC energy estimator
0x35	16:0	DRC_1_AE[16:0]	DRC_1_AE[16:0], DRC energy estimator (release) (Note: When set to peak mode, this value need to adjust)
0x36	16:0	DRC_AD[16:0]	DRC_AD[16:0] DRC release time
0x37	16:0	DRC_AA[16:0]	DRC_AA[16:0] DRC attack time

16.2.5 DRC Timing Equation

<table>
<tr><th>DRC Description</th><th>Equation</th></tr>
<tr><td>AA/AE/AD/1-AE Timing Equation</td><td>
Equation: AA = $(1-e^{-2.2/(ta*fs)}) \times 2^{15}$
ta = AA/AD/AE timing,
fs = sampling rate
For example: ta = 0.15ms, fs = 48k
AA = $(1-e^{-2.2/(0.00015*48000)}) \times 2^{15} = 8627.352$
DEC = 8627
HEX = 0x21B3
<table>
<tr><th>Threshold</th><th>T_Dec</th><th>T_Hex</th></tr>
<tr><td>0.15ms</td><td>8627</td><td>0x21B3</td></tr>
<tr><td>.
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<tr><td>400ms</td><td>3.75</td><td>0x3</td></tr>
<tr><td>.
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</table>
Note: For the different Sampling Rate, the maximum timing will be
<table>
<tr><th>f_S (Sampling Rate)</th><th>Maximum Time (Unit: s)</th></tr>
<tr><td>192kHz</td><td>0.375</td></tr>
<tr><td>96kHz</td><td>0.750</td></tr>
<tr><td>48khz</td><td>1.500</td></tr>
<tr><td>32kHz</td><td>2.250</td></tr>
<tr><td>24kHz</td><td>3.000</td></tr>
<tr><td>16kHz</td><td>4.500</td></tr>
<tr><td>12kHz</td><td>6.000</td></tr>
<tr><td>8kHz</td><td>9.000</td></tr>
</table>
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<table>
<tr><th>DRC Description</th><th>Equation</th></tr>
<tr><td>DRC_T: Threshold</td><td>T is the threshold of the DRC
Equation: T = −(Threshold)/0.0625 (dB)
For example: T = −10dB,
−(−10)/0.0625 = 160
T_Dec = 160
T_Hex = DEC2HEX (160) = 0xA0
<table><tr><th>Threshold</th><th>T_Dec</th><th>T_Hex</th></tr><tr><td>-10dB</td><td>160</td><td>0xA0</td></tr><tr><td>.
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<tr><td>DRC_Ratio: Compression Ratio</td><td>K is the compression ratio of the DRC
Equation: K_Hex= DEC2HEX (Ratio_Value)
For example: If compression Ratio is 50%
• The Ratio_Value is 128^0.5 = 64
• K_Dec = 64
• K_Hex = DEC2HEX (64) = 0x0040
• Note: the maximum value for the full compression is 128
<table><tr><th>Ratio</th><th>K_Dec</th><th>K_Hex</th></tr><tr><td>Full Comp (100%)</td><td>128</td><td>0x0080</td></tr><tr><td>.
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<tr><td>DRC_O: Make up gain</td><td>DRC_O is the offset of the DRC
Equation: DRC_O = (Offset-24)/0.0625
For example: Offset = 0dB
• Abs[(0-24/0.0625)] = 384
• DRC_O_Dec = 384
• DRC_O_Hex = DEC2HEX (384) = 0x0180
<table><tr><th>Offset</th><th>O_Dec</th><th>O_Hex</th></tr><tr><td>0dB</td><td>384</td><td>0x0180</td></tr><tr><td>.
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.</td></tr><tr><td>10dB</td><td>224</td><td>0x00E0</td></tr><tr><td>.
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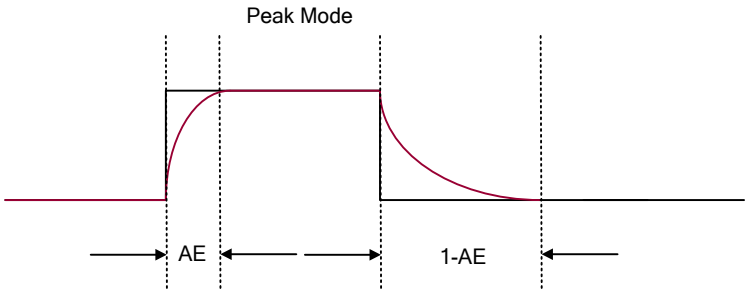
16.3 Peak Mode

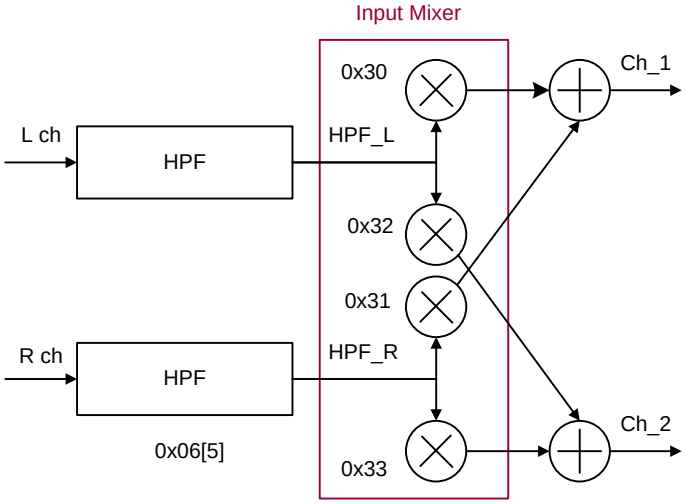
Block Diagram & Description
→The detecting threshold using different calculated methods. Peak mode: AE and 1-AE is independent 

Address	BITS	Name	Description
0x06	3	DRC_PEAK	0: RMS mode 1: Peak mode Note: The peak mode is recommended to use.

16.4 Input Mixer

Block Diagram and Description

→ Input mixer range is from mute to 6dB.



→ Default setting is CH2_IN_MIX_1 is from HPF_R

→ Default setting is CH1_IN_MIX_0 is from HPF_L

Address	BITS	Name	Description
0x30	23:0	CH1_IN_MIX_0	u[23:17], mix_0[16:0] u: Unused
0x31	23:0	CH1_IN_MIX_1	u[23:17], mix_1[16:0] u: Unused
0x32	23:0	CH2_IN_MIX_0	u[23:17], mix_0[16:0] u: Unused
0x33	23:0	CH2_IN_MIX_1	u[23:17], mix_1[16:0] u: Unused

16.4.1 Input Mixer Gain Setting

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0x30, 0x31,
0x32, 0x33,</td><td>16:0</td><td>mix_1[16:0], mix_0[16:0]</td><td>Equation: 20Log (Dec/32768)
Range: 6dB (0XFFFF) to Mute (0x00000000)
For example: 6dB, Gain = 20Log (65535/32768) = 6dB
Hex = 0xFFFF
Dec = 65535

<table>
<tr><th>Gain</th><th>Dec</th><th>Hex</th></tr>
<tr><td>6dB</td><td>65535</td><td>0X00FFFF</td></tr>
<tr><td>2dB</td><td>41252</td><td>0X00A124</td></tr>
<tr><td>.
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<tr><td>0</td><td>32768</td><td>0X008000</td></tr>
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</table>

16.4.2 Mixer Inverse Phase Setting

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0x30, 0x31,
0x32, 0x33,</td><td>16:0</td><td>mix_1[16:0], mix_0[16:0]</td><td>Equation: Hex = DEC2HEX
For example: Gain = 6dB,
Hex = 0x010000
Phase Inverse: Hex = DEC2HEX (–65535) = 0x010000

<table>
<tr><th>Gain</th><th>Dec</th><th>Hex</th></tr>
<tr><td>6dB</td><td>–65535</td><td>0X010000</td></tr>
<tr><td>4dB</td><td>–51791</td><td>0x013523</td></tr>
<tr><td>.
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<tr><td>0</td><td>–32768</td><td>0X018000</td></tr>
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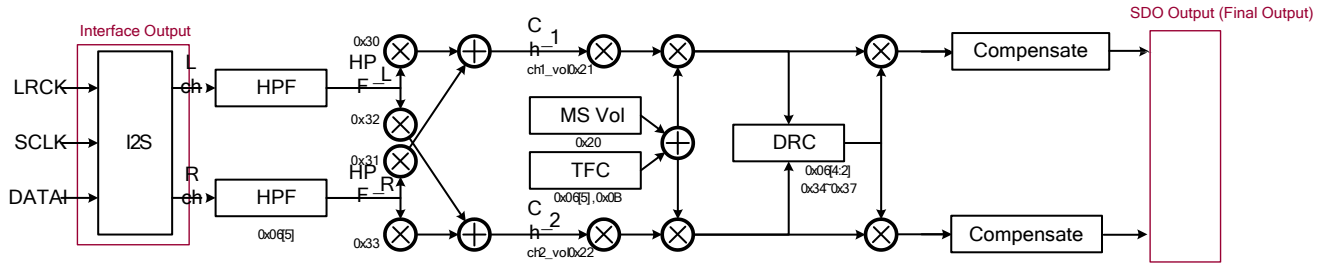
16.5 SDO Output Configure

Block Diagram and Description

→ The final stage of whole signal path is SDO output configure. It output the final level of each channel before digital filter. And output the I^2S data before the HPF.



Address	BITS	Name	Description
0x04	5:4	SDO_SEL[1:0]	00: Reserved 01: Interface output 10: Final output 11: Reserved

17 Operation

17.1 Error Reporting

The FAULTB pin is for report error status. The FAULTB goes low when protection happens. This pin is open-drain configuration, a pull-up resistor is needed.

17.2 Clock Detection

The RT9120E can accept SCLK to be as 32fs, 48fs and 64fs and supports only a 1xfs LRCK. The internal oscillator will check SCLK input constantly. If clock is lost, the RT9120E will shut down the power stage automatically.

17.3 Volume Control

The RT9120E has master volume MS_VOL and volume CH1_VOL, CH2_VOL control for each channel. The step of each volume is 0.0625dB per step, from 24dB to mute. CH1 and CH2 also have mute control, CH1_MUTE and CH2_MUTE respectively.

17.4 Built-In Anti-POP Function

An internal soft-start function controls the duty ramp-up rate of the output PWM voltage to minimize the POP noise during start-up. Similarly, during power shutdown, the duty also ramps-down to eliminate the POP noise. This function also acts when the PWDNN pin turns-ON/OFF.

17.5 Overcurrent Protection

The RT9120E provides OCP function to prevent the device from damages during overload or short-circuit conditions.

The current function is detected by an internal sensing circuit. When the inductor is shorted to each other and to GND, the OCP function is designed to operate in the latch mode.

17.6 Undervoltage Protection

The RT9120E monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin falls below the undervoltage threshold, 4V (which can be programmable.), the UVP circuit turns off the output immediately, or the latch mode can be configured for use.

17.7 Overvoltage Protection

The RT9120E monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin rises above the overvoltage threshold, 30V, the OVP circuit turns off the output immediately and operates in auto-recovery mode, or the latch mode can be configured for use.

17.8 Over-Temperature Protection

The over-temperature protection function will turn off the power MOSFET when the junction temperature exceeds 150°C (minimum). Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation, or the latch mode can be configured for use.

17.9 Common Mode Hopping Mode

The RT9120E builds in Common Mode Hopping (CMH) mode to reduce pulse width at small signal, inductor current ripple is reduced and hence light load efficiency is improved.

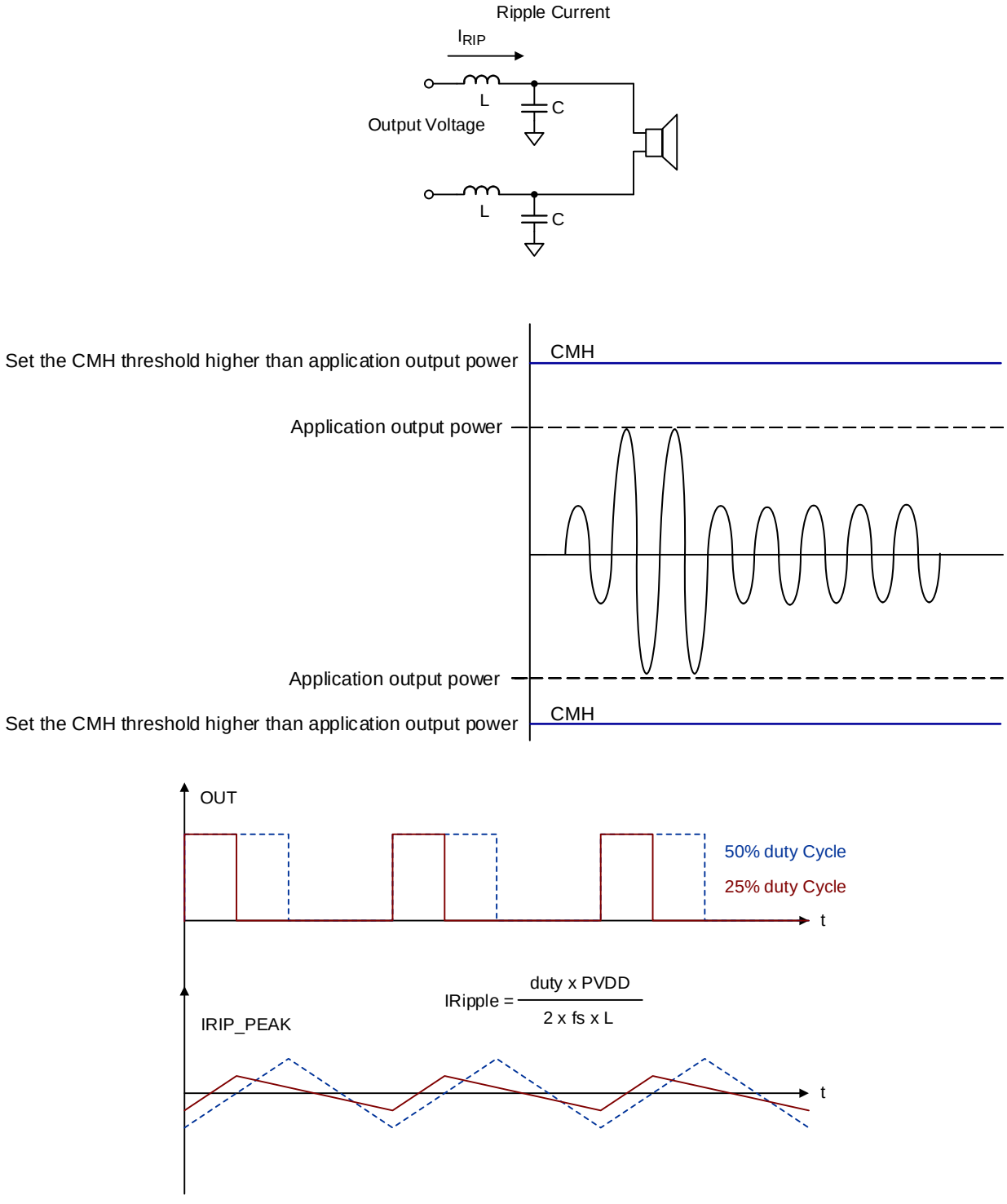


Figure 1. Current Ripple with CMH

Address	BITS	Name	Equation
0x94	7:0	D_CMH_TH [7:0]	CMH threshold: 20*log10(CMH_TH/2^8) + 2dB Output power: $10^{(D+Vol\_Gain)/20}$ x 3.5 X Output_Gain (Vp) Use the output power to calculate the CMH threshold **Note 17**. • If application output power is 12W, set the CMH threshold higher than 12W, like 13W, 14W, or 15W. By set register 0x94 • For the CMH threshold, recommended threshold not over 11Vp for 4Ω • For 6Ω, recommended not over 12.2Vp

17.10 Spread Spectrum

There are two methods, one is spread spectrum frequency, the other is added noise to triangular modulation.

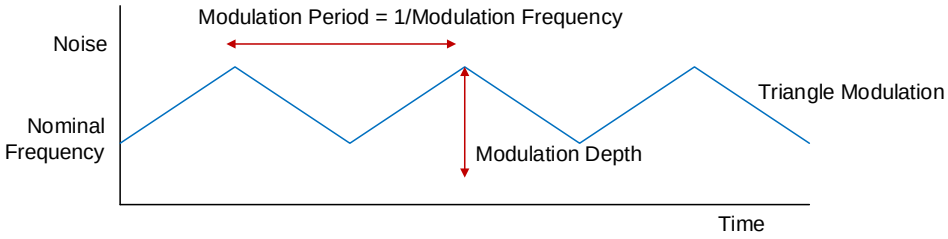


Figure 2. Current Ripple with CMH

Address	BITS	Name	Description
0x09	7	D_FSS_EN	Spread spectrum enable 0: Disable (default) 1: Enable
	6	PWM_MODEWHITE	Noise select 0: Pink noise (default) 1: White noise
	5	PWM_SELCOEF	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4
	4	PWM_NOISE_EN	Add noise to TRI_GEN 0: Disable (default) 1: Enable
	3:2	D_NOISE_AMP	Nosie amplitude for SSC 00: 5.78% (default) 01: 11.55% 10: 17.33% 11: 23.1%

Address	BITS	Name	Description
	1:0	D_FSS_AMP	Spread spectrum frequency variation amplitude 00: 16.60% 01: 33.19% (default) 10: 33.19% 11: 49.79%

17.11 Channel to Channel Phase Shift

The RT9120E has channel to channel 180-degree PWM phase shift. To minimize the EMI.

17.12 Multi Device PWM Phase Change

The RT9120E has chip to chip phase control function. Chip1 Channel 1 is used as a reference for other channels, and Chip2 channel 1 output PWM phase can be shifted from 0 to 315 degree, each step 45 degree.

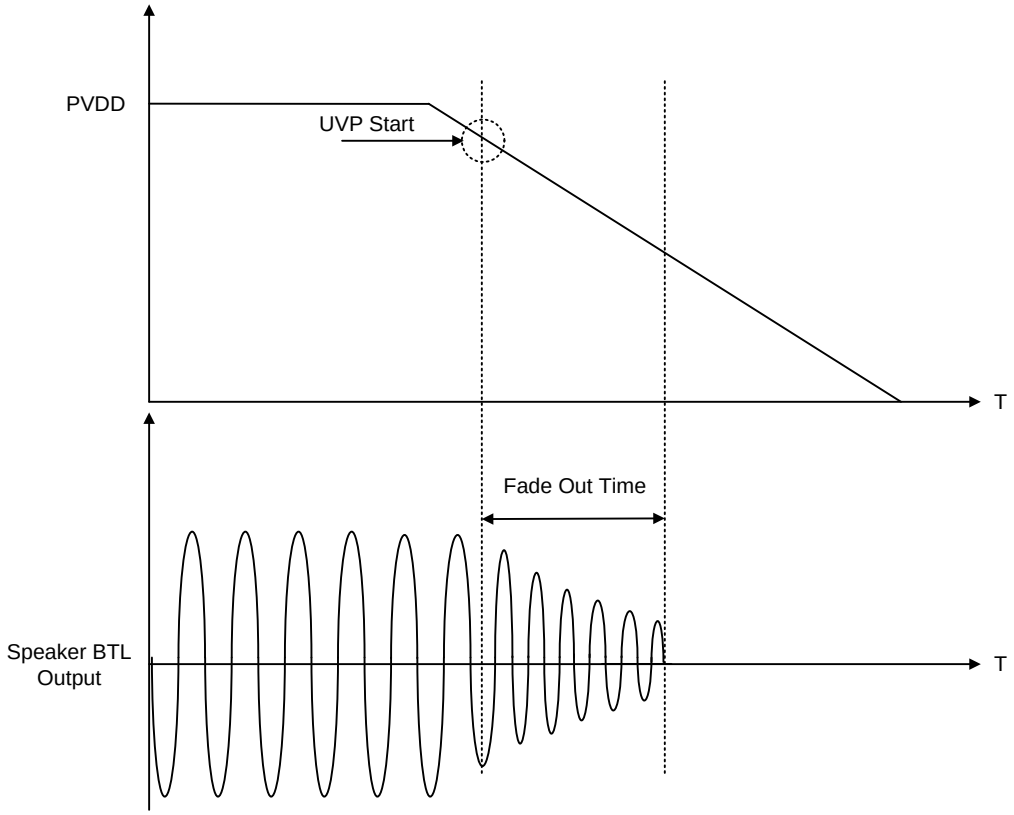
Address	BITS	Name	Description
0x07	7:5	D_PWM_PHASE	PWM output phase select 000: 0 (default) 001: 45 010: 90 011: 135 100: 180 101: 225 110: 270 111: 315

17.13 UVP Speaker Fade Out Function

The RT9120E has UVP fade function, which is used for the when suddenly AC pull off.

Block Diagram and Description

UVP voltage selection for PVDD
The UVP voltage can programmable. Once PVDD voltage drops below the preset value, RT9120E will ramp down signal to turn off the speaker



Note: There are no relation between the VOL_RAMP and UVP RAMP.

Address	BITS	Name	Description
0x6C	2:0	D_UVP_PVDD_SEL[2:0]	Select UVP level for PVDD power domain 000: 4.1V (default) 001: 6V 010: 8.5V 011: 9.5V 100: 10.9V 101: 12.7V 110: 15.4V 111: 20V
0x71	1	D_OV_FAULT_RAMP	PVDD OVP protection behavior 0: HZ_PROT directly 1: Power-off sequence (default)

18 Application Information

(Note 18)

18.1 I²C Bus Specification

The RT9120E supports the I²C protocol via the input ports SCL and SDA. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The RT9120E is always a slave device in all of its communications. It can operate at up to 400kb/s.

18.2 Communication Protocol

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition. START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer. STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the RT9120E and the bus master. During the data input, the RT9120E samples the SDA signal on the rising edge of clock SCL. For correct device operation, the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

18.3 Boost Capacitor Selection

For the large power output, and low frequency, the boost capacitor can be chosen from 0.47μF to 1μF. Reference value can be referred to in the table below:

Test Condition	Capacitor Value
PVDD = 24V, R = 8Ω, Output Power > 2x25W, 20Hz, BTL Mode	1μF
PVDD = 24V, R = 4Ω, Output Power > 2x20W, 20Hz, BTL Mode	0.47μF
PVDD = 24V, R = 4Ω, Output Power > 60W, 20Hz, PBTL Mode	1μF
PVDD = 24V, R = 8Ω, Output Power > 35W, 20Hz, PBTL Mode	1μF

18.4 Device Addressing

The RT9120E supports 4 different address settings. The default device address is 0011001 when A_SEL = DVDD, 0011000 when A_SEL = GND, 0011011 when A_SEL with 600kΩ resistor to DVDD and 0011010 when A_SEL with 600kΩ resistor to GND.

A_SEL	Device Address
DVDD	0011001
GND	0011000
With 600kΩ to DVDD	0011011
With 600kΩ to GND	0011010

18.5 LC Filter Selection

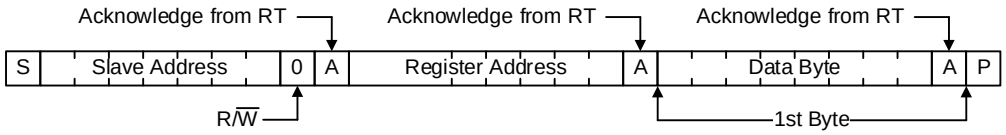
To accommodate different PWM switching and to prevent large current ripple, refer to the table below to select the appropriate LC combination.

PWM	Inductor	Capacitor Value
384kHz	10μH to 8.2μH	0.68μF to 0.47μF
768kHz	4.7μH	0.47μF to 0.22μF

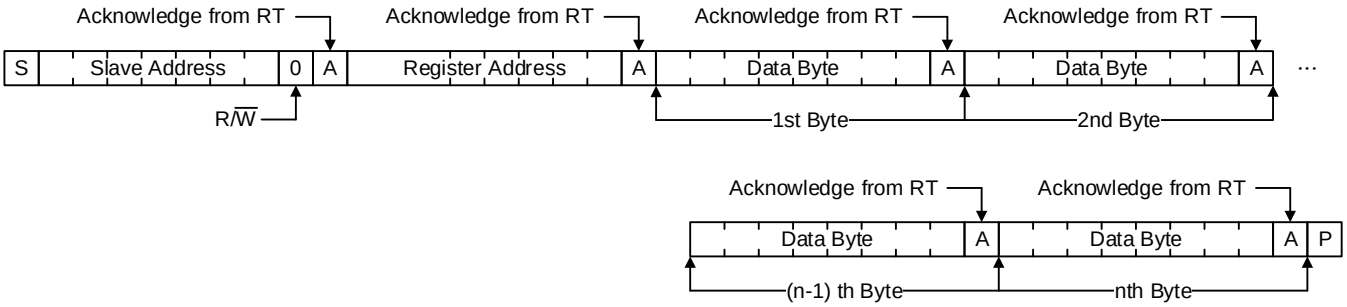
18.6 I²C Write Control

Following the START condition, the master sends a device select code with the RW bit set to 0. The RT9120E acknowledges this and the writes for the byte of internal address. After receiving the internal byte address, the RT9120E again responds with an acknowledgement.

■ Writing One Byte of Data to RT (With 1-Byte)



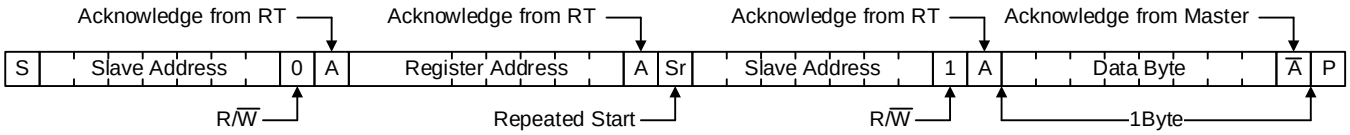
■ Writing n Bytes of Data to RT (With N-Byte)



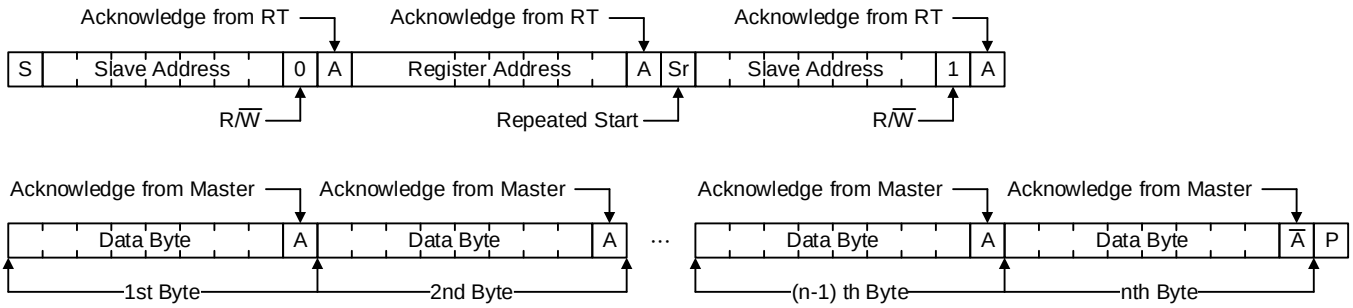
18.7 I²C Read Control

Following the START condition the master sends a device select code with the RW bit set to 1. The RT9120E acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

■ Reading One Indexed Byte of Data from RT (With 1-Byte)

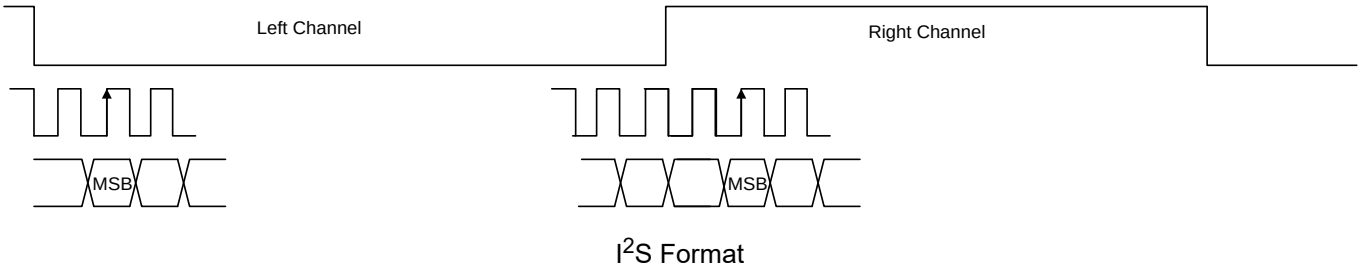


■ Reading n Indexed Words of Data from RT (With N-Byte)

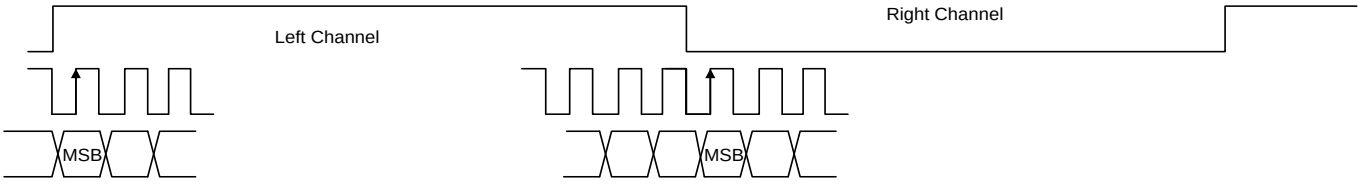


18.8 Audio Interface

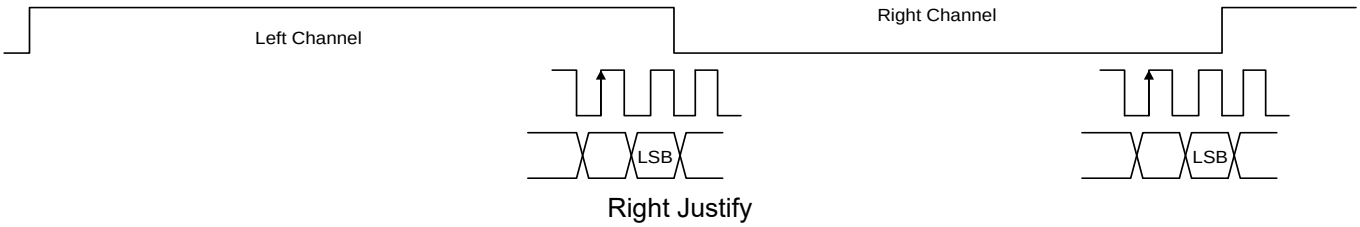
The RT9120E supports four kinds of audio interface, I²S, Left justify, Right justify, and TDM. Each kind of interface support 32bits, 24bits, 20bits, and 16 bits format. The timing diagram is shown below.



I²S Format

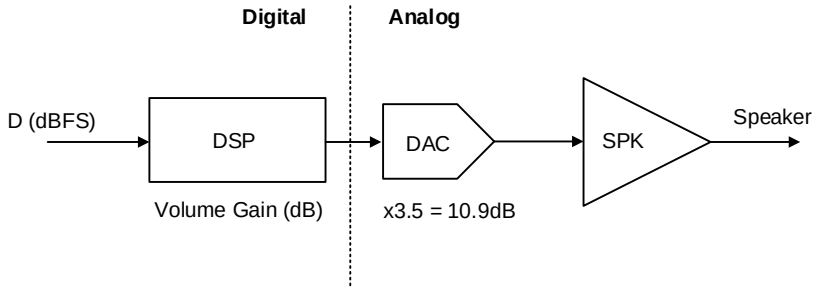


Left Justify



Address	BITS	Name	Description
0x02	2:0	AUD_FMT	000: I²S (default) 001: Left Justify 010: Right Justify 011: DSP mode 100: EIAJ Others: TDM mode
	5:4	AUD_BITS	00: 16bits I²S 01: 20bits I²S 10: 24bits I²S (default) 11: 32bits I²S

18.9 Amplification Gain



SPK_Gain : Class-D Output Gain
0x07 b[4:0]→00000 : -6dB
00001 : -5dB
00010 : -4dB
00011 : -3dB
00100 : -2dB
00101 : -1dB
00110 : 0dB
00111 : 1dB
01000 : 2dB
01001 : 3dB
01010 : 4dB
01011 : 5dB
01100 : 6dB
01101 : 7dB
01110 : 8dB
01111 : 9dB
10000 : 10dB
10001 : 11dB
10010 : 12dB
10011 : 13dB
10100 : 14dB
10101 : 15dB
10110 : 16dB
10111 : 17dB

$10^{(D+Vol\_Gain)/20}$ x 3.5 X Output_Gain (Vp)

Output voltage calculation formula = $10^{(D+Vol\_Gain)/20}$ x 3.5 X Hard clipping threshold X Output_Gain (Vp)
Note: There is −2dB at Digital Filter. The DAC 10.9dB has been included the −2dB. So, the hard clipping only work when threshold < −2dB.

Address	BITS	Name	Description
0x07	4:0	D_SPK_GAIN[4:0]	Class-D output gain 00000: –6dB 00001: –5dB 00010: –4dB 00011: –3dB 00100: –2dB 00101: –1dB 00110: 0dB 00111: 1dB 01000: 2dB 01001: 3dB 01010: 4dB 01011: 5dB 01100: 6dB 01101: 7dB 01110: 8dB 01111: 9dB 10000: 10dB 10001: 11dB 10010: 12dB 10011: 13dB (default) 10100: 14dB 10101: 15dB 10110: 16dB 10111: 17dB 11000 ~ 11111: No setting

18.10 Master Volume Gain

Address	BITS	Name	Equation
0x20	10:0	MS_VOL[10:0]	Equation: 24dB – (Dec x 0.0625) Range: 24dB (0X000) to mute (0x7ff) For example: 10dB, Hex = 0xE0 Dec = 224 Gain = 24dB – (224 x 0.0625) = 10dB

Gain	Dec	Hex
24dB	0	0x00
10dB	224	0XE0
. . .	. . .	. . .
0dB	384	0x180
. . .	. . .	. . .

18.11 Volume Ramp

00: 4.33ms from mute to 0dB (0.5dB per step, each step is 20.83μs)

01: 8.66ms from mute to 0dB (0.25dB per step, each step is 20.83μs) (default)

10: 17.33ms from mute to 0dB (0.125dB per step, each step is 20.83μs)

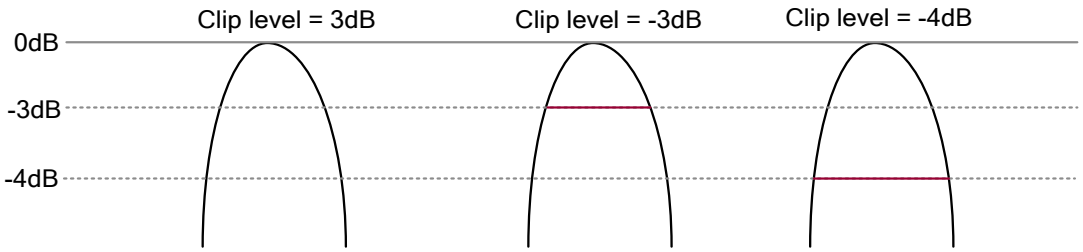
11: 34.65ms from mute to 0dB (0.0625dB per step, each step is 20.83μs)

Note: The ramp time is fixed, it is sampling rate independent.

Address	BITS	Name	Description
0x0A	1:0	VOL_RAMP_MODE[1:0]	00: 4.33ms from mute to 0dB (0.5dB per step, each step is 20.83μs) 01: 8.66ms from mute to 0dB (0.25dB per step, each step is 20.83μs) (default) 10: 17.33ms from mute to 0dB (0.125dB per step, each step is 20.83μs) 11: 34.65ms from mute to 0dB (0.0625dB per step, each step is 20.83μs)

18.12 Hard Clip Function

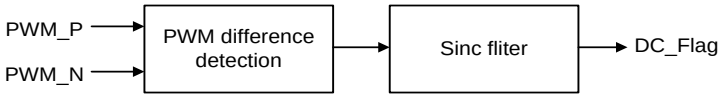
To clip the signal with different threshold, operate in time domain.



Address	BITS	Name	Description
0x06	0	HARD_CLIP_EN	0: Disable hard clip (default) 1: Enable hard clip
0x27	10:0	HARD_CLIP_TH[10:0]	Hard clip threshold for hard clip, when threshold>0, there is no any clipping effect happened. 11'h180: 0dB 0.0625db per step Note: Due to there is –2dB at digital filter, so hard clipping only works when threshold < –2dB.

18.13 DC Protection Function

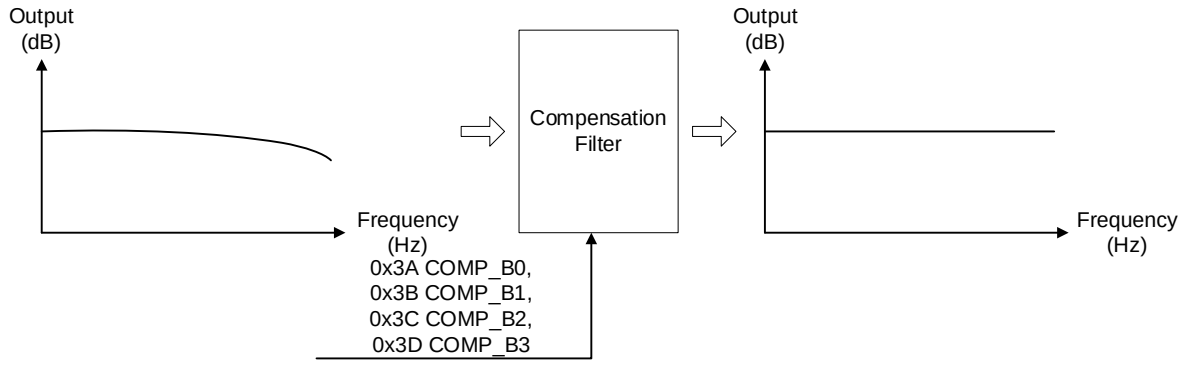
It is to use to protect the loudspeaker, when there are some DC exists at the output. The method is to detect DC at final stage (PWM), calculate the difference of the PWM and a Sinc filter to decide the DC level. The IC will shut down when detect the DC.



Address	BITS	Name	Description
0x14	7:4	Reserved	
	3:2	DC_TH[1:0]	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%
	1	DC_TIME_SEL	Detection time 0: 342ms (default) 1: 684ms
	0	DC_EN	0: DC Protection disable 1: DC protection enable (default)

18.14 Compensate Filter

Compensation filter is purpose to compensate internal gain from DAC, this filter can also compensate the frequency response affected by LC filter, the recommended setting will base on different application circuit to fit the curve.



Compensate	Description									
Compensate	B0, B1, B2, B3: Compensate coefficient									
Gain										
Gain	0.1dB	0.2dB	0.3dB	0.4dB	0.5dB	0.6dB	0.7dB	0.8dB	0.9dB	1dB
Coefficient										
B3	00000	1FFFF	00003	00006	00005	00005	00004	00002	00002	00008
B2	0000E	0001E	00022	00026	0003A	00048	0005C	00073	00081	0007F
B1	1FFA1	1FF43	1FEDE	1FE79	1FE19	1FDB1	1FD51	1FCE9	1FC81	1FC14
B0	080A0	0813E	081FF	082C0	0835A	0840F	084A8	0854D	08602	086E0

Address	BITS	Name	Description
0x06	6	COMP_EN	0: Compensation filter disable (default) 1: Compensation filter enable (Not available for 96kHz and 192kHz sampling rate)
0x3A	23:17	Reserved	Compensate B0 coefficient
	16:0	COMP_B0	
0x3B	23:17	Reserved	Compensate B1 coefficient
	16:0	COMP_B1	
0x3C	23:17	Reserved	Compensate B2 coefficient
	16:0	COMP_B2	
0x3D	23:17	Reserved	Compensate B3 coefficient
	16:0	COMP_B3	

18.15 PBTL Function

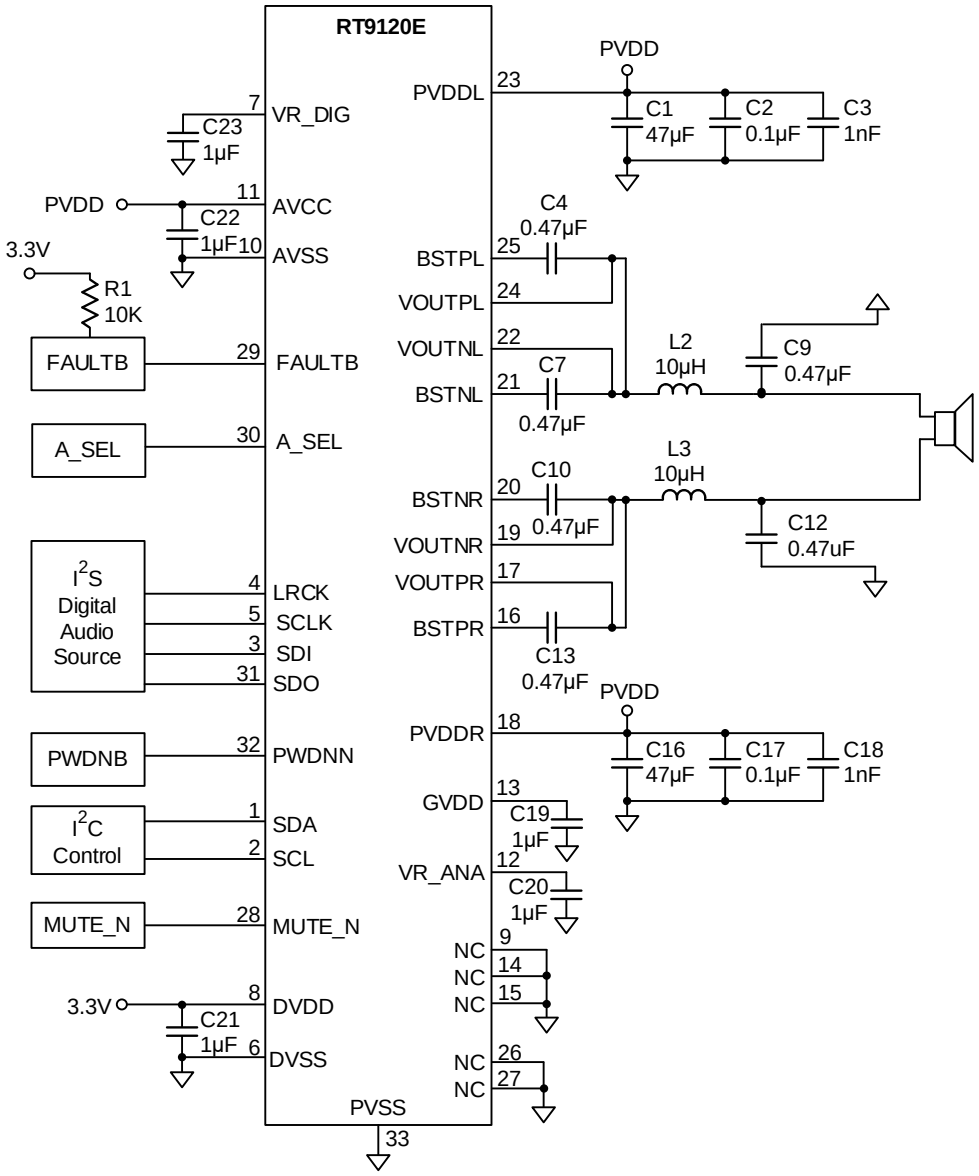
It can be configured by the hardware, and need to change the software setting

The input signal can be configured by the input mixer, from register 0x30 to configure the input signal. The default signal for the PBTL is from 0x30 L channel signal.

Address	BITS	Name	Description
0x05	4	D_PBTL	0: BTL (default) 1: PBTL

Address	BITS	Name	Description
0x30	16:0	CH1_IN_MIX_0	u[23:17], mix_0[16:0] u: Unused
0x31	16:0	CH1_IN_MIX_1	u[23:17], mix_1[16:0] u: Unused

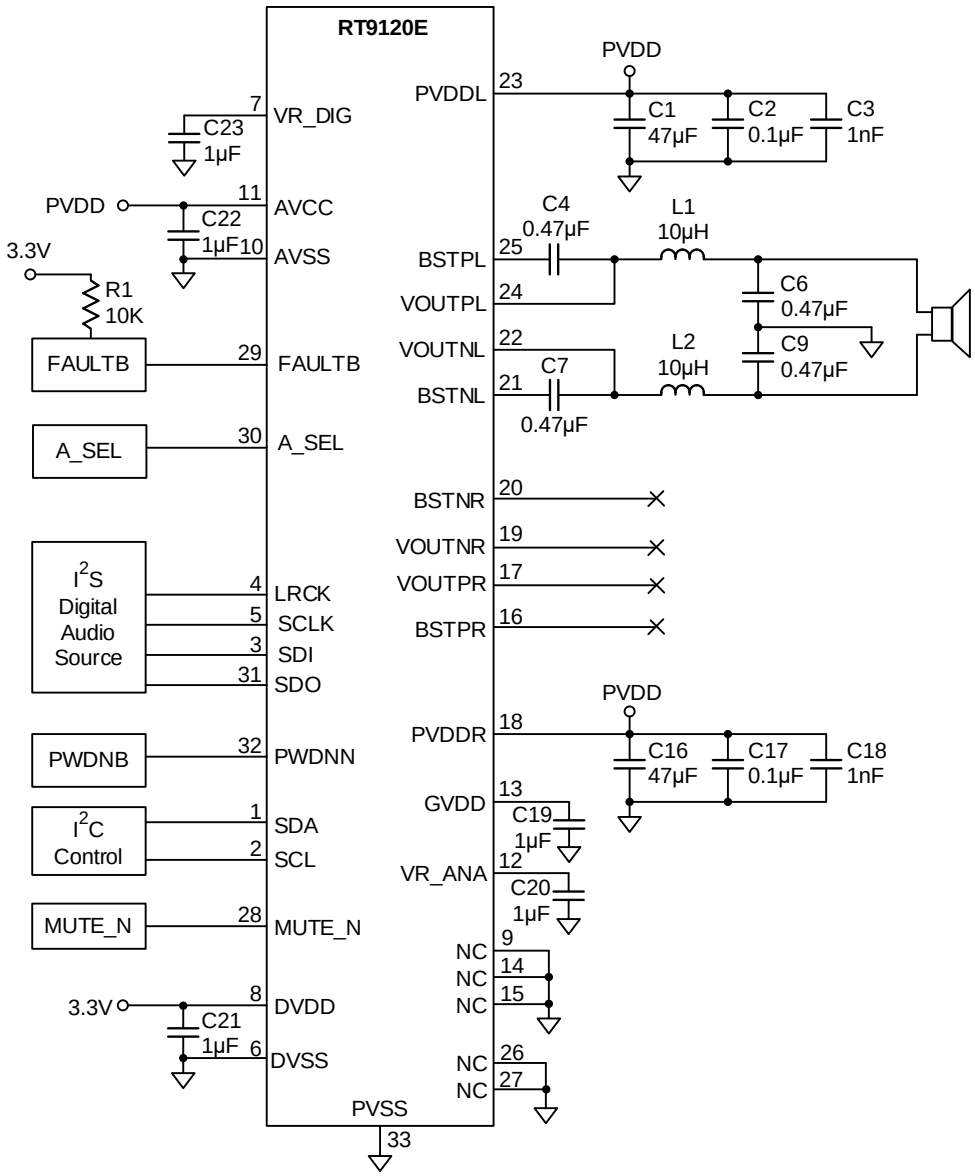
18.16 Mono PBTL Application Circuit

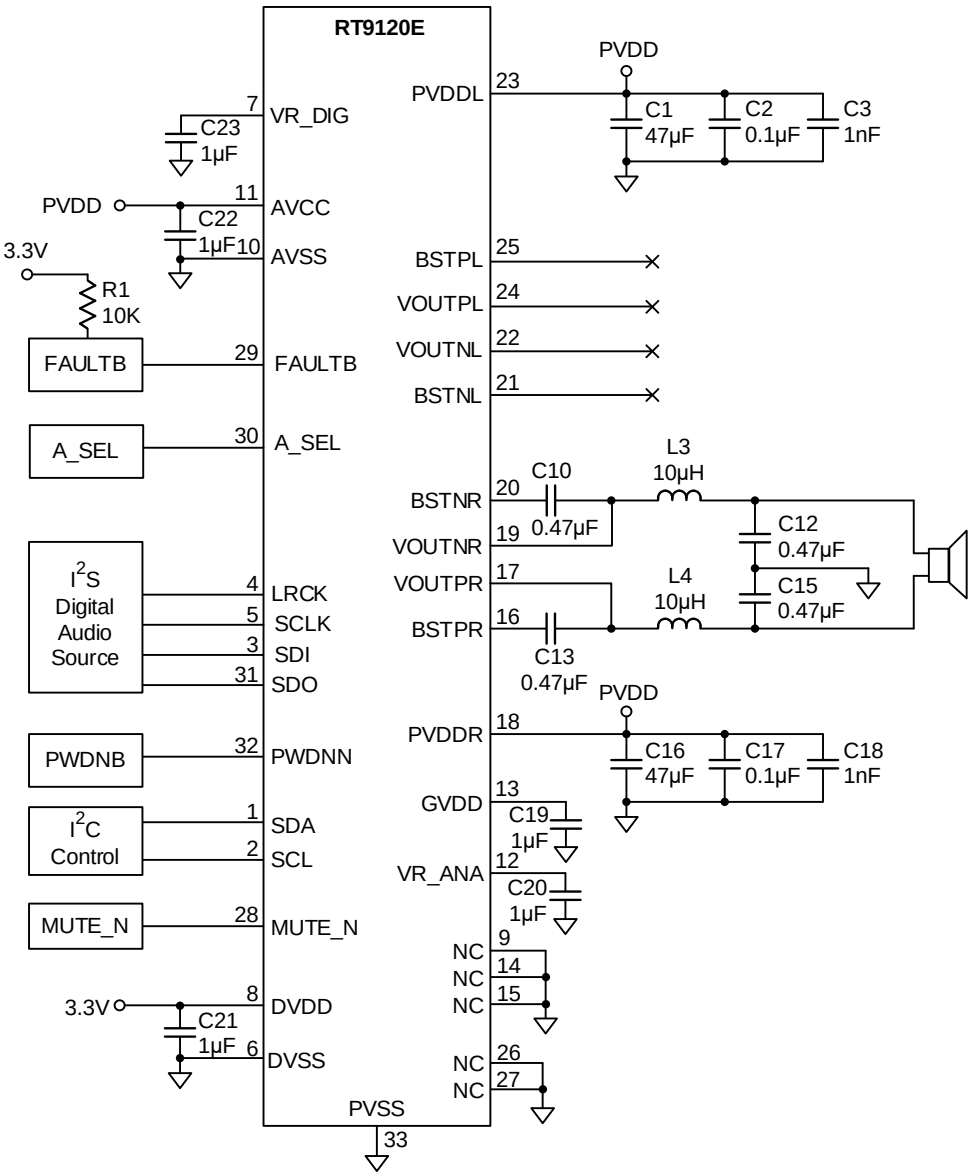


18.17 Mono Configuration

To use the mono configuration, It can be configured by register setting.

Address	BITS	Name	Description
0x15	7	D_RLPF_EN	DAC RCH LPF enable 0: Force off 1: Follow sequence (default)
	6	D_LLPF_EN	DAC LCH LPF enable 0: Force off 1: Follow sequence (default)
	5	D_EN_RCH_PWR	RCH PWR stage enable 0: Force off 1: Follow sequence (default)
	4	D_EN_LCH_PWR	LCH PWR stage enable 0: Force off 1: Follow sequence (default)
	3	D_RDAC_EN	DAC RCH enable 0: Force off 1: Follow sequence (default)
	2	D_LDAC_EN	DAC LCH enable 0: Force off 1: Follow sequence (default)
	1	D_EN_MD_RCH	MD RCH enable 0: Force off 1: Follow sequence (default)
	0	D_EN_MD_LCH	MD LCH enable 0: Force off 1: Follow sequence (default)

Mono Configuration	Example
Use Left Channel	Set the Bit[7], Bit[5], Bit[3], Bit[1] to Zero, others keep 1 

Mono Configuration	Example
Use Right Channel	Set the Bit[6], Bit[4], Bit[2], Bit[0] to Zero, others keep 1 

18.18 Protection Behavior

If the protection behavior happened, the IC will automated detect, the error condition can be checked by the register or the FAULTB pin.

18.18.1 Protection Flag

Address	BITS	Name	Description
0x10	7	ADS_ERR	Address R detection error 0: No ADS detect error (default) 1: R detect error, write 1 to clear flag
	6	DC_ERR	DC flag report 0: No DC error (default) 1: DC error
	5	I2S_ERR	0: No SCLK error (default) 1: SCLK error, write 1 to clear flag
	4	PLL_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write0 to clear flag
	3	OC_ERROR	0: No OC error (default) 1: OC, write 1 to clear flag
	2	OV_ERROR	0: No OV error (default) 1: OV, write 1 to clear flag
	1	OT_ERROR	0: No OT error (default) 1: OT, write 1 to clear flag
	0	UV_ERROR	0: No UV error (default) 1: UV, write 1 to clear flag

18.18.2 Protection Type

Protection	Auto-recovery	Shutdown Amp (Latch Type)	Fault pin pull low
DC Protection	No	Yes	Yes
SCLK ERROR	Yes. The default setting is Auto-recovery.	No	Yes, but the MASK can be configured by the 0x11 bit[5]
LRCK ERROR	Yes. The default setting is Auto-recovery.	No	Yes, but the MASK can be configured by the 0x11 bit[4]
OC ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[3]	Yes, but the MASK can be configured by the 0x11 bit[3]
OV ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[2]	Yes, but the MASK can be configured by the 0x11 bit[2]
OT ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[1]	Yes, but the MASK can be configured by the 0x11 bit[1]
UV ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[0]	Yes, but the MASK can be configured by the 0x11 bit[0]

When protection happened, there are 2 types of the protection behavior can be use.

1. Latch Type: Will shut down the AMP directly.
2. Auto-Recovery Type: The AMP will enter the auto-recovery mode, until the protection behavior stop, the AMP will continued to work.

3. The DC protection only has the latch type.

18.19 Fault Behavior Type Select

If the protection behavior happened, the IC will automate detect, there are some error types can been configured by below list.

Address	BITS	Name	Description
0x12	3	OC_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch
	2	OV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch
	1	OT_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch
	0	UV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch

18.19.1 Fault Mask

Address	BITS	Name	Description
0x11	6	DC_ERROR_MASK	Fault mask for DC error 0: Not mask (default) 1: Mask
	5	SCLK_ERROR_mask	Fault mask for SCLK error 0: Not mask 1: Mask (default)
	4	PLL_ERROR_mask	Fault mask for LRCK error 0: Not mask 1: Mask (default)
	3	OC_ERROR_mask	Fault mask for OC error 0: Not mask (default) 1: Mask
	2	OV_ERROR_mask	Fault mask for OV error 0: Not mask (default) 1: Mask
	1	OT_ERROR_mask	Fault mask for OT error 0: Not mask (default) 1: Mask
	0	UV_ERROR_mask	Fault mask for UV error 0: Not mask (default) 1: Mask

18.20 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-32L 5x5 package, the thermal resistance, θ_{JA}, is 27.7°C/W on a standard JEDEC 51-7 high effective- thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (150°C - 25°C) / (27.7°C/W) = 4.51W for a VQFN-32L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

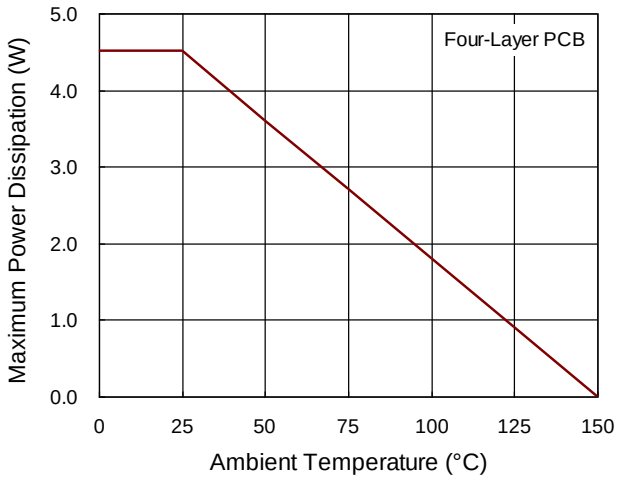
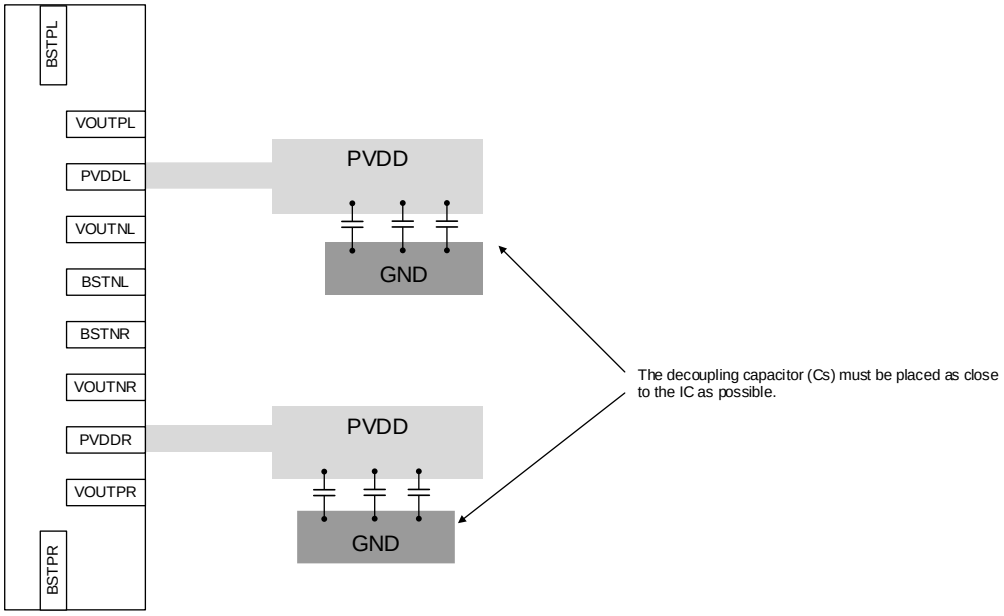


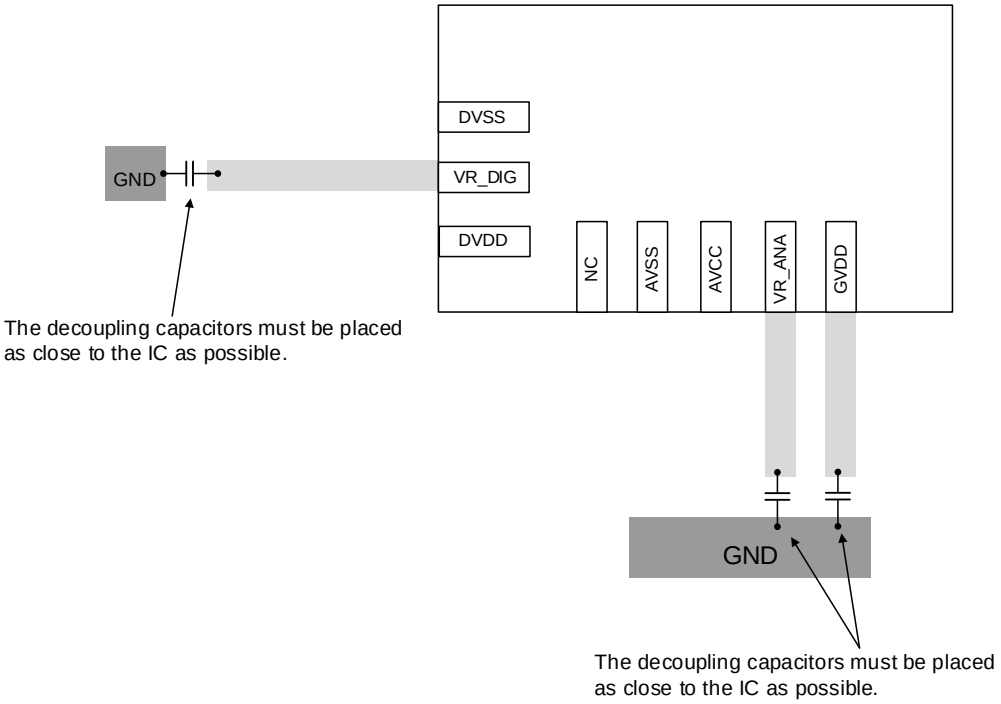
Figure 3. Derating Curve of Maximum Power Dissipation

18.21 Layout Guide

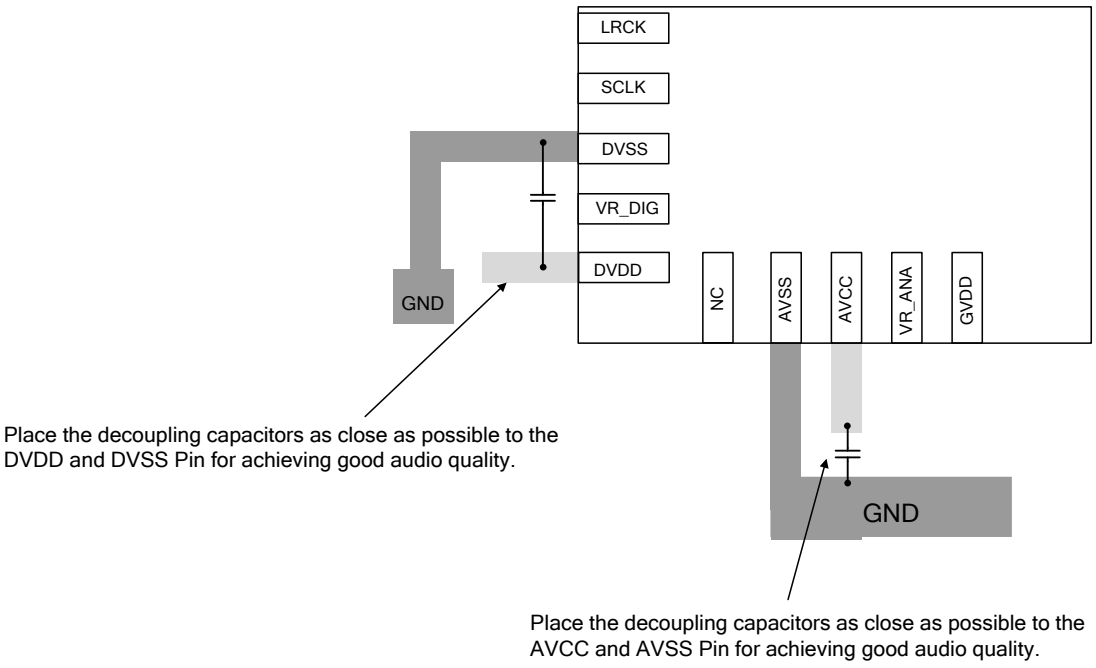
Place the decoupling capacitors as close as possible to the PVCC and GND, then use shortest trace to link these capacitors, and use more vias for GND link to GND layer to reduce parasitic inductance and resistance. The trace width is 30mil at least.



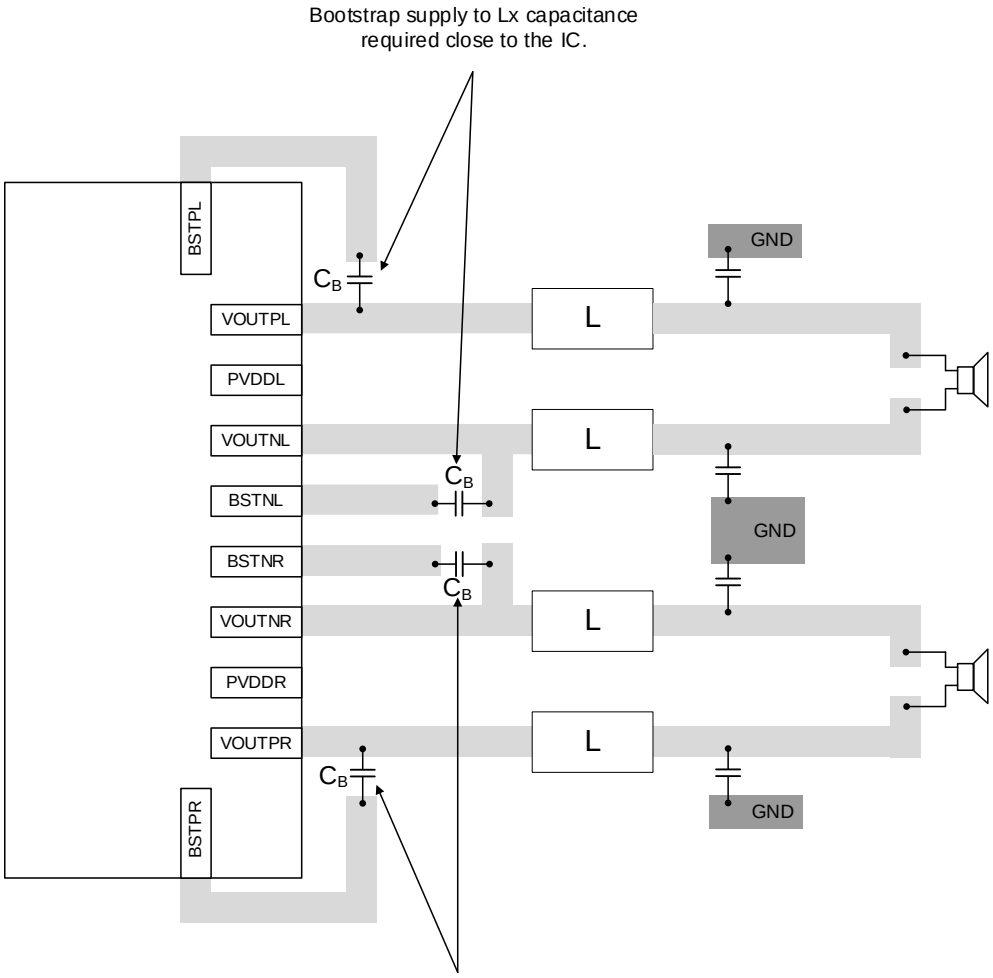
The VR_DIG VR_ANA and GVDD decoupling capacitors must be placed as close to the IC as possible.



Place the decoupling capacitors as close as possible to the DVDD and DVSS pin, AVCC and AVSS pin for achieving good audio quality, the trace width of DVDD is 6mil at least and the trace width of AVCC is 30mil at least.



The traces of VOUTPL VOUTNL VOUTPR and VOUTNR should be kept equal width and length respectively, and Bootstrap supply to Lx capacitance required close to the IC.



If possible, coplanar ground fill on both sides for differential pair of speaker out shielding.

Note 18. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

19 Functional Register Description

The register description which is described as prohibit is not allowed to be set.

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x00	2	DEV_ID	15:0	R	DEVICE_ID[15:0]		16'h5143
0x01	1	I2S_CLK_FMT	7:4	R/W	SR_MODE[2:0]	Sampling Rate report 0000: 8kHz 0001: 11.025/12kHz 0010: 16kHz 0011: 22.05/24kHz 0100: 32kHz 0101: 44.1/48kHz (default) 0110: 88.2/96kHz 0111: 192kHz Others: Reserved Others: Not supported/SCLK loss/LRCK loss	4'b0101
			3:0	R/W	BCK_MODE[2:0]	BCK mode report 0000: BCK = 32fs 0001: BCK = 48fs 0010: BCK = 64fs (default) 0011: BCK = 96fs 0100: BCK = 128fs 0101: BCK = 192fs 0110: BCK = 256fs 0111: BCK = 384fs 1000: BCK = 512fs Others: Reserved Note: for the 48fs, 96fs, 192fs, 384fs, 512fs, set 0xF8 bit[6] to 0.	4'b0010

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x02	1	I2S_DATA_FMT	7	RW	BCK_TX_EDGE	I²S data out launch edge selection 0: BCK_RX_EDGE = 0, launch with falling edge; BCK_RX_EDGE = 1, launch with rising edge (default) 1: BCK_RX_EDGE = 0, launch with rising edge; BCK_RX_EDGE = 1, launch with falling edge	0
			6	RW	BCK_RX_EDGE	0: RX @ BCK rising edge & TX @ BCK falling edge (default) 1: RX @ BCK falling edge & TX @ BCK rising edge	0
			5:4	RW	AUD_BITS	Audio bits for signal process 00: 16 bits 01: 20 bits 10: 24 bits (default) 11: 32 bits	10
			3	RW	TDM_DSP_OFFSET	TDM or DSPM offset selection 0: Without offset (DSPMB) 1: 1 bit clock offset (DSPMA) (default)	1
			2:0	RW	AUD_FMT	I²S format selection 000: I²S (default) 001: Left Justify 010: Right Justify 011: DSP mode 100: EIAJ Others: TDM mode	000
0x03	1	SIL_CTRL	7	RW	SIL_DET_EN	Silence detection enable 0: Disable 1: Enable (default)	1
			6	R	Reserved		0
			5:4	RW	SIL_TH_SEL	Prohibited	11
			2:0	RW	SIL_HOLD_TIME	Prohibited	010

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x04	2	SDIO_SEL	7:6	R	Reserved		00
	1		5:4	RW	SDO_SEL	00: No output (default) 01: Interface output 10: Final output 11: Peak level detect result	00
	1		3:2	RW	CH1_SI	00: SDIN-L to CH1 (default) 01: SDIN-R to CH1 1X: 0 to CH1	00
	1		1:0	RW	CH2_SI	00: SDIN-L to CH2 01: SDIN-R to CH2 (default) 1X: 0 to CH2	01
0x05	1	SYS_CTL	7	RW	SR_AUTO_DET	Sampling rate detection enable bit detect sampling rate and BCK mode 0: Disable, manual set 0x01 SR mode and BCK mode 1: Enable (default)	1
			6	RW	DRE_OFFSET_EN	DRE offset calibration enable 0: Disable 1: Enable	0
			5	RW	D_MODU_MODE	PWM Modulator Mode Selection 0: BD mode (default) 1: CMH mode	0
			4	RW	D_PBTL	0: BTL (default) 1: PBTL	0
			3:2	RW	D_SPK_VT_FREQ	VTRI frequency 00: 384kHz 01: 768kHz (default) 10: 768kHz 11: None	01
			1:0	RW	AMP_CTRL	AMP control 00: Amp off (default) 01: Amp on 10: Force entry silence mode 11: Mute	00

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x06	1	DIG_BLK_EN	7	RW	HARD_CLIP_EN	Hard clip enable 0: Disable (default) 1: Enable	0
			6	RW	COMP_EN	Compensation filter enable (not available in 96k and 192kHz Sampling Rate) 0: Disable (default) 1: Enable	0
			5	RW	HPF_EN	High-Pass filter enable 0: Disable 1: Enable (default)	1
			4	RW	TFC_EN	Thermal foldback control enable 0: Disable (default) 1: Enable	0
			3	RW	DRC_PEAK	DRC mode selection 0: RMS Mode 1: Peak Mode (default)	1
			2	RW	DRC_EN	DRC Enable 0: Disable (default) 1: Enable	0
			1	RW	DRC_N_EN	DRC Noise Gate Enable 0: Disable (default) 1: Enable	0
			0	RW	DRC_HYS_EN	DRC hysteresis enable 0: Disable 1: Enable (default)	1

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x07	1	ANA_OUT_CTRL	7:5	RW	D_PWM_PHASE	PWM output phase select 000: 0 (default) 001: 45 010: 90 011: 135 100: 180 101: 225 110: 270 111: 315	000
			4:0	RW	D_SPK_GAIN	Class-D output gain 5'h00: –6dB 5'h01: –5dB 5'h02: –4dB 5'h03: –3dB 5'h04: –2dB 5'h05: –1dB 5'h06: 0dB 5'h07: 1dB 5'h08: 2dB 5'h09: 3dB 5'h0A: 4dB 5'h0B: 5dB 5'h0C: 6dB 5'h0D: 7dB 5'h0E: 8dB 5'h0F: 9dB 5'h10: 10dB 5'h11: 11dB 5'h12: 12dB 5'h13: 13dB (default) 5'h14: 14dB 5'h15: 15dB 5'h16: 16dB 5'h17: 17dB 11000 ~ 11111: No setting	10011

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x08	1	OLSL_CTRL	7	RW	D_PLL_REF_SEL	Prohibited	0
			6	RO	Reserved	Prohibited	0
			5	RO	D_OLSL_DETs_DONE	Open/Short Load detection finish 0: Not enable or under detection (default) 1: Finish	0
			4	RW	D_OLSL_DET_EN	Open/Short Load detection enable 0: Disable (default) 1: Enable	0
			3	RO	D_OPEN_LOAD_L	Open load report for channel L 0: Normal (default) 1: Open	0
			2	RO	D_OPEN_LOAD_R	Open load report for channel R 0: Normal (default) 1: Open	0
			1	RO	D_SHORT_LOAD_L	Short load report for channel L 0: Normal (default) 1: Open	0
			0	RO	D_SHORT_LOAD_R	Short load report for channel R 0: Normal (default) 1: Open	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x09	1	PWM_SS_OPT	7	RW	D_FSS_EN	Spread spectrum enable 0: Disable (default) 1: Enable	0
			6	RW	PWM_MODEWHITE	Noise select 0: Pink noise (default) 1: White noise	0
			5	RW	PWM_SELCOEF	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4	0
			4	RW	PWM_NOISE_EN	Add noise to TRI_GEN 0: Disable (default) 1: Enable	0
			3:2	RW	D_NOISE_AMP	Nosie amplitude for SSC 00: 5.78% (default) 01: 11.55% 10: 17.33% 11: 23.1%	00
			1:0	RW	D_FSS_AMP	Spread spectrum frequency variation amplitude 00: 16.60% 01: 33.19% (default) 10: 33.19% 11: 49.79%	01

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x0A	1	VOL_RAMP	7:6	RO	Reserved	Prohibited	00
			5	RW	CH2_MUTE	CH2 Mute 0: Unmute 1: Mute	0
			4	RW	CH1_MUTE	CH1 Mute 0: Unmute 1: Mute	0
			3	RW	SKIP_RAMP	Skip Volume Ramp 0: Ramp with VOL_RAMP_MODE (default) 1: Skip Ramp	0
			2	RO	Reserved	Prohibited	0
			1:0	RW	VOL_RAMP_MODE	Volume Slew step control 2'b00: 4.33ms from mute to 0dB (0.5dB per step, each step is 20.83μs) 2'b01: 8.66ms from mute to 0dB (0.25dB per step, each step is 20.83μs) (default) 2'b10: 17.33ms from mute to 0dB (0.125dB per step, each step is 20.83μs) 2'b11: 34.65ms from mute to 0dB (0.0625dB per step, each step is 20.83μs)	01
0x0B	1	TFC_CTRL	7:6	R	Reserved	Prohibited	00
			5	R	D_TFC_UPBOUN_FLAG	Prohibited	0
			4	R	D_TFC_LOWBOUN_FLAG	Prohibited	0
			3:2	R/W	TFC_TH	Thermal fold back active threshold 00: Temp 110°C (default) 01: Temp 120°C 10: Temp 130°C 11: Temp 140°C	00
			1:0	R/W	TFC_RATE	Thermal fold back attack/release rate 00: 0.0625dB/50ms (default) 01: 0.0625dB/100ms 10: 0.0625dB/200ms 11: 0.0625dB/400ms	00
0x0C	1	Reserved	7:0	R/W	Reserved	Prohibited	00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x10	1	ERR_RPT	7	R/W	ADS_ERR	Address R detection error 0: No ADS detect error (default) 1: R detect error, write 1 to clear flag	0
			6	R	DC_ERR	DC flag report 0: No DC error (default) 1: DC error	0
			5	R/W	I2S_ERR	0: No SCLK error (default) 1: SCLK error, write 1 to clear flag	0
			4	R/W	PLL_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write0 to clear flag	0
			3	R/W	OC_ERROR	0: No OC error (default) 1: OC, write 1 to clear flag	0
			2	R/W	OV_ERROR	0: No OV error (default) 1: OV, write 1 to clear flag	0
			1	R/W	OT_ERROR	0: No OT error (default) 1: OT, write 1 to clear flag	0
			0	R/W	UV_ERROR	0: No UV error (default) 1: UV, write 1 to clear flag	0
0x11	1	ERR_MASK	7	RO	Reserved	Prohibited	0
			6	RW	DC_ERROR_MASK	Fault mask for DC error 0: Not mask (default) 1: Mask	0
			5	RW	I2S_ERROR_MASK	Fault mask for SCLK error 0: Not mask 1: Mask (default)	1
			4	RW	PLL_ERROR_MASK	Fault mask for LRCK error 0: Not mask 1: Mask (default)	1
			3	RW	OC_ERROR_MASK	Fault mask for OC error 0: Not mask (default) 1: Mask	0
			2	RW	OV_ERROR_MASK	Fault mask for OV error 0: Not mask (default) 1: Mask	0
			1	RW	OT_ERROR_MASK	Fault mask for OT error 0: Not mask (default) 1: Mask	0
			0	RW	UV_ERROR_MASK	Fault mask for UV error 0: Not mask (default) 1: Mask	0

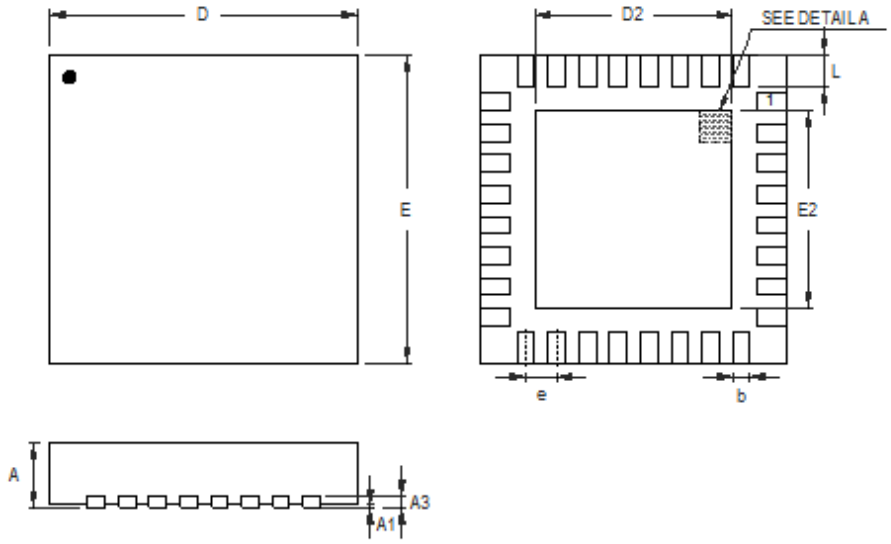
ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x12	1	ERR_TYPE	7:4	RO	Reserved	Prohibited	0000
			3	RW	OC_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
			2	RW	OV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
			1	RW	OT_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
			0	RW	UV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	0
0x13	1	AUTO_RCVRY	7:5	RO	Reserved	Prohibited	000
			4	RW	I2S_LOSS_ERR_EN	I^2S clock loss report as error enables 0: Not report (default) 1: Report	0
			3:0	R/W	RCVRY_TIME[3:0]	Power Stage auto-recovery time 0000 ~ 0001: No setting 0010: 299ms (default) 0011: 449ms 0100: 598ms 0101: 748ms 0110: 898ms 0111: 1047ms 1000: 1197ms 1001: 1346ms 101X: 1496ms 11XX: 1496ms	0010
0x14	1	DC_PROT	7:4	R	Reserved	Prohibited	0000
			3:2	R/W	DC_TH[1:0]	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%	10
			1	R/W	DC_TIME_SEL	Detection time 0: 342ms (default) 1: 684ms	0
			0	R/W	DC_EN	DC protection enable 0: Disable 1: Enable (default)	1
0x20	2	MS_VOL	15:11	R	Reserved	Prohibited	00000
			10:0	R/W	MS_VOL[10:0]	Master Volume control 11'h000: 24dB 11'h180: 0dB 11'h7FF: mute (default) 0.0625dB per step	11'h7FF

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x21	2	CH1_VOL	15:11	R	Reserved	Prohibited	00000
			10:0	R/W	CH1_VOL[10:0]	CH1 Volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step	11'h180
0x22	2	CH2_VOL	15:11	R	Reserved	Prohibited	00000
			10:0	R/W	CH2_VOL[10:0]	CH2 Volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step	11'h180
0x23	2	DRC_TH	15:11	R	Reserved	Prohibited	00000
			10:0	R/W	DRC_TH	DRC threshold 11'h000: 0dB (default) 11'h180: −24dB 11'h67E: −103.875dB 11'h67F ~ 11'h7FF: Not available 0.0625dB per step	11'h000
0x24	2	DRC_RATIO	15:8	R	Reserved	Prohibited	8'h00
			7:0	R/W	DRC_RATIO	DRC compress ratio 8'h00: No compression 8'h80 (default) 8'h80 ~ 8'hFF: Full compression 1/128 per step	8'h80
0x25	2	DRC_OFFSET	15:11	R	Reserved	Prohibited	00000
			10:0	R/W	DRC_OFFSET	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FE: −103.875dB 11'h7FF: Not available 0.0625dB per step	11'h180
0x26	2	DRC_NG_TH	15:11	R	Reserved	Prohibited	00000
			10:0	R/W	DRC_NG_TH	Noise gate threshold 11'h000: 0dB 11'h180: −24dB 11'h640: −100dB (default) 11'h67E: −103.875dB 11'h67F ~ 11'h7FF: Not available 0.0625dB per step	11'h640

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x27	2	HARD_CLIP_TH	15:11	R	Reserved	Prohibited	00000
			10:0	R/W	HARD_CLIP_TH[10:0]	Hard clip threshold when HARD_CLIP_EN = 1 > 0dB is not allowable for hard clip threshold setting 11'h180: 0dB (default) 0.0625db per step	11'h180
0x30	3	CH1_IN_MIX_0	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH1_IN_MIX_0	CH1_IN_MIX_0	17'h08000
0x31	3	CH1_IN_MIX_1	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH1_IN_MIX_1	CH1_IN_MIX_1	17'h00000
0x32	3	CH2_IN_MIX_0	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH2_IN_MIX_0	CH2_IN_MIX_0	17'h00000
0x33	3	CH2_IN_MIX_1	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH2_IN_MIX_1	CH2_IN_MIX_1	17'h08000
0x34	3	DRC_AE	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_AE	DRC energy estimator	17'h08000
0x35	3	DRC_1-AE	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_1-AE	DRC energy estimator when releasing	17'h00000
0x36	3	DRC_AD	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_AD	DRC release time	17'h08000
0x37	3	DRC_AA	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_AA	DRC attack time	17'h08000
0x38	3	RMS_RPT_AE	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	RMS_RPT_AE	Prohibited	17'h008000
0x3A	3	COMP_B0	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B0	Compensation filter coefficient B0	17'h08000
0x3B	3	COMP_B1	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B1	Compensation filter coefficient B1	17'h00000
0x3C	3	COMP_B2	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B2	Compensation filter coefficient B2	17'h00000
0x3D	3	COMP_B3	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B3	Compensation filter coefficient B3	17'h00000
0x3E	4	CH1_RMS_RPT	31:0	R	CH1_RMS_RPT[31:0]	Prohibited	32'h00000000
0x3F	4	CH2_RMS_RPT	31:0	R	CH2_RMS_RPT[31:0]	Prohibited	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x40	1	SW_RESET	7	W	Prohibited	Prohibited	1'b0
			6:0	R	Reserved	Prohibited	7'h00
0x6C	1	UVP_OPT	7	R	D_VCORE_OK	Prohibited	1
			6	RW	D_EN_DVDD_UV	0: Disable 1: Enable (default)	1
			5:4	RW	D_UVP_DVDD_VTH	Adjust UVP threshold for detecting DVDD = 3.3V Rising: 11: 2.7V 10: 2.6V 01: 2.5V (default) 00: 1.48 (= VR_DIG) Falling: 11: 2.8V 10: 2.7V 01: 2.6V (default) 00: 1.55 (= VR_DIG)	01
			2:0	RW	D_UVP_PVDD_SEL	Select UVP level for PVDD power domain 000: 4.1V (default) 001: 6V 010: 8.5V 011: 9.5V 100: 10.9V 101: 12.7V 110: 15.4V 111: 20V	000
0x94	1	CMH_TH	7:0	RW	D_CMH_TH	Threshold of CMH to BD mode modulation 8'h00: DRE_TH (CMH switch with DRE) Others: 20*log10 (CMH_TH/2^8) + 2dB 8'h25: −14.80dB 8'hCA: −0.06dB 8'hCB ~ 8'hFF: Force CMH mode	00100101

20 Outline Dimension



DETAIL A

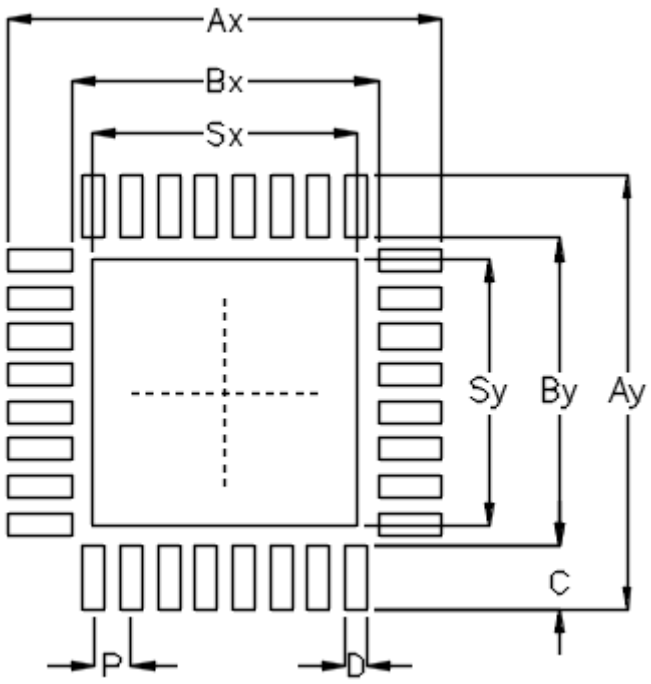
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 32L QFN 5x5 Package

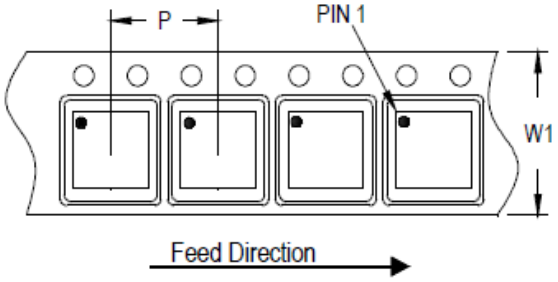
21 Footprint Information

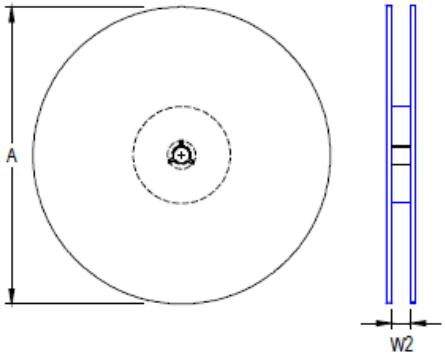


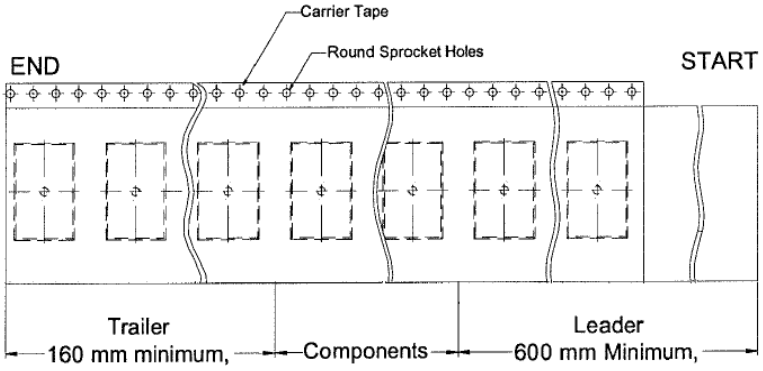
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-32	32	0.50	5.80	5.80	4.10	4.10	0.85	0.30	3.55	3.55	±0.05

22 Packing Information

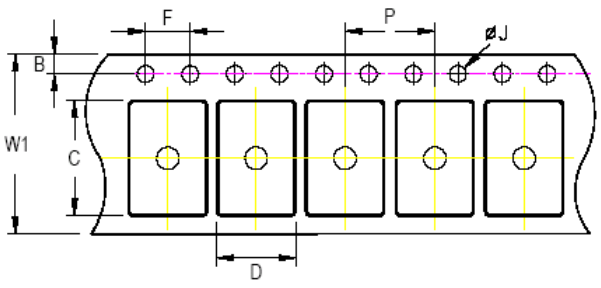
22.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

22.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 5x5	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

22.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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23 Datasheet Revision History

Version	Date	Description	Item
00	2025/2/17	Final	*Marking Information on page 2* - Updated marking information