RICHTEK®

RT9094A

2A Ultra-Low Dropout Voltage LDO Regulators with Soft-Start

1 General Description

The RT9094A is a very low dropout linear regulator that operates from an input voltage as low as 0.8V. The device is capable of supplying 2A of output current with a typical dropout voltage of only 100mV. A VBIAS supply is required to run the internal reference and LDO circuitry while output current comes directly from the VIN supply for high-efficiency regulation. User-programmable soft-start limits the input inrush current and minimizes stress on the input power. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility provides an easy-to-use robust power management solution for a wide variety of applications.

The RT9094A is stable with an output capacitor greater than or equal to 2.2μF. A precise reference and error amplifier deliver 1% accuracy over load, line, and temperature. Current limit and over-temperature protection are also included. The RT9094A is available in the WDFN-10L 3x3 package. The recommended ambient temperature range is −40°C to 85°C.

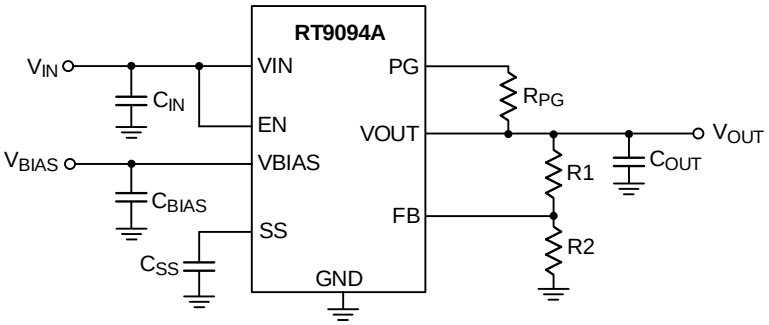
2 Features

- **Ultra-Low V_{IN} Range: 0.8V to 5.5V**
- **VBIAS Voltage Range: 2.7V to 5.5V**
- **VOUT Voltage Range: 0.8V to 3.6V**
- **Low Dropout: 100mV Typical at 2A, V_{BIAS} = 5V**
- **1% Accuracy Over Line/Load/Temperature**
- **Power-Good Indicator for Easy Sequence Control**
- **Programmable Soft-Start Provides Linear Voltage Startup**
- **Stable with Any Output Capacitor ≥ 2.2μF**
- **Current Limit and Over-Temperature Protection**

3 Applications

- PCs, Servers, Modems, and Set-Top-Boxes
- FPGA Applications
- DSP Core and I/O Voltages
- Instrumentation
- Post-Regulation Applications
- Applications With Sequencing Requirements

4 Simplified Application Circuit



5 Ordering Information

RT9094A □□□

Pin 1 Orientation
Empty: Quadrant 1
(2): Quadrant 2, Follow EIA-481

Package Type(1)
QW: WDFN-10L 3x3 (W-Type)

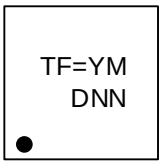
Lead Plating System
G: Richtek Green Policy Compliant(2)

A: WDFN-10L 3x3

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

6 Marking Information



TF= : Product Code
YMDNN : Date Code

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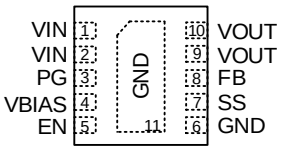
7 Pin Configuration

(TOP VIEW)

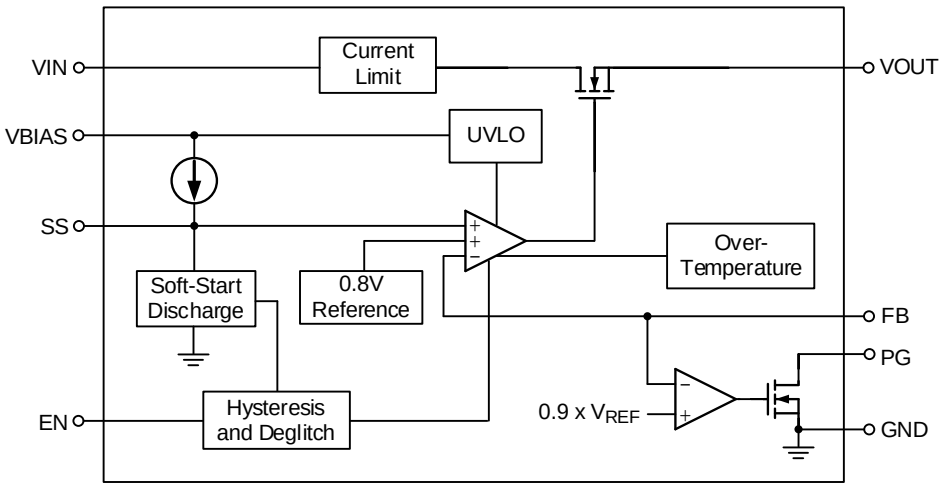


WDFN-10L 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	VIN	Power input of the device.
3	PG	Power-good indicator. An open-drain, active-high output that indicates the status of VOUT. A pull-up resistor from 10kΩ to 1MΩ should be connected from this pin to a supply of up to 5.5V.
4	VBIAS	Bias input pin. Providing input voltage for internal control circuitry.
5	EN	Chip enable (Active-High). Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. Connect to VIN if not being used.
6 11 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	SS	Connect a capacitor between this pin and the ground to set the soft-start ramp time of the output voltage.
8	FB	Feedback pin. Connect this pin to an external voltage divider to set the output voltage.
9, 10	VOUT	Regulated output voltage. A minimum of 2.2μF capacitor should be placed directly at this pin.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Output Voltage, VOUT ---------- –0.3V to (V_{IN} + 0.3V)
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage ---------- 0.8V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WDFN-10L 3x3	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	40.4	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	70.4	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	13.6	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	41.5	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.2	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board, which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

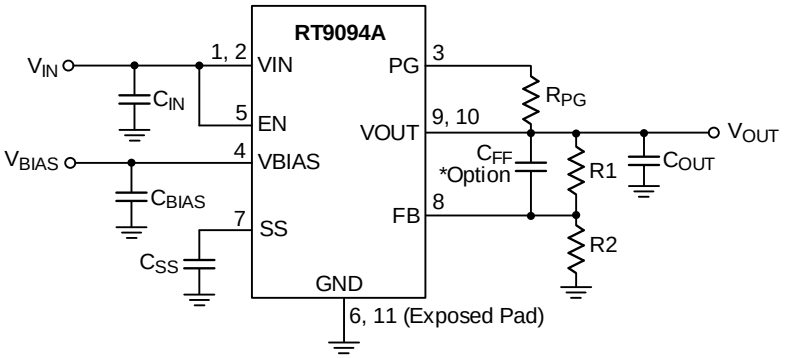
(V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.3V, V_{BIAS} = 5V, C_{BIAS} = 0.1μF, C_{IN} = C_{OUT} = 10μF, C_{SS} = 1nF, I_{OUT} = 50mA, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}		V_{OUT} + V_{DROP}	--	5.5	V
VBIAS Pin Voltage	V_{BIAS}		2.7	--	5.5	V
Reference Voltage	V_{REF}	T_A = 25°C	0.796	0.8	0.804	V
Output Voltage Range	V_{OUT}	V_{IN} = 5V, I_{OUT} = 2A	V_{REF}	--	3.6	V
Output Voltage Accuracy	V_{OUT_ACC}	2.97V ≤ V_{BIAS} ≤ 5.5V, 50mA ≤ I_{OUT} ≤ 2A	−1	±0.5	1	%
Line Regulation	ΔV_{LINE_REG}	$V_{OUT\ (Normal)}$ + 0.3 ≤ V_{IN} ≤ 5.5V	--	0.03	--	%/V
Load Regulation	ΔV_{LOAD}	50mA ≤ I_{OUT} = 2A	--	0.09		%/A
VIN Dropout Voltage	V_{DROP_VIN}	I_{OUT} = 2A, V_{BIAS} − $V_{OUT\ (Normal)}$ ≥ 3.25V	--	100	150	mV
VBIAS Dropout Voltage	V_{DROP_VBIAS}	I_{OUT} = 2.0A, V_{IN} = V_{BIAS}	--	--	1.3	V
		I_{OUT} = 1.0A, V_{IN} = V_{BIAS}	--	--	1.2	
		I_{OUT} = 0.5A, V_{IN} = V_{BIAS}	--	--	1.1	
Current Limit	I_{LIM}	V_{OUT} = 80% × $V_{OUT\ (Normal)}$	2.5	--	5.5	A
Bias Pin Current	I_{BIAS}		--	1	2	mA
Shutdown Supply Current (I_{GND})	I_{SHDN}	V_{EN} = 0.4V	--	1	50	μA
Feedback Pin Current	I_{FB}		−1	0.15	1	μA
Power-Supply Rejection (VIN to VOUT)	PSRR (Note 6)	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	60	--	dB
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	30	--	
Power-Supply Rejection (VBIAS to VOUT)		1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	50	--	dB
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	30	--	
Output Noise Voltage	Vn (Note 6)	100Hz to 100kHz, I_{OUT} = 1.5A, C_{SS} = 0.001μF	--	25 x V_{OUT}	--	μV_{RMS}
Minimum Startup Time	t_{STR} (Note 6)	R_{LOAD} for I_{OUT} = 1A, C_{SS} = open	--	200	--	μs
Soft-Start Charging Current	I_{SS}	V_{SS} = 0.4V	--	440	--	nA
Enable Input Voltage Rising Threshold	V_{EN_R}		1.1	--	5.5	V
EN Input Voltage Falling Threshold	V_{EN_F}		0	--	0.4	
Enable Pin Hysteresis	V_{EN_HYS}		--	50	--	mV
Enable Pin Deglitch Time	V_{EN_DG}		--	20	--	μs
Enable Pin Current	I_{EN}	V_{EN} = 5V	--	0.1	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power-Good Voltage Threshold	V_{PG}	V_{OUT} decreasing	85	90	94	%V_{OUT}
Power-Good Trip Hysteresis	V_{PG_HYS}		--	3	--	%V_{OUT}
Power-Good Output Low Voltage	V_{PG_L}	I_{PG} = 1mA (sinking), V_{OUT} < V_{IT}	--	--	0.3	V
Power-Good Leakage Current	I_{PG_LK}	V_{PG} = 5.25 V, V_{OUT} > V_{IT}	--	0.1	1	μA
Over-Temperature Protection Threshold	T_{OTP}	Shutdown, temperature increasing	--	165	--	°C
		Reset, temperature decreasing	--	140	--	

Note 6. Guaranteed by design.

15 Typical Application Circuit



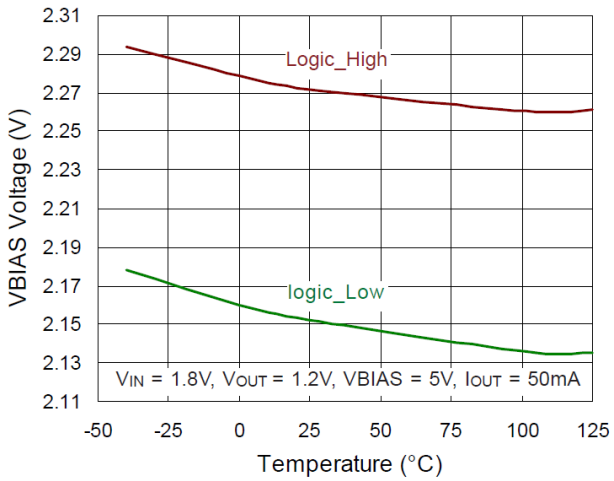
*: The feedforward capacitor is optional for the transient response and circuit stability improvement.

Table 1. Suggested Component Value

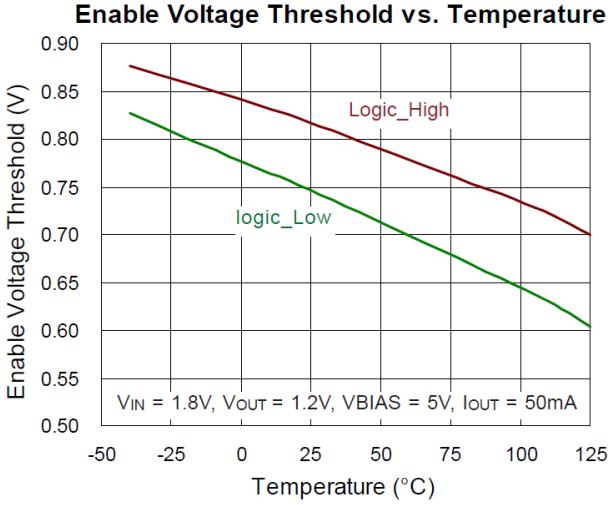
VOUT (V)	R1 (kΩ)	R2 (kΩ)
0.8	Short	Open
0.9	0.619	4.99
1.0	1.13	4.53
1.05	1.37	4.42
1.1	1.87	4.99
1.2	2.49	4.99
1.5	4.12	4.75
1.8	3.57	2.87
2.5	3.57	1.69
3.3	3.57	1.15

16 Typical Operating Characteristics

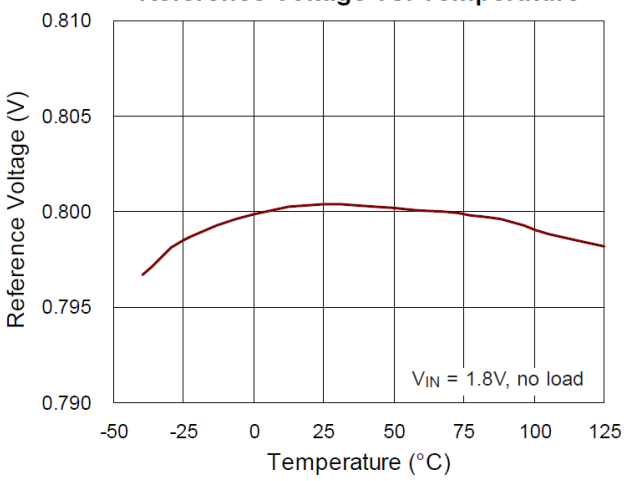
VBIAS Voltage UVLO vs. Temperature



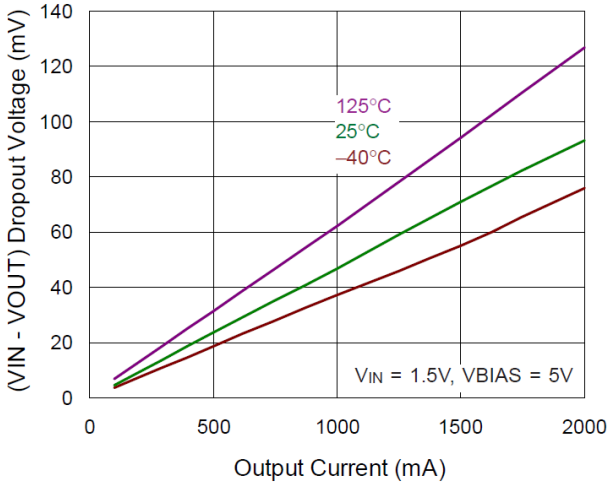
Enable Voltage Threshold vs. Temperature



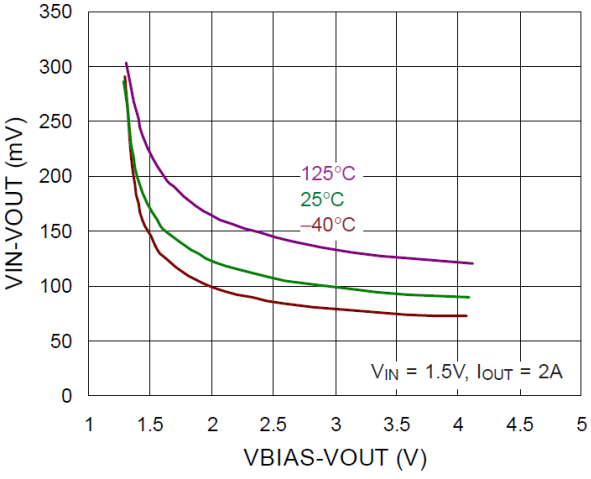
Reference Voltage vs. Temperature



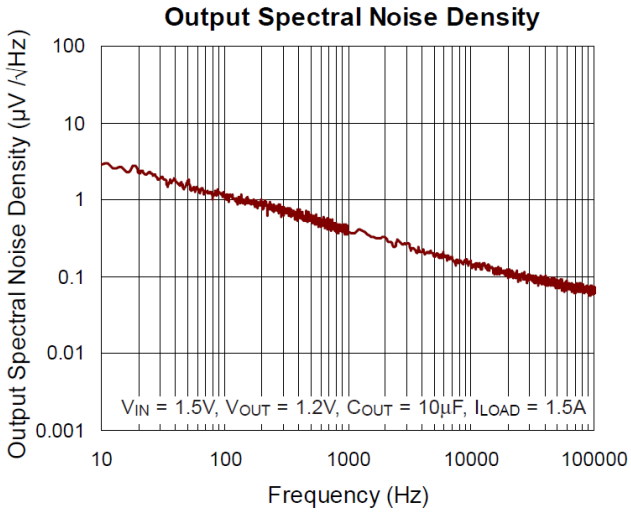
Dropout Voltage vs. Output Current

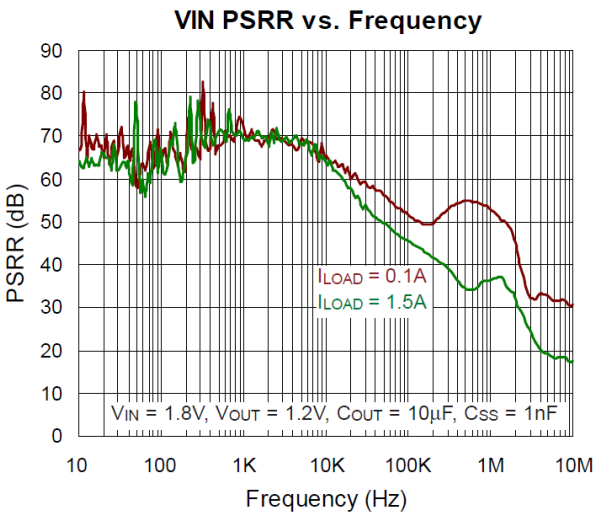


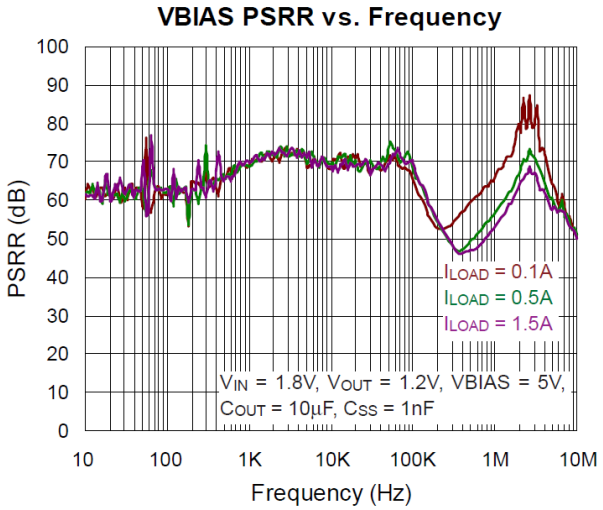
VIN Dropout Voltage vs. (VBIAS - VOUT)

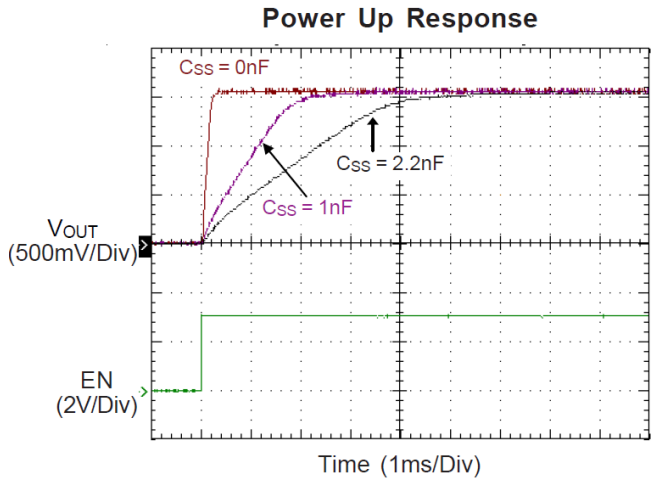


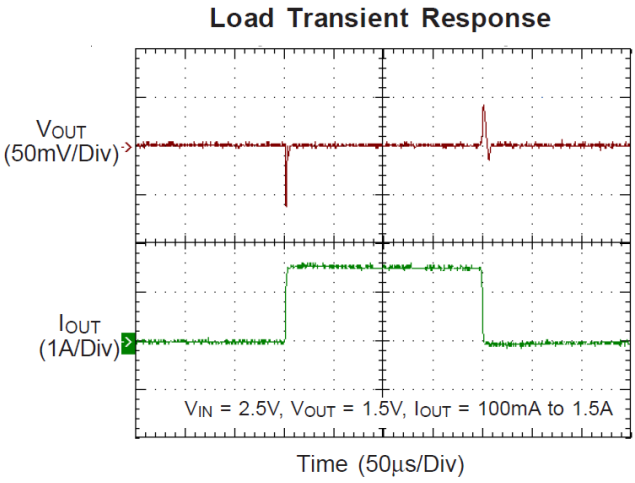
Output Spectral Noise Density











17 Operation

The RT9094A is a very low dropout linear regulator that operates from an input voltage as low as 0.8V. It provides a highly accurate output that is capable of supplying 2A of output current with a typical dropout voltage of only 100mV. The output voltage range is from 0.8V to 3.6V.

17.1 VIN and VBIAS Supply

The VBIAS input supplies the internal reference and LDO circuitry while all output current comes directly from the VIN input for high efficiency regulation. With an external VBIAS 3.25V above VOUT, offers the RT9094A very low dropout performance (150mV maximum at 2A), which allows the device to be used in place of a DC-DC converter and still achieve good efficiency. This provides designers to achieve the smallest, simplest, and lowest cost solution.

For applications where an auxiliary bias voltage is not available or low dropout is not required, it is suggested that VBIAS be 1.3V above VOUT and attention on power rating and thermal management is needed.

17.2 Enable and Shutdown

The EN pin is active high. Applying a voltage above 1.1V ensures that the LDO regulator turns on, while the regulator turns off if the V_{EN} falls below 0.4V. The enable circuitry has a typical 50mV hysteresis and a deglitching feature for use with relatively slowly ramping analog signals. That helps avoid on-off cycling caused by small glitches in the V_{EN} signal. A fast rise-time signal must be used to enable the RT9094A if precise turn-on timing is required. If the enable function is not used, EN can be connected to either VIN or VBIAS. If EN is connected to VIN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

17.3 Soft-Start Function

The RT9094A includes a soft-start feature to prevent excessive current flow during start-up. When the LDO is enabled, an internal soft-start current (I_{SS}) charges the external soft-start capacitor (C_{SS}) to build a ramp-up voltage internally. The RT9094A achieves a linear and monotonic soft-start by tracking the voltage ramp until the voltage exceeds the internal reference. The soft-start ramp time can be calculated using Equation 1:

$$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.44\mu A} \quad (1)$$

17.4 Power-Good Indicator

When the output voltage is greater than $V_{IT} + V_{HYS}$, the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. If VOUT drops below V_{IT} or if VBIAS drops below 1.9V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled, OCP or OTP triggered.

17.5 Overcurrent Protection

The RT9094A has built-in overcurrent protection. When an overcurrent condition (typically 3A) is detected, the RT9094A will fold back and limit the current to typical 2.25A. It allows the device to supply surges of up to 3A while preventing overheating in a short circuit event.

17.6 Thermal Shutdown and Over-Temperature Protection

At higher temperatures, or in cases where internal power dissipation causes excessive self-heating on the IC, the thermal shutdown circuitry will shut down the LDO when the junction temperature exceeds approximately 160°C. It will re-enable the LDO once the junction temperature drops back to approximately 140°C. The RT9094A will cycle in and out of thermal shutdown without latch-up or damage until the overstress condition is removed. Long-term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

18 Application Information

(Note 7)

The RT9094A is a low dropout regulator that features soft-start capability. It provides EN and PG for easy system sequence control, and includes built-in overcurrent and over-temperature protection for safe operation.

18.1 Dropout Voltage

Because of two power supply inputs VIN and VBIAS, and one VOUT regulator output, there are two specified dropout voltages. The first is the VIN Dropout voltage, which is the voltage difference (V_{IN} – V_{OUT}) when VOUT starts to decrease by the percentage specified in the Electrical Characteristics table.

The second is the VBIAS dropout voltage, which is the voltage difference (V_{BIAS} – V_{OUT}) when VIN and VBIAS pins are joined together and VOUT starts to decrease. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. In these applications, it is suggested that VBIAS be 1.3V above VOUT and attention on power rating and thermal considerations.

18.2 Input, Output, and Bias Capacitor Selection

The device is designed to be stable for all available types and values of output capacitors ≥ 2.2μF. The device is also stable with multiple capacitors in parallel, which can be of any type or value. The capacitance required on the VIN and VBIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} is 1μF and the minimum recommended capacitor for V_{BIAS} is 0.1μF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7μF. Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close to the pins as possible for optimum performance.

18.3 Adjusting Output Voltage

The output voltage of the RT9094A is adjustable from 0.8V to 3.6V using external voltage divider resisters, as shown in Typical Application Circuit. R1 and R2 can be calculated the output voltage. In order to achieve the maximum accuracy specifications, R2 should be ≤ 4.99kΩ.

18.4 Power-Up Sequence Requirement

The RT9094A supports powering on the input VIN, VBIAS, and EN pins in any order without damaging the device. Generally, connecting the EN and VIN for most applications is acceptable, as long as VIN and V_{EN} are greater than the EN threshold (typical 1.1V) and the input ramp rate of VIN and VBIAS is faster than the output settled soft-start ramp rate. If the VIN/BIAS input source ramp rate is slower than the output settled soft-start time, the output will track the input supply ramp-up level and minus the dropout voltage until it reaches the settled output voltage level. In another scenario, if EN is connected to VBIAS, and the provided VIN is present before VBIAS, the output soft-start will proceed as programmed. While VBIAS and V_{EN} are present before VIN is applied and the settled soft-start time has expired, then VOUT tracks the VIN ramp-up. If the soft-start time has not expired, the output tracks the VIN ramp-up until the output reaches the value set by the charging soft-start capacitor.

18.5 Thermal Considerations

Thermal protection limits power dissipation in the RT9094A. When power dissipation on the pass element (P_{DIS} = (V_{IN} – V_{OUT}) x I_{OUT}) is too high and raises the junction operation temperature over 160°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools down by 20°C.

The output is shorted to ground when there is short circuit at the output. This procedure can reduce the chip temperature and provide maximum safety to end users when output short circuit occurs.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under

Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, $\theta_{JA(EVB)}$, is 41.5°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (41.5°C/W) = 2.41W for a WDFN-10L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

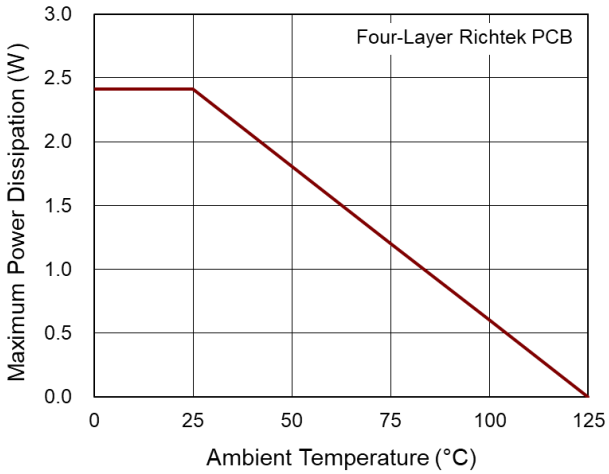


Figure 1. Derating Curve of Maximum Power Dissipation

18.6 Layout Considerations

For best performance of the RT9094A, the following PCB layout suggestions are highly recommended:

- Place the input capacitor as close as possible to IC to minimize the power loop area.
- Minimize the power trace length and avoid using vias for the input and output capacitors connections.

Figure 2 shows the examples for the layout reference, which helps the inductive parasitic components minimization, load transient reduction, and good circuit stability.

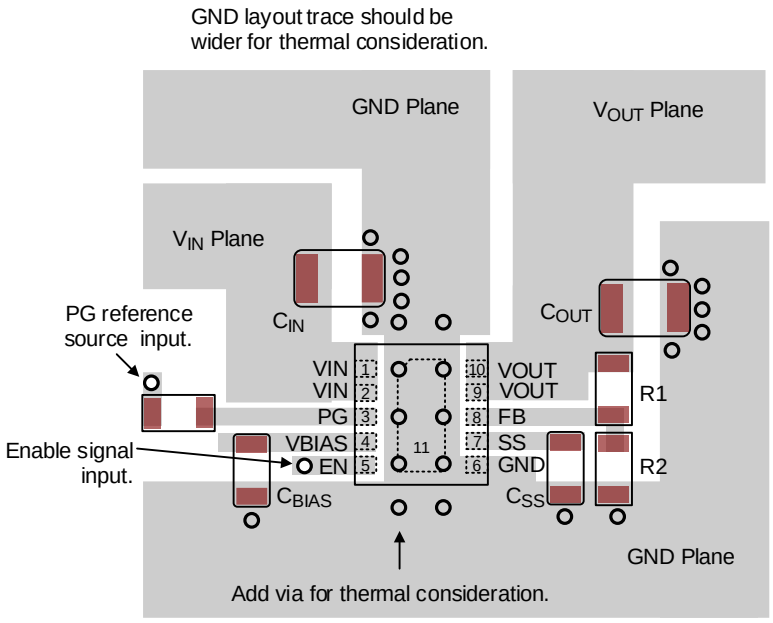
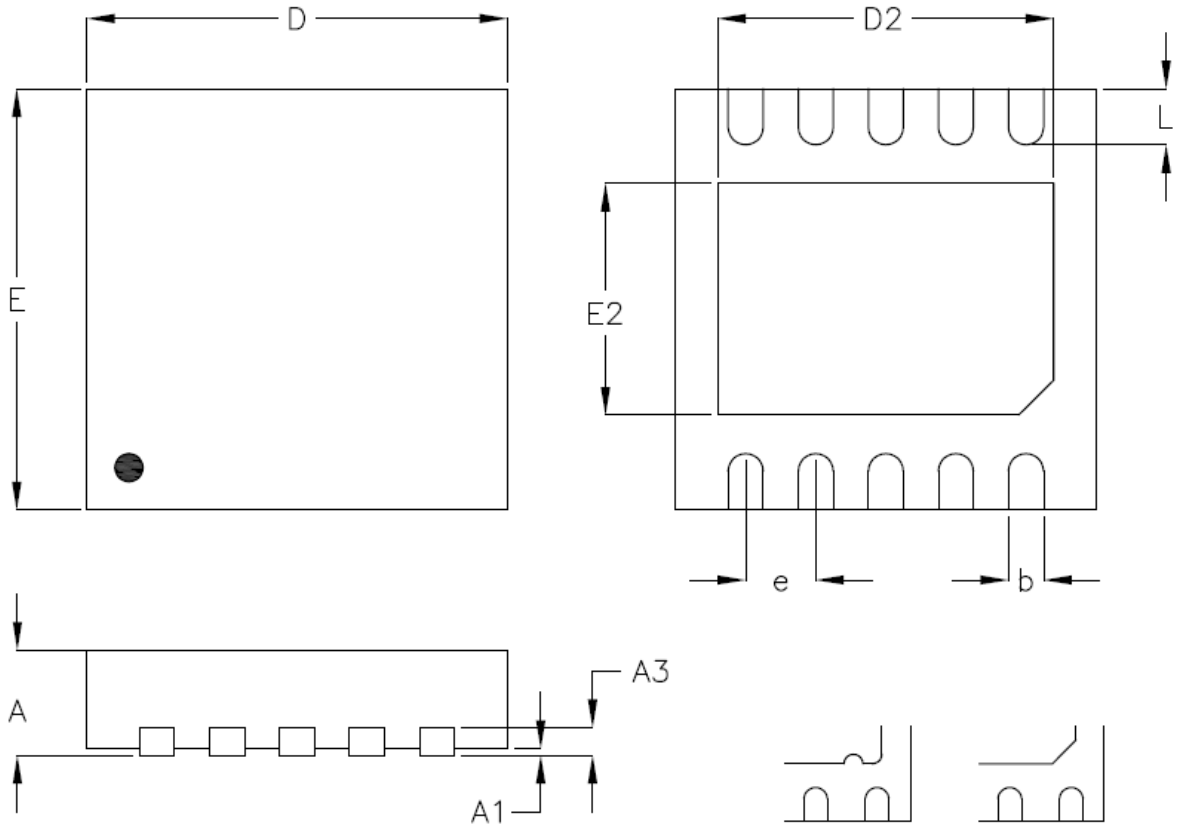


Figure 2. PCB Layout Guide

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Outline Dimension

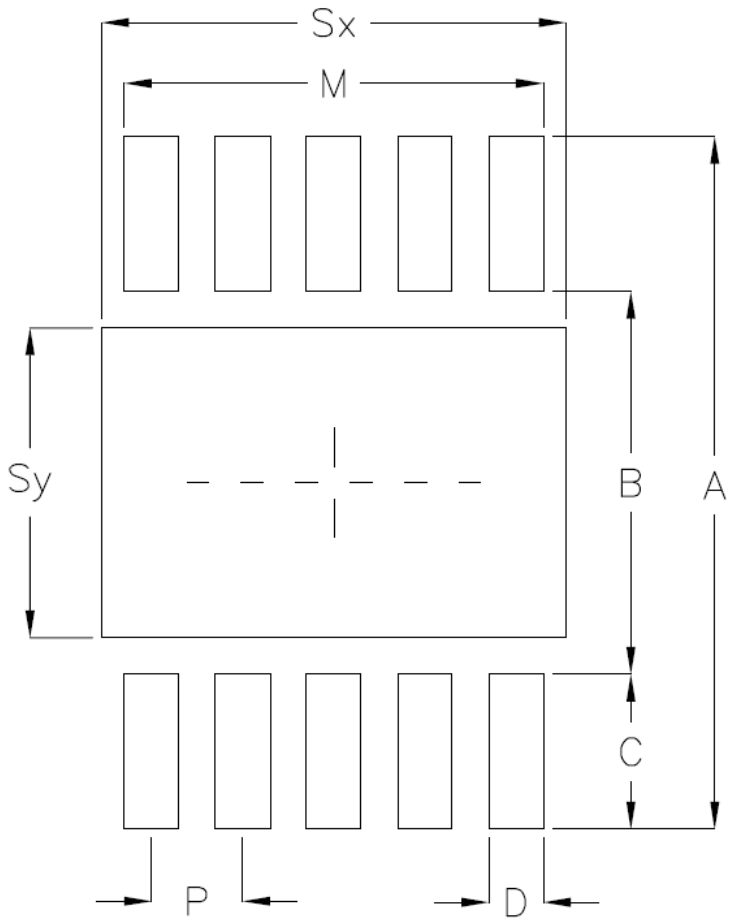


Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

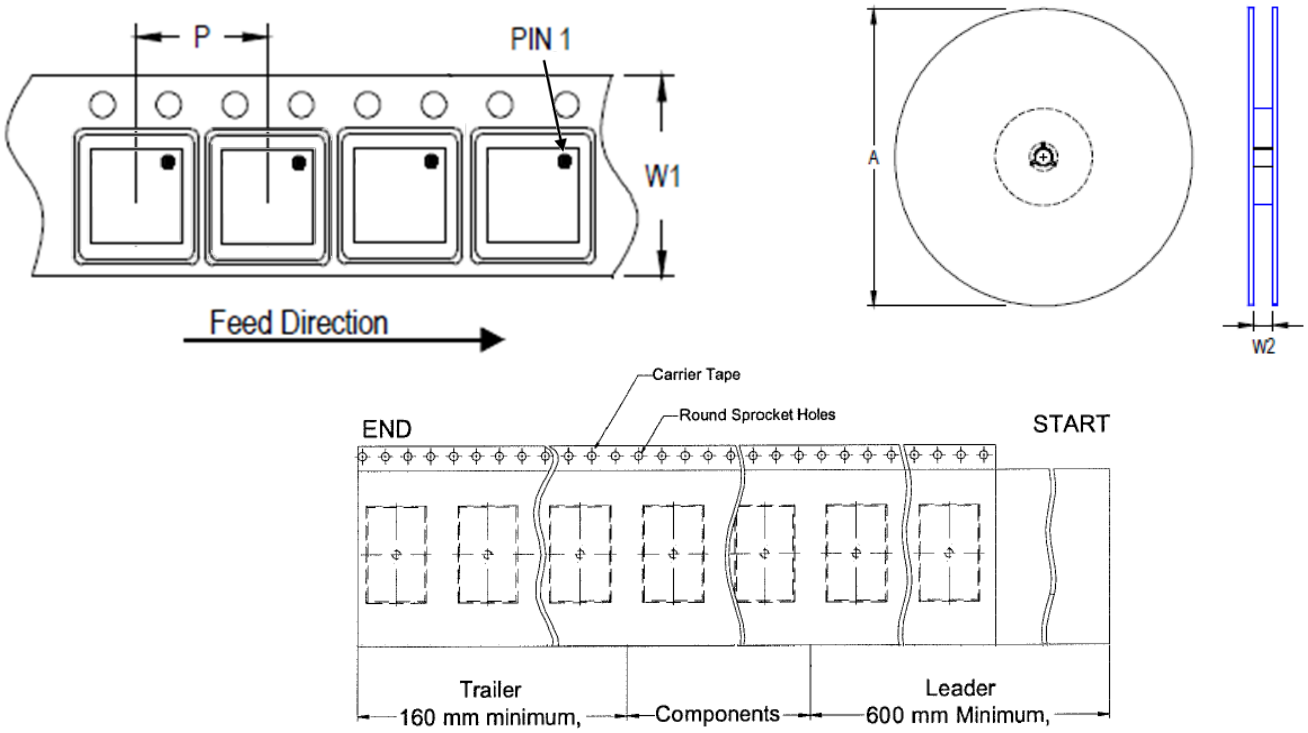
20 Footprint Information



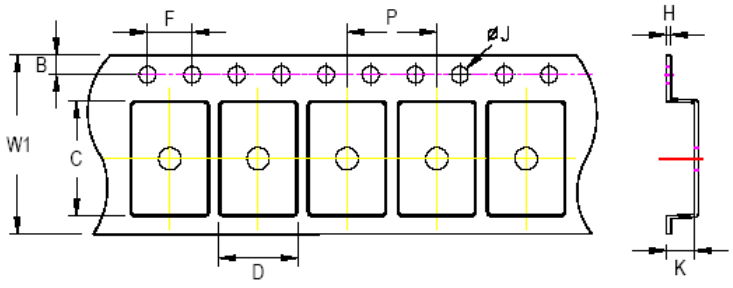
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 3x3	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
00	2022/1/18	Final	
01	2024/3/25	Modify	*General Description on page 1* *Features on page 1* *Ordering Information on page 2* *Electrical Characteristics on page 7* *Operation on page 12, 13* *Application Information on page 14* *Packing Information on page 19, 20, 21*
02	2025/2/13	Modify	*Changed the names PGOOD to PG.* *Ordering Information on page 2* *Application Information on page 13, 15* *Packing Information on page 18, 20, 20*