RICHTEK®

RT9058

36V, 2μA I_Q, 100mA Low Dropout Voltage Linear Regulator

1 General Description

The RT9058 is a low-dropout (LDO) linear voltage regulator featuring high input voltage, low dropout voltage, ultra-low operating current, and compact packaging. With a quiescent current as low as 2μA, the RT9058 is particularly suitable for battery-powered devices.

The RT9058's stability is easily maintained with a variety of output capacitors, including tiny ceramic capacitors, across its wide input voltage range of 3.5V to 36V and load current range of 0mA to 100mA. The RT9058 offers commonly output voltages of 2.5V, 3V, 3.3V, 5V, 6V, 9V, and 12V.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

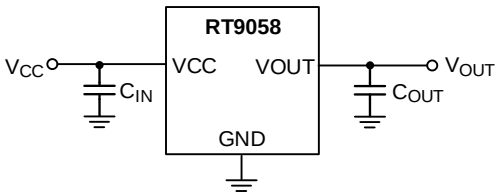
2 Features

- **2μA Quiescent Current**
- **±2% Output Accuracy**
- **100mA Output Current**
- **3.5V to 36V Input Voltage Range**
- **Dropout Voltage:**
  - **0.35V at 10mA/VCC 5V**
  - **0.5V at 10mA/VCC 3.5V**
- **Fixed Output Voltage: 2.5V, 3V, 3.3V, 5V, 6V, 9V, 12V**
- **Stable with Ceramic or Tantalum Capacitors**
- **Current Limit Protection**
- **Over-Temperature Protection**
- **SOT-23-3, SOT-89-3 Packages**

3 Applications

- Portable, Battery Powered Equipment
- Ultra Low Power Microcontrollers
- Notebook Computers

4 Simplified Application Circuit



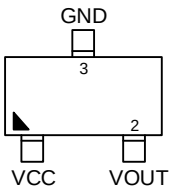
5 Ordering and Marking Information

Part Number	Output Voltage	Package	Marking Information
RT9058-25GV	2.5V	SOT-23-3	00=
RT9058-25GVL		SOT-23-3 (L)	2A=
RT9058-25GX		SOT-89-3	00=
RT9058-30GV	3.0V	SOT-23-3	2H=
RT9058-30GVL		SOT-23-3 (L)	2G=
RT9058-30GX		SOT-89-3	10=
RT9058-33GV	3.3V	SOT-23-3	03=
RT9058-33GVL		SOT-23-3 (L)	2B=
RT9058-33GX		SOT-89-3	01=
RT9058-50GV	5.0V	SOT-23-3	06=
RT9058-50GVL		SOT-23-3 (L)	2C=
RT9058-50GX		SOT-89-3	02=
RT9058-60GV	6.0V	SOT-23-3	0R=
RT9058-60GVL		SOT-23-3 (L)	2D=
RT9058-60GX		SOT-89-3	0D=
RT9058-90GV	9.0V	SOT-23-3	0N=
RT9058-90GVL		SOT-23-3 (L)	2E=
RT9058-90GX		SOT-89-3	0C=
RT9058-C0GV	12.0V	SOT-23-3	0M=
RT9058-C0GVL		SOT-23-3 (L)	2F=
RT9058-C0GX		SOT-89-3	0B=

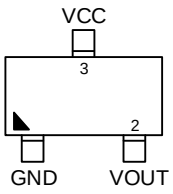
Table of Contents

6 Pin Configuration

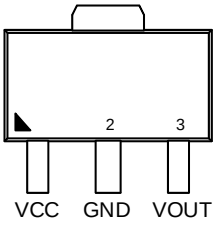
(TOP VIEW)



SOT-23-3



SOT-23-3 (L-Type)

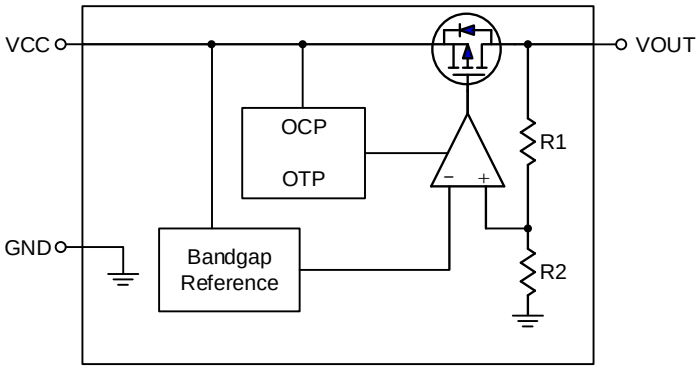


SOT-89-3

7 Functional Pin Description

Pin No.			Pin Name	Pin Function
SOT-23-3	SOT-23-3 (L-Type)	SOT-89-3		
1	3	1	VCC	Supply input. A general 1μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.
2	2	3	VOUT	LDO output pins. A ceramic capacitor of 2.2μF or larger (with 1μF or greater effective capacitance) is required for stability. The output capacitor should be placed as close to the device as possible to minimize the resistive and inductive impedance between the VOUT pin and the load.
3	1	2	GND	The exposed pad should be soldered to a large PCB area and connected to GND to achieve maximum power dissipation.

8 Functional Block Diagram



9 Absolute Maximum Ratings

(Note 1)

- VCC to GND ---------- –0.3V to 40V
- VOUT to GND

  RT9058-C0/RT9058-60/RT9058-90 ---------- –0.3V to 15V

  RT9058-25/RT9058-30/RT9058-33/RT9058-50 ---------- –0.3V to6V
- VOUT to VCC---------- –40V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C

  SOT-23-3 ---------- 0.41W

  SOT-89-3 ---------- 20.6W
- Package Thermal Resistance (Note 2)

  SOT-23-3, θ_{JA} ---------- 243.3°C/W

  SOT-89-3, θ_{JA} ---------- 167.7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model)---------- 2kV

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

10 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VCC ---------- 3.5V to 36V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

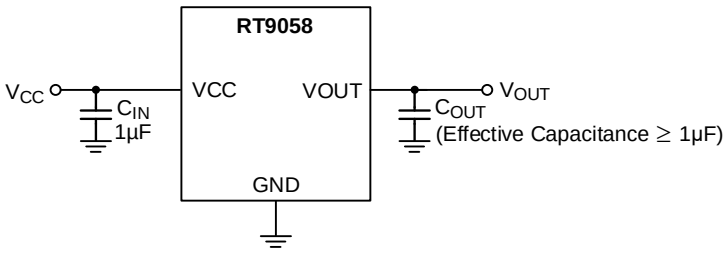
Note 4. The device is not guaranteed to function outside its operating conditions.

11 Electrical Characteristics

((VOUT +1) < VCC < 36V, TA = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Range			2.5	--	12	V
DC Output Accuracy		ILOAD = 10mA	–2	--	2	%
Dropout Voltage		ILOAD = 10mA	--	0.3	0.5	V
VCC Quiescent Current	IQ	ILOAD = 0mA, VOUT ≤ 5.5V, VCC = 12V	--	2	3.5	µA
		ILOAD = 0mA, VOUT > 5.5V, VCC = 12V	--	3.5	5	
Line Regulation		ILOAD = 10mA	--	0.2	0.5	%
Load Regulation		0 < ILOAD < 50mA, VCC = VOUT + 2V	–0.5	--	0.5	%
Output Current Limit		VOUT = 0.5 x VOUT (normal)	115	175	300	mA
Power Supply Rejection Rate	PSRR	f = 100Hz, IOUT = 25mA	--	–70	--	dB
		f = 100kHz, IOUT = 25mA	---	–40	--	
Output Noise Voltage BW = 10Hz - 100kHz	VON	COUT = 1µF	--	27 x VOUT	--	µVRMS
Thermal Shutdown Temperature		ILOAD = 30mA	--	150	--	°C
Thermal Shutdown Hysteresis			--	20	--	°C

12 Typical Application Circuit



For stability requirements, COUT must have a minimum value of 1µF for the RT9058, and this capacitance must be maintained across the entire expected operating temperature range. It should also be located as close as possible to the regulator.

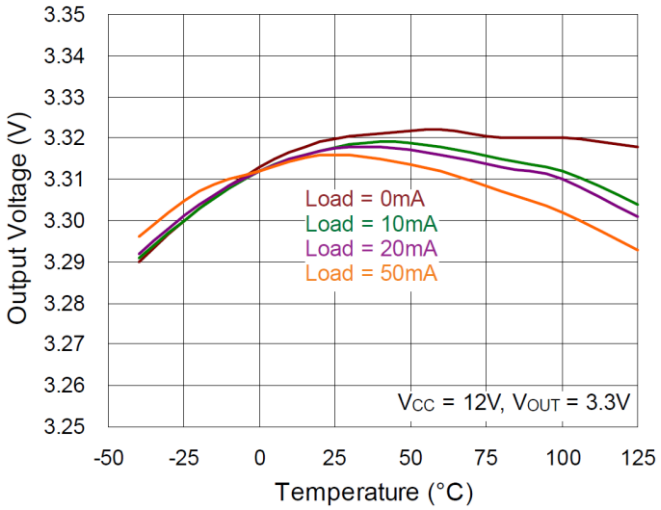
Note 5. All input and output capacitive parameters recommended here refer to the effective capacitance. It is necessary to account for any derating effects, such as DC bias, to accurately consider the effective capacitance.

Table 1. Recommended External Components

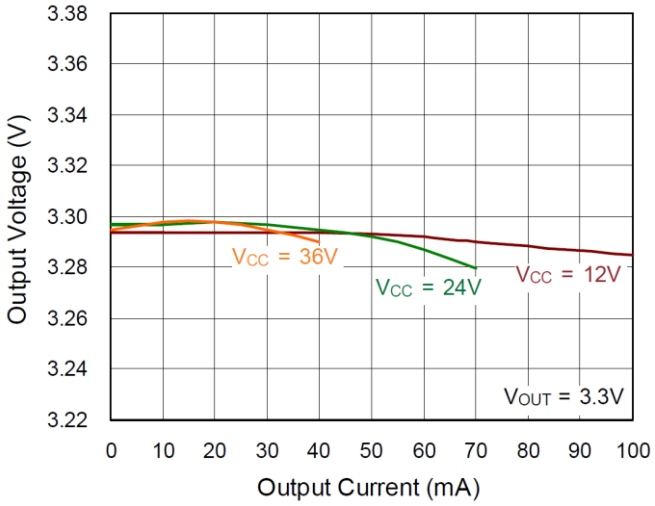
Component	Description	Vendor P/N
CIN	1µF, 50V, X7R, 1206	GCJ31CR71H105KA12 (Murata)
COUT	2.2µF, 16V, X7R, 0805	GGM21BR71C225KA64 (Murata)

13 Typical Operating Characteristics

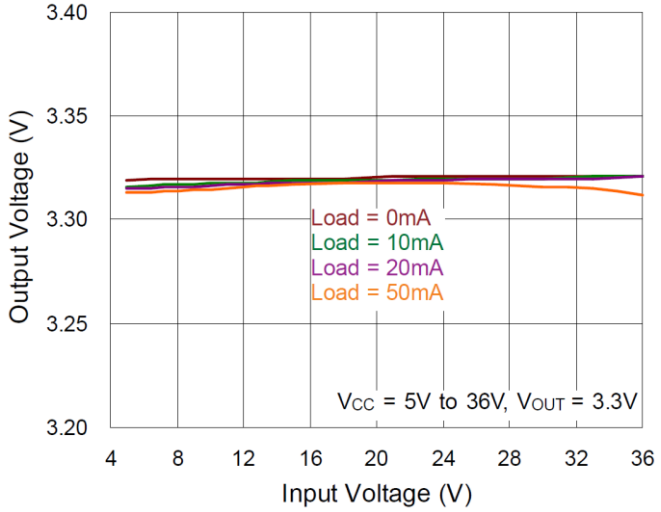
Output Voltage vs. Temperature



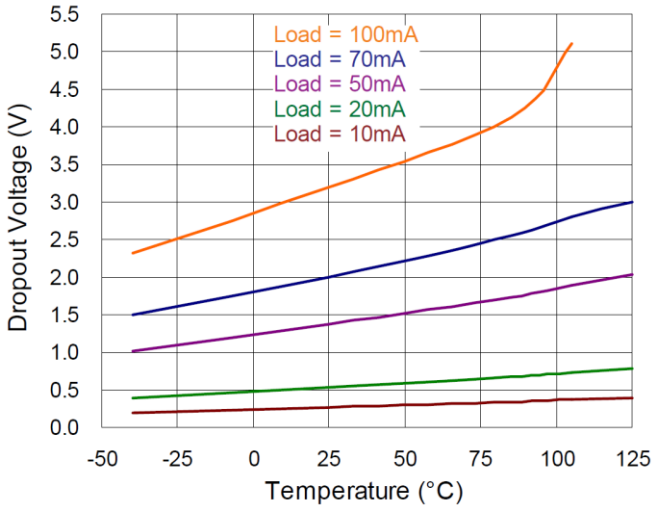
Output Voltage vs. Output Current



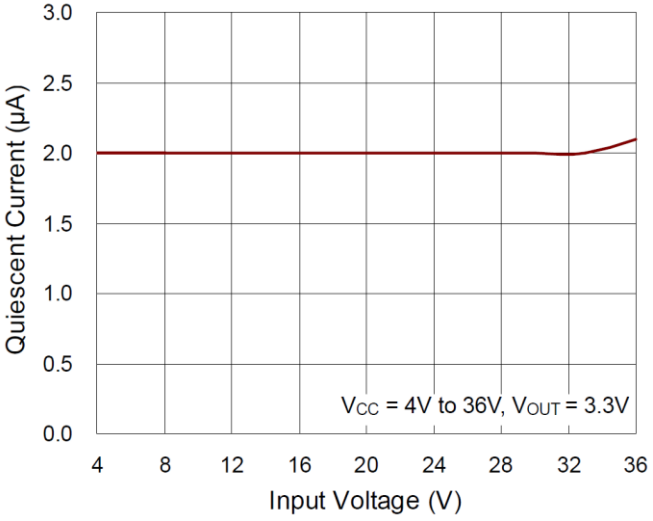
Output Voltage vs. Input Voltage



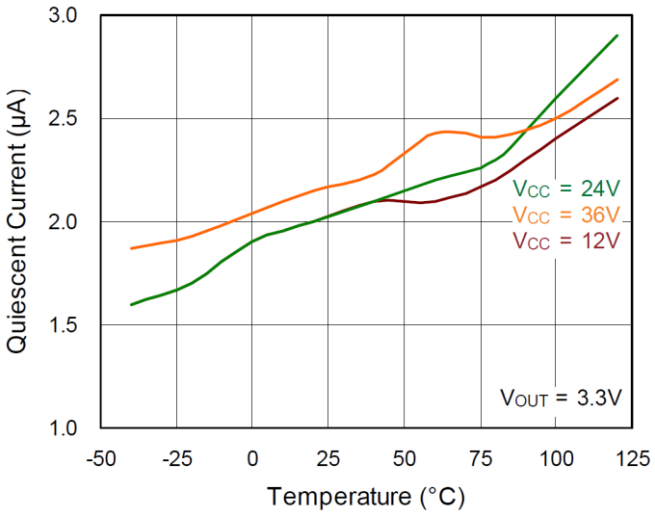
Dropout Voltage vs. Temperature



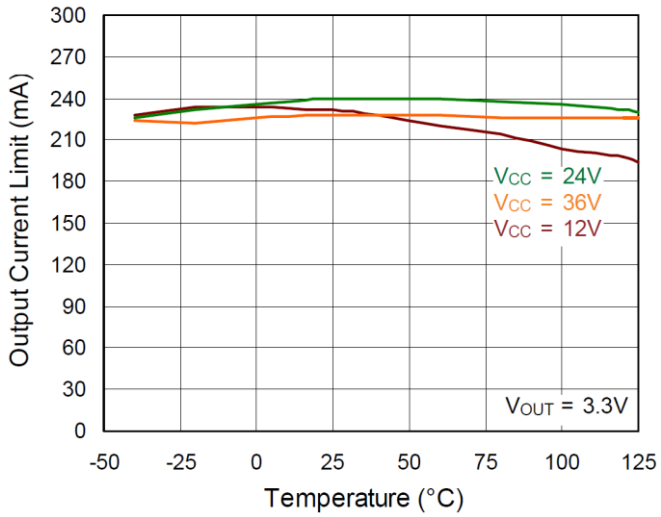
Quiescent Current vs. Input Voltage



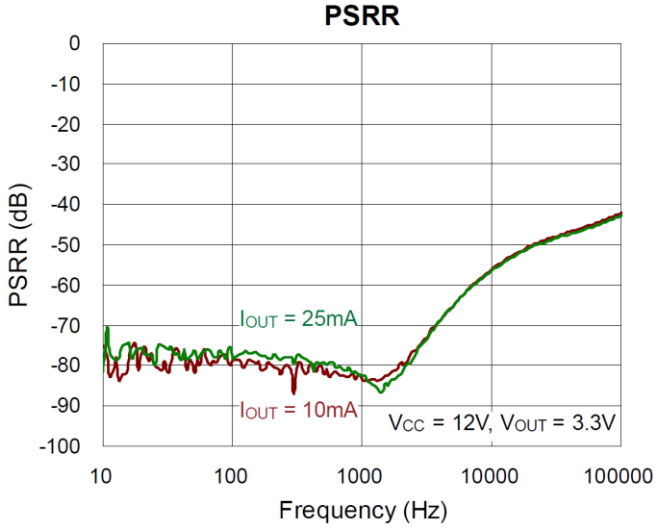
Quiescent Current vs. Temperature



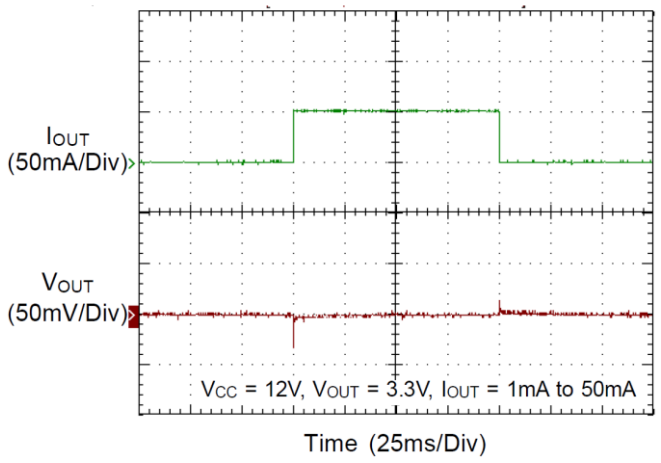
Output Current Limit vs. Temperature



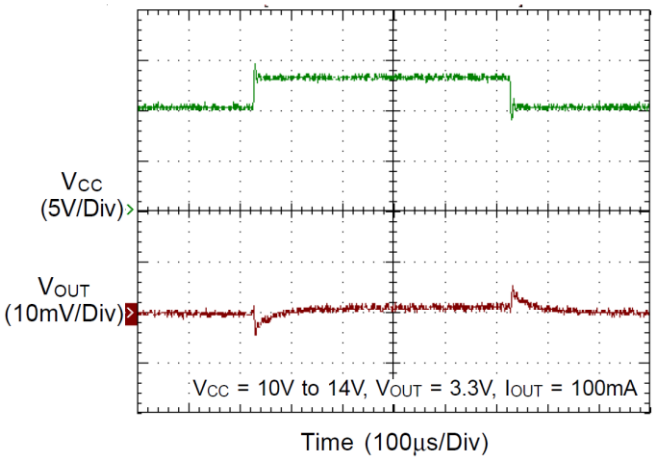
PSRR



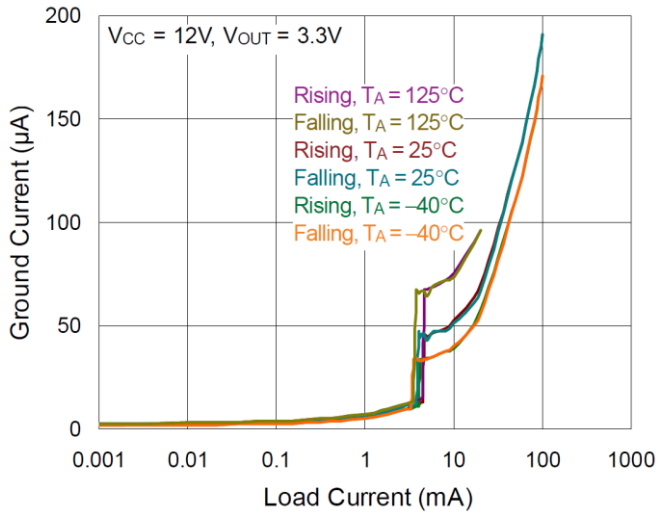
Load Transient Response



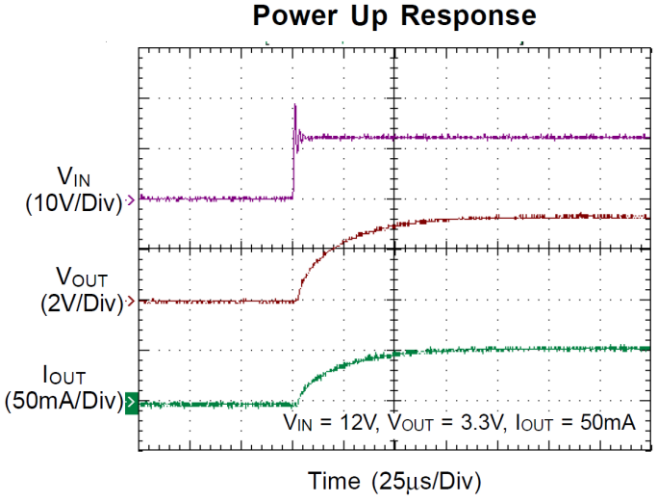
Line Transient Response



Ground Current vs. Load Current



Power Up Response



14 Operation

The RT9058 is a high-input-voltage linear regulator designed specifically to minimize the need for external components. The input voltage range extends from 3.5V to 36V. The minimum output capacitance required for stable operation is an effective 1μF, considering the capacitor's temperature and voltage coefficient. For normal power-on operation, the slew rate of the VCC rising time should be slower than 45mV/μs.

14.1 Error Amplifier

The Error Amplifier compares the feedback voltage from an internal voltage divider with an internal reference voltage. It then adjusts the gate voltage of the P-MOSFET to maintain output voltage regulation.

14.2 Current Limit Protection

The RT9058 features a current limit function to prevent damage from output overload or short-circuit conditions. The output current is monitored by an internal sensing transistor.

14.3 Over-Temperature Protection

The over-temperature protection function shuts off the P-MOSFET when the internal junction temperature exceeds 150°C (typical) or the output current exceeds 4mA. Once the junction temperature decreases by approximately 20°C, the regulator will automatically resume normal operation.

15 Application Information

(Note 6)

Like any low-dropout linear regulator, the RT9058 requires proper selection of external input and output capacitors for stability and performance. An input capacitor of 1μF or larger should be used and placed close to the IC's VCC and GND pins. Any output capacitor that meets the minimum Equivalent Series Resistance (ESR) of 1mΩ and has an effective capacitance greater than 1μF may be used. It should be placed close to the IC's VOUT and GND pins.

15.1 C_{IN} and C_{OUT} Selection

The RT9058 is designed to support low-series-resistance (ESR) ceramic capacitors. Because of their good capacitive stability across different temperatures, X7R, X5R, and COG-rated ceramic capacitors are recommended. The use of Y5V-rated capacitors is not recommended due to their large capacitance variations.

However, the capacitance of ceramic capacitors varies with operating voltage and temperature, which design engineers need to consider. It is customary to derate ceramic capacitors by 50%. To ensure stability, an output ceramic capacitor of 2.2μF or greater (or 1μF of effective capacitance) is suggested. The input capacitor should be selected to minimize the transient voltage drop during load current steps; at least a 2.2μF input capacitor is highly recommended to maintain minimal input impedance. If there is significant inductance in the traces between the RT9058 input pin and the power supply, a fast load transient may induce voltage ringing at the VIN level that exceeds the device's absolute maximum rating, potentially damaging it. Adding more input capacitors can help to restrict the ringing and keep it within the device's absolute maximum ratings. These capacitors should be placed as close as possible to the pins for optimal performance and stability.

15.2 Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at a specific output current. The dropout voltage VDROP also can be expressed as the voltage drop on the pass-FET at a specific output current (I_{RATED}) when the pass-FET is fully operating in the ohmic region and can be characterized as a resistance $R_{DS(ON)}$. Thus, the dropout voltage can be defined as $V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$. For normal operation, the suggested LDO operating range is $V_{IN} > V_{OUT} + V_{DROP}$ to ensure good transient response and PSRR performance. However, operation in the ohmic region will severely degrade the performance severely.

15.3 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOT-23-3 package, the thermal resistance, θ_{JA}, is 243.3°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a SOT-89-3 package, the thermal resistance, θ_{JA}, is 167.7°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (243.3°C/W) = 0.41W for a SOT-23-3 package.

$P_{D(MAX)}$ = (125°C – 25°C) / (167.7°C/W) = 0.6W for a SOT-89-3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

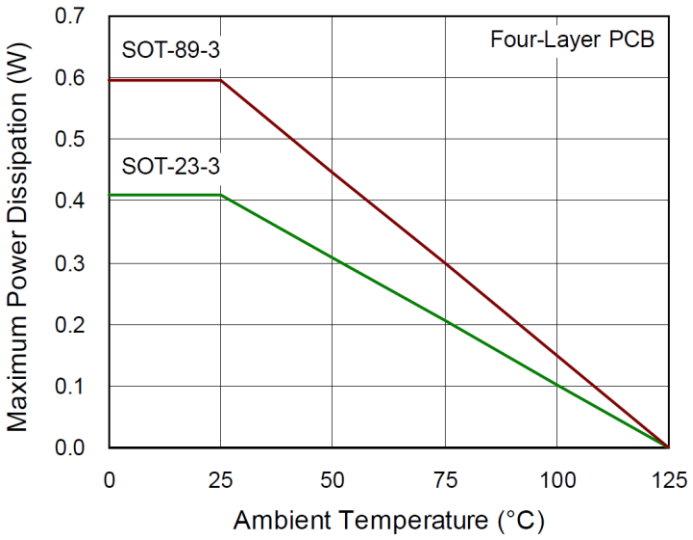
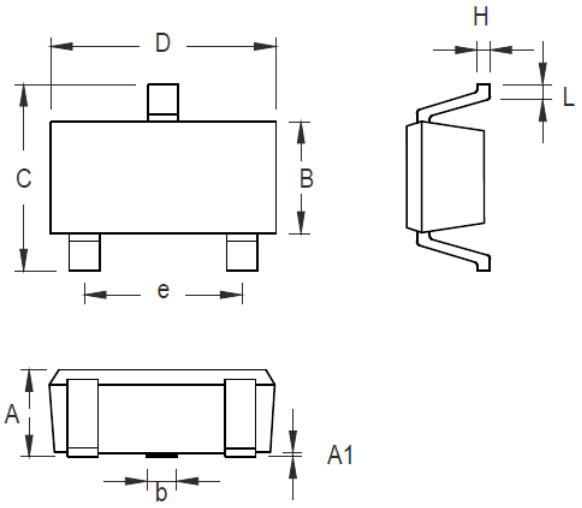


Figure 1. Derating Curve of Maximum Power Dissipation

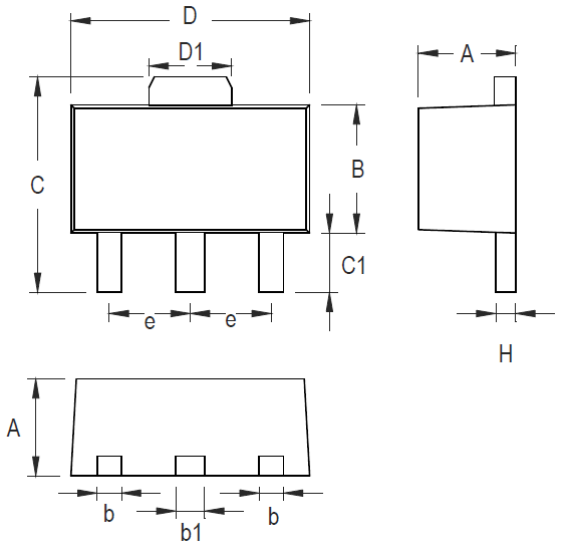
Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

16 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.508	0.014	0.020
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	1.803	2.007	0.071	0.079
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

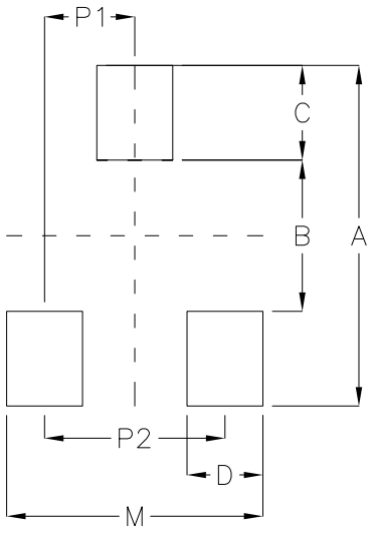
SOT-23-3 Surface Mount Package



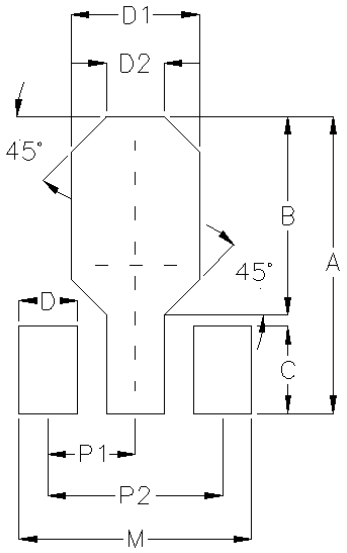
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.397	1.600	0.055	0.063
b	0.356	0.483	0.014	0.019
B	2.388	2.591	0.094	0.102
b1	0.406	0.533	0.016	0.021
C	3.937	4.242	0.155	0.167
C1	0.787	1.194	0.031	0.047
D	4.394	4.597	0.173	0.181
D1	1.397	1.753	0.055	0.069
e	1.448	1.549	0.057	0.061
H	0.356	0.432	0.014	0.017

3-Lead SOT-89 Surface Mount Package

17 Footprint Information



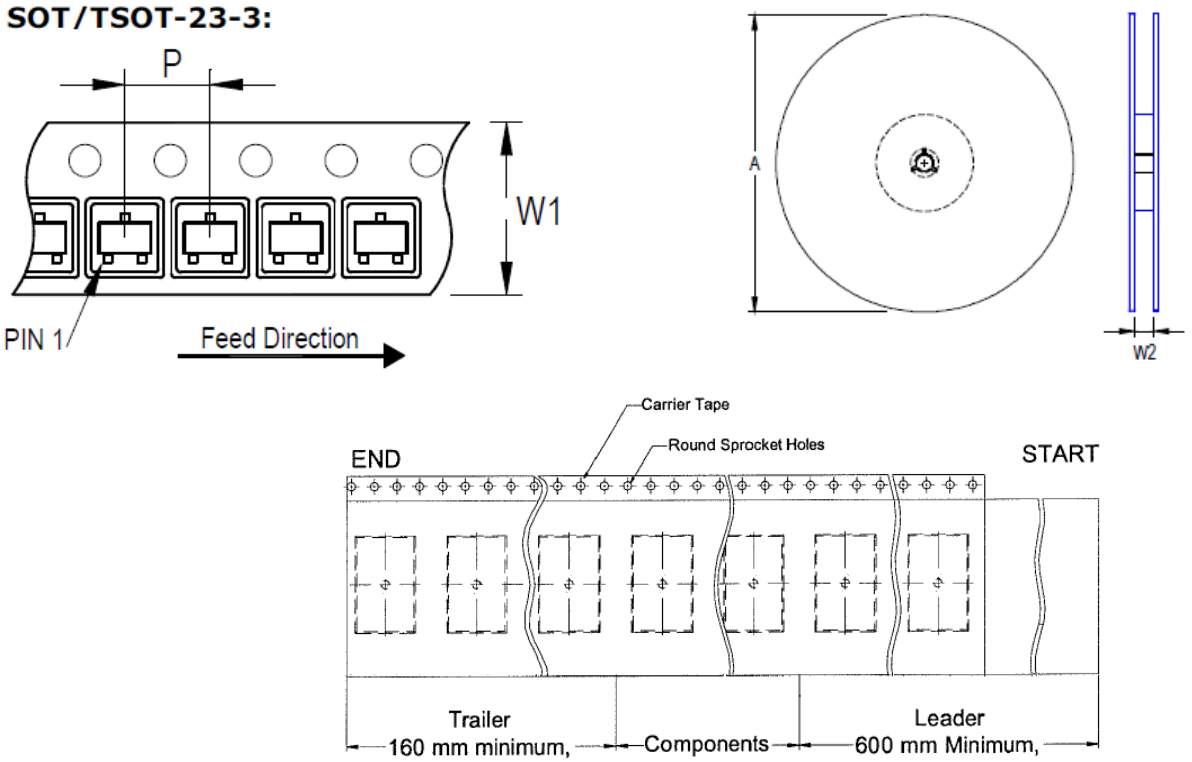
Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P1	P2	A	B	C	D	M	
TSOT-23/SOT-23	3	0.95	1.90	3.60	1.60	1.00	0.80	2.70	±0.10



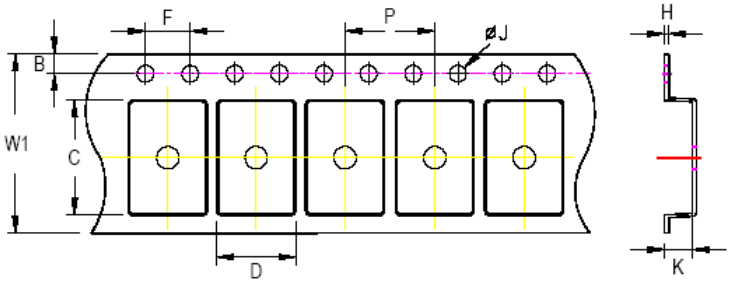
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P1	P2	A	B	C	D	D1	D2	M	
SOT-89	3	1.50	3.00	5.10	3.40	1.50	1.00	2.20	1.00	4.00	±0.10

18 Packing Information

18.1 Tape and Reel Data - SOT-23-3



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT/TSOT-23-3	8	4	180	7	3,000	160	600	8.4/9.9



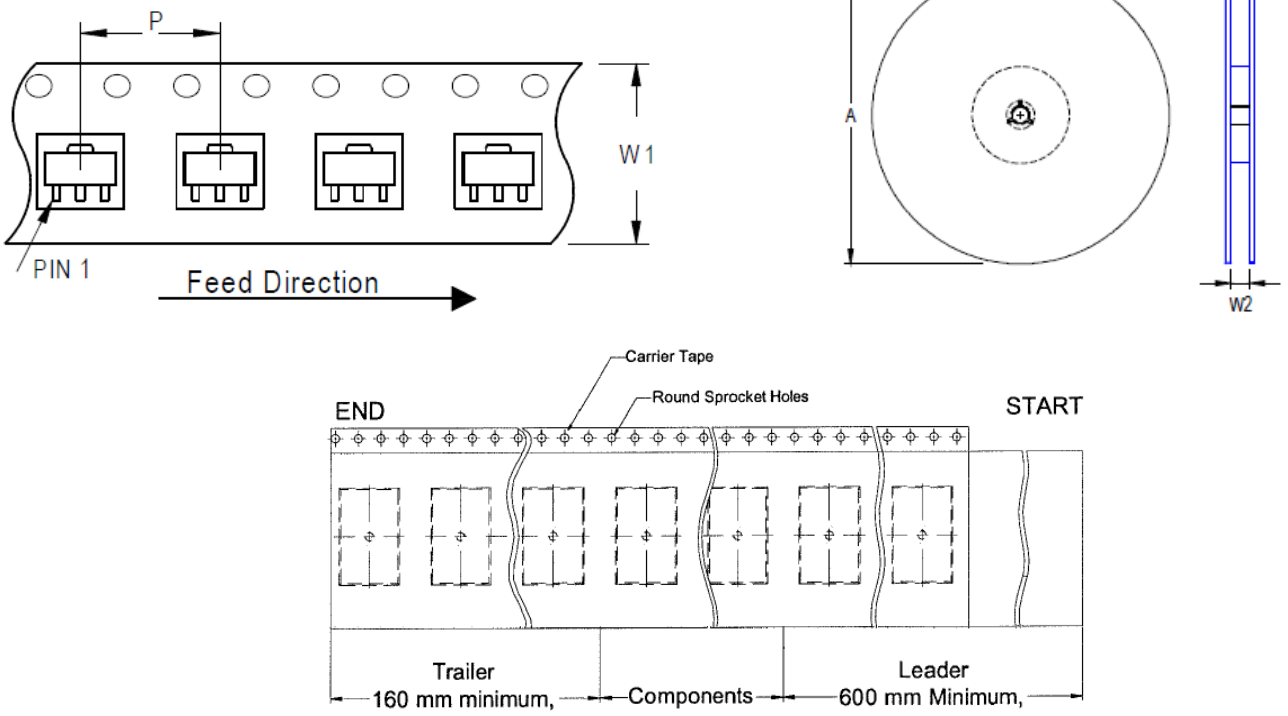
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

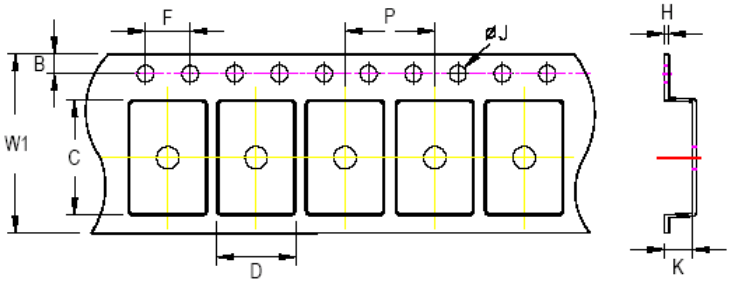
Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

18.2 Tape and Reel Data - SOT-89-3

SOT-89:



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT-89	12	8	180	7	1,000	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

18.3 Tape and Reel Packing - SOT-23-3

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT/TSOT-23-3	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

18.4 Tape and Reel Packing - SOT-89-3

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-89	7”	1,000	Box A	3	3,000	Carton A	12	36,000
			Box E	1	1,000	For Combined or Partial Reel.		

18.5 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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19 Datasheet Revision History

Version	Date	Description	Item
03	2024/3/26	Modify	General Description on P1 Functional Pin Description on P4 Typical Application Circuit on P7 Application Information on P11 Footprint Information on P15, 16 Packing Information on P17 to 21