

10A, Fully Integrated Synchronous Boost Converter

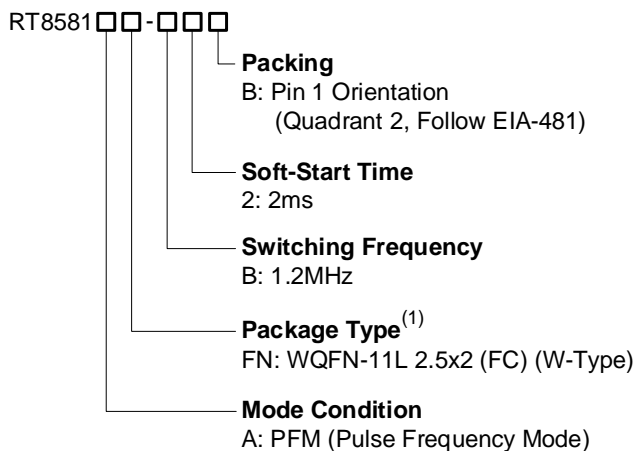
1 General Description

The RT8581 is a boost converter that integrates built-in power transistors, synchronous rectification, and low supply current to provide a compact solution for systems using advanced Li-Ion batteries. The RT8581 is capable of supplying significant energy when the battery voltage falls below the voltage required by system power ICs.

The RT8581 is designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below the system's minimum voltage requirement.

The RT8581 is available in the WQFN-11L 2.5x2 (FC) package. The recommended junction temperature range spans from -40°C to 125°C, while the ambient temperature range extends from -40°C to 85°C.

2 Ordering Information



Note 1.

Richtek products are Richtek Green Policy compliant and marked with ⁽¹⁾ indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

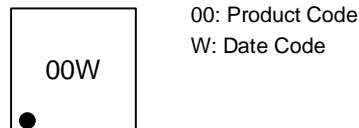
3 Features

- **Input Voltage Range: 2V to 12V**
- **Output Voltage Range: 4.5V to 12.6V**
- **Up to 94.5% Efficiency at $V_{IN} = 5V$, $V_{OUT} = 12V$, and $I_{OUT} = 1A$**
- **Soft-Start-Up Time (< 2msec)**
- **Adjustable Peak Current Limit: Up to 10A (Typical)**
- **PFM Operation Mode at Light Load**
- **Internal Synchronous Rectifier**
- **Overvoltage Protection at 13.2V**
- **Over-Temperature Protection**
- **WQFN-11L 2.5x2 (FC) Package**

4 Applications

- RF PA Drivers
- NAND Flashes
- Backup Power
- Motor Drivers
- Optical Sensor Drivers
- Portable POS Terminals

5 Marking Information



6 Simplified Application Circuit

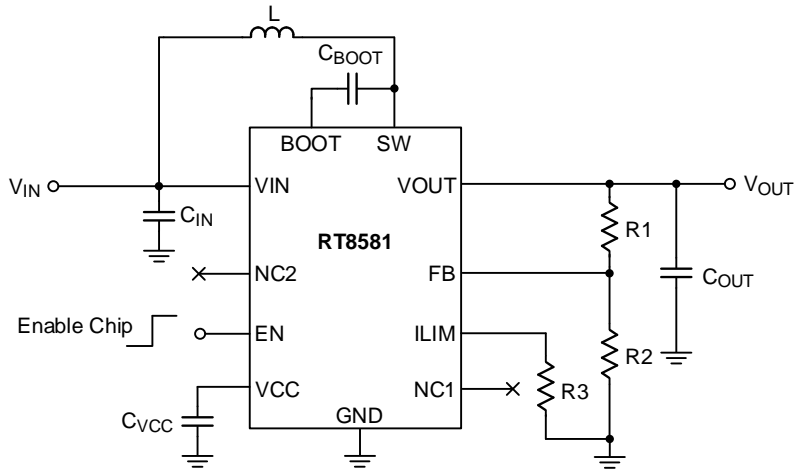
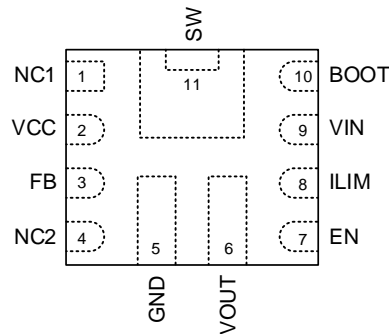


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7 Pin Configuration

(TOP VIEW)

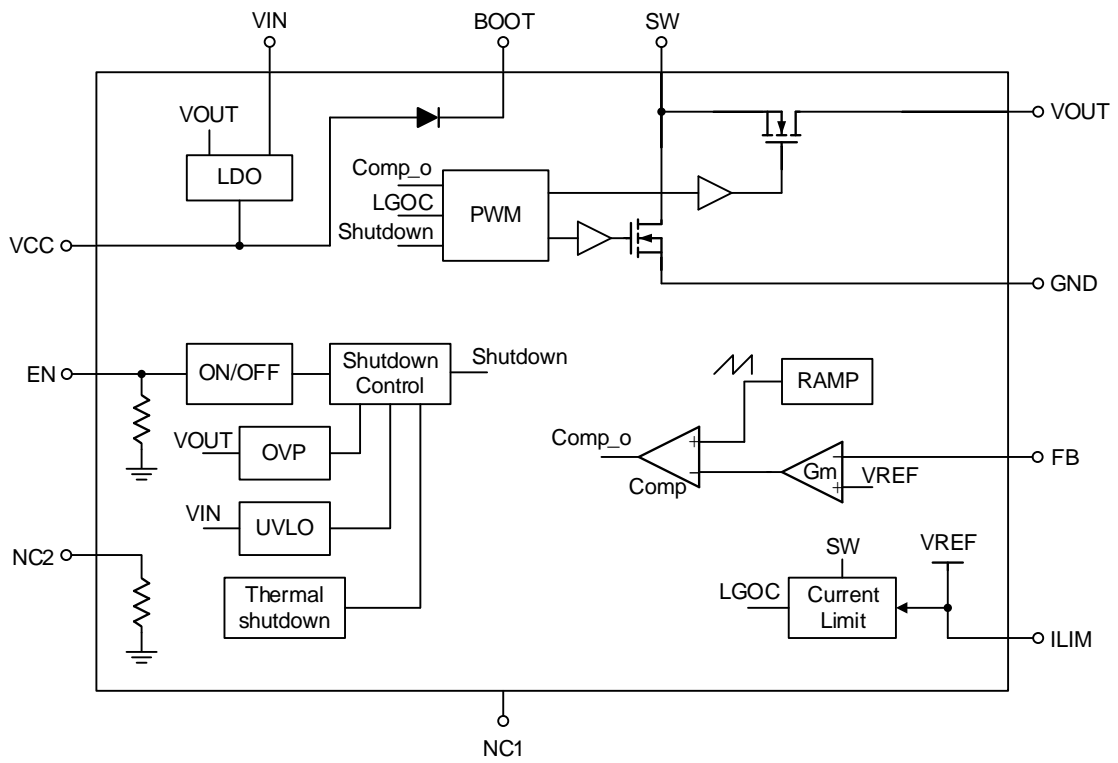


WQFN-11L 2x2.5 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	NC1	No internal connection.
2	VCC	Output of the internal regulator. A ceramic capacitor of more than 1 μ F is required between this pin and ground.
3	FB	Output voltage feedback. A resistor divider connecting to this pin sets the output voltage.
4	NC2	No internal connection.
5	GND	Ground. This is power and signal ground reference for the chip. The C _{OUT} bypass capacitor should be returned with the shortest path possible to this pin.
6	VOUT	Output voltage. Place C _{OUT} as close as possible to the device.
7	EN	Enable input. When this pin is set to high, the circuit is enabled.
8	ILIM	Adjustable switching peak current limit. An external resistor should be connected between this pin and the GND pin.
9	VIN	Input voltage. This pin has to connect to input power and is used to supply chip internal power.
10	BOOT	Power supply for high-side MOSFET gate driver. A capacitor must be connected between this pin and the SW pin.
11	SW	Switching node. The power inductor should be connected between SW and power input.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN, SW, VOUT, NC1 ----- -0.3V to 14.5V
- EN, VCC, ILIM, FB, NC2 ----- -0.3V to 6V
- BOOT ----- -0.3V to SW+6V
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 WQFN-11L 2.5x2 (FC) ----- 1.89W
- Package Thermal Resistance (Note 3)
 WQFN-11L 2.5x2 (FC), θ_{JA} ----- 52.92°C/W
 WQFN-11L 2.5x2 (FC), θ_{JC} ----- 4.74°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- -40°C to 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 4)
 HBM (Human Body Model) ----- $\pm 2\text{kV}$
 CDM (Charged-Device Model) ----- $\pm 500\text{V}$

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at $T_A = 25^\circ\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Input Voltage Range (Boost Mode) ----- 2V to $V_{OUT(SET)} - 0.2\text{V}$
- Output Voltage Range ----- 4.5V to 12.6V
- Input Capacitor (Effective value), $C_{IN(\text{Min})}$ ----- 10 μF
- Output Capacitor (Effective value), C_{OUT} ----- 10 μF to 1000 μF
- Inductance (Effective value), L
 Switching Frequency ----- 1 μH to 4.7 μH
- Ambient Temperature Range ----- -40°C to 85°C
- Junction Temperature Range ----- -40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

($V_{IN} = 2.5V$ to $5.5V$, $V_{OUT} = 5V$ to $12.6V$, $C_{IN} = 10\mu F$, $C_{OUT} = 66\mu F$, $L1 = 4.7\mu H$, Frequency = $1.2MHz$. All typical (Typ) limits apply for $T_A = 25^\circ C$, unless otherwise specified. All minimum (Min) and maximum (Max) apply over the full operating ambient temperature range ($-40^\circ C \leq T_A \leq 125^\circ C$).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Input Voltage Range	V_{IN}		2	--	12	V
V_{IN} UVLO Threshold	V_{UVLO}	Rising	1.8	1.9	2	V
		Falling	1.7	1.8	1.9	
V_{IN} UVLO Hysteresis	V_{UVLO_HYS}		--	100	--	mV
VCC Regulation	VCC	$V_{IN} = 8V$, $I_{CC} = 2mA$	4.75	5	5.25	V
VCC UVLO Threshold	V_{CC_UVLO}	VCC falling	--	2.5	--	V
Into V_{IN} Operating Quiescent Current	I_Q (non-switching)	IC enabled, no load, $V_{IN} = 2.7V$ to $5.5V$, $V_{FB} = 1.3V$, $V_{OUT} = 12V$ (Temp = $-40^\circ C$ to $85^\circ C$)	--	3	5	μA
Into V_{OUT} Standby Mode Quiescent Current	I_{Q_STBY} (non-switching)	IC enabled, no load, $V_{IN} = 2.7V$ to $5.5V$, $V_{FB} = 1.3V$, $V_{OUT} = 12V$ (Temp = $-40^\circ C$ to $85^\circ C$)	--	30	50	μA
Shutdown Current	ISD	IC disabled, $V_{IN} = 2.7V$ to $5.5V$ (Temp = $-40^\circ C$ to $85^\circ C$)	--	1	3	μA
Output						
Output Voltage Range	V_{OUT}		4.5	--	12.6	V
Reference Voltage at FB pin	V_{FB}	PWM mode	1.188	1.212	1.236	V
		PFM mode	--	1.224	--	
Leakage Current into FB pin	I_{LK_FB}	$V_{FB} = 1.2V$	--	--	100	nA
Output Overvoltage Protection Threshold	V_{OVP}	V_{OUT} rising	12.7	13.2	13.6	V
Output Overvoltage Protection Hysteresis	V_{OVP_HYS}	V_{OUT} falling below V_{OVP}	--	0.25	--	V
Soft-Start Time	tSS1	C_{OUT} (Effective) = $47\mu F$, $I_{OUT} = 0A$	--	2	--	ms
Power Switch						
On-Resistance of High-Side MOSFET	$R_{DS(on)_H}$	$V_{CC} = 5V$	--	27	44	$m\Omega$
On-Resistance of Low-Side MOSFET	$R_{DS(on)_L}$		--	19	31	
Switching Frequency						
Switching Frequency Range	fsw	$V_{IN} = 5V$, $V_{OUT} = 12V$	1.08	1.2	1.32	MHz
Minimum On-Time	tON_min	$V_{CC} = 5V$	--	90	180	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit						
Peak Current Limit	ILIM	RILIM = 127kΩ	7.3	8.1	8.9	A
		RILIM = 100kΩ	9	10	12	
Internal Reference Voltage at the ILIM Pin	VILIM		--	1.212	--	V
Enable, Mode						
Input Voltage Logic-Low	VIL	VIN = 5V, VOUT = 12V	--	--	0.4	V
Input Voltage Logic-High	VIH		0.8	--	--	
EN Pull-Down Resistor	REN		--	700	--	kΩ
MODE Pull-Down Resistor	RMODE		--	420	--	kΩ
Over-Temperature Protection						
Over-Temperature Threshold	TOTP	TJ rising	--	150	--	°C
Over-Temperature Hysteresis	TOTP_HYS	TJ falling below Tsd	--	20	--	

13 Typical Application Circuit

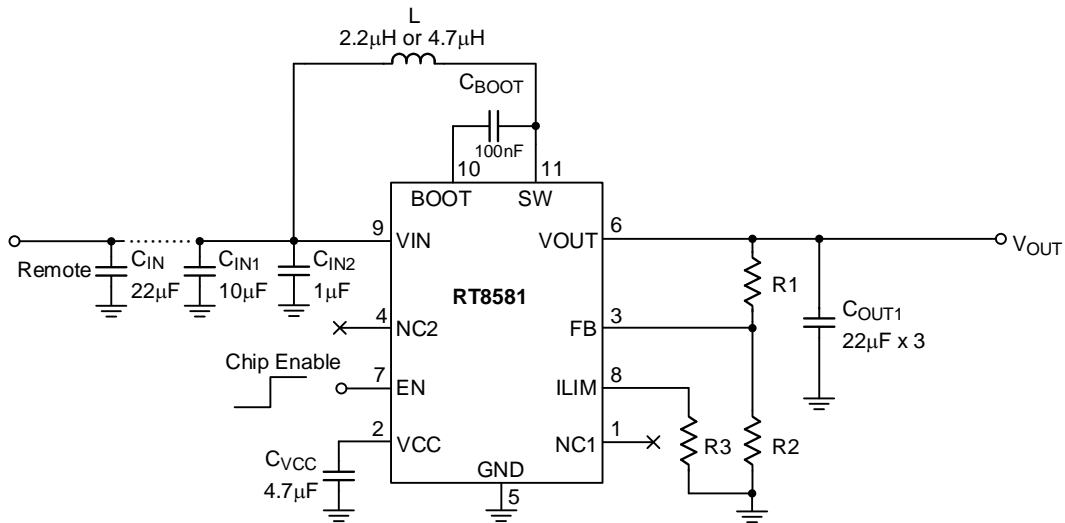
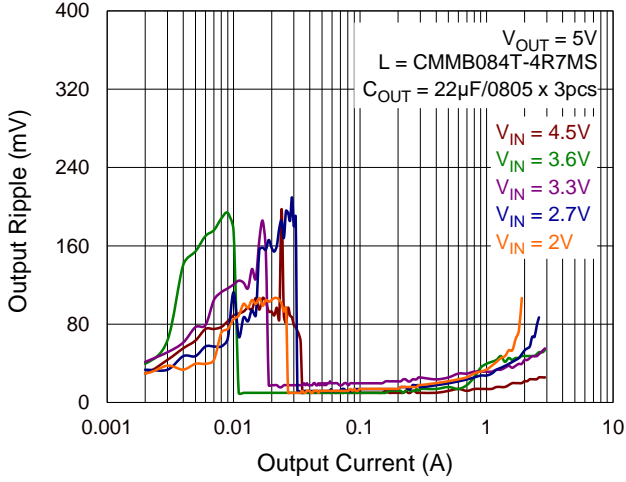


Table 1. Recommended Components Information

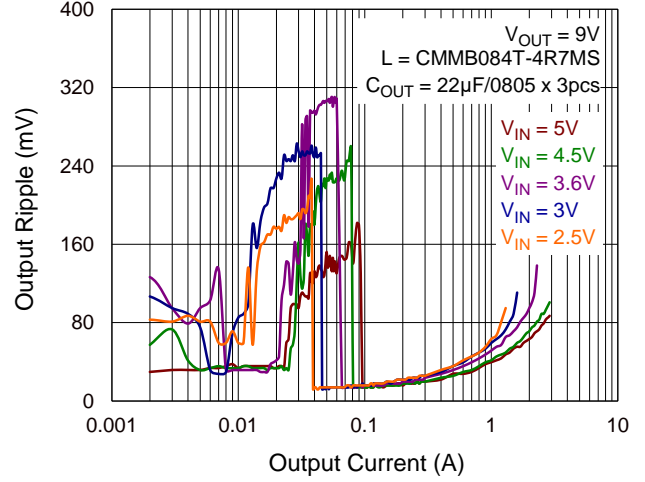
Reference	Part Number	Description	Package	Manufacturer
C _{IN} (Remote)	GRM31CR61C476ME44	47μF/16V/X5R	1206	Murata
C _{IN1}	GRM21BR61E226ME44	22μF/25V/X5R	0805	Murata
C _{IN2}	GRM155R61C105KA12	1μF/16V/X5R	0402	Murata
C _{OUT1}	GRM21BR61E226ME44	22μF/25V/X5R, 3pcs	0805	Murata
C _{BOOT}	GRM155R61H104KE19	100nF/50V/X5R	0402	Murata
C _{VCC}	GRM185R61C475KE11	4.7μF/10V/X5R	0603	Murata
L	CMME053T- 4R7MS	4.7μH/I _{sat} (Max) = 5.1A	5050	Cyntec
	CMME053T- 2R2MS	2.2μH/I _{sat} (Max) = 7A	5050	Cyntec
	CMMB084T- 4R7MS	4.7μH/I _{sat} (Max) = 10.8A	8080	Cyntec
	CMMB084T- 2R2MS	2.2μH/I _{sat} (Max) = 12.7A	8080	Cyntec

14 Typical Operating Characteristics

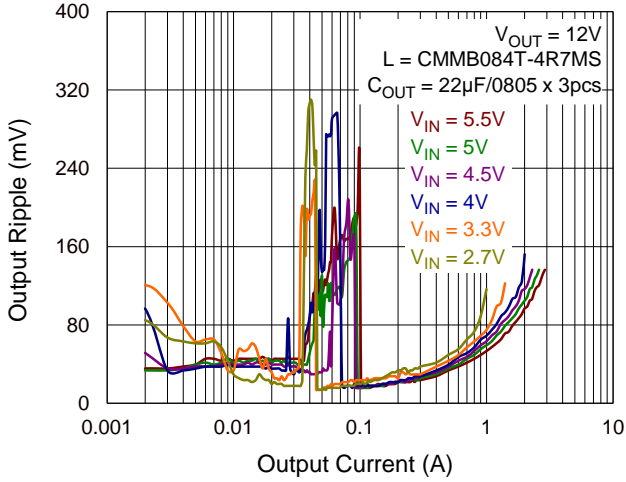
Output Ripple vs. Output Current



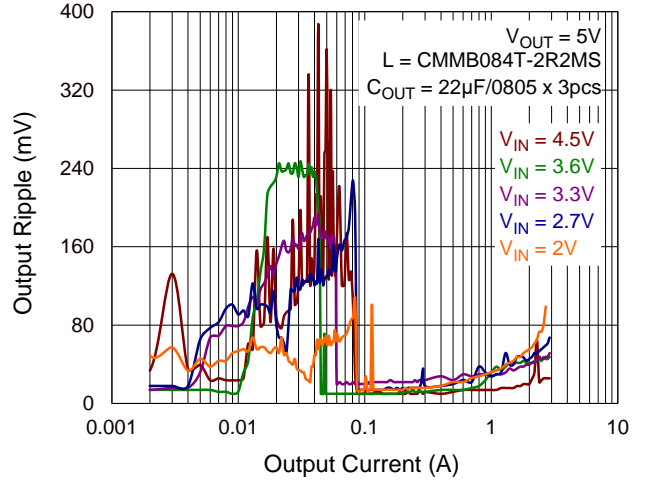
Output Ripple vs. Output Current



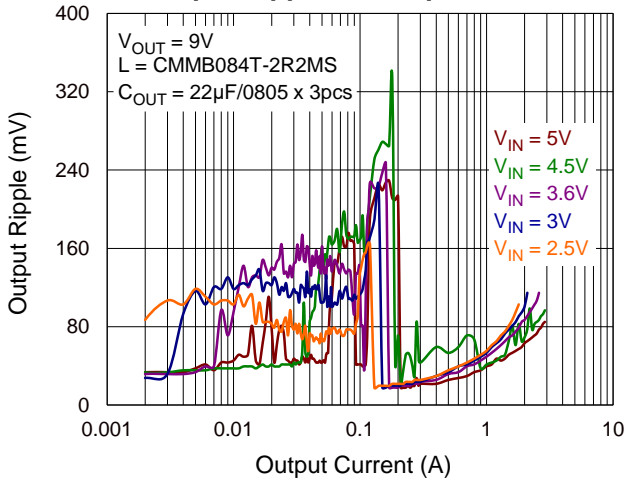
Output Ripple vs. Output Current



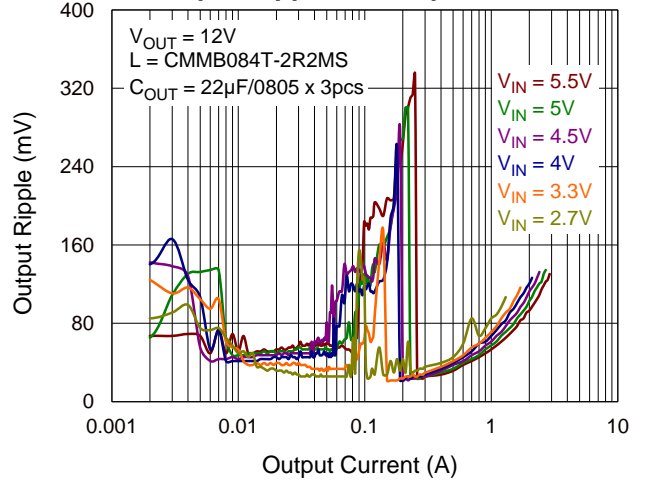
Output Ripple vs. Output Current

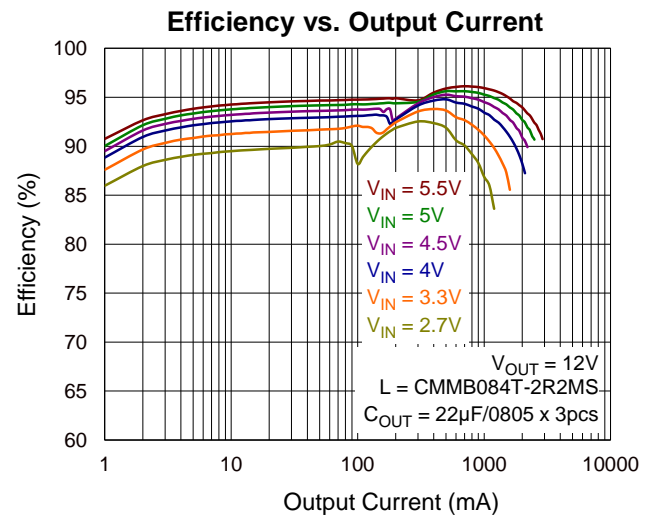
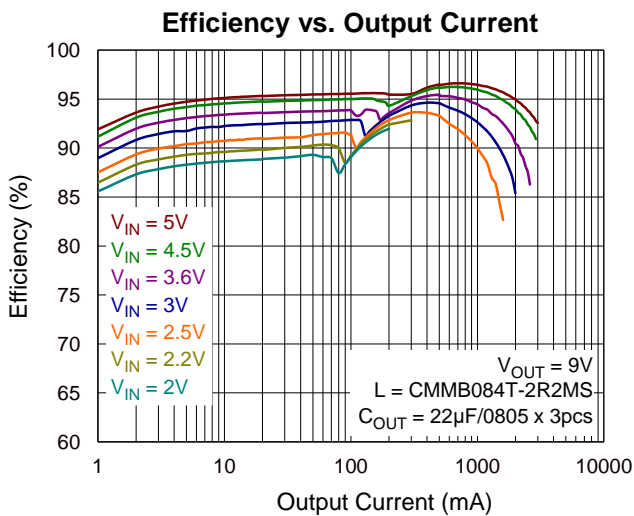
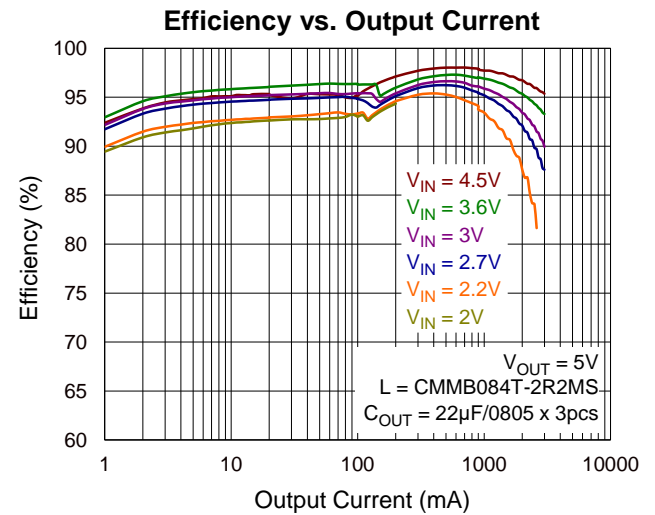
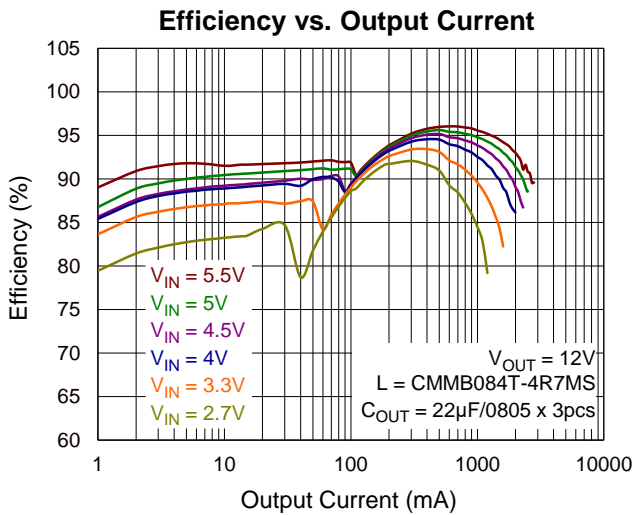
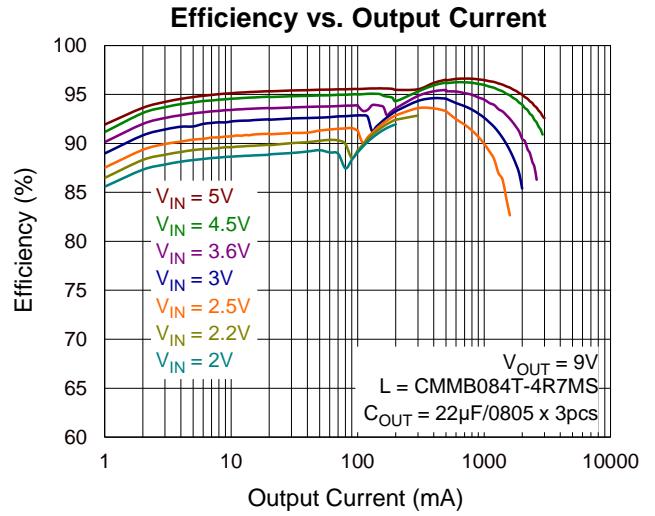
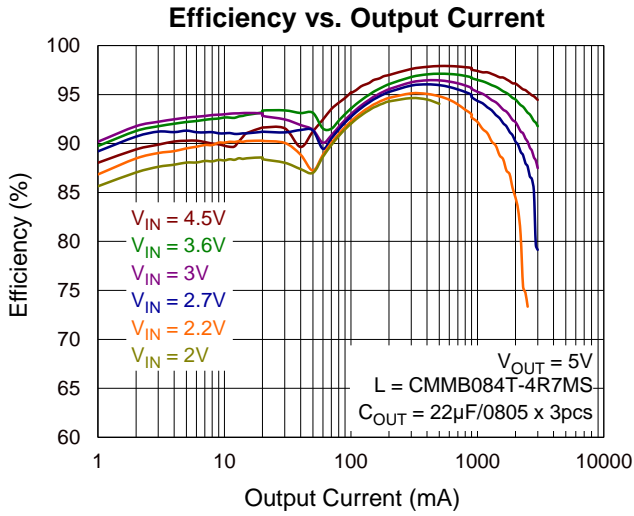


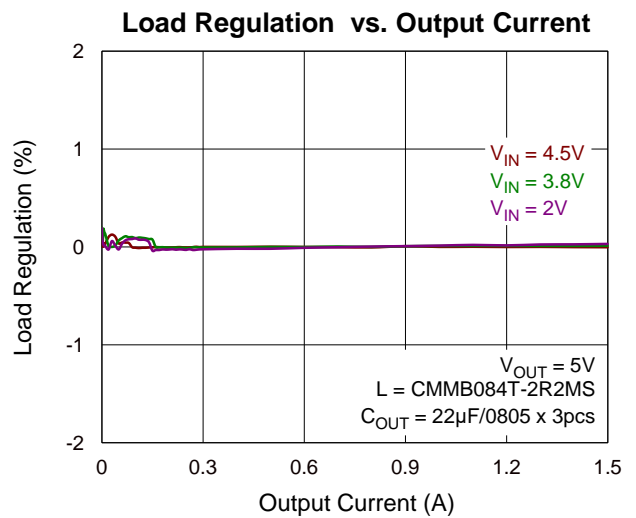
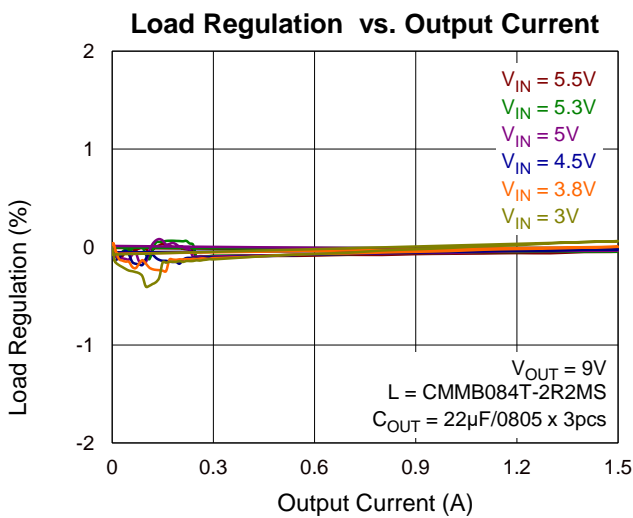
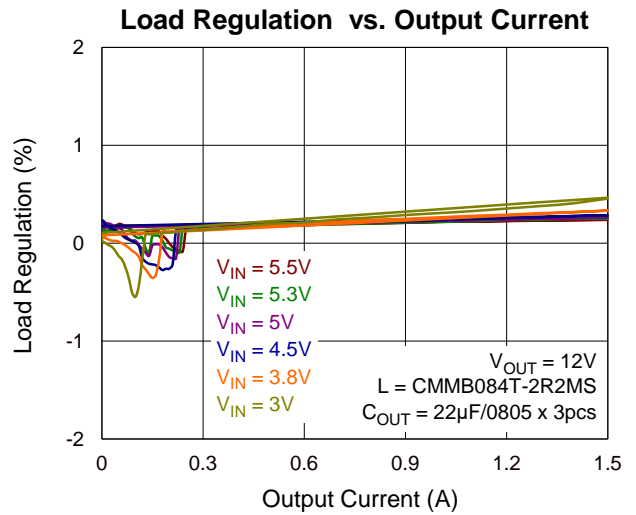
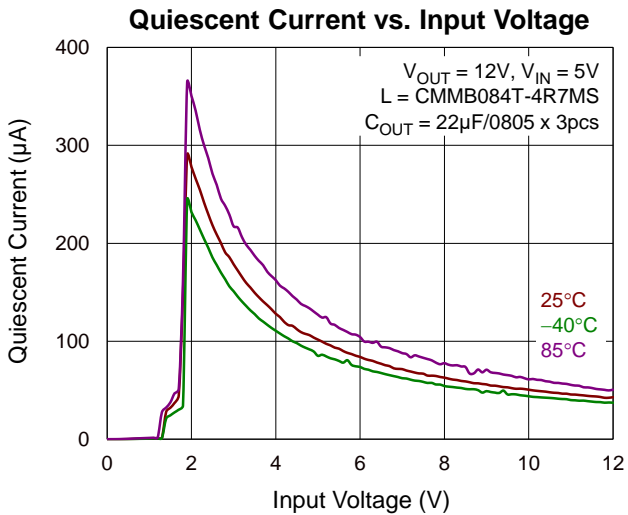
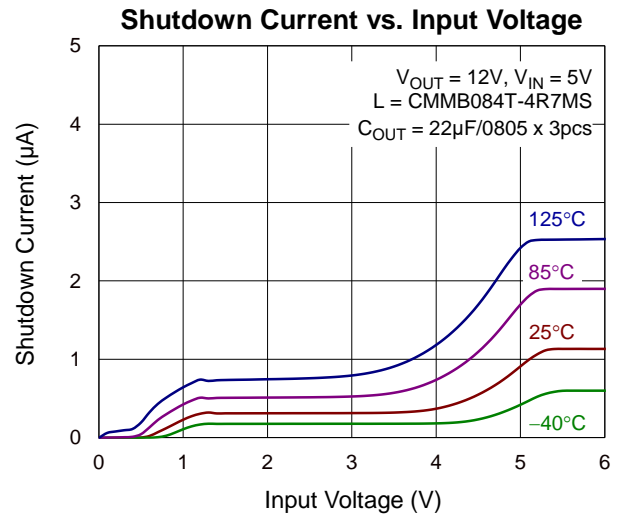
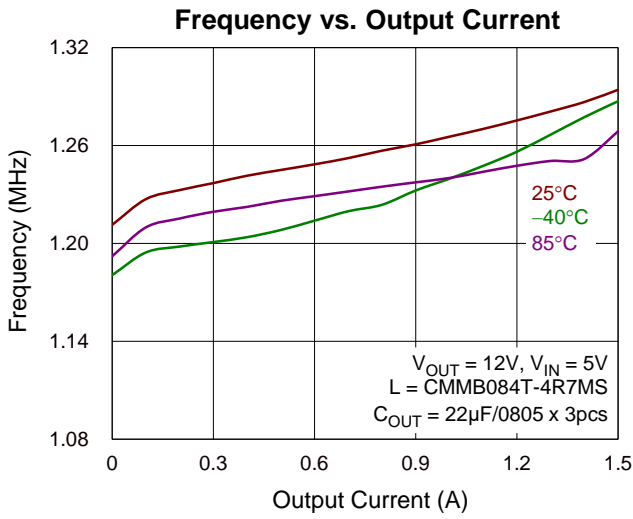
Output Ripple vs. Output Current

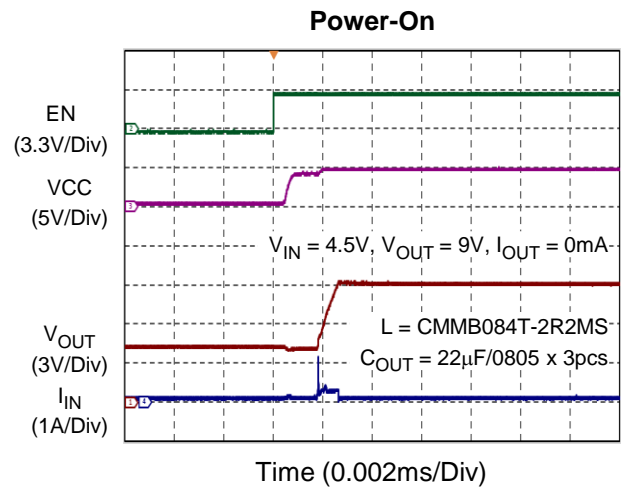
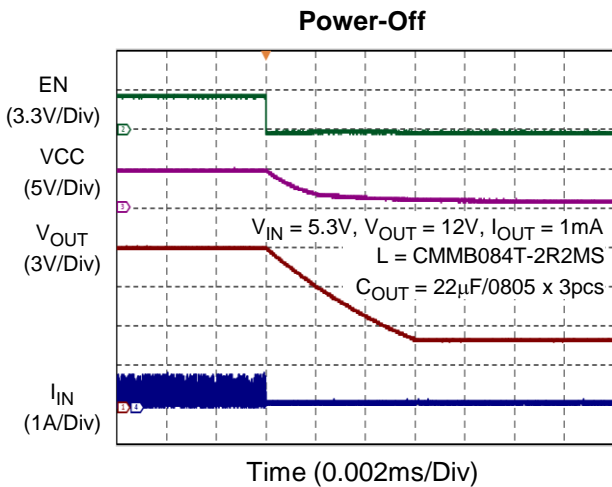
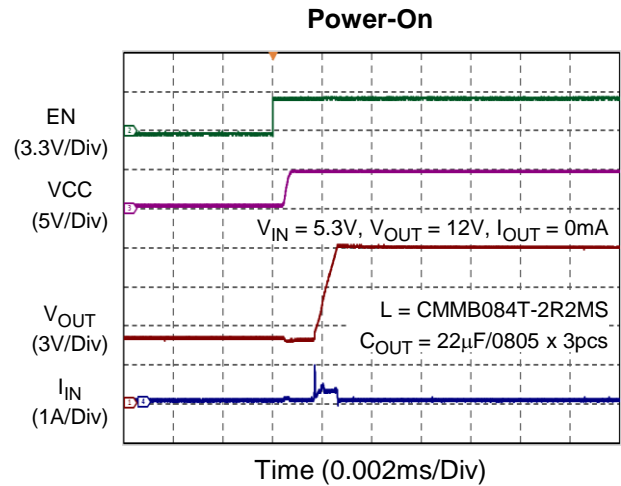
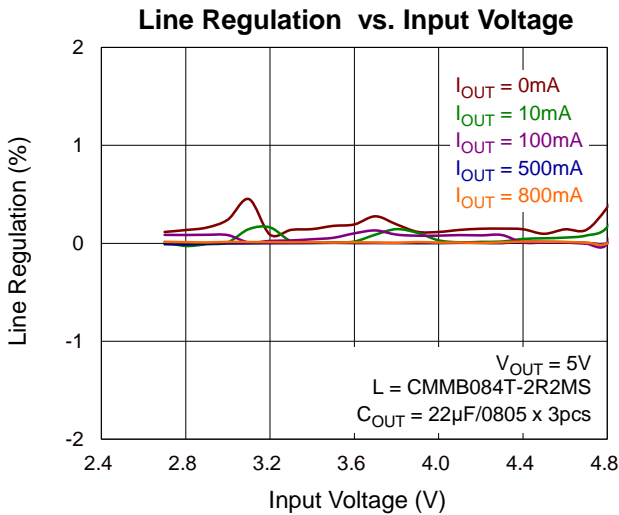
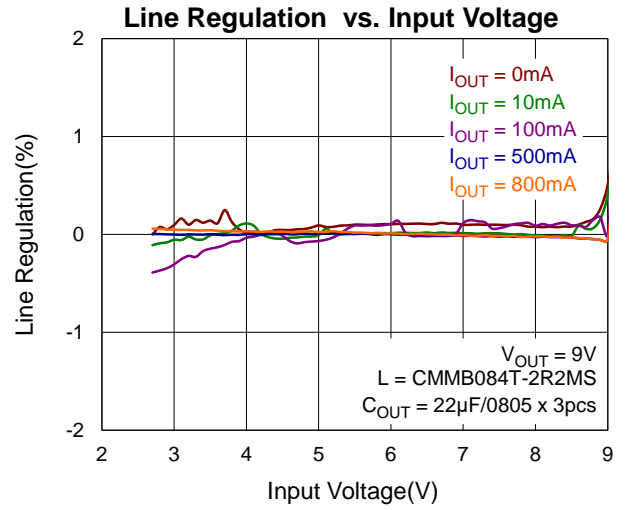
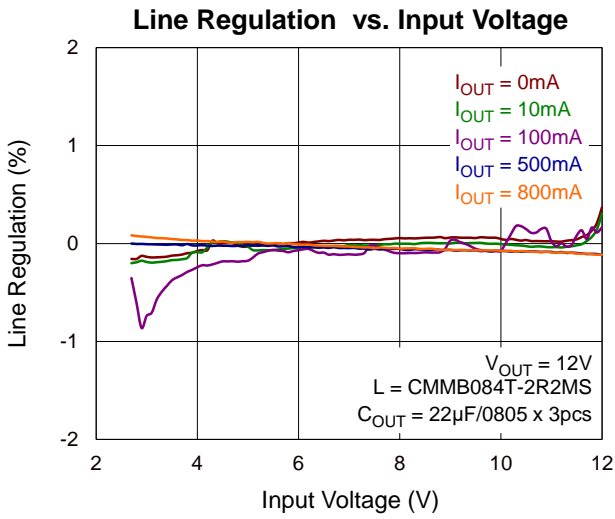


Output Ripple vs. Output Current

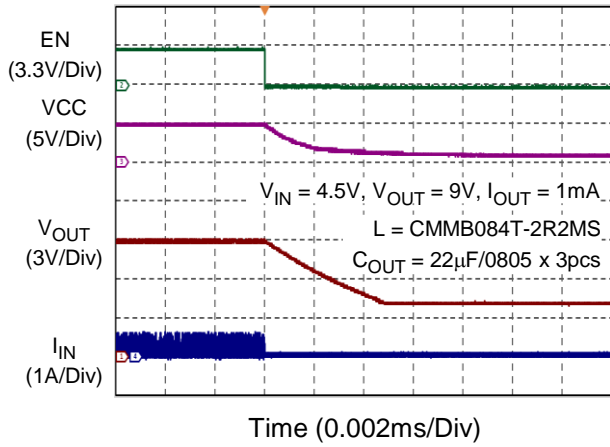




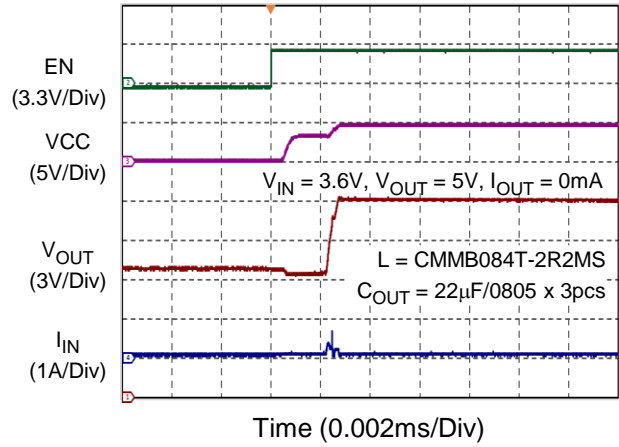




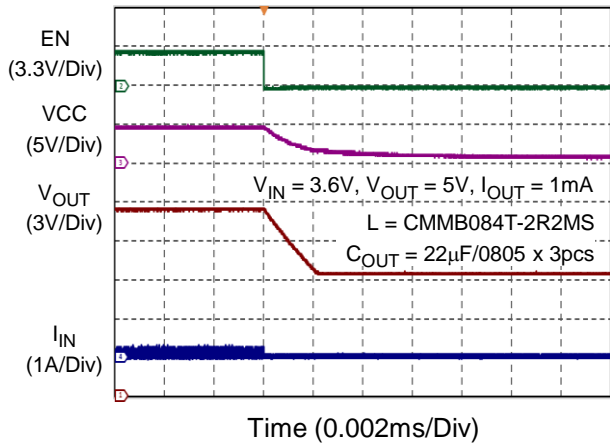
Power-Off



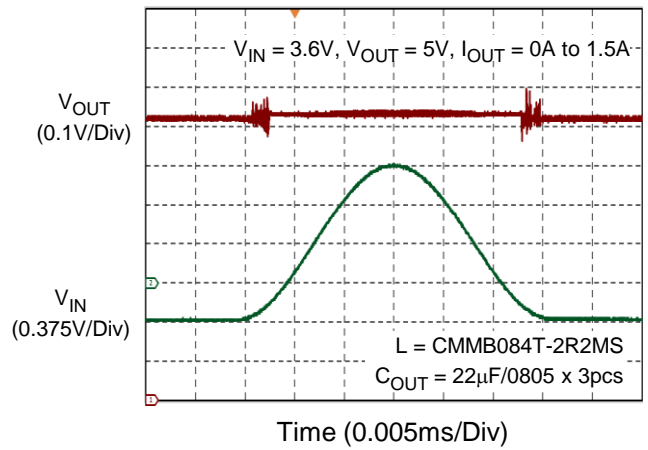
Power-On



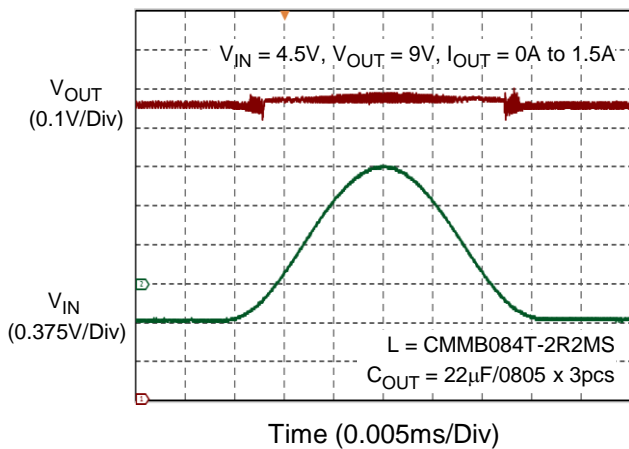
Power-Off



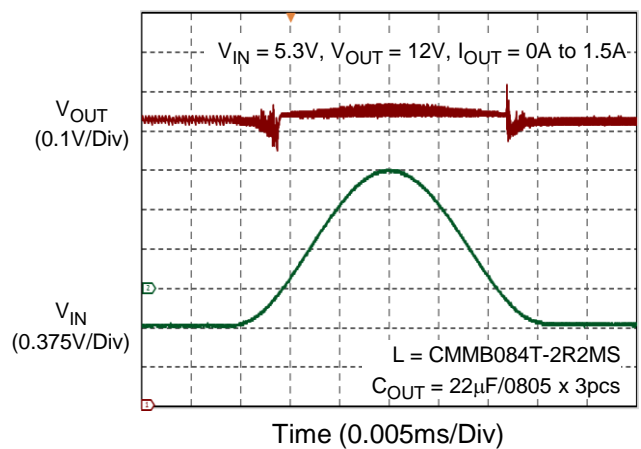
Stability



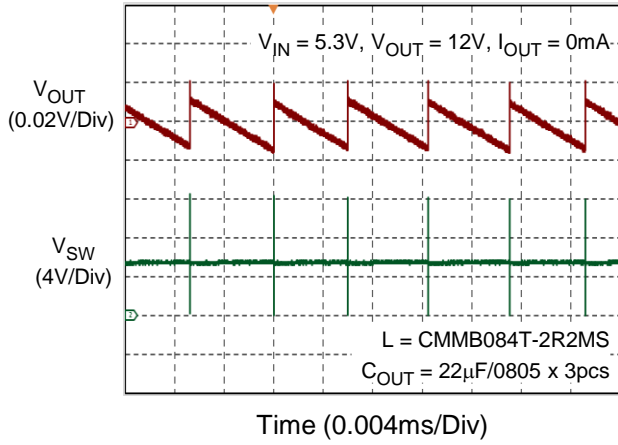
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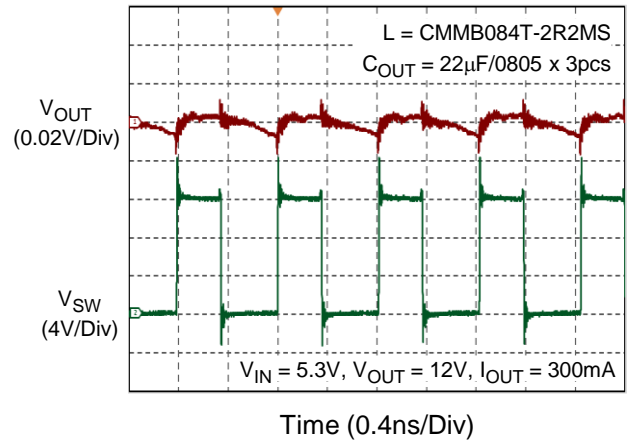
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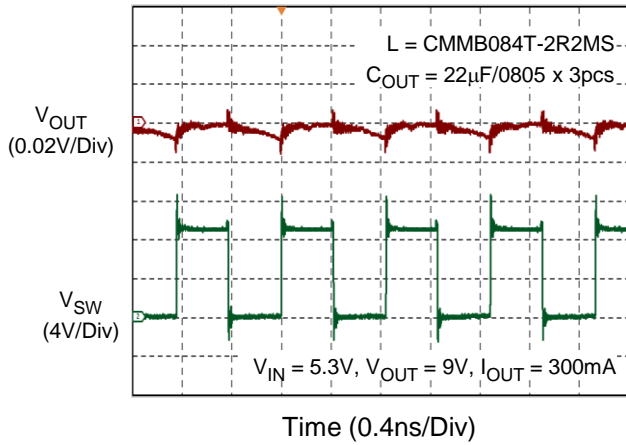
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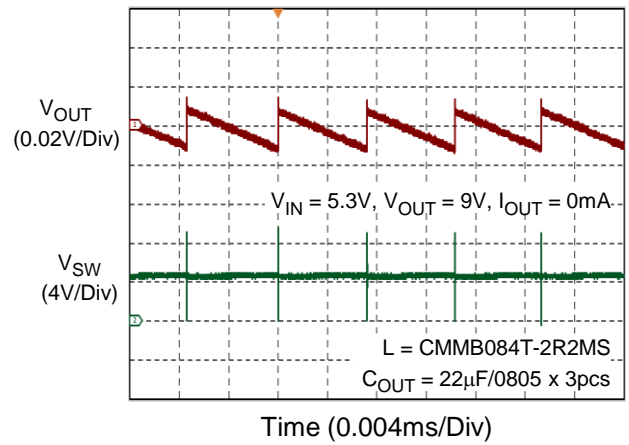
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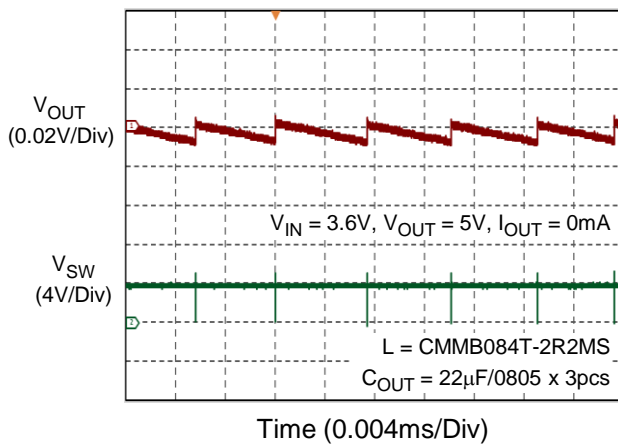
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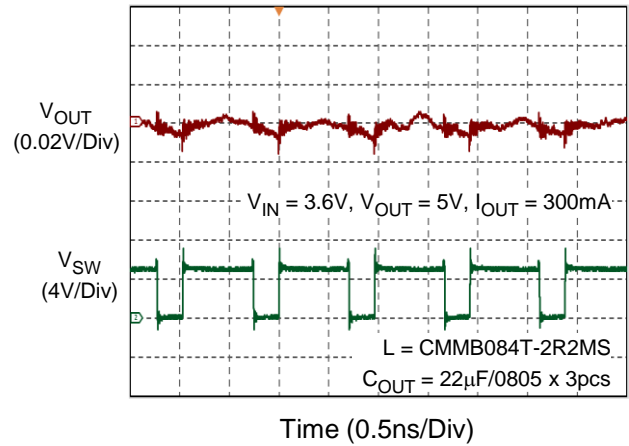
Output Ripple



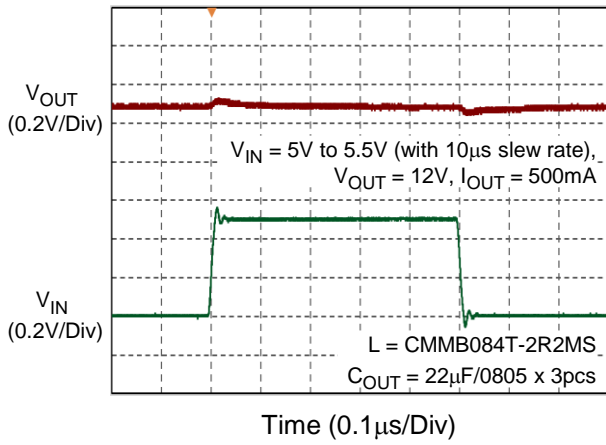
Output Ripple



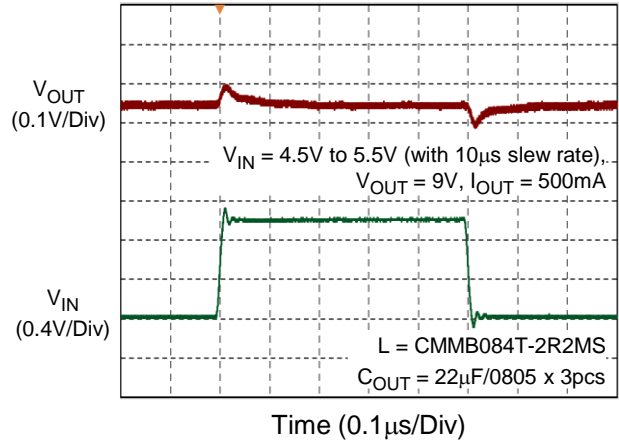
Output Ripple



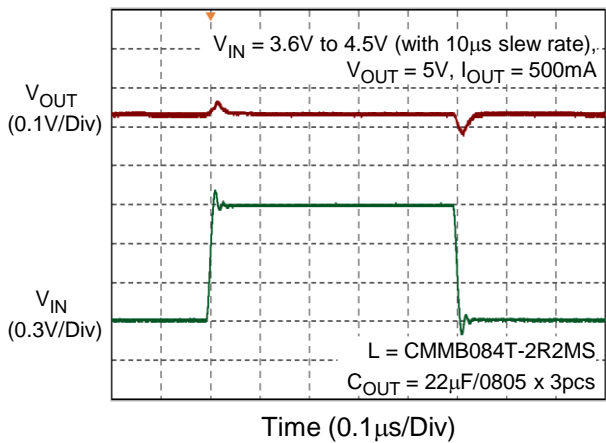
Line Transient



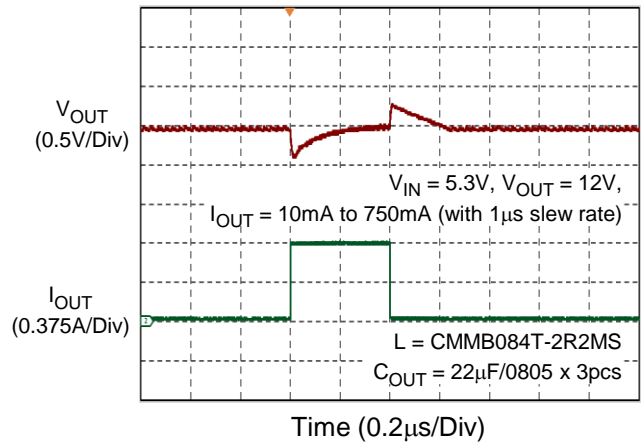
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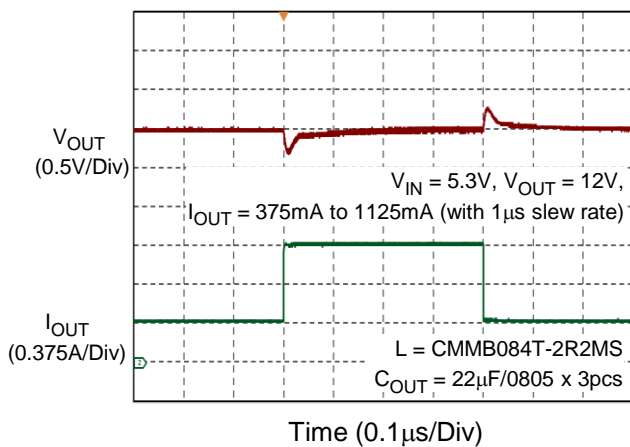
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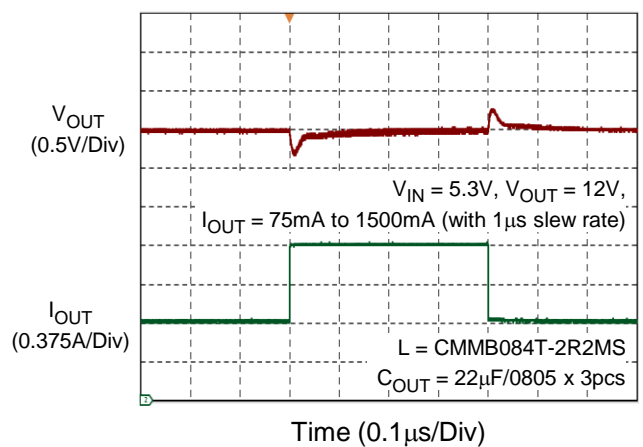
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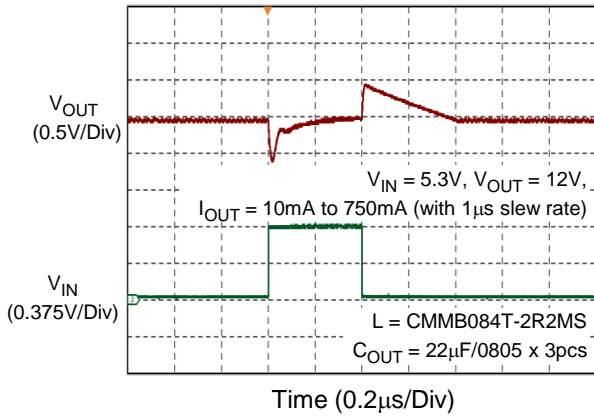
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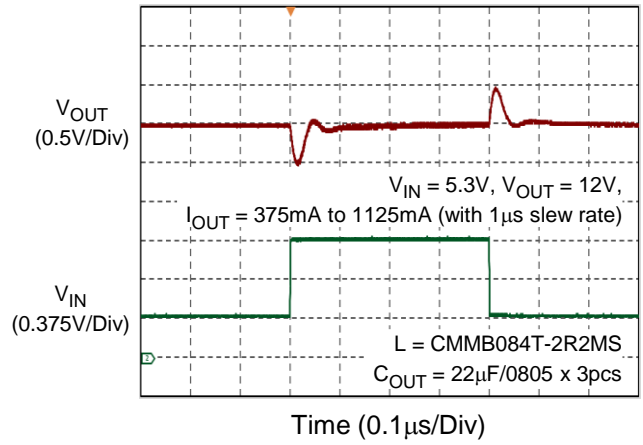
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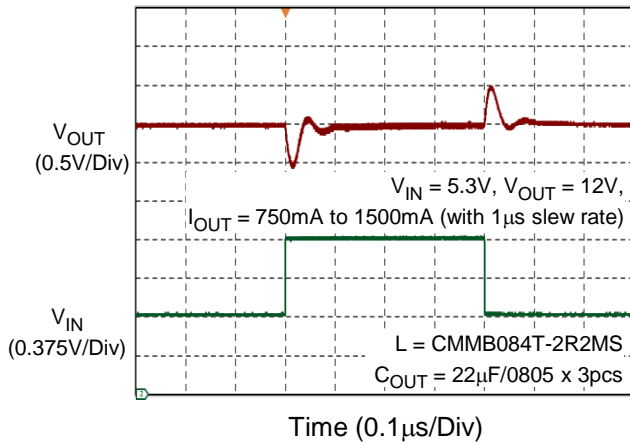
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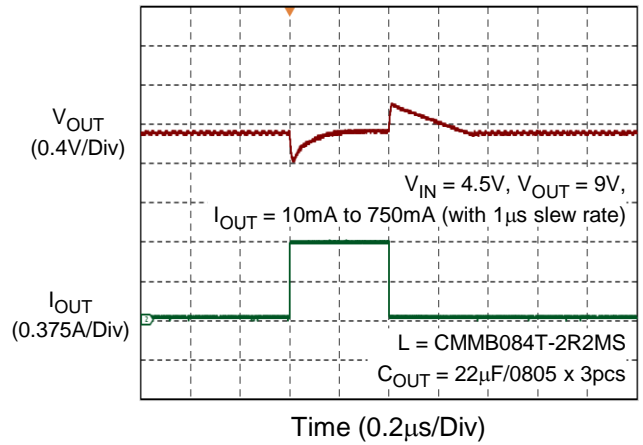
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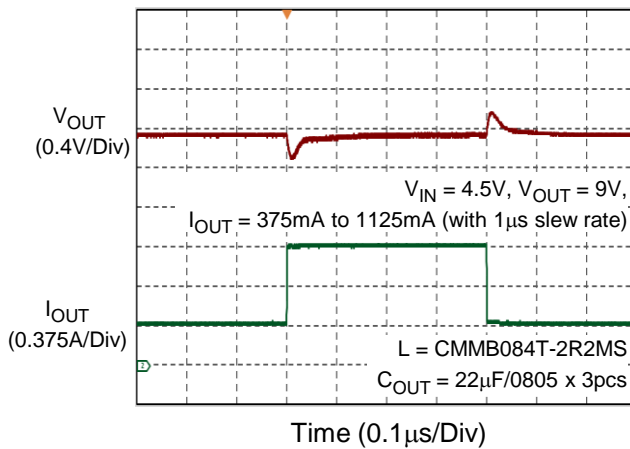
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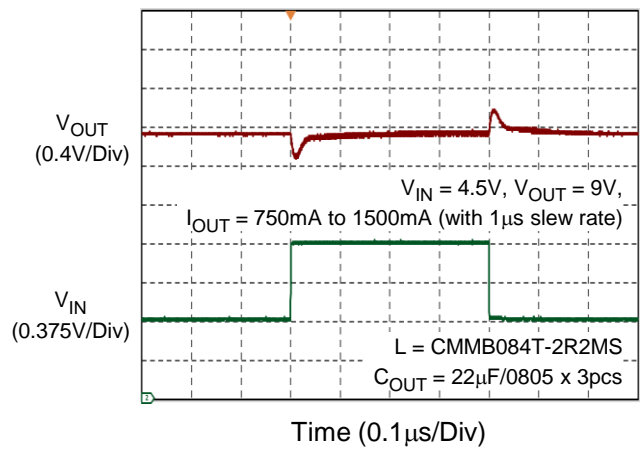
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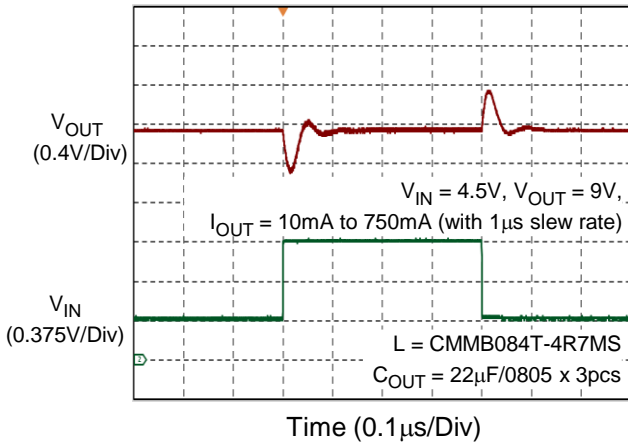
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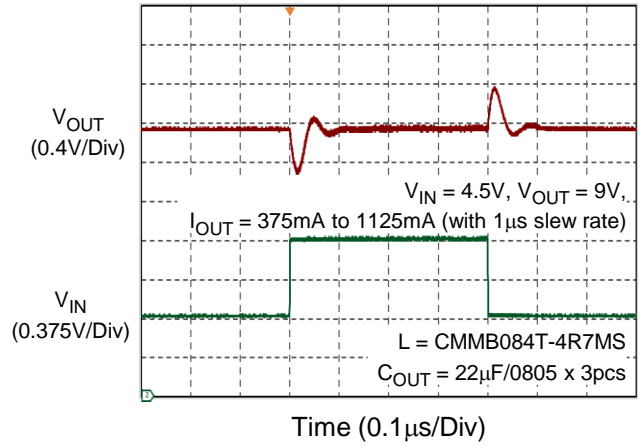
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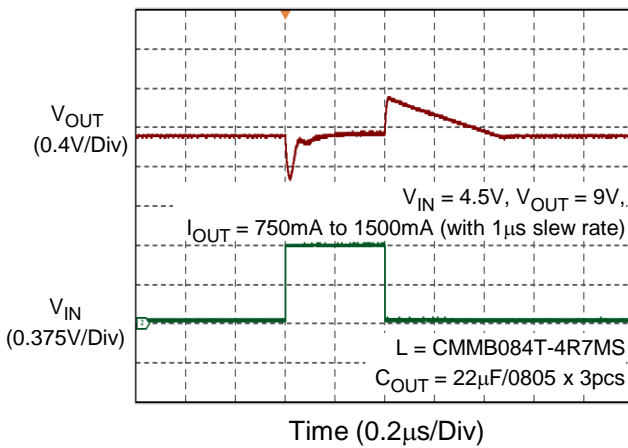
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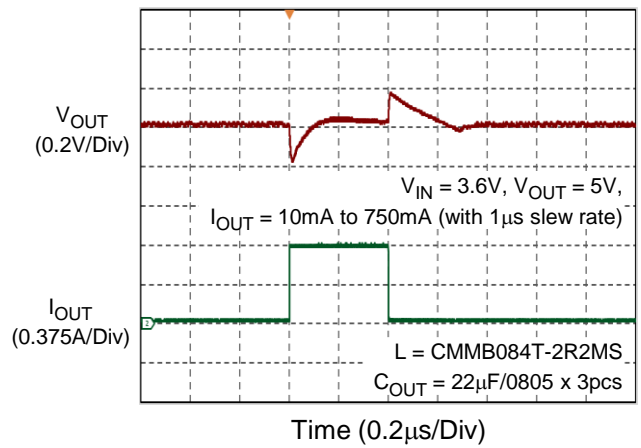
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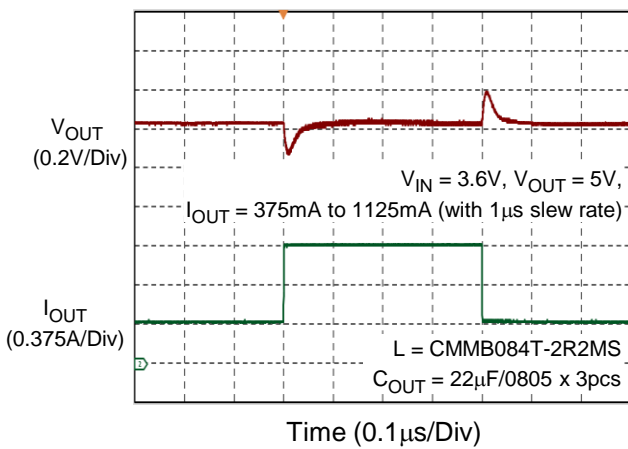
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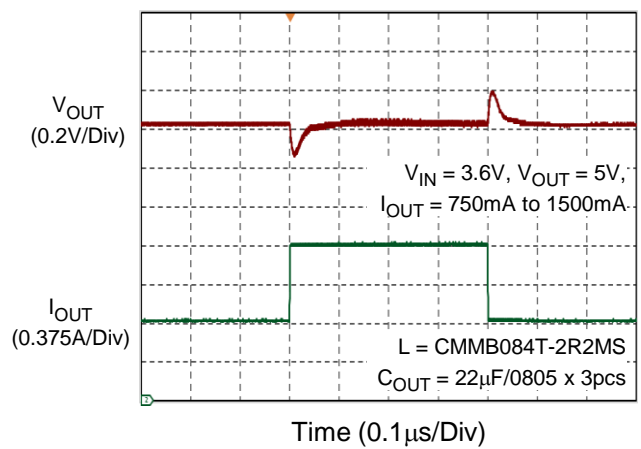
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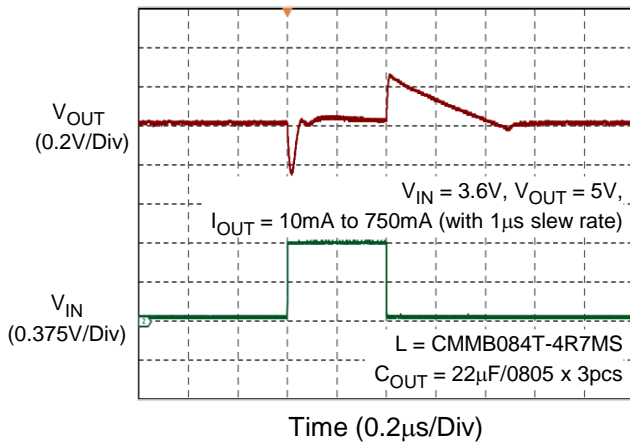
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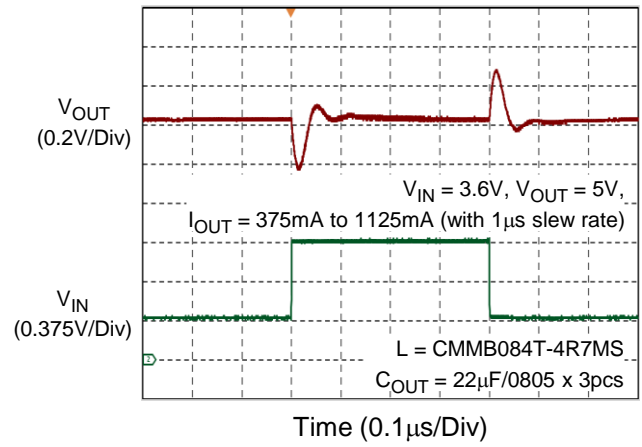
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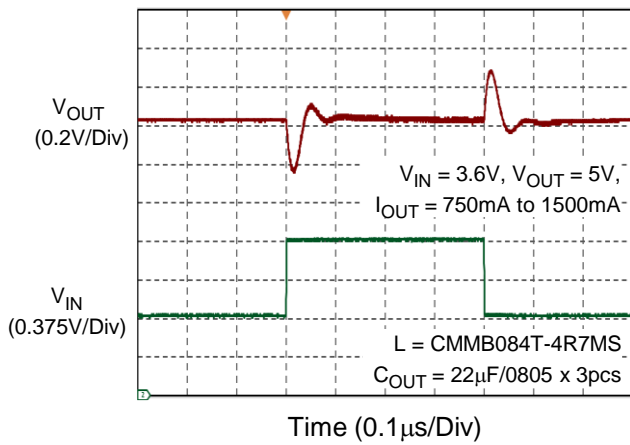
Load Transient



Load Transient



Load Transient



15 Operation

15.1 Enable Function

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the logic-high threshold, the device starts operating with soft-start. Once the EN pin is set at low, the device will shut down. In shutdown mode, the converter stops switching and consumes less than 5μA. Because of the body diode of the high-side MOSFET, the input voltage goes through the body diode and appears at the VOUT pin at shutdown mode.

15.2 Soft-Start Function

After the EN pin is pulled to a logic high voltage, the internal soft-start circuitry gradually ramps up the output voltage. This process help to minimize inrush current during start-up. The typical soft-start time is 2ms.

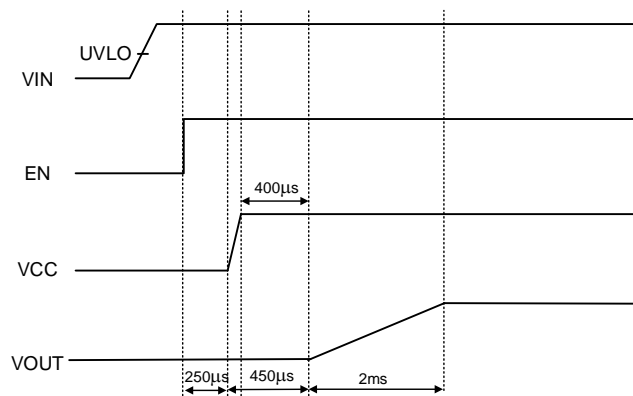


Figure 1. Soft-Start State

15.3 Adjustable Peak Current Limit

The RT8581 employs a cycle-by-cycle peak-current limit detection scheme to sense inductor current during the on-time. When the loading current exceeds the peak current-limit threshold, the on-time is reduced until the current falls back to the peak-current threshold. The on-time is determined by the $(V_{OUT} - V_{IN}) / V_{OUT}$ ratio. As the load current increases further, the output voltage decreases. The peak inductor current limit can be set by R_{LIM} , and the current limit can be calculated using the following equation:

$$I_{LIM} = \frac{1030000}{R_{LIM}}$$

* For a typical 8A current limit, the resistor value is 127kΩ for the RT8581.

15.4 Forced Pulse Width Modulation Mode

In order to avoid acoustic noise at light loads, the boost converter operates in FPWM (Forced Pulse Width Modulation) mode as the inductor current is in CCM (Continuous Current Mode) and the switching frequency is fixed. When the current through the MOSFET is zero, the high-side MOSFET is not turned off, and the on-time is determined by the $(V_{O}-V_{IN})/V_{O}$ ratio of the switching period. In FPWM mode, the RT8581 can achieve lower output ripple compared to PFM mode. However, the efficiency will be lower under light load conditions.

15.5 Pulse Frequency Modulation Mode

To save power and enhance efficiency under light load conditions, the boost converter operates in PFM (Pulse Frequency Modulation) mode as the inductor current enters DCM (Discontinuous Current Mode). When the current through the MOSFET drops to zero, the high-side MOSFET is turned off until the next switching cycle. In PFM mode, the RT8581 extends the high-side MOSFET off-time during the switching period to deliver less energy to the output and regulate the output voltage.

16 Application Information

(Note 6)

16.1 Output Voltage Setting

The output voltage is adjustable via an external resistive divider. The resistive divider must be connected between V_{OUT} , FB, and GND. The output voltage can be calculated using the equation below:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

16.2 Inductor Selection

The primary concern of inductor selection is the maximum loading of the application. An example is given based on the application conditions and equations below.

Application conditions:

$V_{IN} = 5V$, $V_{OUT} = 12V$, $I_{OUT} = 1.5A$, converter efficiency = 86.25%, Frequency = 1.2MHz, $L = 4.7\mu H$.

Typical peak inductor current limit is 8A ($R_{LIM} = 127k\Omega$).

Step 1: Calculate input current (I_{IN}).

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \text{Eff}} = 4.174A$$

Step 2: Calculate the duty cycle of the boost converter.

$$D = 1 - \frac{V_{IN} \times \text{Eff}}{V_{OUT}} = 0.640$$

Step 3: Calculate the peak current of the inductor.

$$I_{L(\text{peak})} = I_{IN} + \frac{V_{IN} \times D}{2 \times L \times f_{sw}} = 4.458A$$

It is recommended to use an inductor with a DC saturation current $\geq 4.5A$.

16.3 Input Capacitor Selection

An input capacitor of at least $10\mu F$ with a rated voltage of 6.3V for DC bias is recommended to improve the transient behavior of the regulator and EMI behavior of the total power supply circuit for SW. It is recommended to place the input capacitor as close as possible to the VIN and GND pins of the IC.

16.4 Output Capacitor Selection

An output capacitor of at least $10\mu F$ (effective value) is recommended to reduce V_{OUT} ripple.

The output voltage ripple is inversely proportional to C_{OUT} .

The output capacitor is selected based on the output ripple which is calculated as follows:

$$V_{\text{Ripple (p-p)}} = \frac{I_{OUT(\text{max})} \times D}{f_{sw} \times C_{OUT}}$$

therefore:

$$C_{OUT} = \left(1 - \frac{V_{IN} \times \text{Eff}}{V_{OUT}}\right) \times \frac{I_{OUT(max)}}{f_{SW} \times V_{Ripple (p-p)}}$$

The maximum $V_{Ripple(p-p)}$ occurs at minimum input voltage and maximum output load.

16.5 Undervoltage-Lockout (UVLO)

The undervoltage-lockout circuit ensures proper operation of the RT8581 by preventing it from activating at low input voltages, which could lead to undefined behavior. This feature also safeguards the battery from deep discharge by inhibiting the power switches from turning on when the conditions are not ideal. For the converter to be enabled, the VIN voltage must exceed 1.9V. If the VIN voltage falls below 1.8V during operation, the converter is disabled. It then waits for the internal IC default parameters to reset until the supply voltage exceeds the UVLO rising threshold. The RT8581 automatically restarts if the input voltage recovers to the UVLO high level.

16.6 Over-Temperature Protection (OTP)

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature decreases below the threshold with a hysteresis, it will resume operation. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over-temperature threshold.

16.7 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to- ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-11L 2.5x2 (FC) package, the thermal resistance, θ_{JA} , is 52.92°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (52.92^\circ\text{C/W}) = 1.89\text{W for a WQFN-11L 2.5x2 (FC) package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curve in [Figure 2](#) allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

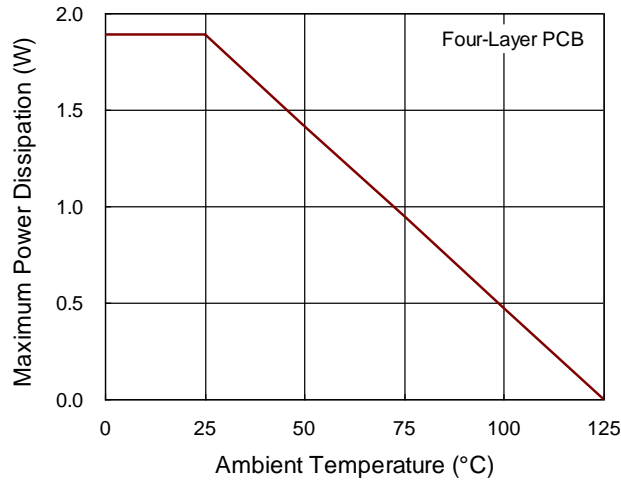


Figure 2. Derating Curve of Maximum Power Dissipation

16.8 Layout Considerations

The PCB layout is a critical factor in preserving the high performance of the RT8581.

Special attention must be given to the high current paths and the fast-switching nodes to ensure the robustness of the RT8581. An improper layout can lead to poor line or load regulation, shifts in ground and output voltage, stability issues, unsatisfactory EMI behavior, and worsened efficiency. To achieve the best performance of the RT8581, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins to ensure effective filtering.
- For thermal consideration, it is necessary to maximize the pure area for the power stage area besides the SW pin.

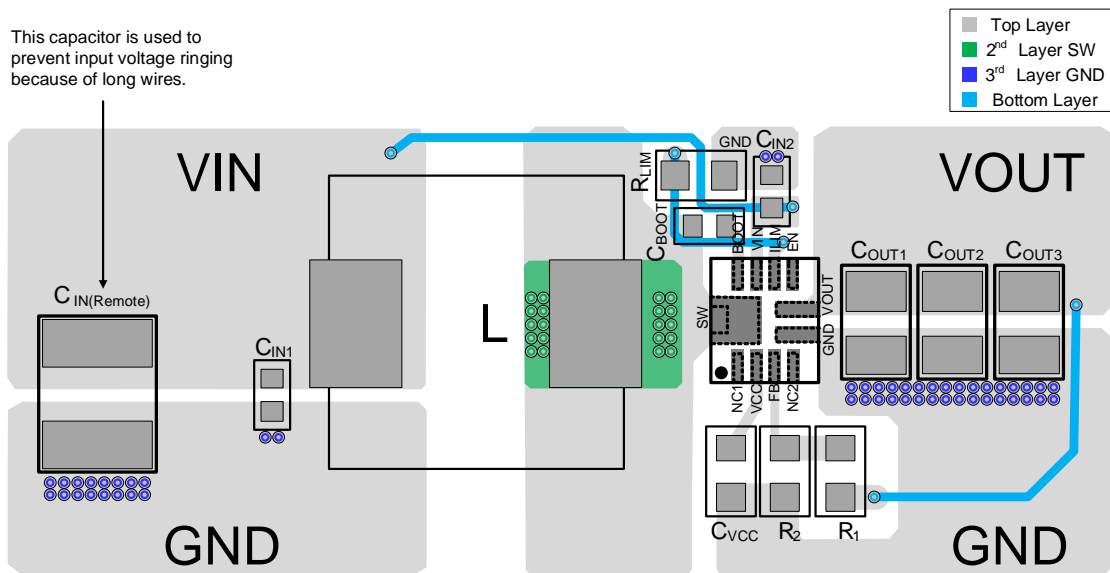
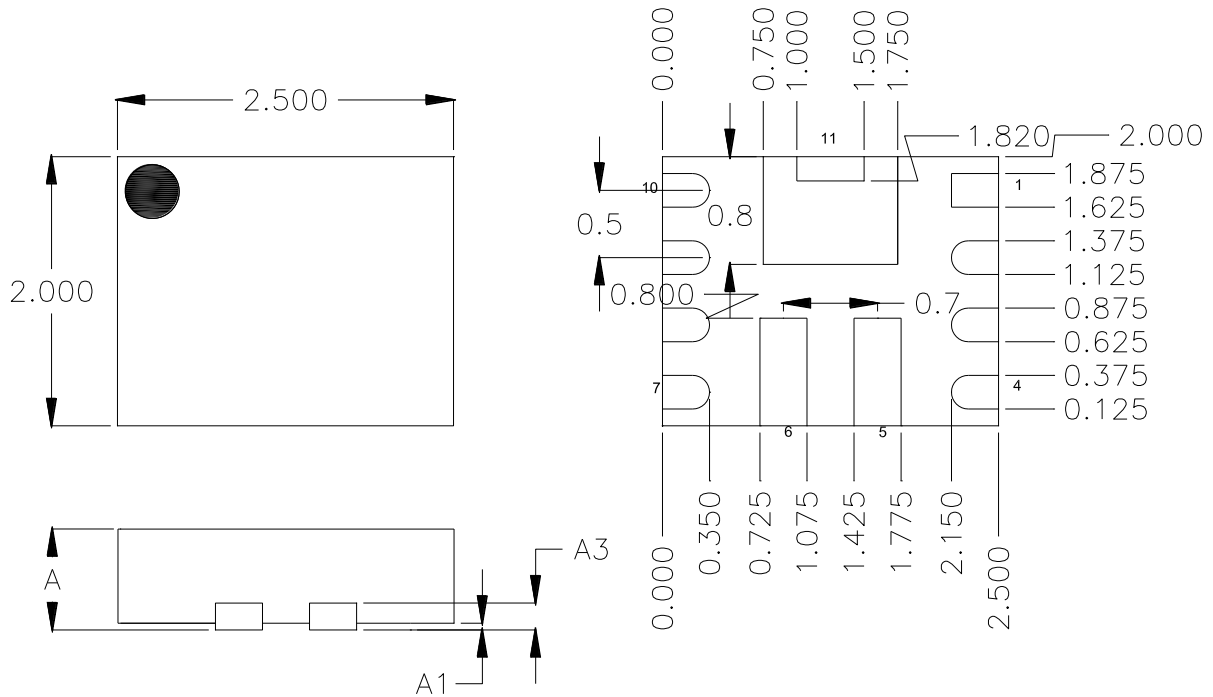


Figure 3. PCB Layout Guide

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek’s product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension

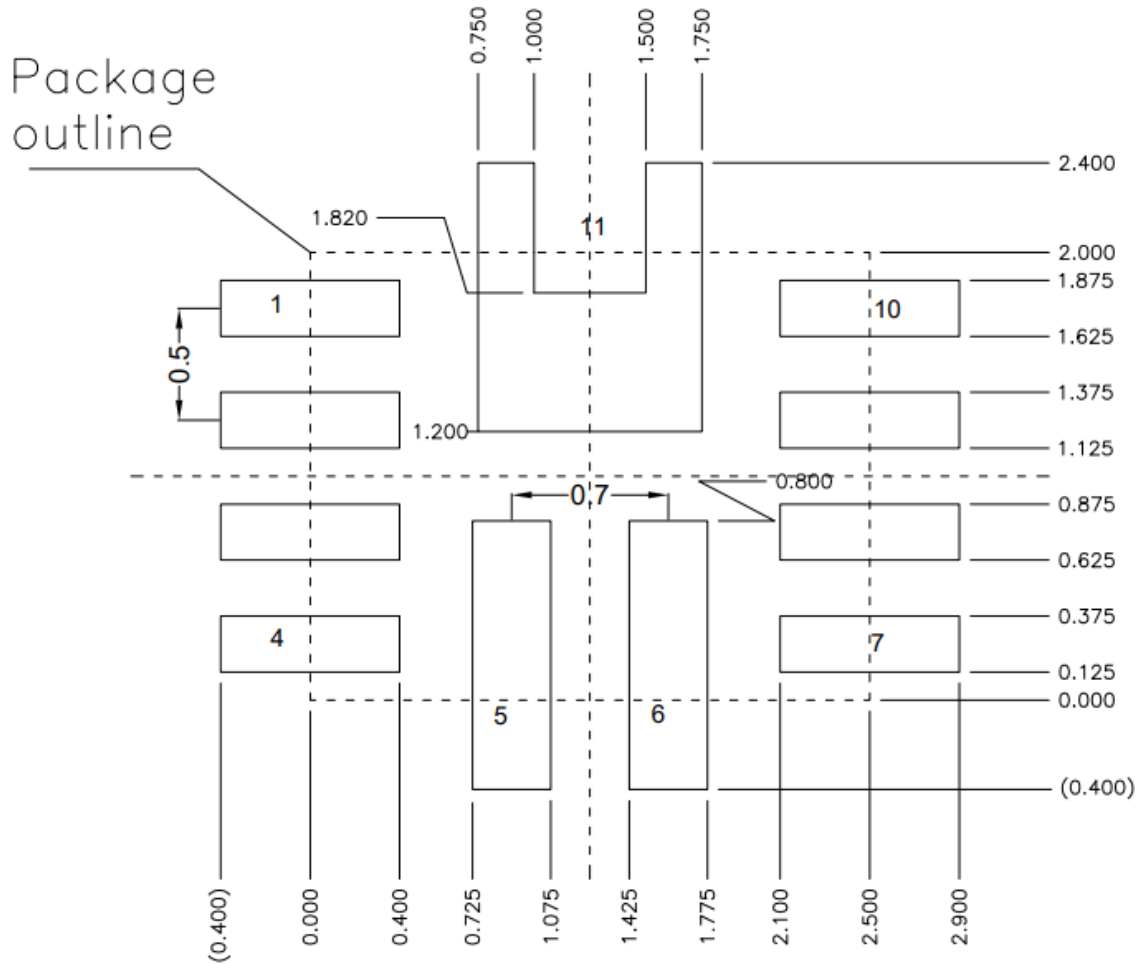


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050 mm

W-Type 11L QFN 2.5x2 Package (FC)

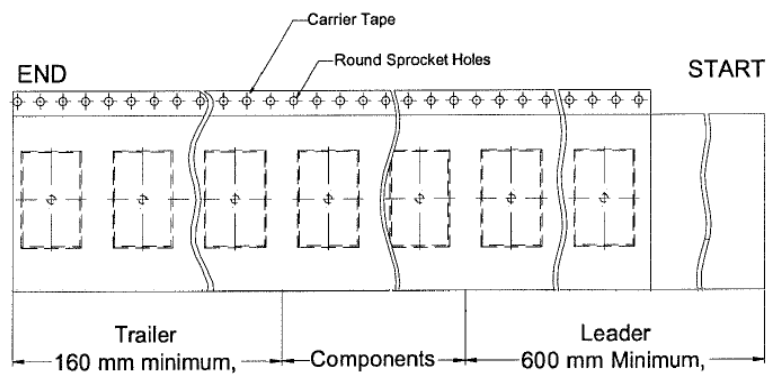
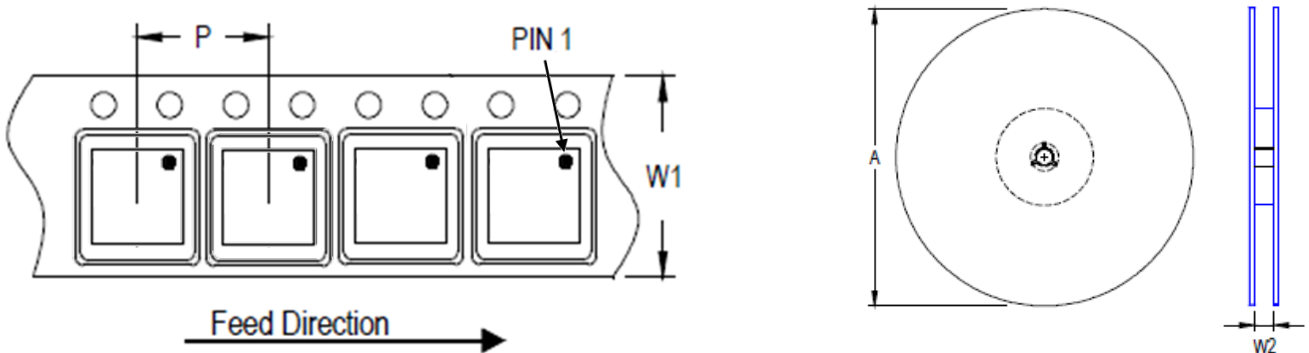
18 Footprint Information



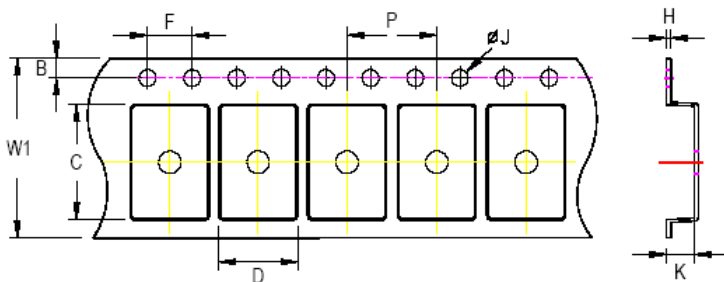
Package	Number of Pins	Tolerance
V/W/U/XQFN2.5x2-11(FC)	11	±0.05 mm

19 Packing Information

19.1 Tape and Reel Data









Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2.5x2	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size.
The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1		P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max	
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.05mm	1.25mm	0.6mm	

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 7"</p>	4	 <p>3 reels per inner box Box A</p>
2	 <p>HIC & Desiccant (1 Unit) inside</p>	5	 <p>12 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box Carton A</p>

Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2.5x2	7"	2,500	Box A	3	7,500	Carton A	12	90,000
Box E			1	2,500	For Combined or Partial Reel.			

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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20 Datasheet Revision History

Version	Date	Description	Item
00	2025/1/3	Final	<i>Removed RT8581B and RT8581C</i>