High Efficiency Single Synchronous Buck PWM Controller

General Description

The RT8125P PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for CPU core, I/O, and chipset RAM supplies in notebook computers.

Richtek Mach Response™ technology is specifically designed for providing 100ns “instant-on” response to load transients while maintaining a relatively constant switching frequency.

The RT8125P achieves high efficiency at a reduced cost by eliminating the current sense resistor found in traditional current mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs. The Buck conversion allows this device to directly step down high voltage batteries at the highest possible efficiency. The RT8125P provides an 1% high accuracy 0.8V reference voltage with minimum 1mA source/sink current for high accuracy output application.

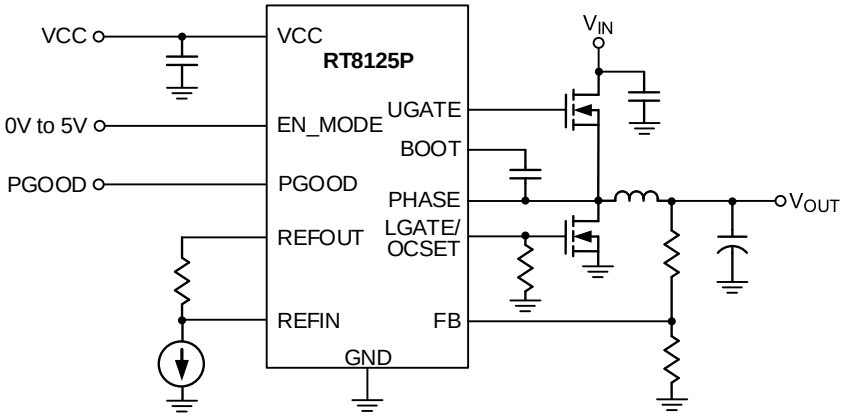
Features

- **Richtek Mach Response™ Technology**
- **1% High Accuracy 0.8V Reference**
- **VCC Input Range: 4.5V to 13.2V**
- **VOUT Operating Range: 0.3V to 3.3V**
- **Power Stage Input Range: 1.5V to 24V**
- **Fixed Operating Frequency: 300kHz**
- **LG_OCSET for Current Limit**
- **PGOOD Indicator**
- **Embedded Bootstrap Switch**
- **High-side Gate Driver Pull Low Resistor (10kΩ)**
- **Current Limit with Low-side Current Sense Scheme**
- **Enable Function with Internal Pull High Current**
- **OVP/UVP/OTP/Pre-OVP/Current Limit**
- **Shutdown Current < 100μA**

Applications

- Generic DC-DC Power Regulator
- Mother Boards and Desktop Servers

Simplified Application Circuit



Ordering Information

RT8125P □□

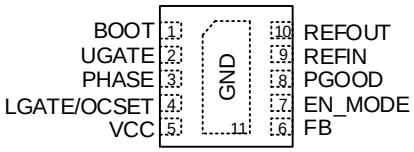
Package Type
QW : WDFN-10L 3x3 (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Pin Configuration



WDFN-10L 3x3

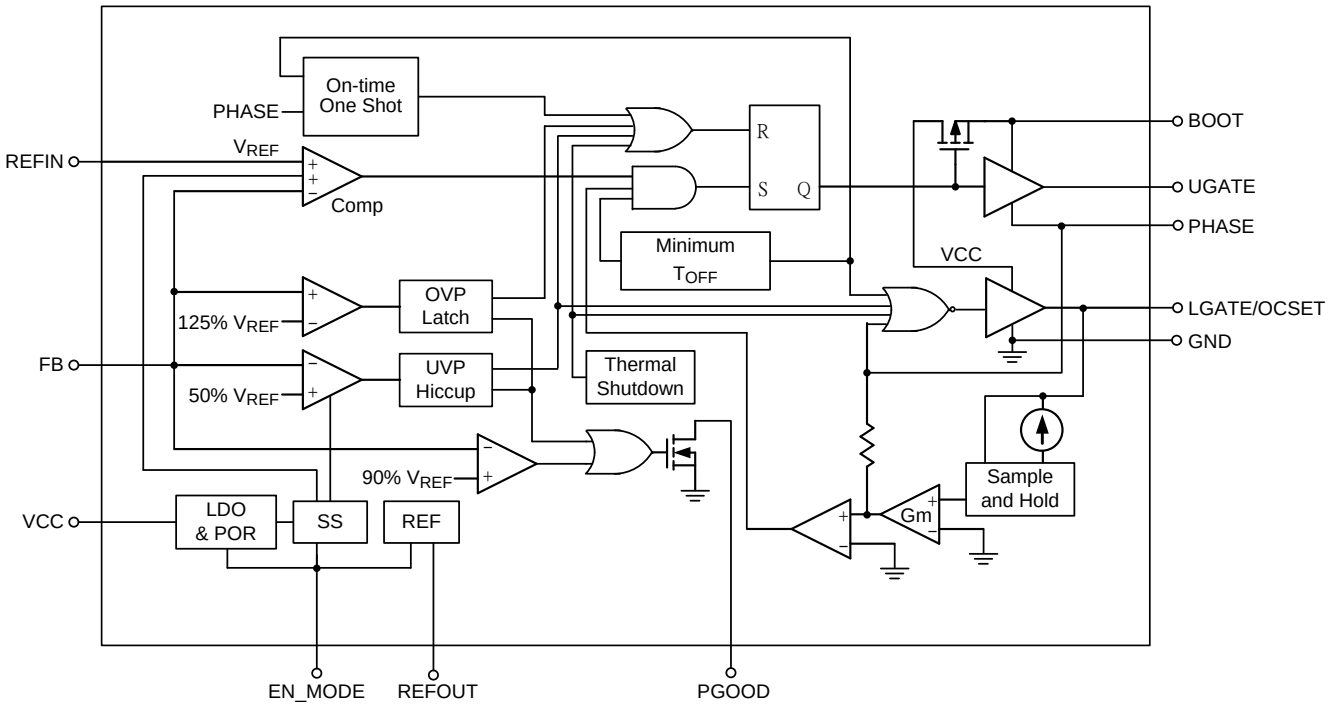
Marking Information

VX=: Product Code
YMDAN: Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap supply for high-side gate driver. Connect a capacitor between this pin and the PHASE pin.
2	UGATE	Gate drive output for the external high-side MOSFET.
3	PHASE	Switch node. It behaves as the current sense comparator input for low-side MOSFET $R_{DS(ON)}$ sensing and reference voltage for on-time generation.
4	LGATE/OCSET	Gate drive output for the low-side external MOSFET. Connect a resistor (R_{OCSET}) between this pin and GND to set the output current limit level. If R_{OCSET} is not present, or the setting threshold greater than 250mV, the OC threshold is internally present to 250mV.
5	VCC	Supply voltage input. It provides the power for the Buck controller, the low-side driver and the bootstrap circuit for high-side driver. Bypass to GND with a 4.7μF ceramic capacitor.
6	FB	V_{OUT} feedback voltage input. Connect the FB to a resistive voltage divider from VOUT to GND to set the output voltage from 0.3V to 3.3V
7	EN_MODE	Enable and mode selection control input. When the voltage of EN_MODE pin is pulled lower than 0.4V, controller remains in shutdown. When the pin voltage is between 1.1V to 1.8V, controller operates into DEM. When the pin voltage is between 2.8V to 5V, controller operates into FCCM.
8	PGOOD	Open-drain Power Good Indicator. High impedance indicates that power is good.
9	REFIN	Reference input. Connect a current console to REFIN pin, and connect a resistor between REFIN and REFOUT to tune up/down FB reference voltage.
10	REFOUT	Reference voltage output. It provides an 1% high accuracy reference 0.8V with 2mA source/sink ability. Bypass to GND with a maximum 6.8nF ceramic capacitor.
11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 15V
- PGOOD, FB, EN_MODE, REFOUT, REFIN ---------- –0.3V to 6.5V
- BOOT to GND ---------- –0.3V to 40V
  - <100ns ---------- –0.3V to 45V
- BOOT to PHASE ---------- –0.3V to 15V
  - <100ns ---------- –0.3V to 20V
- PHASE to GND
  - DC ---------- –5V to 25V
  - <100ns ---------- –10V to 30V
- UGATE to GND ---------- –0.3V to 40V
  - <100ns ---------- –10V to 45V
- UGATE to PHASE
  - DC ---------- –0.3V to 15V
  - <100ns ---------- –5V to 20V
- LGATE to GND
  - DC ---------- –0.3V to 15V
  - <100ns ---------- –5V to 20V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 3x3 ---------- 3.27W
- Package Thermal Resistance (Note 2)
  - WDFN-10L 3x3, θ_{JA} ---------- 30.5°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, VIN ---------- 1.5V to 24V
- Supply Voltage, VCC ---------- 4.5V to 13.2V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, V_{IN} = 15V, EN_MODE = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
VCC POR Threshold		Rising edge	3.75	4.1	4.5	V
		Hysteresis	--	0.3	--	
V_{CC} Quiescent Supply Current	I_Q	FB forced above the regulation Point, EN_MODE = 5V, REFOUT Current = 0	--	500	850	μA
V_{CC} Shutdown Current	I_{SHDN}	V_{CC} current, EN_MODE = 0V	--	--	100	μA
REFOUT (Note 5)	V_{REFOUT}	V_{CC} = 4.5V to 13.2V, sink/ source current = 2mA	786	794	802	mV
REFOUT Source/Sink Current	I_{REFOUT}		--	--	2	mA
FB Input Bias Current		FB = 0.8V	–1	0	1	μA
REFIN Input Voltage Range			0.3	--	3.3	V
Switching Frequency	f_{SW}	(Note 6)	270	300	330	kHz
Minimum Off-Time	t_{OFF_MIN}		250	--	--	ns
Current Sensing						
IOCSET			9	10	11	μA
Soft-Start Time	t_{SS}	REFIN = 0.8V, no load	--	0.7	--	ms
Protection Function						
Current Limit Setting Range	V_{OCSET}	LGATE	20	--	250	mV
Current-limit threshold	V_{OCSET}	R_{OCSET} = NC	--	250	--	mV
UV Threshold		UVP Detect, FB Lower than REFIN Voltage	225	300	375	mV
OVP Threshold		OVP Detect, FB Higher than REFIN Voltage	225	300	375	mV
REFIN Absolute OVP Threshold			3.35	3.5	--	V
Thermal Shutdown		Latch	--	140	--	°C
Zero Current Crossing Threshold	V_{PH_ZC}		–5	--	4	mV
Driver On-Resistance						
UGATE Driver Source	$R_{UGATEsr}$	V_{BOOT} – V_{PHASE} = 12V, source current = 100mA	--	1.5	3	Ω
UGATE Driver Sink	$R_{UGATEsk}$	BOOT – PHASE = 12V, I_{SINK} = 10mA	--	2.25	4	Ω
LGATE Driver Source	$R_{LGATEsr}$	V_{CC} = 12V, source current = 100mA	--	1.5	3	Ω
LGATE Driver Sink	$R_{LGATEsk}$	V_{CC} = 12V, I_{SINK} = 10mA	--	1	2	Ω
Dead Time		LGATE rising (PHASE = 1.5V)	--	30	--	ns
		UGATE rising	--	30	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Boost Charging Switch On-Resistance		VCC to BOOT, 10mA	--	--	80	Ω
EN_MODE Threshold						
EN_MODE Input Voltage	V_{IH_FCCM}	FCCM, V_{CC} = 4.5V to 13.2V	2.8	--	5	V
	V_{IH_DEM}	DEM, V_{CC} = 4.5V to 13.2V	1.1	--	1.8	
	V_{IL}	Shutdown, V_{CC} = 4.5V to 13.2V	--	--	0.4	
EN_MODE Internal Pull High Current		EN_MODE = Floating	5	--	--	μA
PGOOD (PGOOD High w/o OVP or UVP)						
PGOOD Blanking Time		PGOOD rising edge after soft-start	1	3	5	ms
Output Low Voltage		I_{SINK} = 4mA	--	--	0.3	V
Leakage Current		High state, forced to 5V	--	--	1	μA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

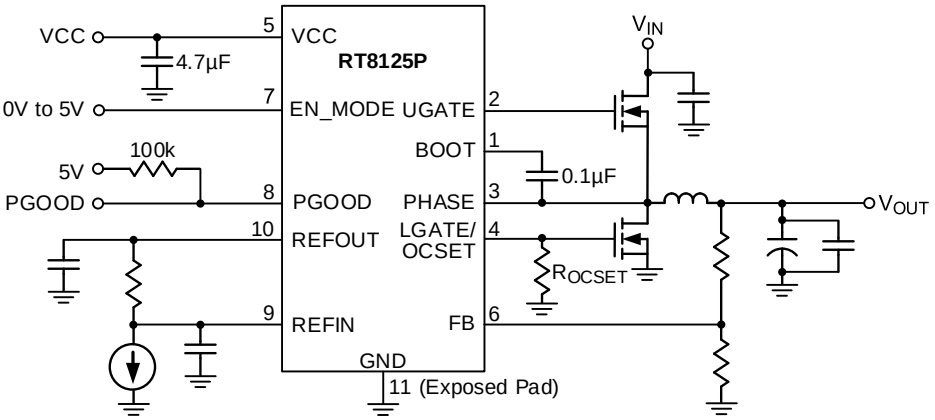
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The reference voltage shift –6mV from 0.8V for offset canceling under feedback valley control.

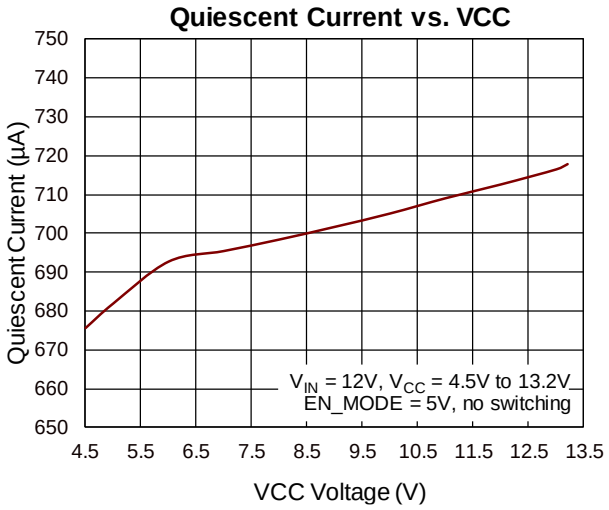
Note 6. No production tested. Test condition V_{IN} = 8V, V_{OUT} = 1.1V, I_{OUT} = 10A using application circuit.

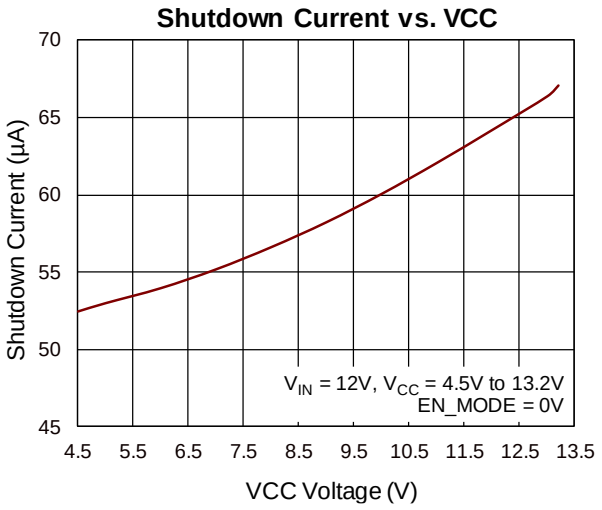
Typical Application Circuit

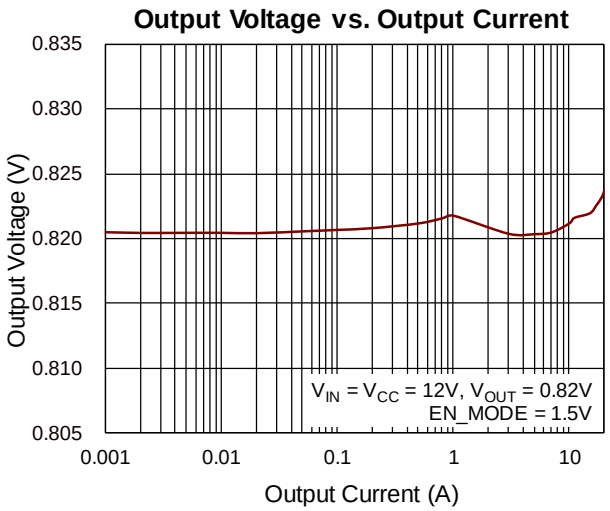


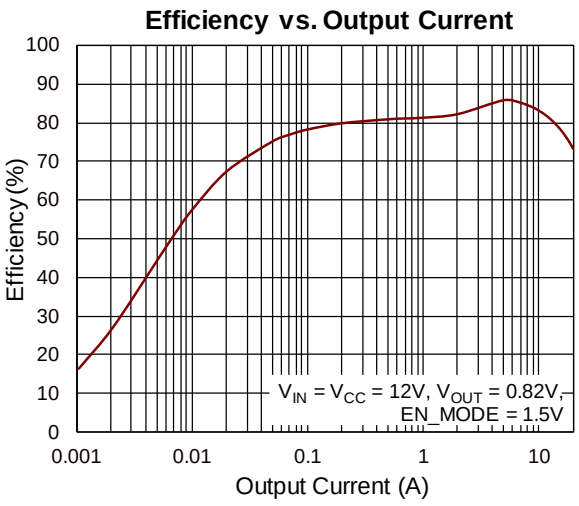
Typical Operating Characteristics

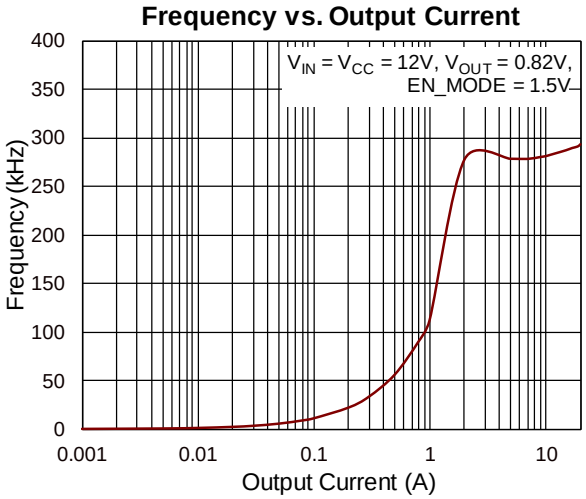
Performance waveforms are tested on the evaluation board of the Typical Application Circuit, V_{IN} = V_{CC} = 12V, V_{OUT} = 0.82V, f_{SW} = 300kHz, L = 0.68µH, C_{OUT} = 560µF/4V OSCON, T_C = 25°C, unless otherwise noted.

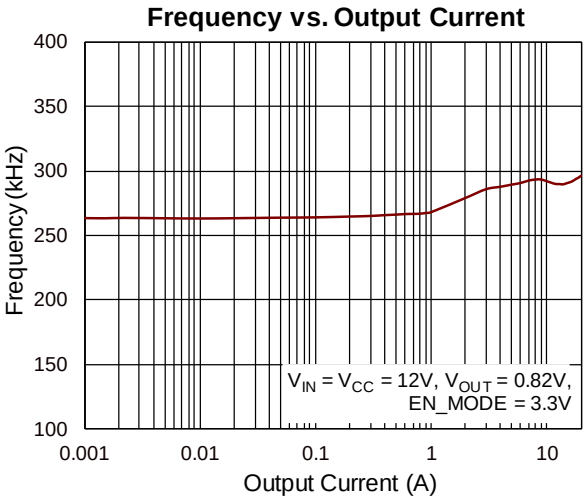




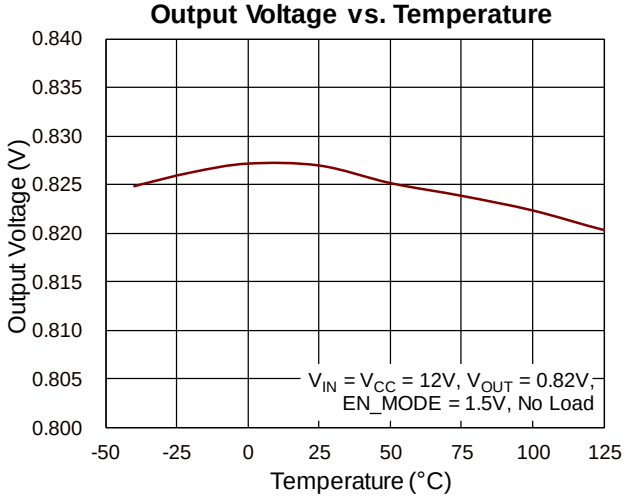




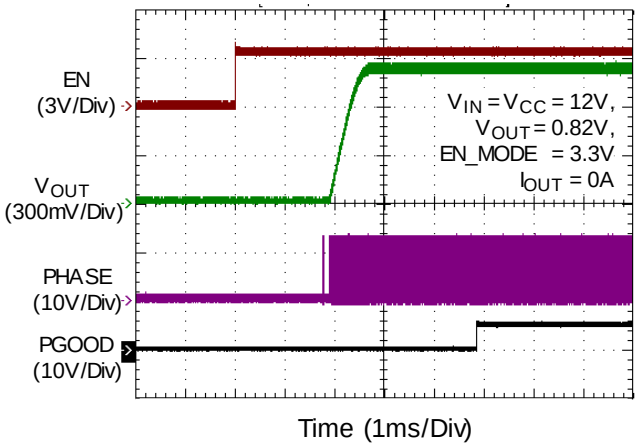




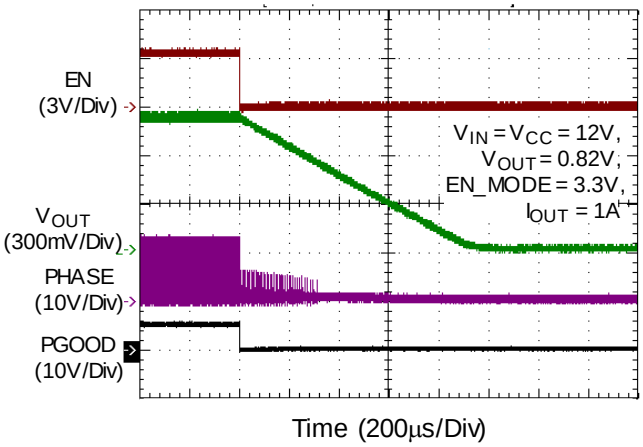
Output Voltage vs. Temperature



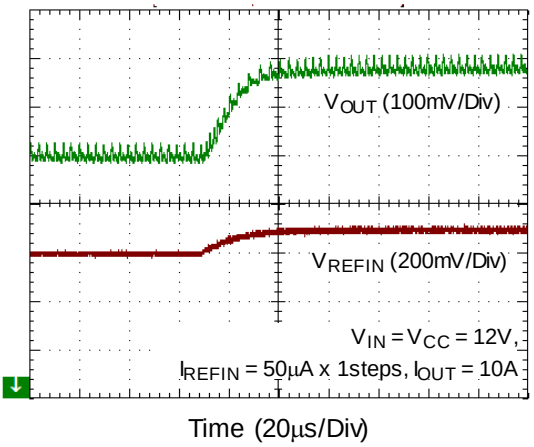
Power On from EN



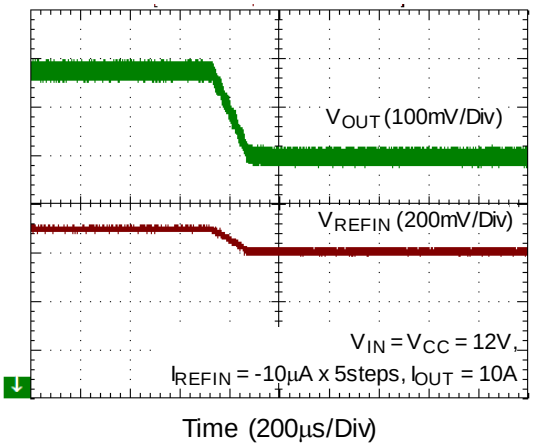
Power Off from EN



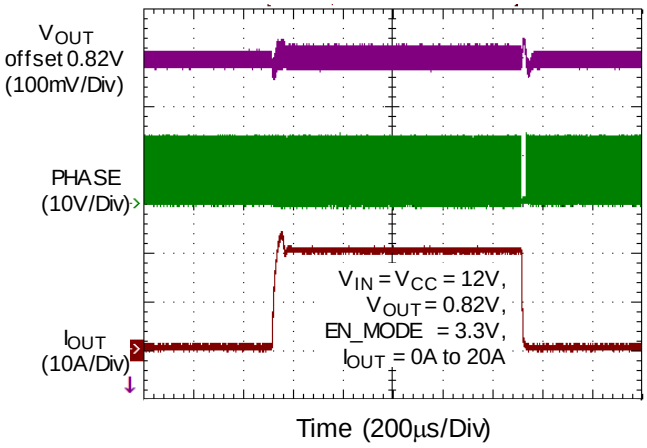
Dynamic Output Voltage Control



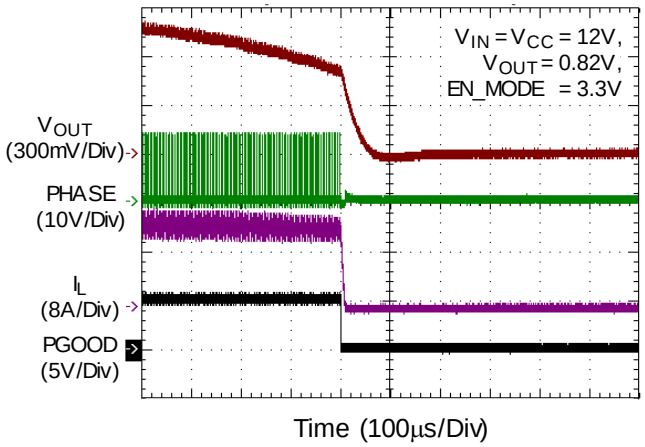
Dynamic Output Voltage Control



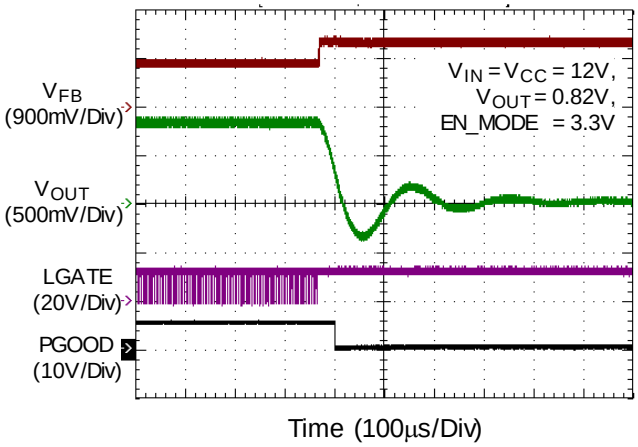
Load Transient Response



Overcurrent Limit



Overvoltage Protection



Operation

The RT8125P is suitable for low external component count configuration with appropriate amount of Equivalent Series Resistance (ESR) capacitor(s) at the output. The output ripple valley voltage is monitored at a feedback point voltage. The synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET is turned off. The pulse width of this one-shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

The on-time comparator has two inputs, one is from the output voltage, the other is from the input voltage. The on-time of the high-side switch is designed to be directly proportional to the output voltage and inversely proportional to the input voltage. The implementation results in a nearly constant switching frequency without the need of a clock generator.

Furthermore, the power up sequence of RT8125P requires that V_{IN} is ready before powering on EN and VCC.

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RT8125P PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for CPU core, I/O, and chipset RAM supplies in notebook computers. Richtek Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology solves the poor load transient response timing problems of fixed frequency current mode PWMs and avoids the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes.

Supply Voltage and Power On Reset (POR)

The input voltage range for VCC is from 4.5 V to 13.2V with respect to GND. An internal linear regulator regulates the supply voltage for internal control logic circuit. A minimum 0.1μF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor near the IC. VCC also supplies the integrated MOSFET drivers. A bootstrap diode is embedded to facilitate PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications.

The Power On Reset (POR) circuit monitors the supply voltage at the VCC pin. If VCC exceeds the POR rising threshold voltage (4.2V typ.), the controller resets and prepares the PWM for operation. If VCC falls below the POR falling threshold during normal operation, all MOSFETs stop switching. The POR rising and falling threshold has a hysteresis (0.12V typ.) to prevent unintentional noise based reset.

Enable and Mode Selection

The EN_MODE pin is a multi-function pin for integrated enable and mode selection. The controller will operate in different mode according to different EN_MODE input voltage level. When the voltage of EN_MODE pin is pulled lower than 0.4V, controller remains in shutdown. When the pin voltage is between 1.1V to 1.8V, controller operates into DEM. When the pin voltage is between 2.8V to 5V, controller operates into FCCM. Figure 1 shows a recommend circuit for EN_MODE control. Complete function requires a resistor divider that connected from 5V source to EN_MODE pin and two N-channel MOSFETs switch. The Q1 switch is used to determine the pin voltage for different operation mode, DEM or FCCM. The Q2 switch is used to enable or disable the RT8125P. In addition to verifying that the resistor divider value can raise the voltage of the EN_MODE pin, it is also necessary to ensure that the 5V source is not pulled down by the divider. Refer to Table 1 for control input level and mode state mapping results.

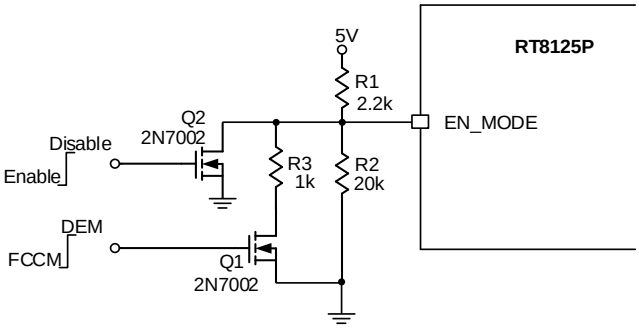


Figure 1. EN_MODE Pin Recommend Circuit

Table 1. States of EN_MODE Control Circuit

Q1	Q2	V_{EN_MODE} (V)	MODE
ON	OFF	1.51	DEM
OFF	OFF	4.5	FCCM
OFF	ON	0	Shutdown

Internal Soft-Start

The RT8125P provides an internal soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered-up. The soft-start function automatically begins once the chip is enabled. An internal current source charges the internal soft-start capacitor such that the internal soft-start voltage ramps up uniformly. The FB voltage will track the internal soft-start voltage during the soft-start interval. After the internal soft-start voltage exceeds the reference voltage, the FB voltage no longer tracks the soft-start voltage but rather follows the reference voltage. Therefore, the duty cycle of the UGATE signal as well as the input current at power up are limited.

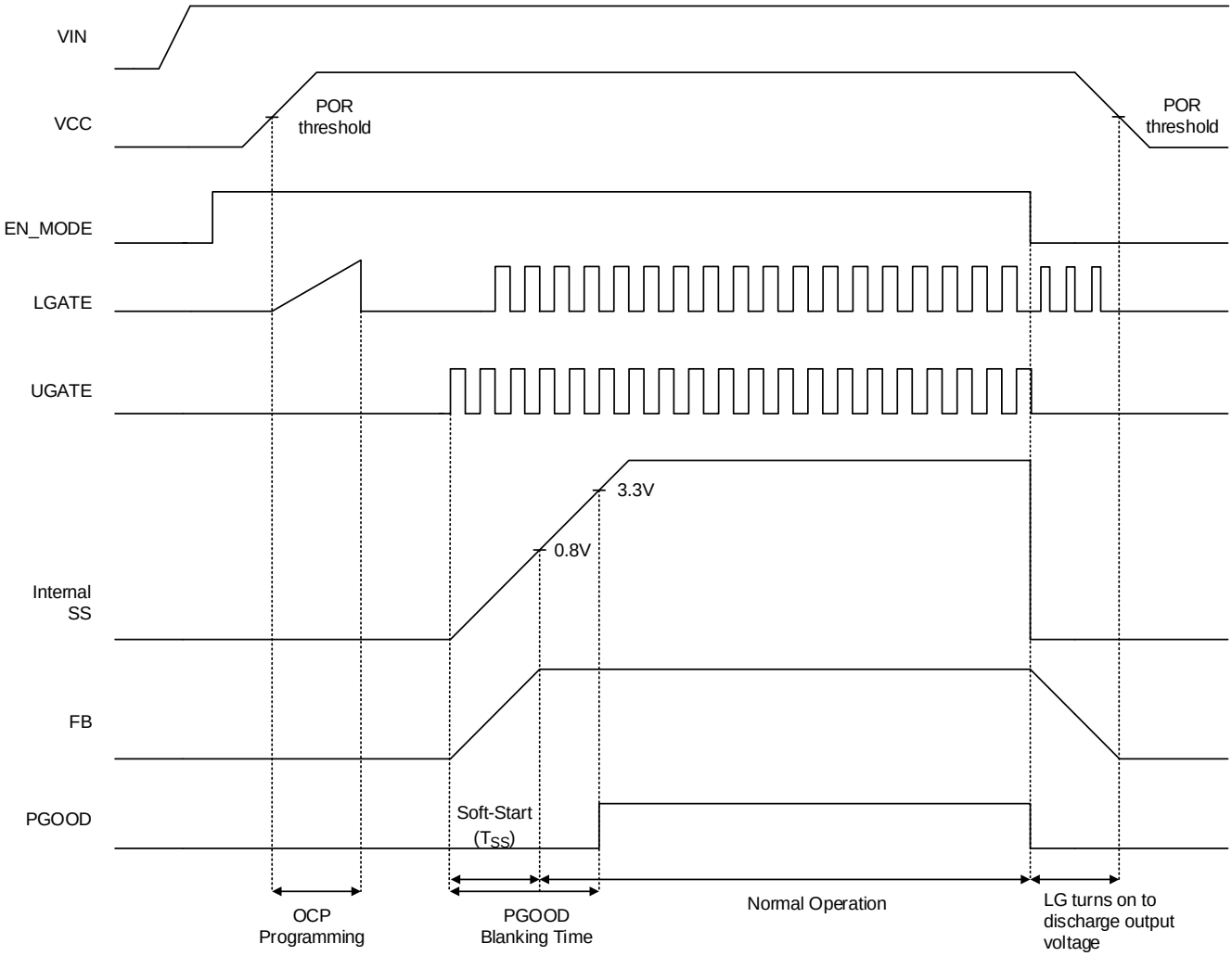


Figure 2. Soft-Start Timing Chart

Soft Discharge

When VCC is less than POR falling threshold or EN goes low, the discharging mode will be active. During discharging mode, LGATE will deliver discharging pulse and an internal switch from FB to GND will also create a path for discharging the output capacitor's residual charge to GND until the phase pin voltage is below 0.7V.

Output Voltage Setting

The RT8125P supports external reference input to provide more flexible applications. The REFIN pin and REFOUT pin are implemented to be external reference input function. The RT8125P allows the output voltage of the DC-DC converter to be adjusted via an external resistor divider. It will try to maintain the feedback pin at REFIN pin input voltage.

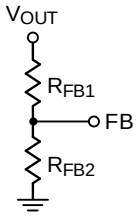


Figure 3. Output Voltage Setting

According to the resistor divider network above, the output voltage is set as:

$$V_{OUT} = \left[V_{REFIN} \times \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \right] + \frac{\Delta V_{OUT}}{2}$$

Note that the reference voltage at DEM exceeds CCM threshold by 1%.

Current Limit

The RT8125P provides lossless overcurrent protection by detecting the voltage drop across the low-side MOSFET when it is turned on. The overcurrent trip threshold is set by an external resistor, R_{OCSET}, at LGATE. During LGATE is turned on, the RT8125P senses the PHASE voltage and compares to the OCP threshold. If the sensed PHASE voltage is lower than the OCP threshold, OCP will be triggered. When OCP is triggered, LGATE will turn on to prevent inductor current from increasing until the OCP condition is released.

Current Limit Setting

Overcurrent threshold is externally programmed by adding a resistor (R_{OCSET}) between LGATE and GND. Once VCC exceeds the POR threshold and the EN pin is enabled, an internal current source I_{OCSET} flows through R_{OCSET}. To maintain the OCP threshold accuracy in temperature variation, the current source (I_{OCSET}) has an approximate 4500ppm/°C temperature slope to compensate the dependency of $R_{DS(ON)}$ of MOSFET. The voltage across R_{OCSET} is stored as the overcurrent protection threshold V_{OCSET}. After that, the current source is switched off. R_{OCSET} can be determined using the following equation:

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

where I_{VALLEY} represents the desired inductor OCP trip current (valley inductor current). If R_{OCSET} is not present, there is no current path for I_{OCSET} to build the OCP threshold. In this situation, the OCP threshold is internally preset to 250mV (typical).

For RT8125P, the OCP threshold is same as steady state during soft-stare period.

To ensure current-limit threshold accuracy, the Ciss of low-side MOSFET must be less than 8nF.

Overvoltage Protection (OVP)

The output voltage is scaled by the divider resistors and fed back to the FB pin. The voltage on the FB pin will be compared with the REFIN Voltage. For voltage related protection functions, including overvoltage protection and undervoltage protection. If the FB voltage is higher than the OVP threshold during operation, OVP will be triggered. When OVP is triggered, UGATE will go low and LGATE will go high to discharge the output capacitor. Once OVP is triggered, controller will be latched unless VCC POR is detected again or EN_MODE pin is reset.

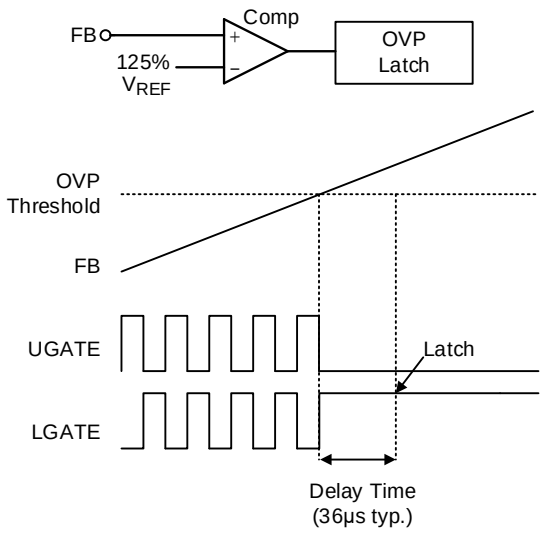


Figure 4. OVP Operation

Undervoltage Protection (UVP)

The voltage on the FB pin is monitored for undervoltage protection. The controller begins to detect UVP after soft-start finishes. If the FB voltage is lower than the UVP threshold during normal operation, UVP will be triggered. When the UVP is triggered, both UGATE and LGATE will go low the RT8125P will enter hiccup mode and continuously try to restart until the UVP situation is removed.

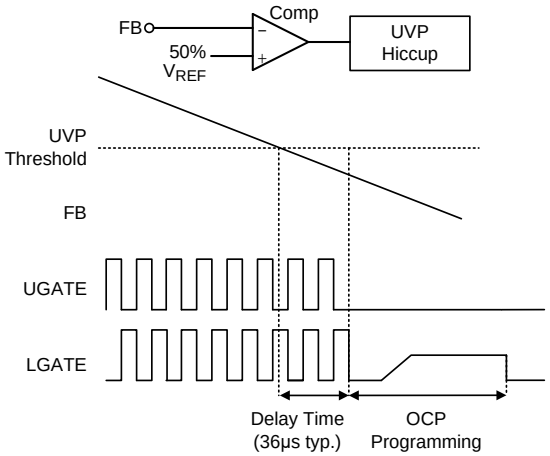


Figure 5. UVP Operation

MOSFET Drivers

The RT8125P integrates high current gate drivers for the two N-MOSFETs to obtain high efficiency power conversion in synchronous Buck topology. A dead time is used to prevent crossover conduction for the high-side and low-side MOSFETs. Because both gate signals are off during dead time, the inductor current freewheels through the body diode of the low-side MOSFET. The freewheeling current and the forward voltage of the body diode contribute to power loss. The RT8125P employs

constant dead time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, elaborate logic circuit is implemented to prevent cross conduction.

For high output current applications, two or more power MOSFETs are usually paralleled to reduce $R_{DS(ON)}$. The gate driver needs to provide more current to switch on/off these paralleled MOSFETs. Gate driver with lower source/ sink current capability result in longer rising/falling time in gate signals, and therefore higher switching loss.

The RT8125P embeds high current gate drivers to obtain high efficiency power conversion. The embedded drivers contribute to the majority of the power dissipation of the controller. Therefore, WDFN package is chosen for its power dissipation rating. If no gate resistor is used, the power dissipation of the controller can be approximately calculated using the following equation:

$$P_{DRIVER} = f_{SW} \times \left(Q_G \times V_{BOOT} + Q_{G\_Low\ Side} \times V_{DRIVER\_Low\ Side} \right)$$

where V_{BOOT} represents the voltage across the bootstrap capacitor and f_{SW} is the switching frequency. It is important to ensure the package can dissipate the switching loss and have enough room for safe operation.

Inductor Selection

The inductor plays an important role in step-down converters because it stores the energy from the input power rail and then releases the energy to the load. From the viewpoint of efficiency, the DC Resistance (DCR) of the inductor should be as small as possible to minimize the conduction loss. In addition, the inductor covers a significant proportion of the board space, so its size is also important. Low profile inductors can save board space especially when the height has a limitation. However, low DCR and low profile inductors are usually

not cost effective.

Additionally, larger inductance results in lower ripple current, which translates into the lower power loss. The inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off among performance, size and cost.

In general, inductance is chosen such that the ripple current ranges between 20% to 40% of the full load current. The inductance can be calculated using the following equation:

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_Full\ Load}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between inductor ripple current and rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters when selecting an input capacitor. Conservatively speaking, an input capacitor should have a voltage rating 1.5 times greater than the maximum input voltage to be considered a safe design. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select a proper capacitor for the RMS current rating. Using more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Placing a ceramic capacitor close to the drain of the high-side MOSFET can also be helpful in reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output capacitor and the inductor form a low-pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in voltage ripple. The output voltage ripples contains two components, ΔV_{OUT_ESR} and ΔV_{OUT_C}.

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR$$

$$\Delta V_{OUT\_C} = \Delta I_L \times \frac{1}{8 \times C_{OUT} \times f_{SW}}$$

When load transient occurs, the output capacitor supplies the load current before controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage sag can be calculated using the following equation:

$$V_{OUT\_SAG} = ESR \times \Delta I_{OUT}$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient.

Therefore ESL contributes to part of the voltage sag. Using a capacitor with low ESL will obtain better transient performance. Generally, using several capacitors connected in parallel will also have better transient performance than just one single capacitor with the same total ESR.

Unlike electrolytic capacitors, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, it is suggested to use a mixed combination of electrolytic capacitor and ceramic capacitor for achieving better transient performance.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the high-side MOSFET is small. Therefore, the switching loss of the high-side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application. However, the small duty cycle means the low-side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low-side MOSFET driver capability and the budget.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

PD(MAX) = (125°C – 25°C)/(30.5°C /W) = 3.28W for a WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and thermal resistance. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

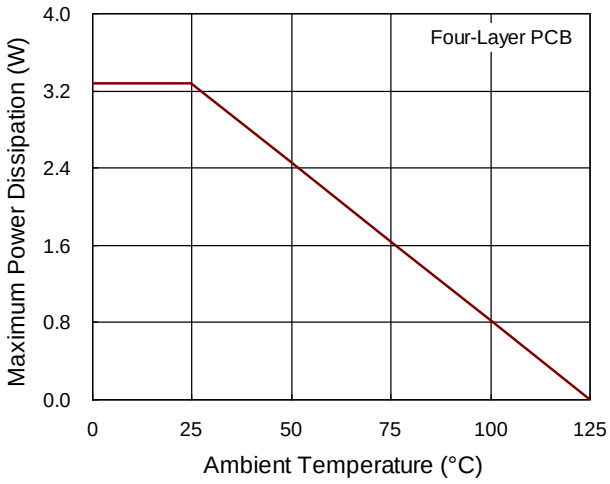


Figure 6. Derating Curve of Maximum Power Dissipation

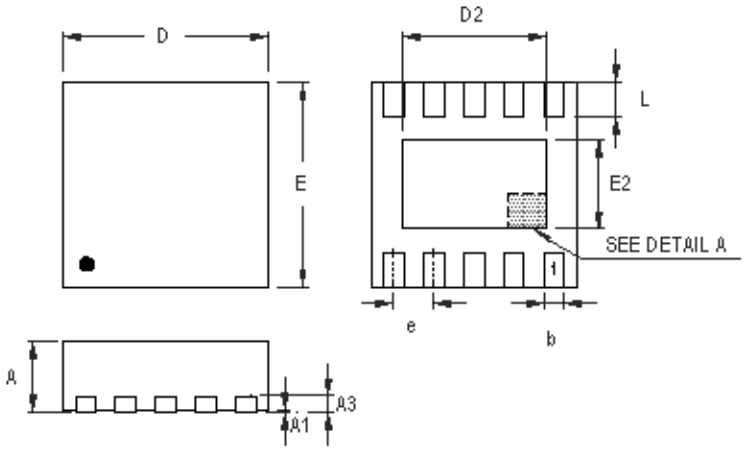
Layout Considerations

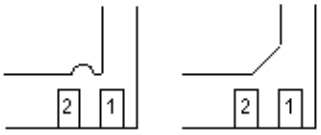
PCB layout is critical to high current high frequency switching converter designs. A good layout can help the controller to function properly and achieve expected performance. On the other hand, PCB without a careful layout can radiate excessive noise, having more power loss and even malfunction in the controller. In order to avoid the above conditions, the general guidelines below can be followed in PCB layout.

- Power stage components should be placed first. Place the input bulk capacitors close to the high-side power MOSFETs, and then locate the output inductor and finally the output capacitors.
- Placing the ceramic capacitor physically close to the drain of the high-side MOSFET. This can reduce the input voltage drop when high-side MOSFET is turned on. If more than one MOSFET is paralleled, each should have its own individual ceramic capacitor.
- Keep the high current loops as short as possible. During high speed switching, the current transition between MOSFETs usually causes di/dt voltage spike due to the parasitic components on PCB trace. Therefore, making the trace length between power MOSFETs and inductors wide and short can reduce the voltage spike and EMI.

- Make MOSFET gate driver path as short as possible. Since the gate driver uses narrow-width high current pulses to switch on/off power MOSFET, the driver path must be short to reduce the trace inductance. This is especially important for low-side MOSFET, because this can reduce the possibility of shoot-through.
- Providing enough copper area around power MOSFETs to help heat dissipation. Using thick copper also reduces the trace resistance and inductance to have better performance.
- The output capacitors should be placed physically close to the load. This can minimize the trace parasitic components and improve transient response.
- All small signal components should be located close to the controller. The small signal components include the feedback voltage divider resistors, function setting components and high frequency bypass capacitors. The feedback voltage divider resistor must be placed close to FB pin, because the FB pin is inherently noise-sensitive.
- Voltage feedback path must be away from switching nodes. The noisy switching node is, for example, the interconnection between high-side MOSFET, low-side MOSFET and inductor. Feedback path must be away from this kind of noisy node to avoid noise pick-up.
- A multi-layer PCB design is recommended. Make use of one single layer as the ground and have separate layers for power rail, or signal is suitable for PCB design.

Outline Dimension





DETAIL A

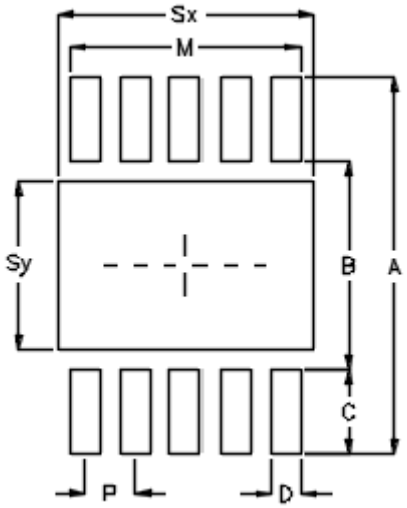
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

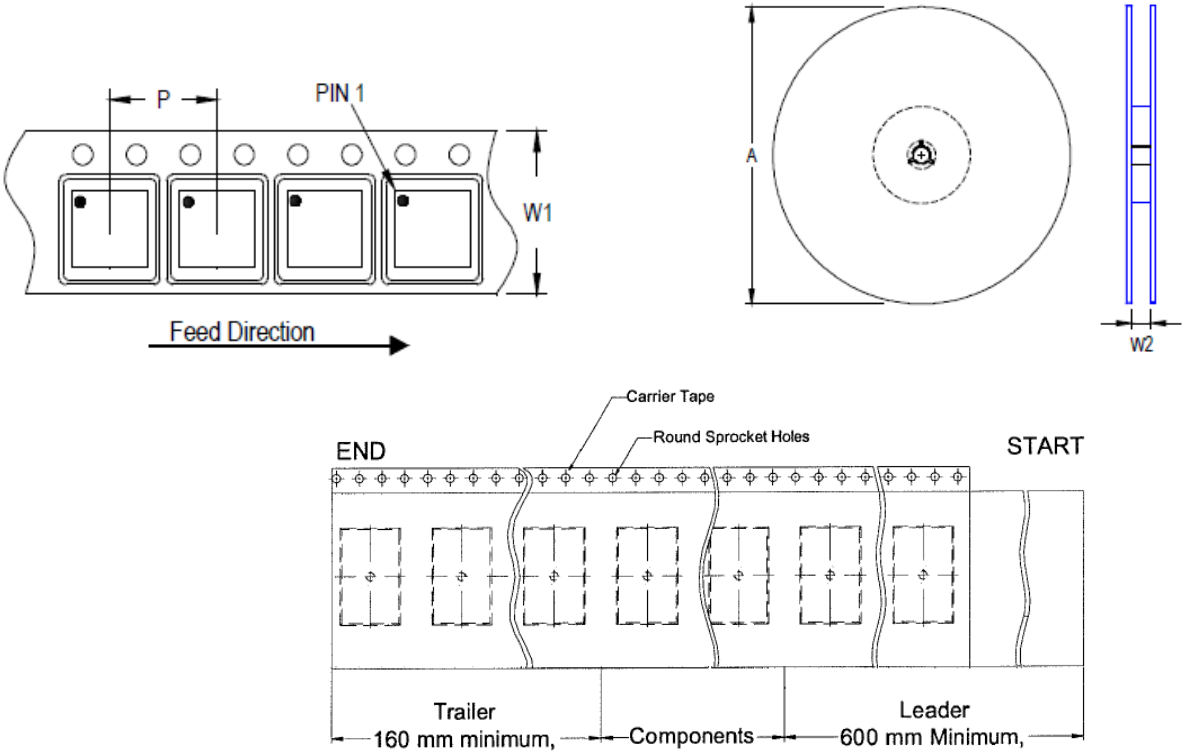
Footprint Information



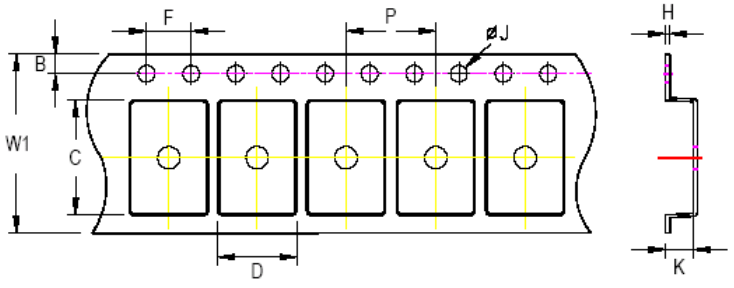
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box					Carton			
	Size	Units	Item	Size(cm)	Weight(Kg)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN & DFN 3x3	7”	1,500	Box A	18.3*18.3*8.0	0.1	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	0.03	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2023/11/27	Final	