18V, 1.5A, 500kHz ACOT™ Step-down Converter in 8 Pin TSOT-23

General Description

The RT7255 is a simple, easy-to-use, 1.5A synchronous step-down DC-DC converter with an input supply voltage range of 4.3V to 18V. The device build-in an accurate 0.6V reference voltage and integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency in a TSOT-23-8 package.

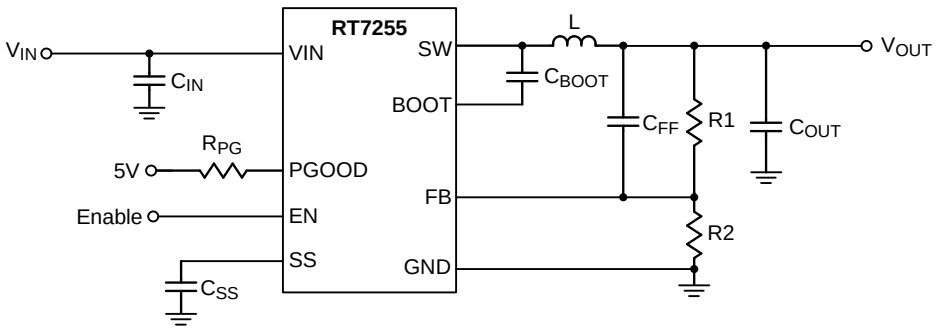
The RT7255 adopts Advanced Constant On-Time (ACOT™) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The RT7255A operates in automatic PSM that maintains high efficiency during light load operation. The RT7255C operates in Forced PWM that helps meet tight voltage regulation accuracy requirements.

The RT7255 senses low-side FETs current for a robust over-current protection. It features cycle-by-cycle current limit protection and prevent the device from the catastrophic damage in output short circuit, over current or inductor saturation. An externally adjustable soft-start function prevents inrush current during start-up. The device also includes input under-voltage lockout, output under-voltage protection, and over-temperature protection (thermal shutdown) to provide safe and smooth operation in all operating conditions. The RT7255 is offered in a TSOT-23-8 package.

Features

- **1.5A Converter With Built-In 230mΩ/130mΩ Low $R_{DS(ON)}$ Power FETs**
- **Input Supply Voltage Range : 4.3V to 18V**
- **Output Voltage Range : 0.6 to 8V**
- **Advanced Constant On-Time (ACOT™) Control**
- **Ultrafast Transient Response**
- **No Needs For External Compensations**
- **Optimized for Low-ESR Ceramic Output Capacitors**
- **0.6V ±1.5% High-Accuracy Feedback Reference Voltage**
- **Low Quiescent Current (500μA typ.)**
- **Optional for Operation Modes :**
  - **Power Saving Mode (PSM) at Light Load (RT7255A)**
  - **Forced PWM Mode (RT7255C)**
- **Light-load V_{OUT} Ripple Reduction Technology in PSM**
- **Fixed Switching Frequency : 500kHz**
- **Externally Adjustable Soft-Start**
- **Monotonic Start-Up for Pre-Biased Output**
- **Input Under-Voltage Lockout (UVLO)**
- **Output Under-Voltage Protection (UVP) with Hiccup Mode**
- **Power Good Indication**
- **Enable Control**
- **Available In TSOT-23-8 Package**

Simplified Application Circuit



Ordering Information

RT7255 □□□

- Package Type
  J8 : TSOT-23-8
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- A : Hiccup + PSM
  C : Hiccup + PWM

Note :

Richtek products are :

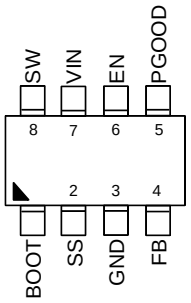
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

Pin Configurations

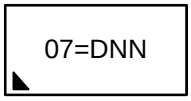
(TOP VIEW)



TSOT-23-8

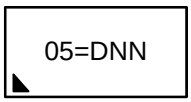
Marking Information

RT7255AGJ8



07= : Product Code
DNN : Date Code

RT7255CGJ8

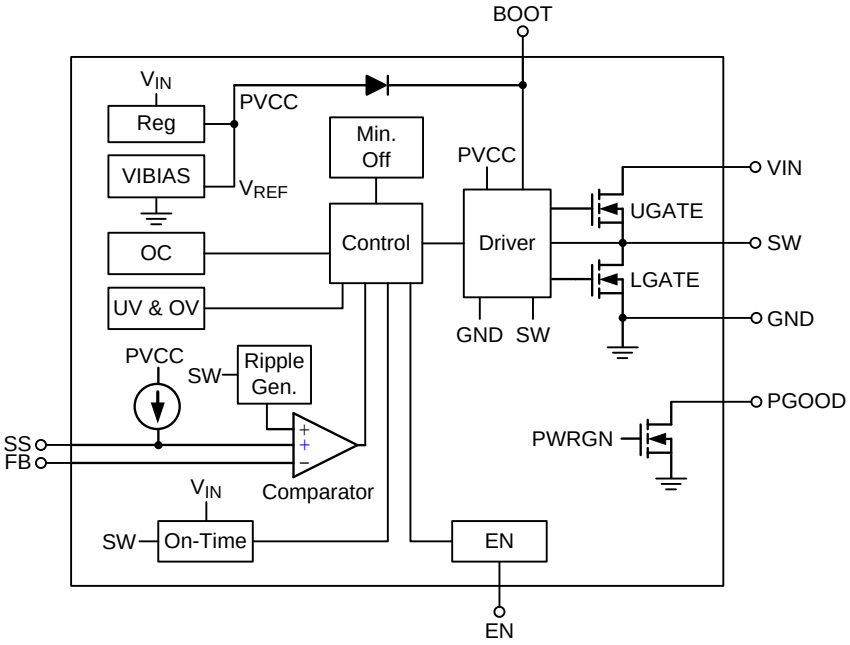


05= : Product Code
DNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap supply for high-side gate driver. Connect a 1μF ceramic capacitor between the BOOT and SW pins.
2	SS	Soft-start time setting. Connect a capacitor from SS to GND to set the soft-start period.
3	GND	Power ground.
4	FB	Feedback voltage input. The pin is used to set the output voltage of the converter via a resistive divider. The converter regulates V_{FB} to 0.6V.
5	PGOOD	Power good indicator output.
6	EN	Enable control input. Connect EN to a logic-high voltage to enable the IC or to a logic-low voltage to disable. Do not leave this high impedance input unconnected. For automatic start up, connect the EN pin to VIN with a 100kΩ resistor.
7	VIN	Power input. The input voltage range is from 4.3V to 18V. Must bypass with a suitable large ceramic capacitor at this pin.
8	SW	Switch node. Connect to external L-C filter.

Function Block Diagram



Operation

The RT7255 is a synchronous step-down converter with advanced constant on-time control mode. Using the ACOT control mode can reduce the output capacitance and fast transient response. It can minimize the component size without additional external compensation network.

Current Protection

The inductor current is monitored via the internal switches cycle-by-cycle. Once the output voltage drops under UV threshold, the RT7255 will enter hiccup mode.

UVLO Protection

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage of VIN is lower than the UVLO falling threshold voltage, the device will be lockout.

Thermal Shutdown

When the junction temperature exceeds the OTP threshold value, the IC will shut down the switching operation. Once the junction temperature cools down and is lower than the OTP lower threshold, the converter will autocratically resume switching.

Absolute Maximum Ratings (Note 1)

- VIN to GND ---------- –0.3V to 20V
- SW to GND ---------- –0.3V to 20V
  <10ns ---------- –5V to 25V
- BOOT to GND ---------- –0.3V to 26V
- BOOT to SW ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  TSOT-23-8 ---------- 0.68W
- Package Thermal Resistance (Note 2)
  TSOT-23-8, θ_{JA} ---------- 145.5°C/W
  TSOT-23-8, θ_{JC} ---------- 13.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4.3V to 18V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current (Shutdown)		I_{SHDN}	V_{EN} = 0V	--	--	12	μA
Supply Current (Quiescent)		I_Q	V_{EN} = 2V, V_{FB} = 1V	--	0.5	--	mA
Switch-On Resistance	High-Side	$R_{DS(ON)\_H}$	VBST – SW = 4.8V	--	230	--	mΩ
	Low-Side	$R_{DS(ON)\_L}$	PVIN = 5V	--	130	--	
Current Limit		I_{LIM}	Valley current	1.7	2.2	2.8	A
Oscillator Frequency		f_{SW}		--	500	--	kHz
Maximum Duty Cycle		D_{MAX}		--	90	--	%
Minimum On-Time		t_{ON_MIN}		--	60	--	ns
Feedback Threshold Voltage		V_{FB}		591	600	609	mV
Enable Input Voltage	Logic-High	V_{EN_H}		1.5	--	--	V
	Logic-Low	V_{EN_L}		--	--	0.4	
VIN Under-Voltage Lockout Threshold-Rising		V_{UVLO}		3.55	3.9	4.25	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Under-Voltage Lockout Threshold-Hysteresis	ΔV_{UVLO}		--	340	--	mV
Soft-Start Period	t_{SS}		--	800	--	μs
Thermal Shutdown Threshold	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
VOUT Discharge Resistance	$R_{Discharge}$	EN = 0V, V_{OUT} = 0.5V	--	50	100	Ω
Power Good Threshold		V_{FB} rising (Good)	87	92	97	%
		V_{FB} falling (Fault)	--	80	--	
Soft-Start Charge Current	I_{SS}	V_{SS} = 0V	--	4	--	μA

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. The measurement case position of θ_{JC} is on the lead of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

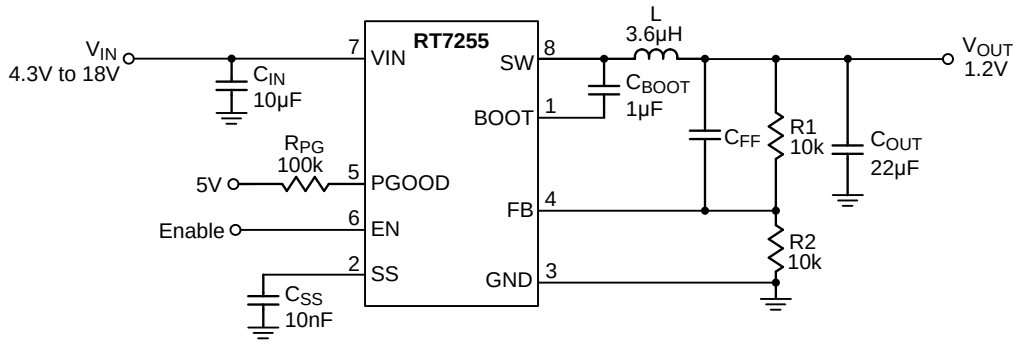
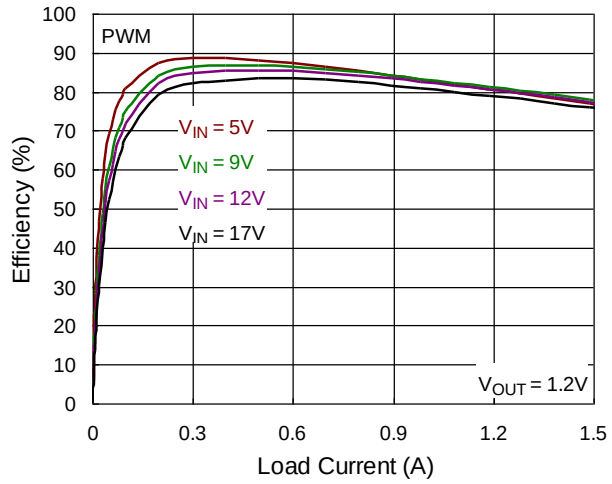


Table 1. Suggested Component Values

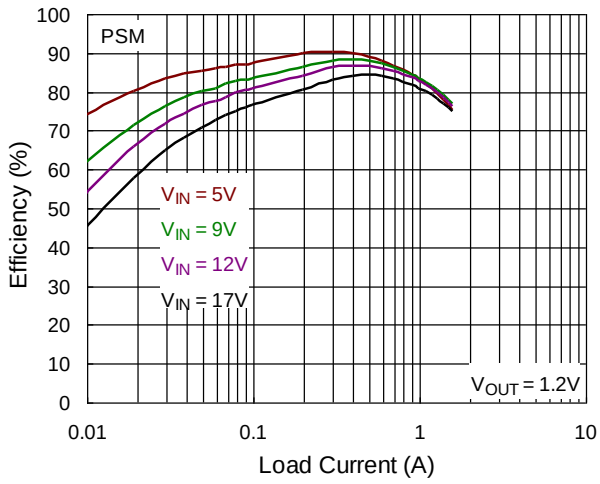
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)	C_{FF} (pF)
5	110	15	10	22	39
3.3	115	25.5	6.8	22	33
2.5	25.5	8.06	4.7	22	NC
1.2	10	10	3.6	22	NC

Typical Operating Characteristics

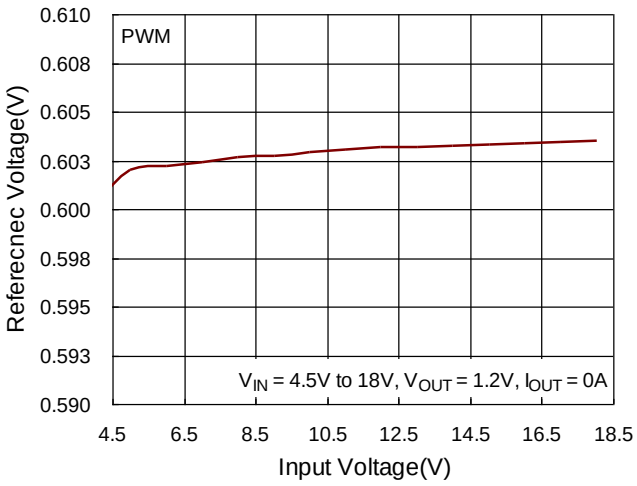
Efficiency vs. Load Current



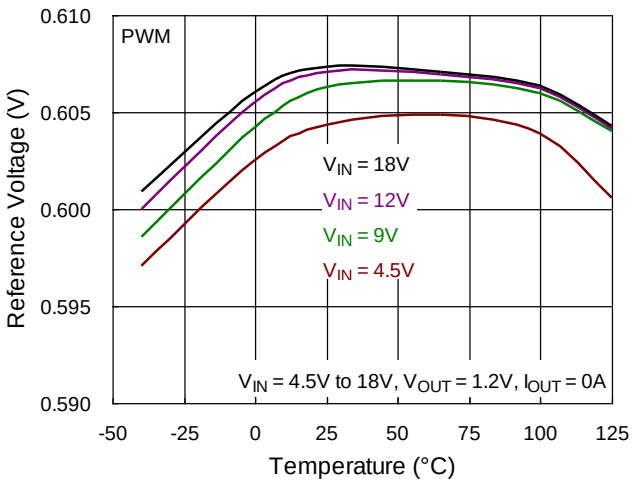
Efficiency vs. Load Current



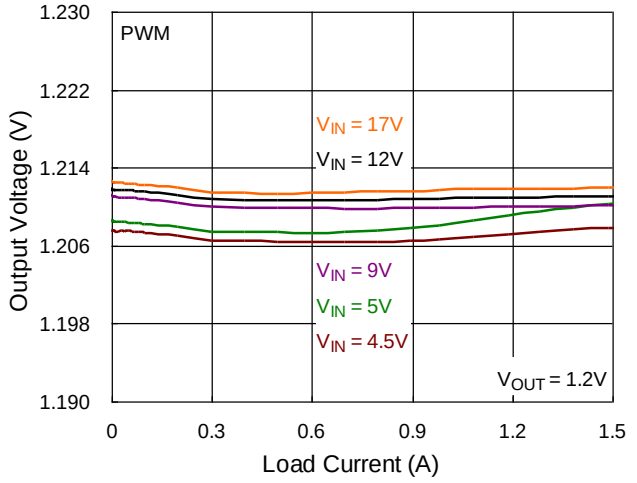
Referecnce Voltage vs. Input Voltage



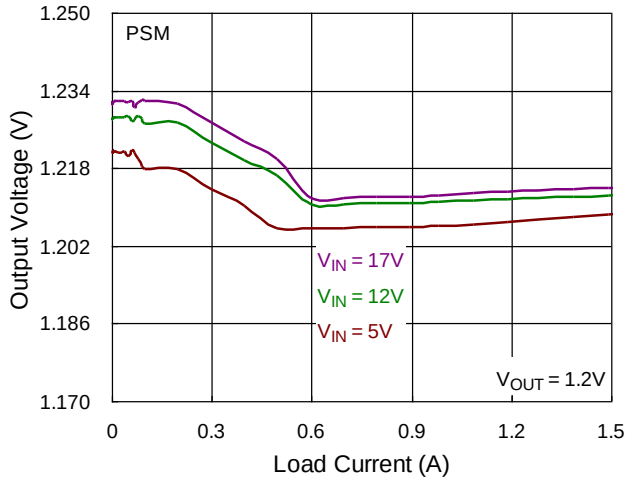
Reference vs. Temperature



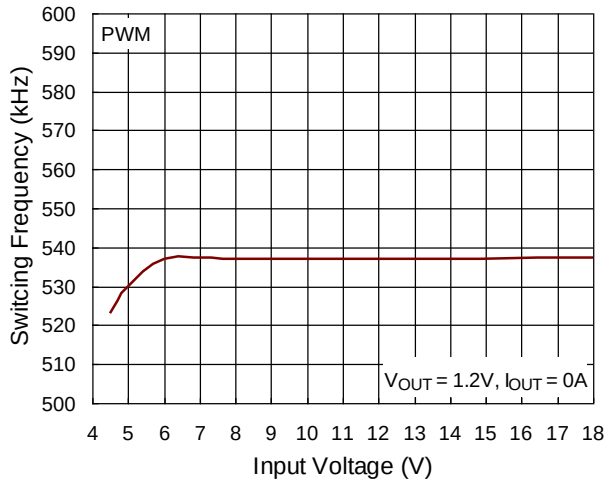
Output Voltage vs. Load Current



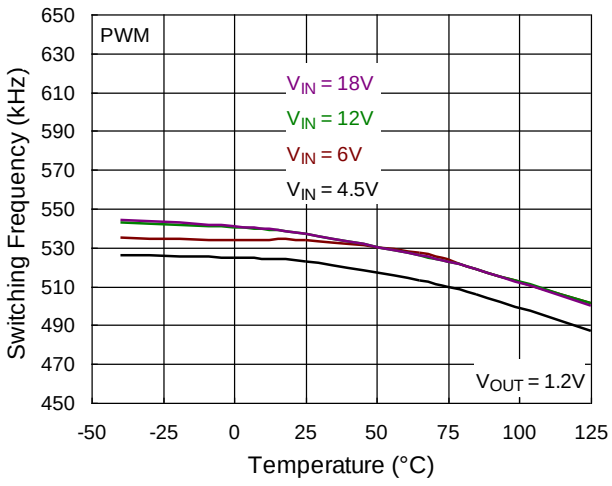
Output Voltage vs. Load Current



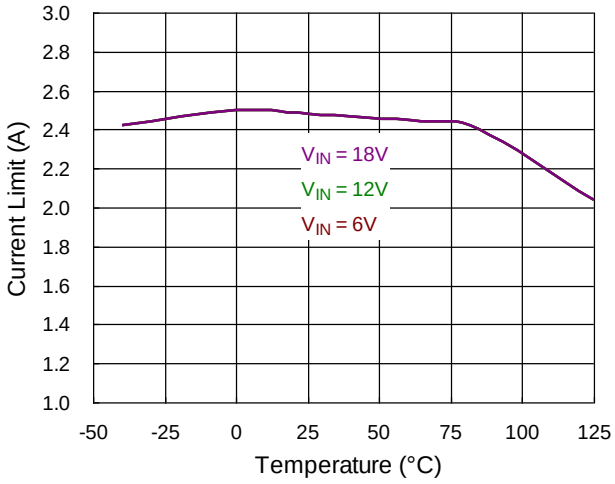
Switching Frequency. vs. Input Voltage



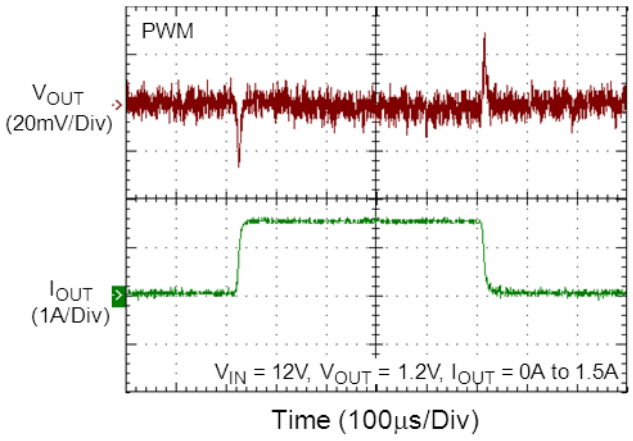
Switching Frequency vs. Temperature



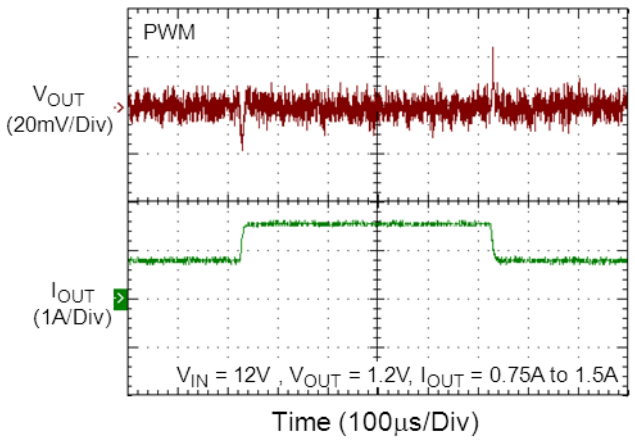
Current Limit vs. Temperature



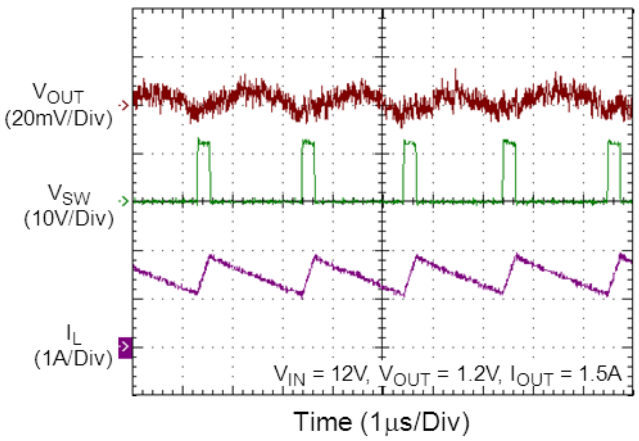
Load Transient Response



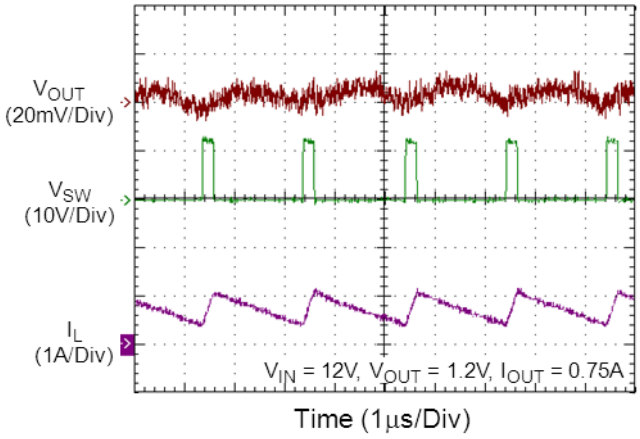
Load Transient Response



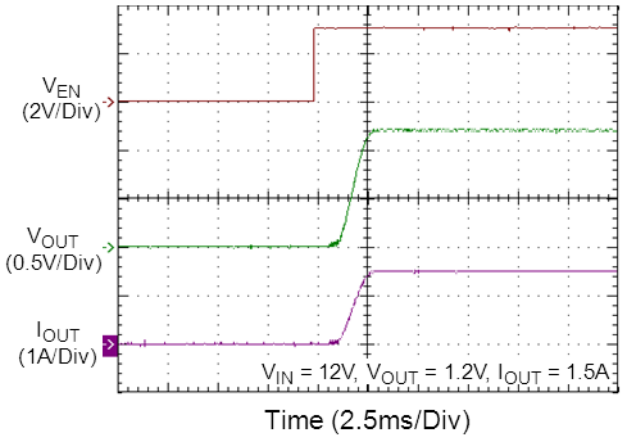
Switching



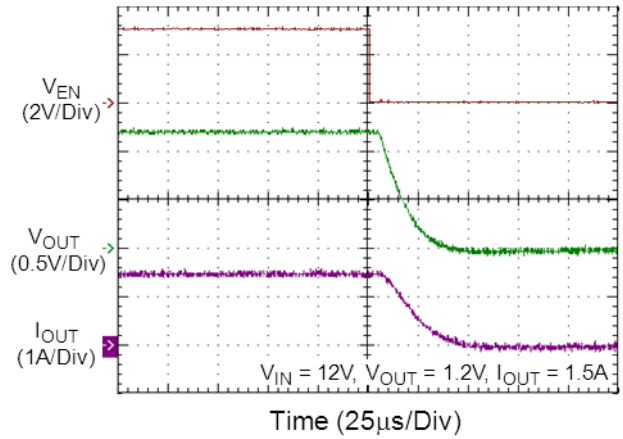
Switching



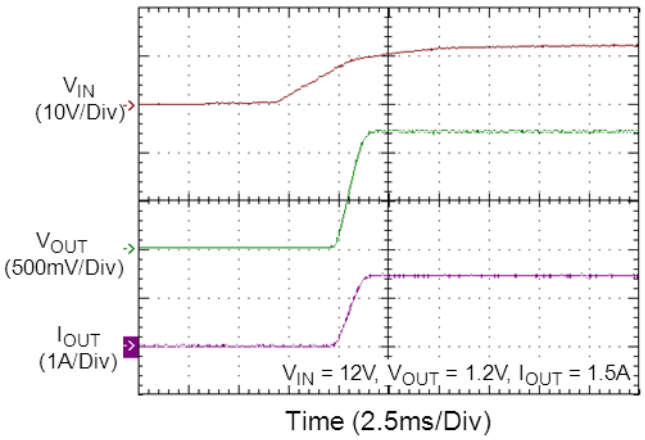
Power On from EN



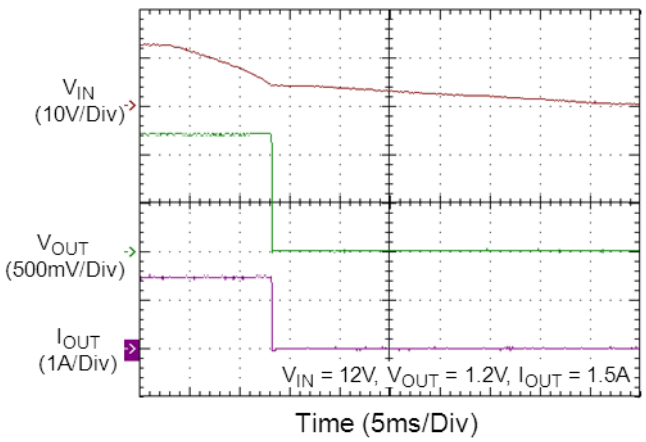
Power Off from EN



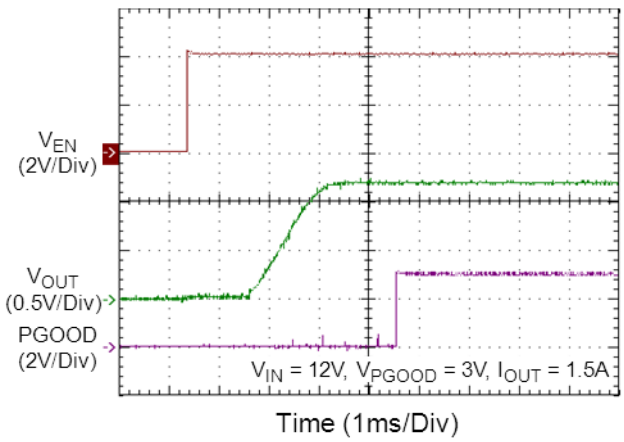
Power On from VIN



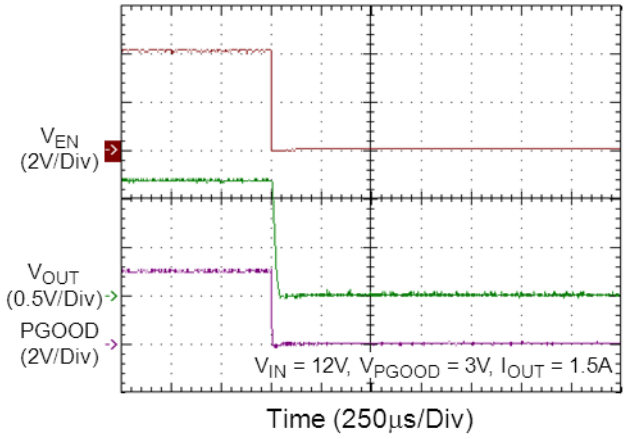
Power Off from VIN



Power Good from EN Turn On



Power Good from EN Turn Off



Application Information

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20% to 40% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

$$I_{L(VALLY)} = I_{OUT(MAX)} - \frac{\Delta I_L}{2}$$

Considering the Typical Operating Circuit for 1.2V output at 1.5A and an input voltage of 12V, using an inductor ripple of 0.6A (40%), the calculated inductance value is :

$$L = \frac{1.2 \times (12 - 1.2)}{12 \times 500kHz \times 0.6} = 3.6\mu H$$

The ripple current was selected at 0.6A and, as long as we use the calculated 3.6μH inductance, that should be the actual ripple current amount. The ripple current and required peak current as below :

$$\Delta I_L = \frac{1.2 \times (12 - 1.2)}{12 \times 500kHz \times 3.6\mu H} = 0.6A$$

$$\text{and } I_{L(PEAK)} = 1.5A + \frac{0.6}{2} = 1.8A$$

Inductor's saturation current should be chosen over IC's current limit.

Input Capacitor Selection

The input filter capacitors are needed to smooth out the switched current drawn from the input power source and to reduce voltage ripple on the input. The actual capacitance value is less important than the RMS current rating (and voltage rating, of course). The RMS input ripple current (I_{RMS}) is a function of the input voltage, output voltage, and load current :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. However, take care when these capacitors are used at the input of circuits supplied by a wall adapter or other supply connected through long, thin wires. Current surges through the inductive wires can induce ringing at the RT7255 input which could potentially cause large, damaging voltage spikes at VIN. If this phenomenon is observed, some bulk input capacitance may be required. Ceramic capacitors (to meet the RMS current requirement) can be placed in parallel with other types such as tantalum, electrolytic, or polymer (to reduce ringing and overshoot).

Choose capacitors rated at higher temperatures than required. Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application. The typical operating circuit use 10μF and one 0.1μF low ESR ceramic capacitors on the input.

Output Capacitor Selection

The RT7255 is optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output Ripple

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

For the Typical Operating Circuit for 1.2V output and an inductor ripple of 0.46A, with 1 x 22μF output capacitance each with about 5mΩ ESR including PCB trace resistance, the output voltage ripple components are :

$$V_{RIPPLE(ESR)} = 0.46A \times 5m\Omega = 2.3mV$$

$$V_{RIPPLE(C)} = \frac{0.46A}{8 \times 22\mu F \times 500kHz} = 5.227mV$$

$$V_{RIPPLE} = 2.3mV + 5.227mV = 7.527mV$$

Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT transient response is very quick and output transients are usually small.

However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's 500kHz switching frequency.

But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components : the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Output Capacitors Stability Criteria

The RT7255's ACOT™ control architecture uses an internal virtual inductor current ramp and other compensation that ensures stability with any reasonable output capacitor. The internal ramp allows the IC to operate with very low ESR capacitors and the IC is stable with very small capacitances. Therefore, output capacitor selection is nearly always a matter of meeting output voltage ripple and transient response requirements, as discussed in the previous sections. For the sake of the unusual application where ripple voltage is unimportant.

Any ESR in the output capacitor lowers the required minimum output capacitance, sometimes considerably. For the rare application where that is needed and useful, the equation including ESR is given here :

$$C_{OUT} \geq \frac{V_{OUT}}{2 \times f_{SW} \times V_{IN} \times (R_{ESR} + 13647 \times L \times V_{OUT})}$$

As can be seen, setting RESR to zero and simplifying the equation yields the previous simpler equation. To allow for the capacitor's temperature and bias voltage coefficients, use at least double the calculated capacitance and use a good quality dielectric such as X5R or X7R with an adequate voltage rating since ceramic capacitors exhibit considerable capacitance reduction as their bias voltage increases.

Feed-forward Capacitor (C_{ff})

The RT7255 is optimized for ceramic output capacitors and for low duty cycle applications. However for high-output voltages, with high feedback attenuation, the circuit's response becomes over-damped and transient response can be slowed. In high-output voltage circuits (V_{OUT} > 3.3V) transient response is improved by adding a small "feed-forward" capacitor (C_{ff}) across the upper FB divider resistor (Figure 1), to increase the circuit's Q and reduce damping to speed up the transient response without affecting the steady-state stability of the circuit. Choose a suitable capacitor value that following below step.

- Get the BW the quickest method to do transient response from 30% load to full load. Confirm the damping frequency. The damping frequency is BW.

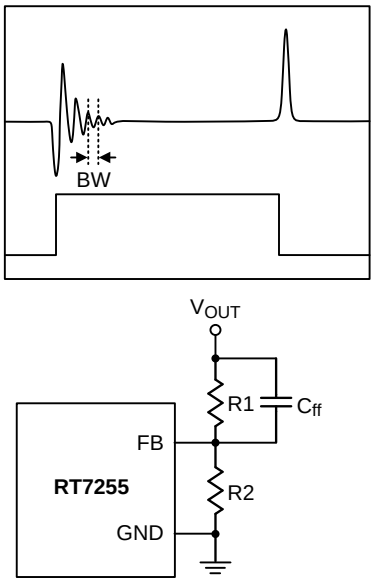


Figure 1. C_{ff} Capacitor Setting

- C_{ff} can be calculated base on below equation :

$$C_{ff} = \frac{1}{2 \times 3.1412 \times R1 \times BW \times 0.8}$$

External Soft-Start (SS)

The RT7255 provides soft-start function. The soft-start function is used to prevent large inrush current while converter is being powered-up. The soft-start timing can be programmed by the external capacitor C_{SS} between SS and GND. An internal current source I_{SS} (6μA) charges an external capacitor to build a soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft start time is calculated as follows :

Soft-Start time t_{SS} = C_{SS} x 0.6 / 6μA

The available capacitance range is from 2.7nF to 120nF. Do not leave SS unconnected

Enable Operation (EN)

For automatic start-up the high-voltage EN pin can be connected to V_{IN}, through a 100kΩ resistor. Its large hysteresis band makes EN useful for simple delay and timing circuits. EN can be externally pulled to V_{IN} by

adding a resistor-capacitor delay (R_{EN} and C_{EN} in Figure 2). Calculate the delay time using EN's internal threshold where switching operation begins (1.4V, typical).

An external MOSFET can be added to implement digital control of EN when no system voltage above 2V is available (Figure 3). In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input under voltage lockout threshold (Figure 4).

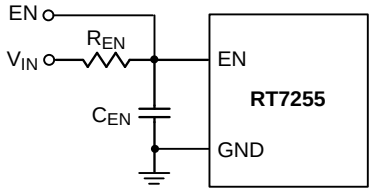


Figure 2. External Timing Control

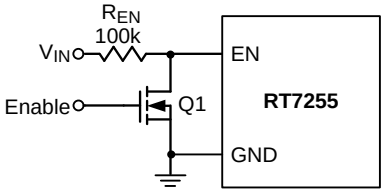


Figure 3. Digital Enable Control Circuit

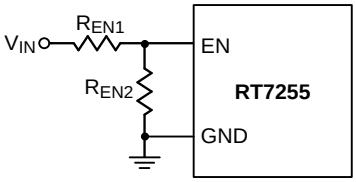


Figure 4. Resistor Divider for Lockout Threshold Setting

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

V_{OUT} = 0.6 x (1 + R1 / R2)

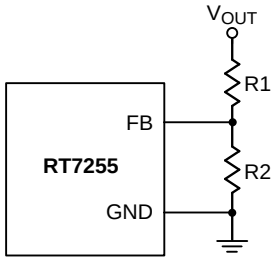


Figure 5. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \times (V_{OUT} - 0.6)}{0.6}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

External BOOT Bootstrap Diode

When the input voltage is lower than 5.5V it is recommended to add an external bootstrap diode between VIN (or VINR) and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

External BOOT Capacitor Series Resistance

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{SW} rises rapidly. During switch turn-off, SW is discharged relatively slowly by the inductor current during the deadtime between high-side and low-side switch on-times. In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<47Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the

high-side switch turn-on and $V_{SW's}$ rise. To remove the resistor from the capacitor charging path (avoiding poor enhancement due to undercharging the BOOT capacitor), use the external diode shown in Figure 6 to charge the BOOT capacitor and place the resistance between BOOT and the capacitor/diode connection.

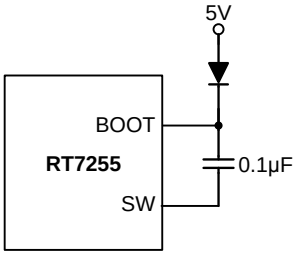


Figure 6. External Bootstrap Diode

Over-Temperature Protection

The RT7255 features an Over-Temperature Protection (OTP) circuitry to prevent from overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will resume operation. To maintain continuous operation, the maximum junction temperature should be lower than 125°C.

Under-Voltage Protection

Hiccup Mode

For the Hiccup, it provides Hiccup Mode Under Voltage Protection (UVP). When the V_{FB} voltage drops below 0.4V, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RT7255 will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during soft-start period.

Clamp Mode

For the Clamp, it provides Current limit protection, Under Voltage Protection (UVP) is disable, when the UV condition is removed, the converter will resume operation.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TSOT-23-8 package, the thermal resistance, θ_{JA}, is 145.5°C/W on a standard four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (145.5°C/W) = 0.68W for TSOT-23-8 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

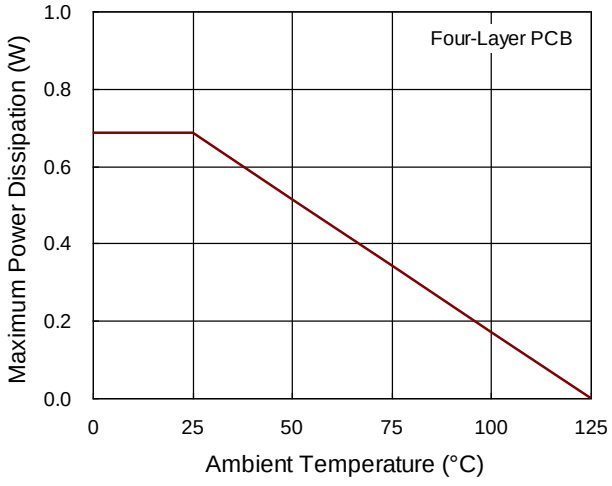


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT7255, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close to the IC as possible.
- Keep the traces of the main current paths as short and wide as possible.
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up. Components near the RT7255
- An example of PCB layout guide is shown in Figure for reference.

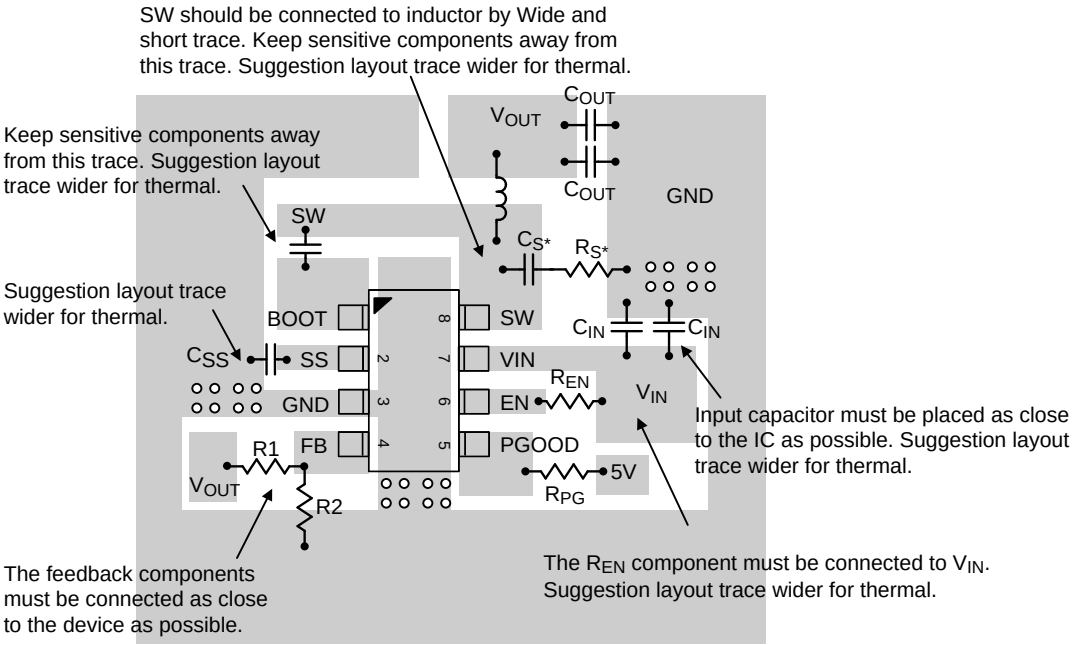
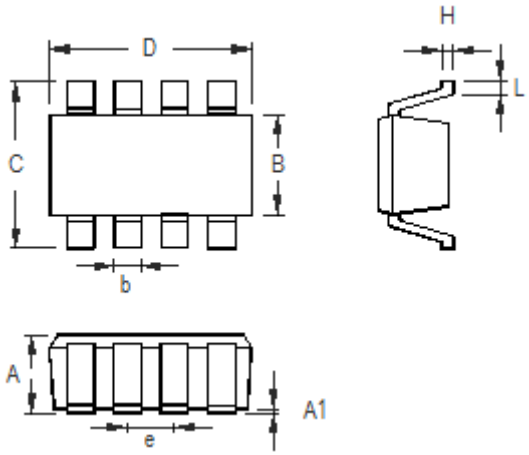


Figure 8. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.220	0.380	0.009	0.015
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.585	0.715	0.023	0.028
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-8 Surface Mount Package

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