12A, 23V, 500kHz, ACOT™ Synchronous Buck Converter with VTT LDO for Memory Power Supply

General Description

The RT7241A provides a complete power supply for DDR3/DDR3L/LPDDR3/DDR4 memory systems. It integrates an Advanced Constant On-Time (ACOT™) mode synchronous Buck converter with a 1.5A sink/source tracking linear regulator.

The PWM converter provides low quiescent supply current, high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low-voltage chipset RAM supplies in notebook computers. The ACOT™ control scheme handles wide input/output voltage ratios with ease and provides a very fast response to load transients with no external compensators.

The 1.5A sink/source VTT LDO maintains fast transient response only requiring 10µF ceramic output capacitance. The RT7241A supports all of the sleep state controls placing VTT at high-Z in S3 and discharging VDDQ and VTT in S4/S5.

The RT7241A provides complete protection features including OCP, OVP, UVP, and thermal shutdown. The RT7241A is available in the UQFN-18L 3x4 package.

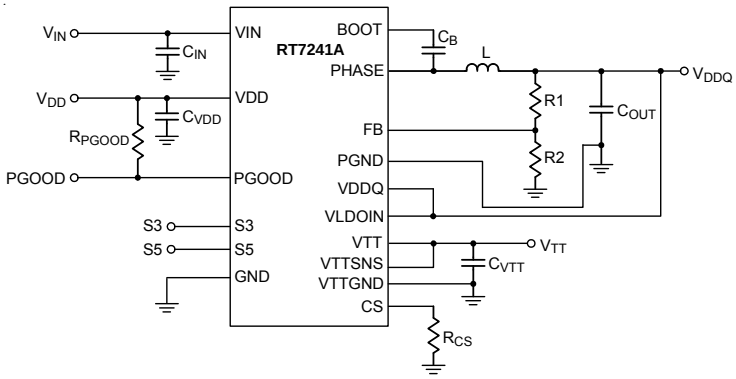
Applications

- DDR3/DDR3L/LPDDR3/DDR4 Memory Power Supplies
- Notebook computers

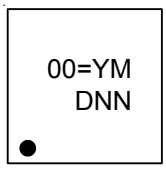
Features

- **DDR3/DDR3L/LPDDR3/DDR4 Complete Solution**
- **PWM Converter (VDDQ)**
  - **100µA Low Quiescent Supply Current at S3 Mode**
  - **ACOT™ Mode Performs Fast Transient Response**
  - **Support MLCC Output Capacitors**
  - **Integrated Low On-Resistance MOSFETs**
    - **17mΩ of High-Side MOSFET**
    - **4.5mΩ of Low-Side MOSFET**
  - **Adjustable from 0.6V to 1.5V Output Range for 1.5V (DDR3), 1.35V (DDR3L), 1.2V (LPDDR3) and 1.2V (DDR4)**
  - **4.5V to 23V Battery Input Range**
  - **500kHz Switching Frequency**
  - **Resistor Adjustable Valley Current Limit**
  - **Over-/Under-Voltage Protection**
  - **Internal Voltage Ramp Soft-Start**
  - **Power Good Indicator**
- **1.5A LDO (VTT)**
  - **Capable to Sink and Source up to 1.5A**
  - **LDO Input Available to Optimize Power Losses**
  - **Require Only 10µF Ceramic Output Capacitor**
  - **Integrated Divider Tracks 1/2 VDDQ for VTT**
  - **Accuracy ±20mV for VTT**
  - **Support High-Z in S3 and Soft-Off in S4/S5**
- **Tracking Mode Discharge Control**
- **Thermal Capable Flip-chip (FC) Package for 12A VDDQ Converter and 1.5A VTT LDO**
- **RoHS Compliant and Halogen Free**

Simplified Application Circuit



Marking Information



00= : Product Code

YMDNN : Date Code

Ordering Information

RT7241A □ □

- Package Type
  QUF : UQFN-18L 3x4 (FC) (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

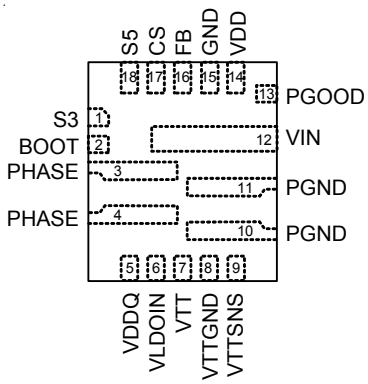
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



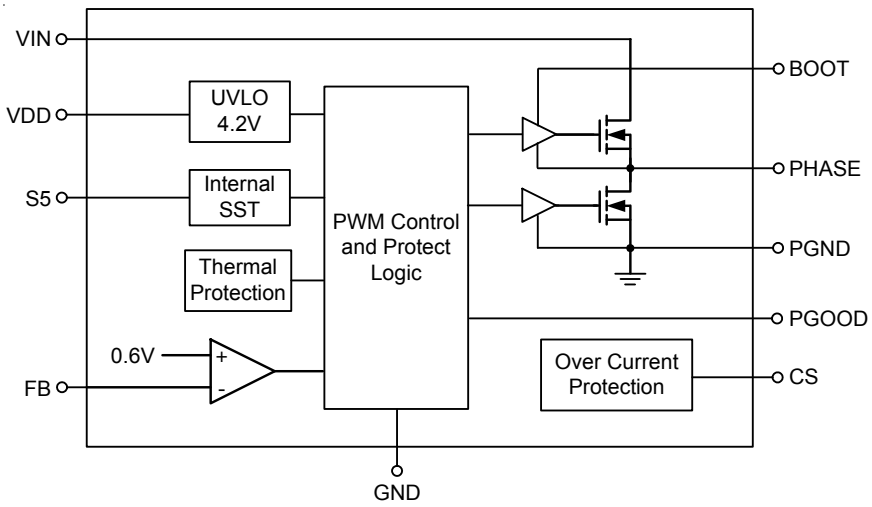
UQFN-18L 3x4 (FC)

Functional Pin Description

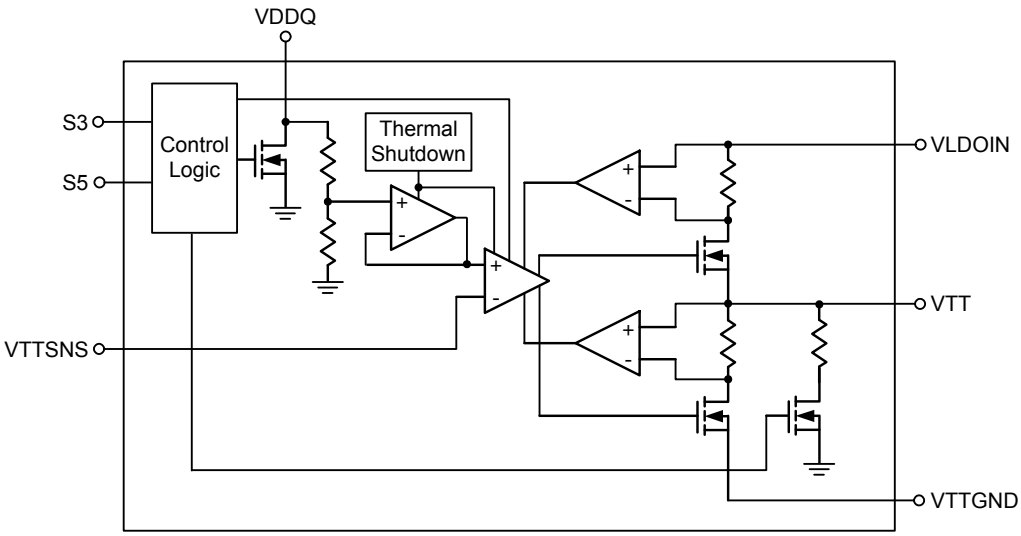
Pin No.	Pin Name	Pin Function
1	S3	VTT LDO enable control input. Do not leave this pin floating.
2	BOOT	Bootstrap supply for high-side gate driver. A capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between the PHASE and BOOT pins to form a floating supply across the power switch driver.
3, 4	PHASE	Switch node. External inductor connection for VDDQ.
5	VDDQ	Reference input for the VTT LDO. An internal discharging circuit is connected to this pin.
6	VLDOIN	Power supply for the VTT LDO.
7	VTT	Power output for the VTT LDO.
8	VTTGND	Power ground for the VTT LDO.
9	VTTSNS	Voltage sense input for the VTT LDO. Connect to the terminal of the VTT LDO output capacitor.
10, 11	PGND	Power ground for VDDQ.
12	VIN	Supply input for VDDQ.
13	PGOOD	Open-drain power good indicator output.
14	VDD	Analog supply input.
15	GND	Analog ground.
16	FB	Feedback voltage input. Connect to a resistive voltage divider from VDDQ to GND to adjust the output of PWM converter.
17	CS	Current limit threshold setting input. Connect to GND through the setting resistor.
18	S5	PWM converter enable control input. Do not leave this pin floating.

Functional Block Diagram

Buck Converter



VTT LDO



Absolute Maximum Ratings (Note 1)

- VIN to PGND ---------- –0.3V to 27V
- SW to PGND ---------- –0.3V to 27.3V
- BOOT to PGND ---------- –0.6V to 33.3V
- S3,VDDQ,VLDOIN,VTT,VTTSNS,PGOOD,VDD,FB,CS,S5 to GND ---------- –0.3V to 6V
- PGND to GND ---------- –0.3V to 0.3V
- PGND to VTTGND ---------- –0.3V to 0.3V
- GND to VTTGND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  UQFN-18L 3x4 (FC) ---------- 3.03W
- Package Thermal Resistance (Note 2)
  UQFN-18L 3x4 (FC), θ_{JA} ---------- 33°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, VIN ---------- 4.5V to 23V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Quiescent Supply Current		FB forced above the regulation point, V_{S5} = 2V, V_{S3} = 0V	80	100	130	μA
I_{VLDOIN} BIAS Current		V_{S5} = V_{S3} = 2V, VTT = no load	--	1	--	μA
I_{VLDOIN} Standby Current		V_{S5} = 2V, V_{S3} = 0V, VTT = no load	--	0.1	10	μA
Shutdown Current		V_{S5} = V_{S3} = 0V	--	2.5	10	μA
PWM Converter						
VDDQ Voltage Range			0.6	--	1.5	V
VDDQ Input Resistance			--	100	--	kΩ
VDDQ Shutdown Discharge Resistance		V_{S5} = 0V	--	15	--	Ω
Switch On-Resistance						
Switch On-Resistance	$R_{DS(ON)\_H}$	V_{BOOT} – V_{PHASE} = 5V	--	17	--	mΩ
	$R_{DS(ON)\_L}$		--	4.5	--	
Current Limit						
Current Limit	I_{LIM}	Valley current of low-side switch, R_{CS} = 165kΩ	--	16	--	A

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency and Min. Off Timer							
Switching Frequency		f_{SW}		425	500	575	kHz
Minimum On Time		t_{ON}		--	60	--	ns
Minimum Off Time		t_{OFF}		--	200	--	ns
Output Under-Voltage and Over-Voltage Protection							
OVP Trip Threshold		V_{OVP}	Measured at FB, with respect to reference voltage	112	117	122	%
OVP Propagation Delay		T_{OVPDLY}	FB force above OVP threshold	--	5	--	μs
UVP Trip Threshold		V_{UVP}	Measured at FB, with respect to reference voltage	60	70	80	%
UVP Propagation Delay		T_{UVPDLY}	FB force below UVP threshold	--	2	--	μs
Reference and Soft-Start							
FB Reference Voltage		V_{REF}		0.594	0.6	0.606	V
FB Input Bias Current			V_{FB} = 0.6V	–1	0.1	1	μA
Soft-Start Time		t_{SS}	From S5 high to 90% of V_{REF}	0.5	1	1.5	ms
Enable and UVLO							
S3, S5 Input Voltage	Logic-High			0.8	--	--	V
	Logic-Low			--	--	0.4	
VDD Input UVLO Threshold			Wake up	3.9	4.2	4.5	V
VDD Input UVLO Hysteresis			Shutdown	--	0.2	--	V
Power Good							
Trip Threshold (Raising)			Measured at FB, with respect to reference, no load	87	91	95	%
Trip Threshold (Hysteresis)				--	3	--	%
Fault Propagation Delay			Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage			I_{SINK} = 1mA	--	--	0.4	V
Leakage Current		I_{LEAK}	High state, forced to 5V	--	--	1	μA
Thermal Shutdown							
Thermal Shutdown		T_{SD}		--	165	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	25	--	°C
VTT LDO							
VTT Output Tolerance		V_{VTTTOL}	VDDQ = VLDOIN = 1.2V / 1.35V / 1.5V / 1.8V, |IVTT| = 0A	–20	--	20	mV
			VDDQ = VLDOIN = 1.2V / 1.35V / 1.5V / 1.8V, |IVTT| = 1A	–30	--	30	
			VDDQ = VLDOIN = 1.2V / 1.35V, |IVTT| = 1.2A	–40	--	40	
			VDDQ = VLDOIN = 1.5V / 1.8V, |IVTT| = 1.5A	–40	--	40	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VTT Source Current Limit	$I_{VTTOCLSRC}$	VTT = 0V	1.6	2.6	3.6	A
VTT Sink Current Limit	$I_{VTTOCLSNK}$	VTT = VDDQ	1.6	2.6	3.6	A
VTT Leakage Current	I_{VTTLK}	S5 = 5V, S3 = 0V, VTT = $\left(\frac{V_{VDDQ}}{2}\right)$	−10	--	10	μA
VTTSNS Leakage Current	$I_{VTTSNSLK}$	I_{SINK} = 1mA	−1	--	1	μA
VTT Discharge Resistance	R_{DSCHRG}	S5 = S3 = 0V	--	6	--	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a four-layer Richtek Evaluation Board.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

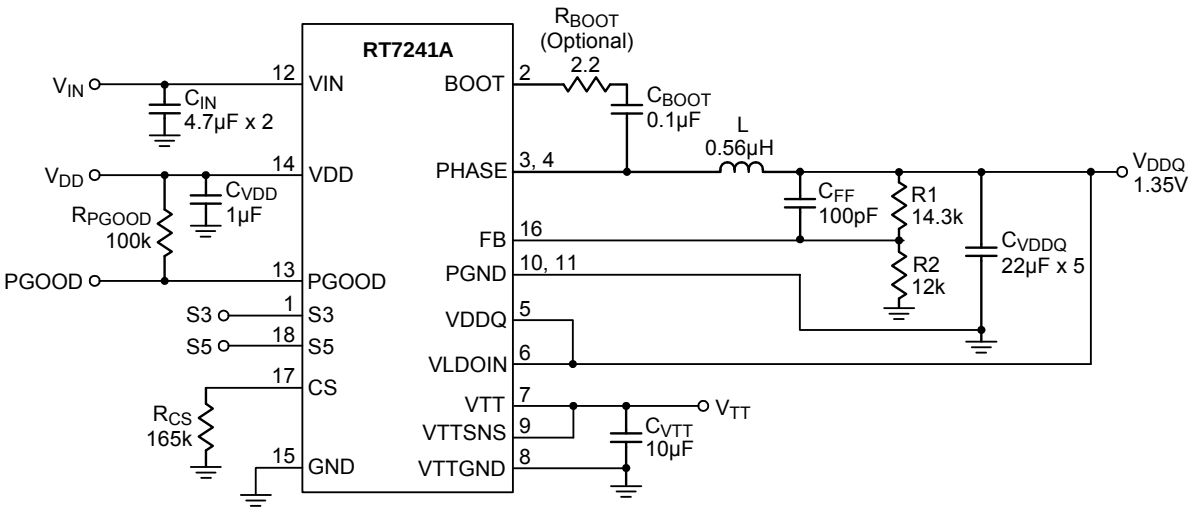


Figure 1. Typical Application Circuit for V_{OUT} = 1.35V

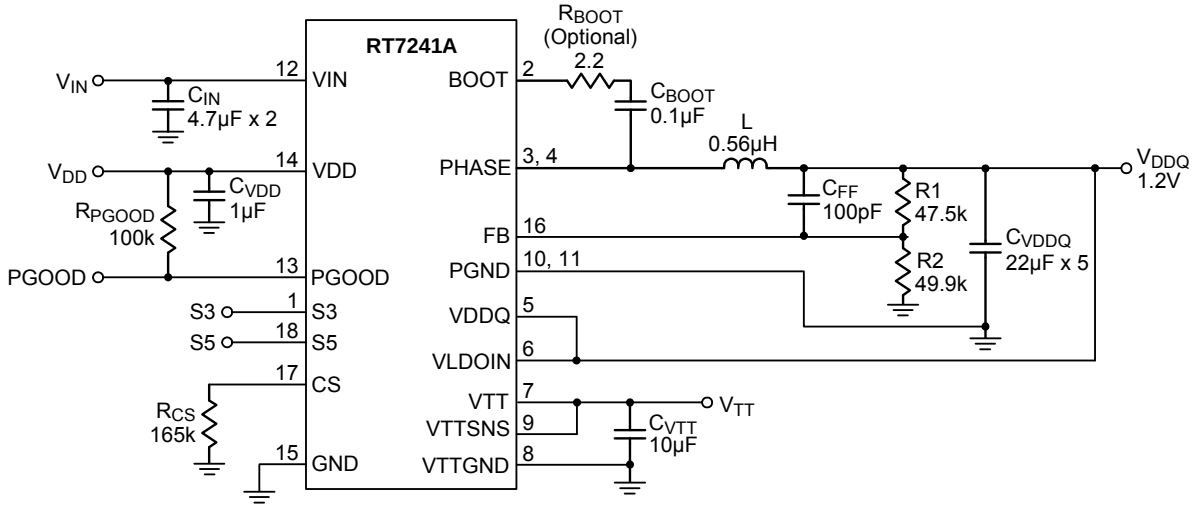
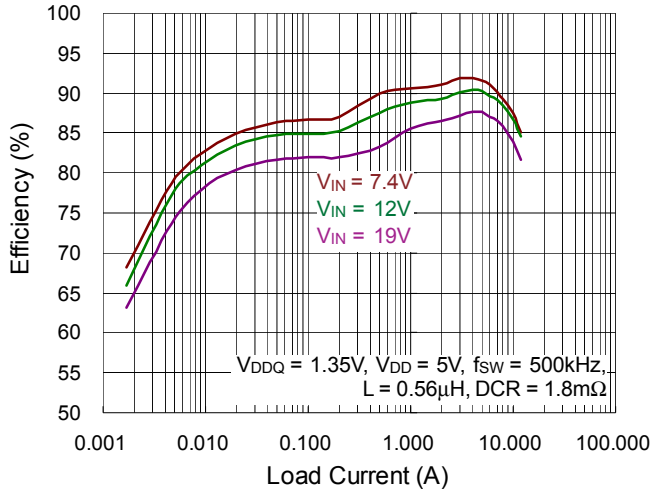


Figure 2. Typical Application Circuit for V_{OUT} = 1.2V

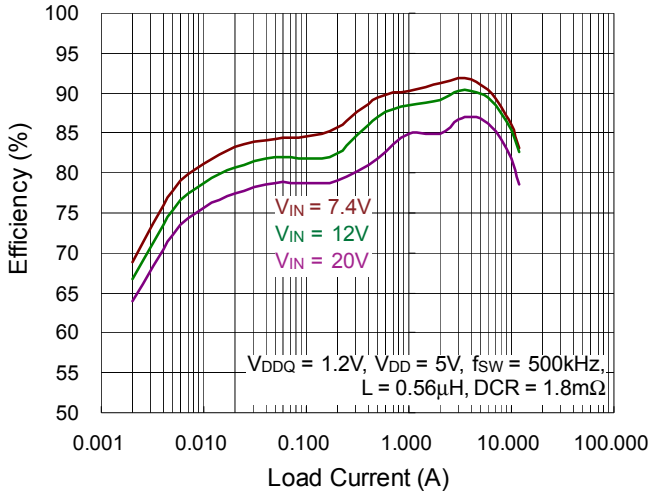
Typical Operating Characteristics

Performance waveforms are tested on the evaluation board of the Typical Application Circuit, V_{IN} = 12V, V_{OUT} = 1.35V, L = 0.56µH, T_J = 25°C, unless otherwise noted.

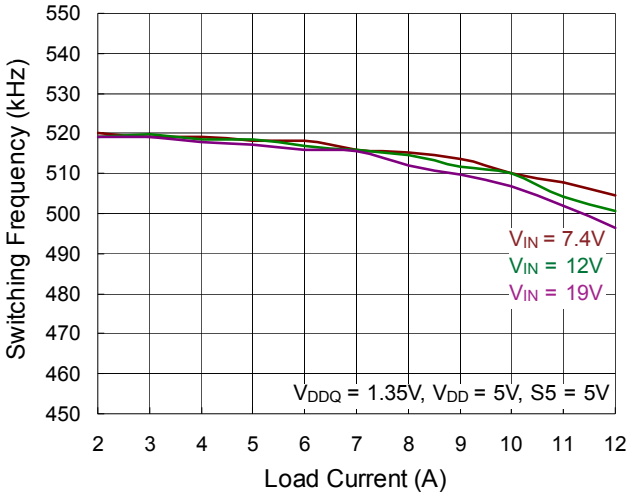
Efficiency vs. Load Current



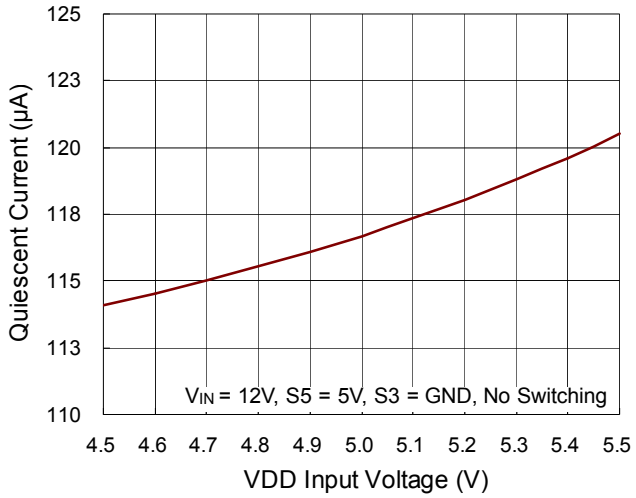
Efficiency vs. Load Current



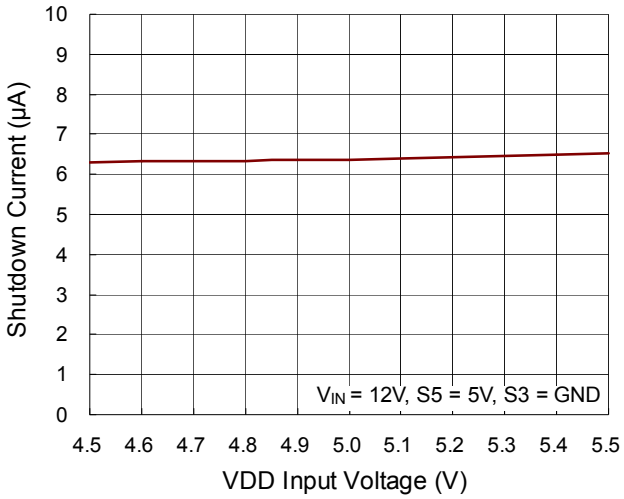
Switching Frequency vs. Load Current



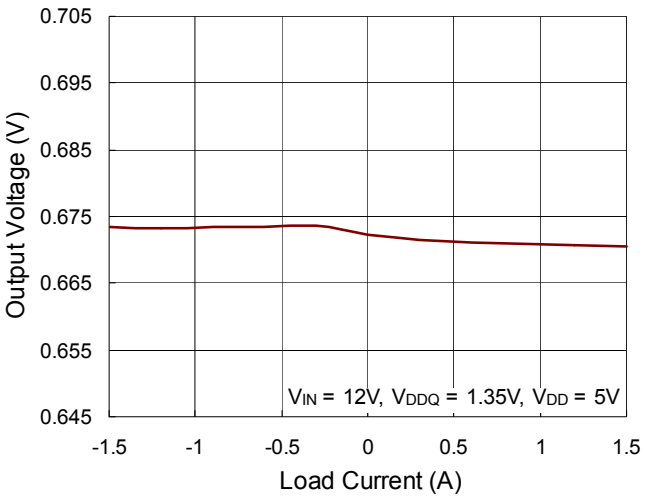
Quiescent Current vs. VDD Input Voltage



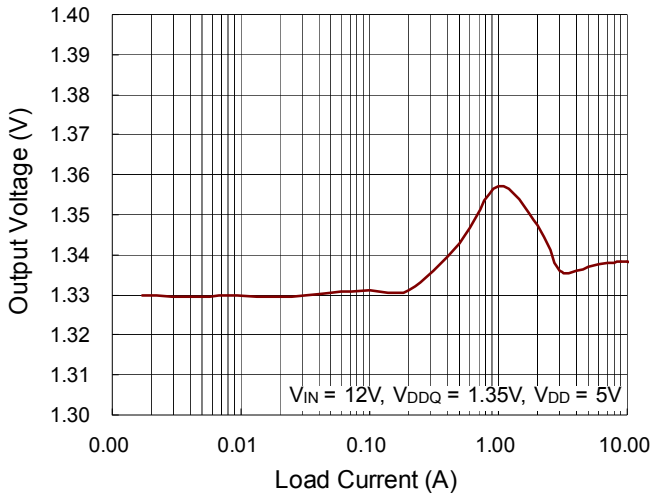
Shutdown Current vs. VDD Input Voltage



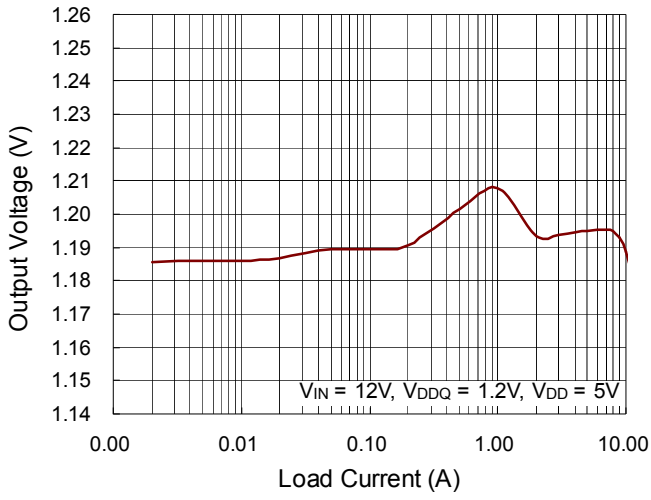
VTT Output Voltage vs. Load Current



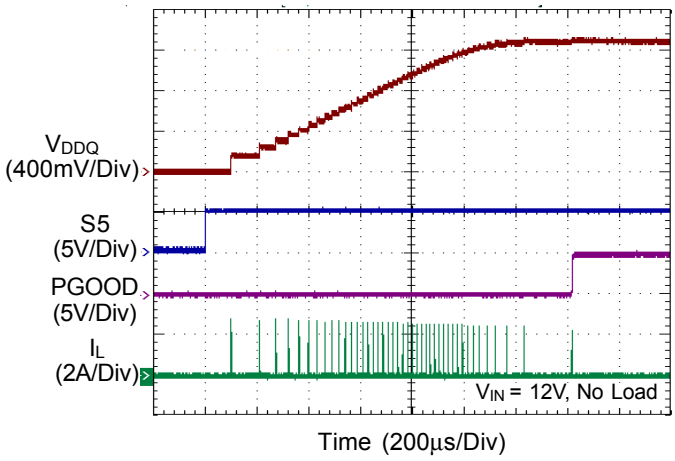
VDDQ Output Voltage vs. Load Current



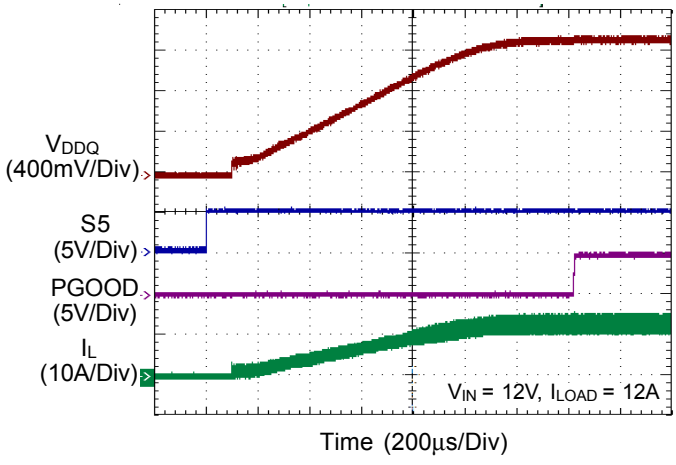
VDDQ Output Voltage vs. Load Current



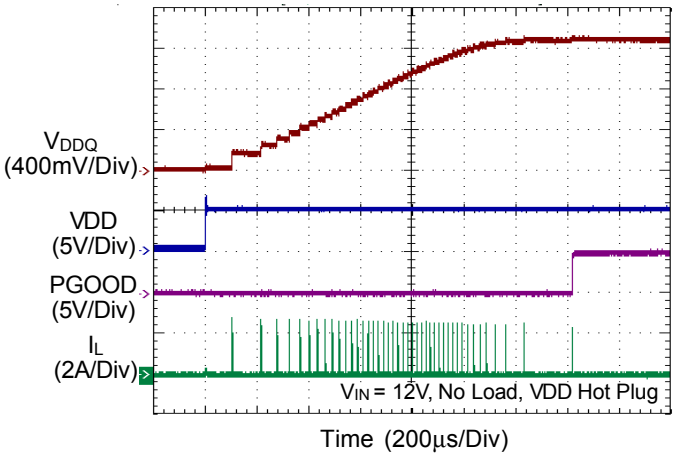
VDDQ Power On by S5



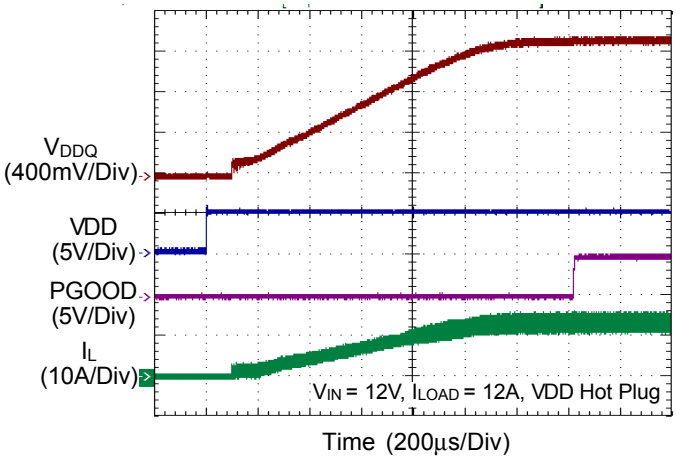
VDDQ Power On by S5



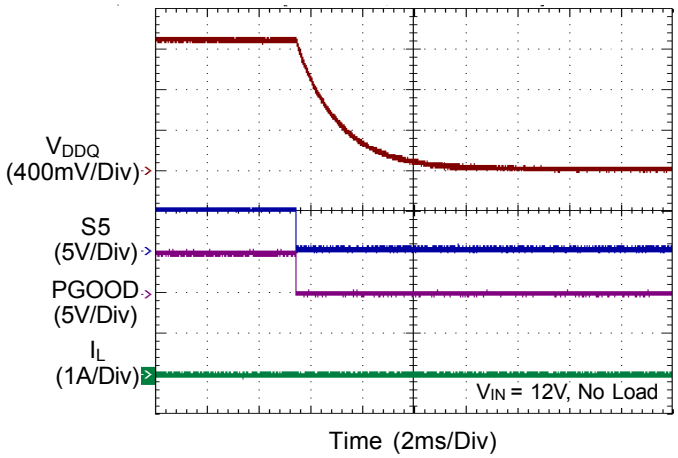
VDDQ Power On by VDD



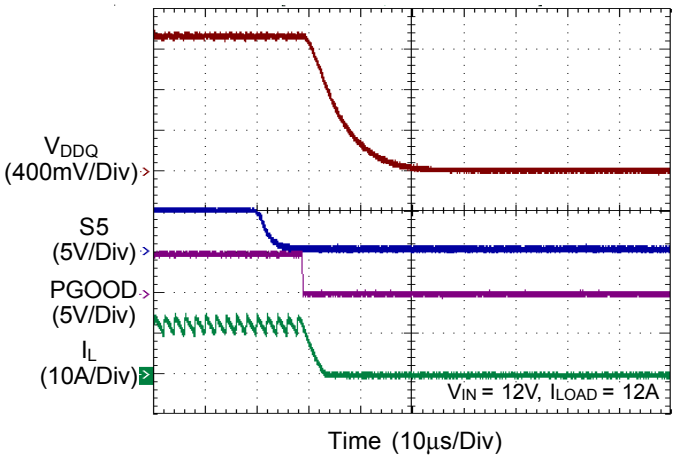
VDDQ Power On by VDD



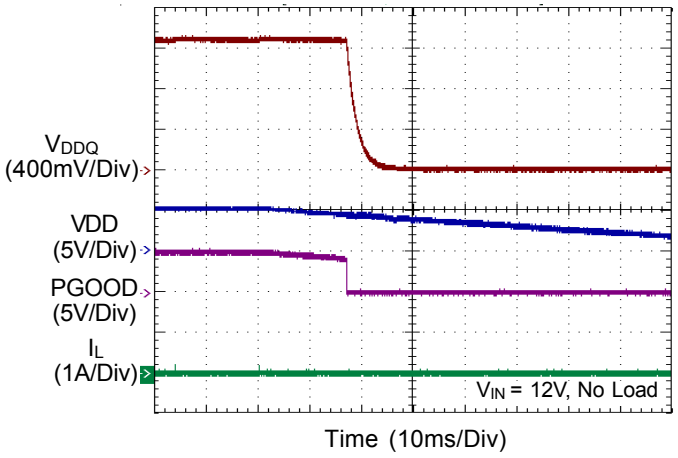
VDDQ Power Off by S5



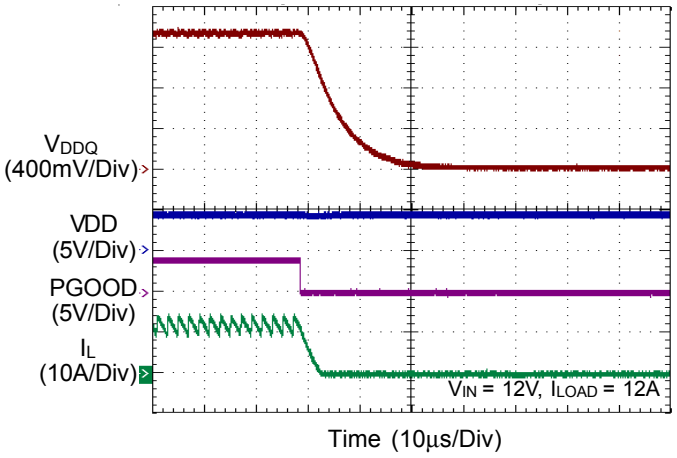
VDDQ Power Off by S5



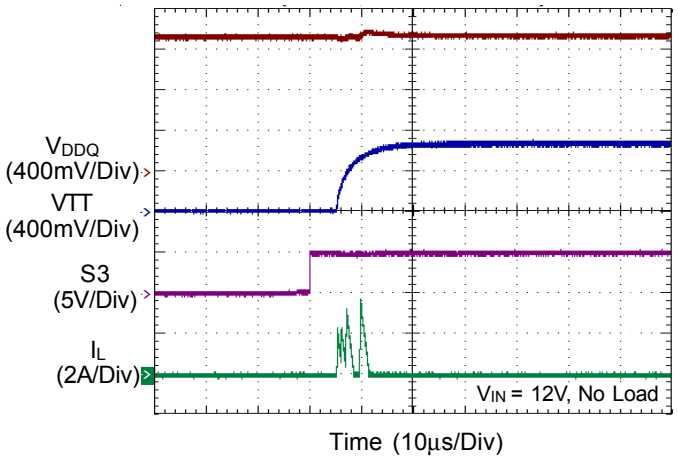
VDDQ Power Off by VDD



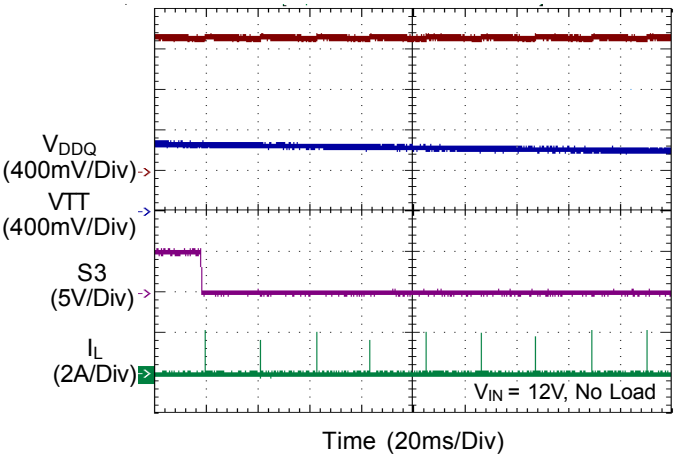
VDDQ Power Off by VDD



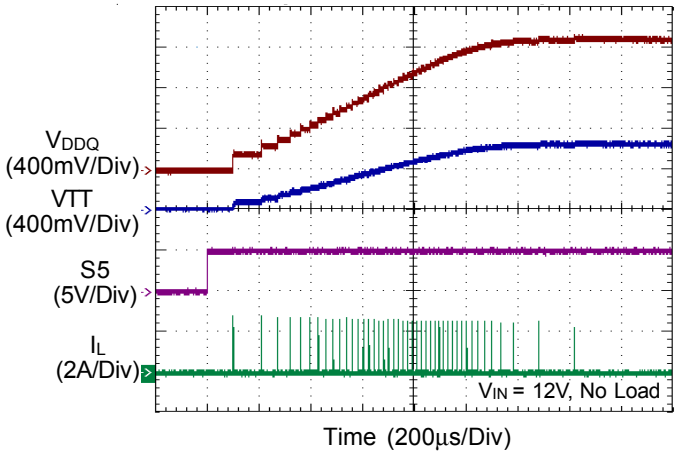
VTT Power On by S3



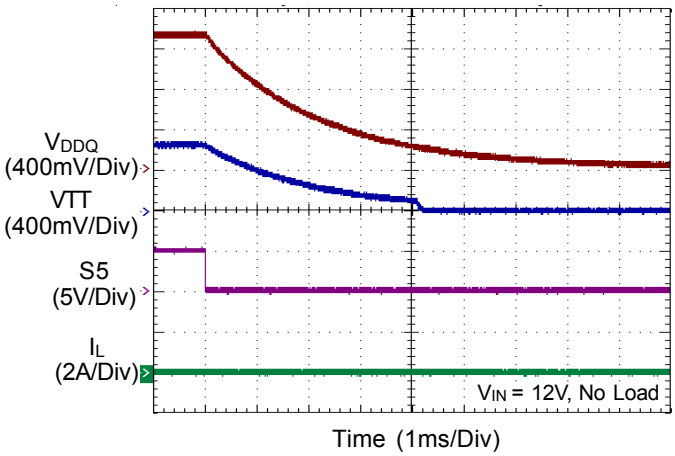
VTT Power Off by S3



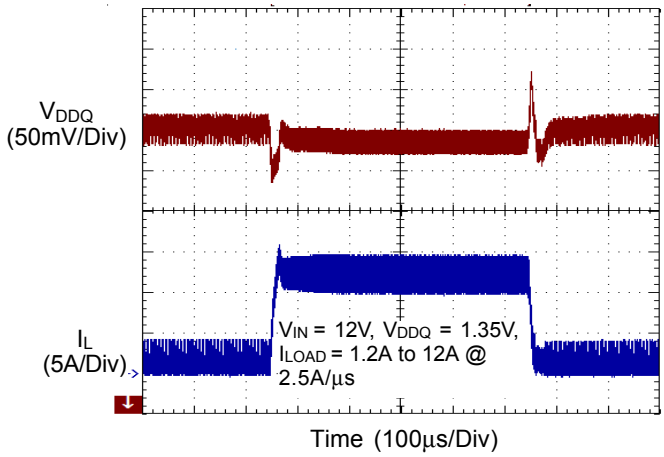
VTT Power On by S5



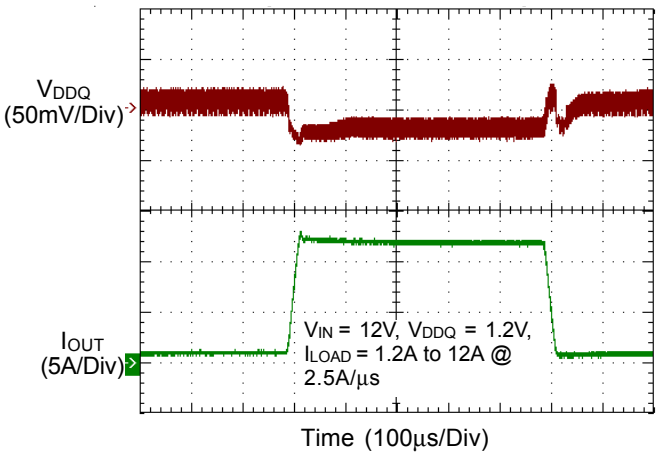
VTT Power Off by S5



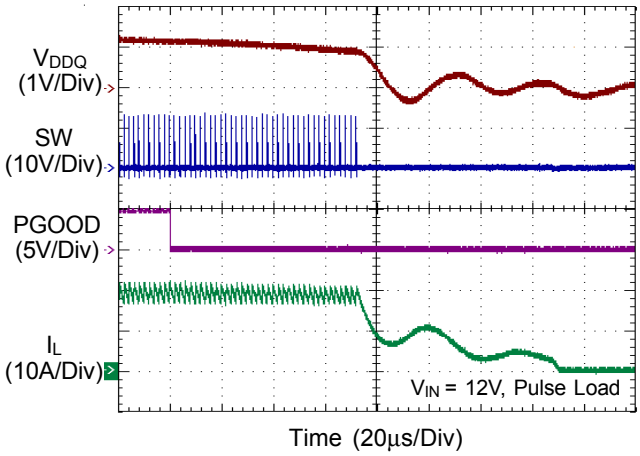
VDDQ Load Transient



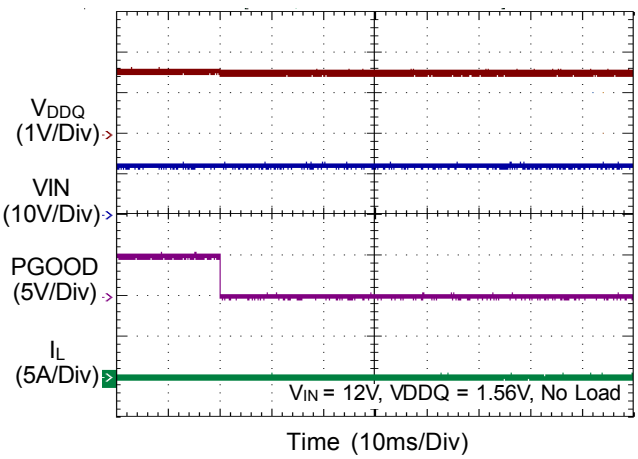
VDDQ Load Transient



UVP



OVP



Application Information

The RT7241A is high-performance 500kHz 12A step-down regulators with internal power switches and synchronous rectifiers. It features an Advanced Constant On-Time (ACOT™) control architecture that provides stable operation for ceramic output capacitors without complicated external compensation, among other benefits. The input voltage range is from 4.5V to 23V. The output voltage is adjustable from 0.6V to 1.5V.

The proprietary ACOT™ control scheme improves conventional constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

The 1.5A sink/source VTT LDO maintains fast transient response, only requiring 10μF of ceramic output capacitance. The RT7241A supports all of the sleep state controls, placing VTT at high-Z in S3 and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5.

ACOT™ Control Architecture

Making the on-time proportional to VOUT and inversely proportional to VIN is not sufficient to achieve good constant-frequency behavior for several reasons. First, voltage drops across the MOSFET switches and inductor cause the effective input voltage to be less than the measured input voltage and the effective output voltage to be greater than the measured output voltage as sensing input and output voltage from LX pin. When the load change, the switch voltage drops change causing a switching frequency variation with load current. Also, at light loads if the inductor current goes negative, the switch dead-time between the synchronous rectifier turn-off and the high-side switch turn-on allows the switching node to rise to the input voltage. This increases the effective on-time and causes the switching frequency to drop noticeably.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. ACOT™ uses this method, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

In order to achieve good stability with low-ESR ceramic capacitors, ACOT™ uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

ACOT™ One-shot Operation

The RT7241A control algorithm is simple to understand. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (200ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

Diode Emulation Mode

In diode emulation mode, the RT7241A automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free wheeling current becomes negative. As the load current is further decreased, it takes longer and longer

time to discharge the output capacitor to the level that requires the next "ON" cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation is shown in Figure 3. and can be calculated as follows :

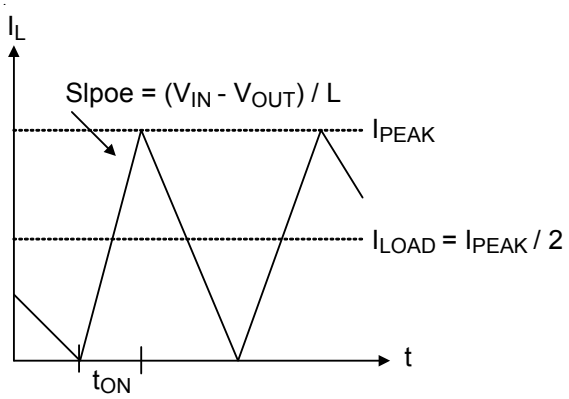


Figure 3. Boundary Condition of CCM/DEM

$$I_{LOAD} = \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

The switching waveforms may appear noisy and asynchronous when light load causes diode emulation operation. This is normal and results in high efficiency. Trade offs in DEM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

During discontinuous switching, the on-time is immediately increased to add "hysteresis" to discourage the IC from switching back to continuous switching unless the load increases substantially. The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for 500kHz switching and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

VTT Linear Regulator

The RT7241A integrates a high performance low dropout linear regulator that is capable of sourcing and sinking currents up to 1.5A. This VTT linear regulator employs ultimate fast response feedback loop so that small ceramic capacitors are enough for keeping track of VDDQ/2 within 40mV at all conditions, including fast load transient. To achieve tight regulation with minimum effect of wiring resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of the VTT output capacitor(s) as a separate trace from the VTT pin. For stable operation, total capacitance of the VTT output terminal can be equal to or greater than 10μF.

Current Limit Setting for VDDQ (CS)

The RT7241A current limit is adjustable by CS pin and it is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between source and drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the current limit, the on-time one-shot is inhibited until the inductor current ramps down below the current limit. Thus, only when the inductor current is well below the current limit, another on-time is permitted. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level (see next section) the IC will stop switching to avoid excessive heat.

The RT7241A also includes a negative current limit to protect the IC against sinking excessive current and possibly damaging the IC. If the voltage across the synchronous rectifier indicates the negative current is too high, the synchronous rectifier turns off until after the next high side on-time.

The RT7241A provides adjustable OCP setting via change the RCS to decide the current limit. The current limit can be derived by the following equation :

$I_{LIM} = 2.64 \times 10^6 / R_{CS}$

The default setting of R_{CS} is 165kΩ, which means current limit is 16A. The maximum current limit should be lower than 20A.

Output Over-voltage Protection and Under-voltage Protection for VDDQ

The RT7241A includes output over-voltage protection (OVP). If the output voltage rises above the regulation level, the high-side switch naturally remains off and the synchronous rectifier will periodically turn on until the inductor current reaches the negative current limit or under-voltage protection is triggered. If the output voltage exceeds the OVP trip threshold for longer than 5μs (typical), the IC's OVP is triggered. The RT7241A also includes output under-voltage protection (UVP). If the output voltage drops below the UVP trip threshold for longer than 2μs (typical) the IC's UVP is triggered. The RT7241A uses latch-off mode OVP and UVP. When the protection function is triggered, the IC will shut down. The IC stops switching and is latched off. To restart operation, toggle S5 or power the IC off by VDD and then on again.

Current Protection for VTT

The LDO has an internally fixed constant over current limit of 2.6A while operating at normal condition.

VDD Under Voltage Lockout (UVLO)

In addition to the enable function, the RT7241A features an UVLO function that monitors the VDD voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when VDD voltage drops below the UVLO-falling threshold.

The IC resumes switching when VDD voltage exceeds the UVLO-rising threshold.

Over Temperature Protection

The RT7241A includes an over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 165°C. Once the junction temperature cools down by approximately 25°C the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 165°C.

Output Management by S3, S5 Control

In DDR2/DDR3 memory applications, it is important to always keep VDDQ higher than VTT/VTTREF, even during start-up and shutdown. The RT7241A provides this management by simply connecting both S3 and S5 terminals to the sleep-mode signals such as SLP_S3 and SLP_S5 in notebook PC system. All VDDQ and VTT are turned on at S0 state (S3 = S5 = high). In S3 state (S3 = low, S5 = high), VDDQ is kept on while VTT is turned off and left at high impedance (high-Z) state. The VTT output is floated and does not sink or source current in this state. In S4/S5 states (S3 = S5 = low), all of the two outputs are disabled and discharged to ground. The code of each state represents the following: S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF. (See Table 1)

Table 1. S3 and S5 Truth Table

STATE	S3	S5	VDDQ	VTT
S0	Hi	Hi	On	On
S3	Lo	Hi	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)

VDDQ and VTT Tracking Discharge Mode

The RT7241A discharges VDDQ and VTT outputs when S5 is low or in the S4/S5 state. In tracking discharge mode, the RT7241A discharges outputs through the internal switch and VTT output tracks half of the VDDQ voltage during this discharge. Note that if VLDOIN is supplied by external voltage source, an input decoupling capacitor about 10μF is needed at the input.

The VTT LDO can handle up to 1.5A for both source/sink, and discharge with high-Z in S3.

Soft-Start

The RT7241A provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramping of internal reference voltage which is compared with FB signal. The typical soft-start duration is 1ms.

Power Good Output (PGOOD)

The power good output is an open drain output that requires a pull-up resistor. When the output voltage is 20% (typical) below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to 93% of its set voltage once more. During soft-start, PGOOD is actively held low and only allowed to be pulled high after soft-start is over and the output reaches 93% of its set voltage. There is a 2.5μs delay built into PGOOD circuitry to prevent false transition.

External Bootstrap Capacitor (C_{BOOT})

Connect a 0.1μF low ESR ceramic capacitor between BOOT pin and LX pin. This bootstrap capacitor provides the gate driver supply voltage for the high side N-channel MOSFET switch.

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since VSW rises rapidly. During switch turn-off, SW is discharged relatively slowly by the inductor current during the dead-time between high-side and low-side switch on-times. In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<10Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and VSW's rise.

Setting the Output Voltage

The output voltage of RT7241A is adjustable and with valley control. There is an easy way to determine the output voltage only by two resistors, R1 and R2. As the feedback circuit shown in Figure 4, the relation of V_{OUT} and V_{REF} can be derived as V_{OUT} = (1+R1/R2) x V_{REF} readily. Generally, the stability is a serious issue for converter. In order to achieve better performance on stability and transient, a feed-forward capacitor, C_{FF}, is added to increase the noise margin and transient response of loop control. However, there is a tradeoff of adding a feed-forward capacitor. An additional dc offset will be generated on output voltage due to the amplified feedback ripple by feed-forward compensator. This is not always the case that every C_{FF} makes the same value of dc offset, it is based on different pole and zero placement generated by R1, R2 and C_{FF}. For simplicity, a symbol named $V_{dc,offset}$ is supposed to be the value of dc offset. This value may influence the performance (e.g. regulation or peak value of V_{OUT}) of converter slightly, the suggested C_{FF} is to select a pair of pole and zero to provide the maximum phase lead at switching frequency.

$$V_{OUT,valley} = \left(1 + \frac{R1}{R2}\right) \times V_{REF} + V_{dc,offset}$$

$V_{OUT,valley}$ is the valley of output voltage, and $V_{dc,offset}$ is used for describing the additional dc offset on V_{OUT}, the value is related to the output voltage ripple and C_{FF}.

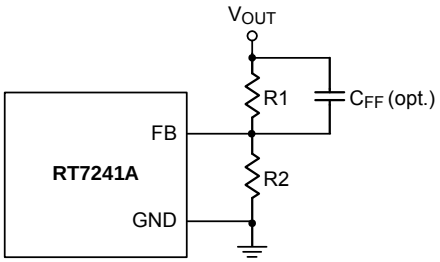


Figure 4. The Equivalent Circuit of Feedback Loop

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses some type of ferrite core is usually best and a shielded core type, although possibly larger or more expensive, will probably give fewer EMI and other noise problems.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 20μF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability. Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5times greater than the maximum input voltage is a conservatively safe design. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[(1 - \frac{V_{OUT}}{V_{IN}}) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right]}$$

The next step is to select a proper capacitor for RMS current rating. One good design uses more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{IN}}{C_{IN} \times f_{SW} \times V_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The typical operating circuit is recommended to use two 10μF and low ESR ceramic capacitors on the input.

Output Capacitor Selection

The RT7241A is optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's 500kHz switching frequency. But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF(MIN)}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Most applications never experience instantaneous full load steps and the RT7241A's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that over-voltage protection and under-voltage protection will not be triggered.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-18L 3x4 (FC) package, the thermal resistance, θ_{JA}, is 33°C/W on a four-layer Richtek evaluation board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (33°C/W) = 3.03W for a UQFN-18L 3x4 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

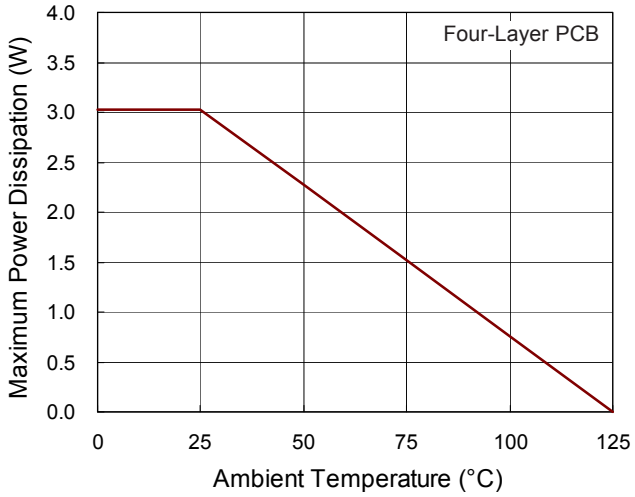


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout. Certain points must be considered before starting a layout using the RT7241A.

- Make the traces of the main current paths as short and wide as possible. Put the input capacitor as close as possible to the device pins (VIN and GND).
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Phase node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the phase node to prevent stray as possible.
- VLDOIN should be connected to VDDQ output with short and wide trace. If different power source is used for VLDOIN, an input bypass capacitor should be placed as close as possible to the pin with short and wide trace.
- The output capacitor for VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- It is strongly recommended to connect VTTSNS to the positive node of VTT output capacitor(s) as a separate trace from the high current power line to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. It is also recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the output capacitor(s).
- The GND pin should be connected to a strong ground plane for heat sinking and noise protection.
- Avoid using vias in the power path connections that have switched currents (from CIN to GND and CIN to VIN) and the switching node (Phase).
- An example of PCB layout guide is shown in Figure 6 for reference.

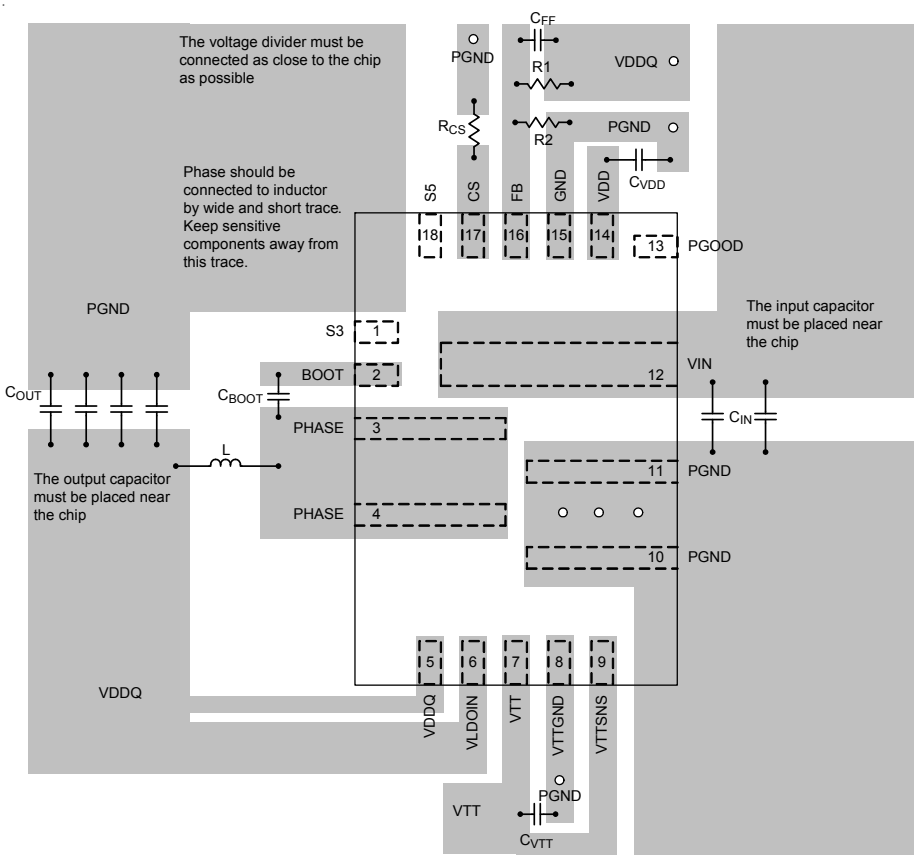
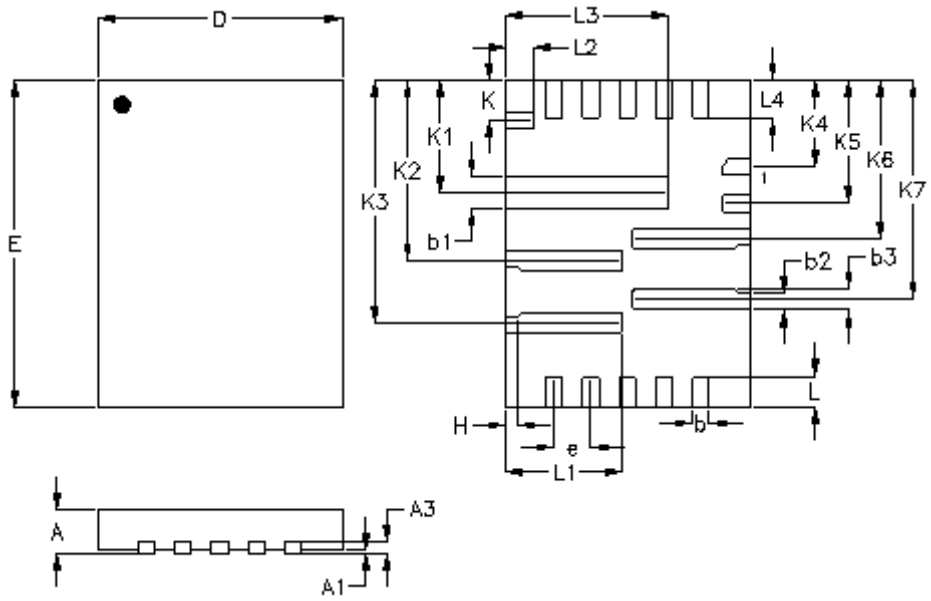


Figure 6. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.175	0.004	0.007
D	2.900	3.100	0.114	0.122
E	3.900	4.100	0.154	0.161
b	0.150	0.250	0.006	0.010
b1	0.350	0.450	0.014	0.018
b2	0.150	0.250	0.006	0.010
b3	0.200	0.300	0.008	0.012
L	0.325	0.425	0.013	0.017
L1	1.390	1.490	0.055	0.059
L2	0.300	0.400	0.012	0.016
L3	1.950	2.050	0.077	0.081
L4	0.420	0.520	0.017	0.020
e	0.450		0.018	
K	0.490		0.019	
K1	1.370		0.054	
K2	2.215		0.087	
K3	2.965		0.117	
K4	1.060		0.042	
K5	1.510		0.059	
K6	1.935		0.076	
K7	2.685		0.106	
H	0.150		0.006	

U-Type 18L QFN 3x4 (FC) Package

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