RICHTEK®

RT6236A/B

# 6A, 18V, 650kHz, ACOT® Synchronous Step-Down Converter

## 1 General Description

The RT6236A/B is a high-performance, synchronous step-down converter that can deliver up to 6A output current, with an input supply voltage range from 4.5V to 18V. The device integrates low $R_{DS(ON)}$ power MOSFETs and an integrated diode for the bootstrap circuit, offering a very compact solution. The RT6236A/B utilizes the Advanced Constant On-Time (ACOT®) control architecture that provides ultrafast transient response and reduces the external component count. In steady state, the ACOT® operates at nearly constant switching frequency across line, load, and output voltage variations, simplifying the EMI filter design. The device offers various functions for enhancing design flexibility, including an independent enable control input pin and a power-good indicator for straightforward sequencing control. To manage inrush current during startup, the device features a programmable soft-start function, adjustable via an external capacitor connected to the SS pin. Comprehensive protection features are integrated, including the device including the cycle-by-cycle current limit, OVP, UVP, input UVLO, and OTP. The RT6236A/B is available in a thermally enhanced UQFN-13JL 2x3 (FC) package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

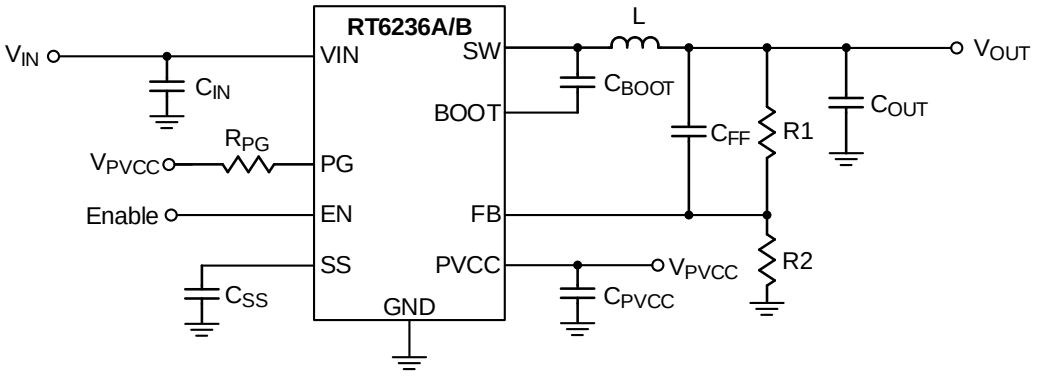
## 2 Features

- **4.5V to 18V Input Voltage Range**
- **Adjustable Output Voltage from 0.7V to 8V**
- **6A Output Current**
- **Steady 650kHz Switching Frequency**
- **Advanced Constant On-Time (ACOT®) Control**
- **Fast Transient Response**
- **Optimized for All Ceramic Capacitors**
- **51mΩ Internal High-Side N-MOSFET and 18mΩ Internal Low-Side N-MOSFET**
- **Up to 95% Efficiency**
- **Externally Adjustable, Pre-Biased Compatible Soft-Start**
- **Power-Good Output**
- **Cycle-by-Cycle Current Limit**
- **Input Undervoltage-Lockout**
- **Output Overvoltage and Undervoltage Protections**
- **Over-Temperature Protection**

## 3 Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

## 4 Simplified Application Circuit



## 5 Ordering Information

RT6236A/B□□□

**Package Type**(1)
QUF: UQFN-13JL 2x3 (U-Type) (FC)

**Lead Plating System**
G: Richtek Green Policy Compliant(2)

H: Hiccup Mode UVP
L: Latched OVP & UVP

A: PSM
B: PWM

**Note 1**.

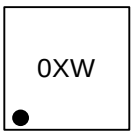
- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

## 6 Marking Information

RT6236AHGQUF


0Z : Product Code
W : Date Code

RT6236BHGQUF

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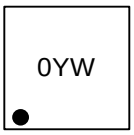
RT6236ALGQUF

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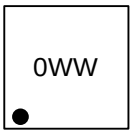
RT6236BLGQUF




0W : Product Code
W : Date Code

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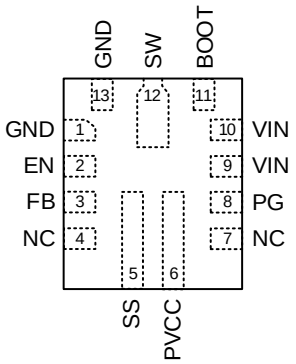
## 7 Pin Configuration

(TOP VIEW)

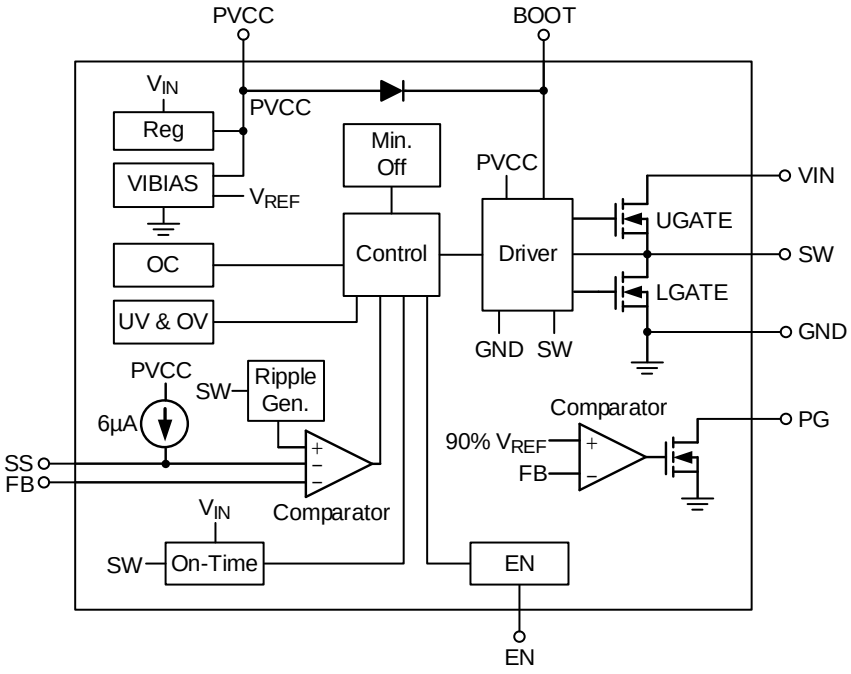



UQFN-13JL 2x3 (FC)

## 8 Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1, 13 | GND | Ground return for the power stage. Use wide PCB traces for the connections. |
| 2 | EN | Enable control input. Enable or disable with an external signal, or adjust the input undervoltage lockout with a resistor divider. |
| 3 | FB | Feedback input. The pin is used to set the output voltage of the converter via a resistor divider. Suggest to place the FB resistor divider as close to the FB pin as possible. |
| 4, 7 | NC | No internal connection. |
| 5 | SS | Soft-start time control pin. Connect a capacitor from the SS pin to GND to set the soft-start time. Do not leave SS unconnected. |
| 6 | PVCC | LDO output for internal analog power. Connect a 1μF capacitor as close to the PVCC pin as possible. It is not recommended to connect PVCC to supply other rails. |
| 8 | PG | Open-drain, power-good indication output. It is pulled low when the feedback voltage is out of the PG threshold, when the IC shuts down from OTP, or when EN is low. Additionally, it remains low until the soft-start sequence is complete. It is recommended to use a 10kΩ to 100kΩ resistor to pull up to the PVCC pin. |
| 9, 10 | VIN | Input voltage. Supports a 4.5V to 18V input voltage range. Suggest to place input capacitors as close to the VIN pins to GND as possible. |
| 11 | BOOT | Bootstrap, supply for the high-side gate driver. Connect a 0.1μF ceramic capacitor between the BOOT and SW pins. |
| 12 | SW | Switch node. Connect to the power inductor. It provides the return path for the internal high-side MOSFET gate driver bootstrap capacitor. Connect a capacitor from BOOT to this pin. |

## 9 Functional Block Diagram



## 10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VIN ---------- –0.3V to 21V
- Switch Voltage, SW ---------- –0.3V to ($V_{IN}$ + 0.3V)
- Switch Voltage, <100ns ---------- –9V to ($V_{IN}$ + 0.3V)
- BOOT Voltage ---------- –0.3V to 27.3V
- BOOT to SW, <100ns ---------- –3V to 9V
- EN to GND ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C

  UQFN-13JL 2x3 (FC) ---------- 1.54W
- Package Thermal Resistance (Note 3)

  UQFN-13JL 2x3 (FC), $\theta_{JA}$ ---------- 64.8°C/W

  UQFN-13JL 2x3 (FC), $\theta_{JC}$ ---------- 7.3°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

**Note 2**. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 3.** $\theta_{JA}$ is measured at $T_A$ = 25°C on a highly thermal conductive 4-Layer test board. $\theta_{JC}$ is measured at the top of the package.

**Note 4.** Devices are ESD sensitive. Handling precautions are recommended.

## 11 Recommended Operating Conditions

(Note 5)

- Supply Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

**Note 5.** The device is not guaranteed to function outside its operating conditions.

## 12 Electrical Characteristics

($V_{IN}$ = 12V, $T_A$ = –40°C to 85°C, unless otherwise specified.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage** | | | | | | |
| VIN Supply Input Voltage | $V_{IN}$ | | 4.5 | -- | 18 | V |
| Undervoltage-Lockout Threshold | $V_{UVLO}$ | | 4 | 4.2 | 4.4 | V |
| Undervoltage-Lockout Threshold Hysteresis | $V_{UVLO\_HYS}$ | | -- | 0.5 | -- | |
| Shutdown Current | $I_{SHDN}$ | $V_{EN}$ = 0V | -- | 1.5 | 10 | μA |
| Quiescent Current | $I_{Q\_NSW}$ | $V_{EN}$ = 2V, $V_{FB}$ = 0.7V | -- | 0.8 | 1.2 | mA |
| **Enable Voltage** | | | | | | |
| EN Input Voltage Rising Threshold | $V_{EN\_R}$ | $V_{EN}$ rising | 1.1 | 1.2 | 1.3 | V |
| Enable Voltage Hysteresis | $V_{EN\_HYS}$ | | -- | 200 | -- | mV |
| **Feedback Voltage** | | | | | | |
| Feedback Voltage Threshold | $V_{FB}$ | 4.5V ≤ $V_{IN}$ ≤ 18V | 0.693 | 0.7 | 0.707 | V |
| Feedback Input Current | $I_{FB}$ | $V_{FB}$ = 0.71V | –0.1 | -- | 0.1 | μA |
| **PVCC Output** | | | | | | |
| PVCC Output Voltage | $V_{PVCC}$ | 6V ≤ $V_{IN}$ ≤ 18V, 0 < $I_{PVCC}$ < 5mA | -- | 5 | -- | V |
| PVCC Line Regulation | $V_{LINE\_REG}$ | 6V ≤ $V_{IN}$ ≤ 18V, $I_{PVCC}$ = 5mA | -- | -- | 20 | mV |
| PVCC Load Regulation | $V_{LOAD\_REG}$ | 0 < $I_{PVCC}$ < 20mA | -- | -- | 100 | |
| PVCC Output Current | $I_{PVCC}$ | $V_{IN}$ = 6V, $V_{PVCC}$ = 4V, $T_A$ = 25°C | -- | 150 | -- | mA |
| **Internal MOSFET** | | | | | | |
| High-Side On-Resistance | $R_{DSON\_H}$ | $V_{BOOT}$ – $V_{SW}$ = 5V | -- | 51 | -- | mΩ |
| Low-Side On-Resistance | $R_{DSON\_L}$ | | -- | 18 | -- | |
| **Current Limit** | | | | | | |
| Low-Side Switch Current Limit | $I_{LIM\_L}$ | | 6.6 | 7.7 | 8.9 | A |
| **Over-Temperature Protection** | | | | | | |
| Over-Temperature Protection Threshold | $T_{OTP}$ | | -- | 150 | -- | °C |
| Over-Temperature Protection Hysteresis | $T_{OTP\_HYS}$ | | -- | 20 | -- | |
| **On-Time Timer Control** | | | | | | |
| On-Time | $t_{ON}$ | $V_{OUT}$ = 1.2V | -- | 153 | -- | ns |
| Minimum On-Time | $t_{ON\_MIN}$ | | -- | 60 | -- | |
| Minimum Off-Time | $t_{OFF\_MIN}$ | | -- | 230 | -- | |
| **Soft-Start** | | | | | | |
| Internal Charge Current | $I_{SS}$ | $V_{SS}$ = 0V | 5 | 6 | 7 | μA |
| **Power Good** | | | | | | |
| PG Rising Threshold | $V_{PG\_LH1}$ | $V_{FB}$ rising (Good) | 85 | 90 | 95 | %$V_{FB}$ |
| | $V_{PG\_HL1}$ | $V_{FB}$ rising (Fault) | -- | 120 | -- | |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PG Falling Threshold | $V_{PG\_LH2}$ | $V_{FB}$ falling (Good) | -- | 112 | -- | %$V_{FB}$ |
| | $V_{PG\_HL2}$ | $V_{FB}$ falling (Fault) | -- | 80 | -- | |
| PG Sink Current | $I_{SK\_PG}$ | PG = 0.1V | 10 | 20 | -- | mA |
| **Output Undervoltage and Overvoltage Protections** | | | | | | |
| OVP Threshold | $V_{OVP}$ | OVP detect | 115 | 120 | 125 | %$V_{FB}$ |
| OVP Propagation Delay | $T_{DLY\_OVP}$ | | -- | 10 | -- | μs |
| UVP Threshold | $V_{UVP}$ | UVP detect | 55 | 60 | 65 | %$V_{FB}$ |
| | $V_{UVP\_HYS}$ | Hysteresis | -- | 10 | -- | |
| UVP Propagation Delay | $t_{DLY\_UVP}$ | | -- | 250 | -- | μs |
| UVP Enable Delay | $t_{HICCUP}$ | Relative to soft-start time | -- | $t_{SS}$ x 1.7 | -- | ms |

## 13 Typical Application Circuit

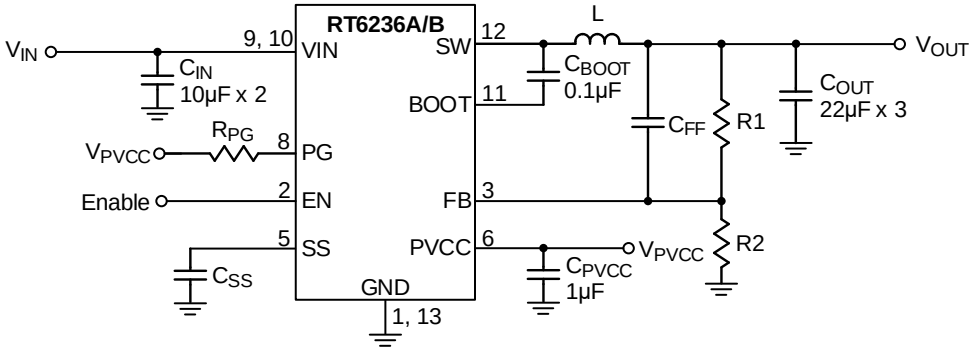
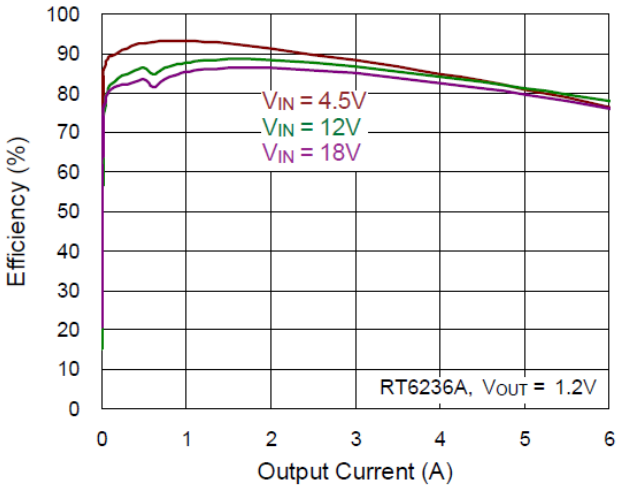



**Table 1. Suggested Component Values ($V_{IN}$ = 12V)**

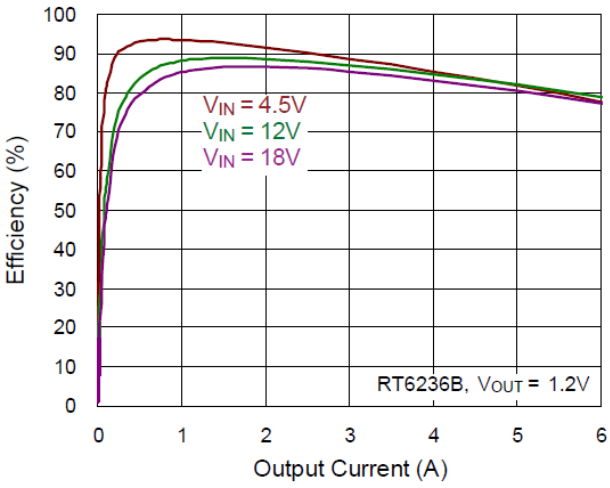
| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) | L (µH) | $C_{OUT}$ (µF) | $C_{FF}$ (pF) |
|---|---|---|---|---|---|
| 1 | 10.2 | 24 | 1 | 66 | -- |
| 1.2 | 17 | 24 | 1 | 66 | -- |
| 1.8 | 37.4 | 24 | 2 | 66 | -- |
| 2.5 | 61.9 | 24 | 2 | 66 | 22 |
| 5 | 147 | 24 | 3.3 | 66 | 22 |

## 14 Typical Operating Characteristics

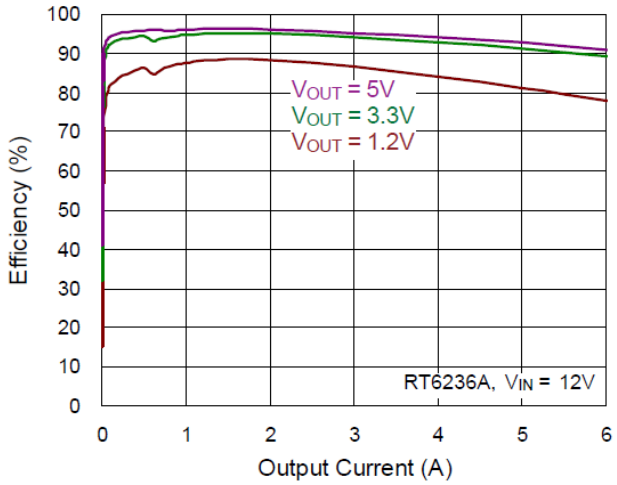
Efficiency vs. Output Current



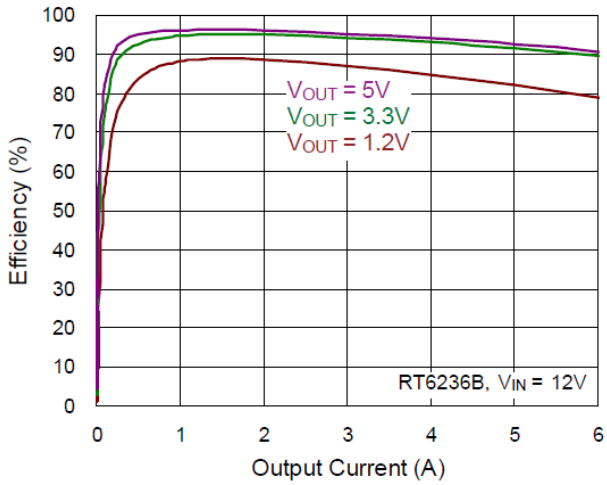

Efficiency vs. Output Current



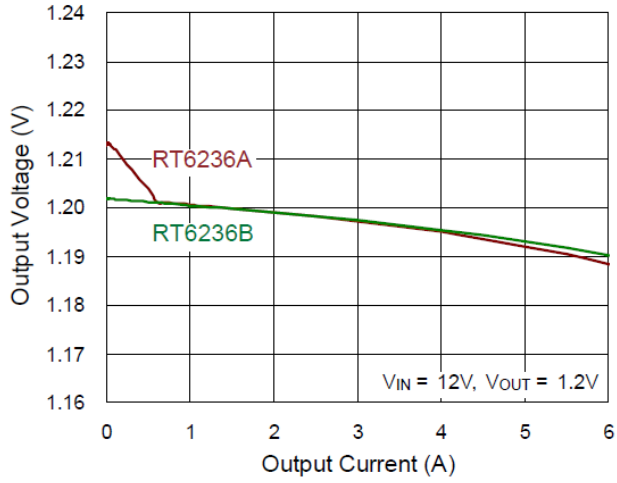

Efficiency vs. Output Current



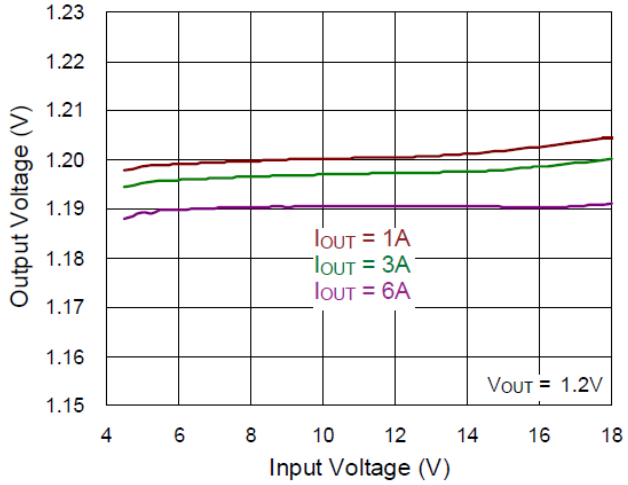

Efficiency vs. Output Current



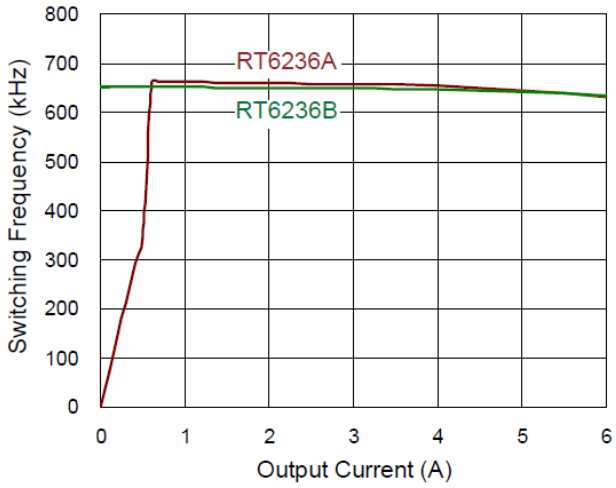

Output Voltage vs. Output Current



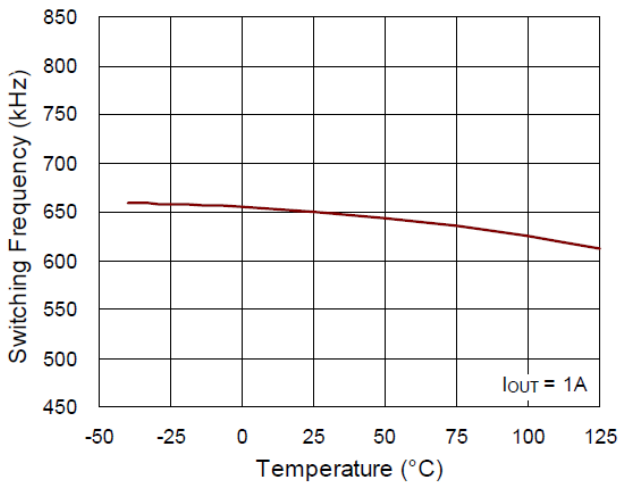

Output Voltage vs. Input Voltage



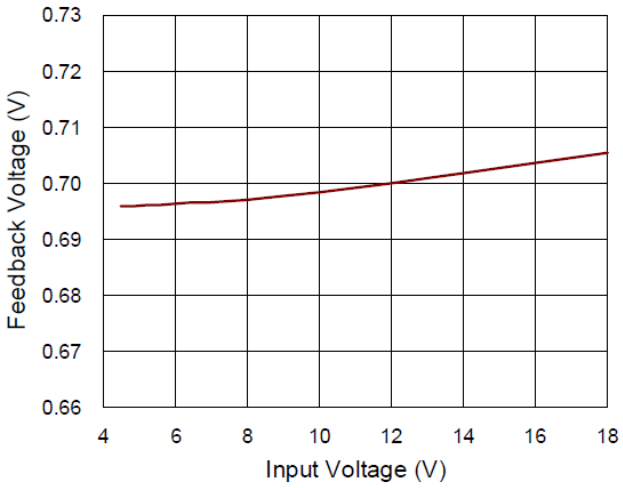
**Switching Frequency vs. Output Current**



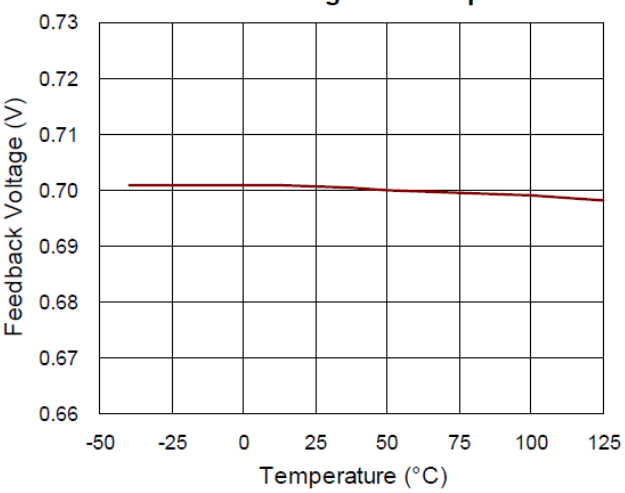

**Switching Frequency vs. Temperature**



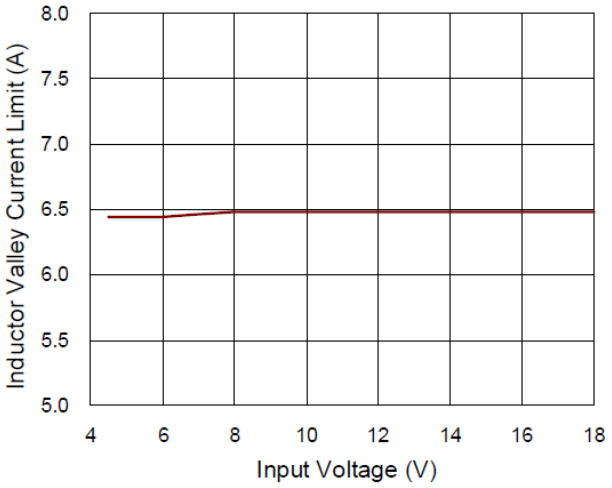

**Feedback Voltage vs. Input Voltage**



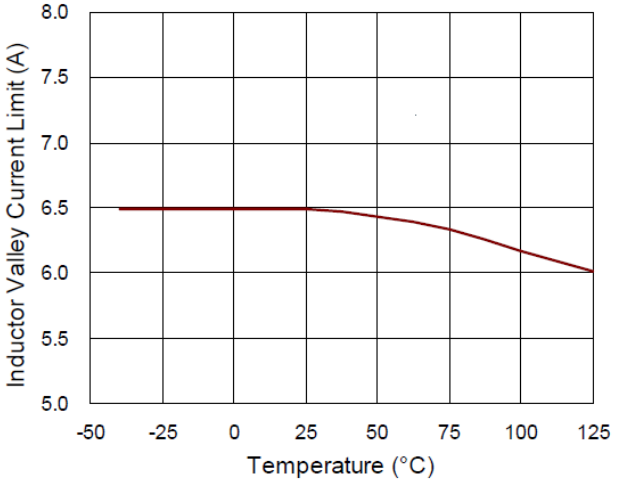

**Feedback Voltage vs. Temperature**



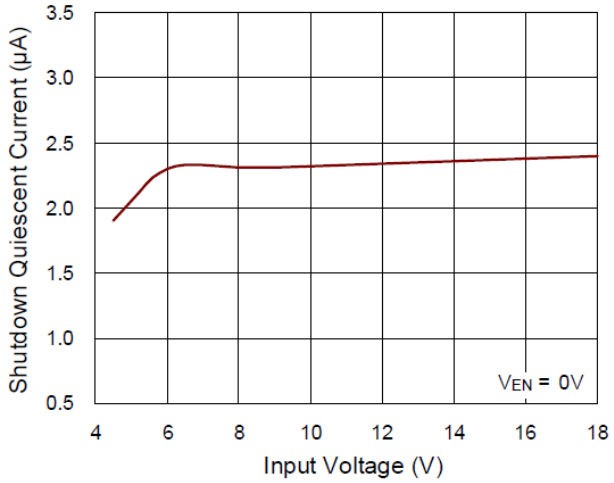

**Inductor Valley Current Limit vs. Input Voltage**



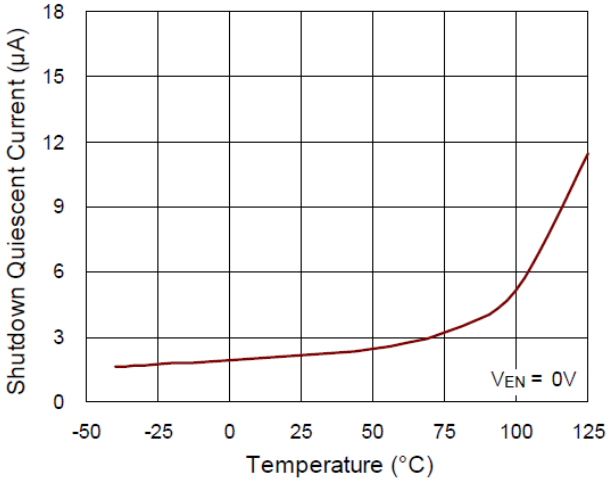

**Inductor Valley Current Limit vs. Temperature**



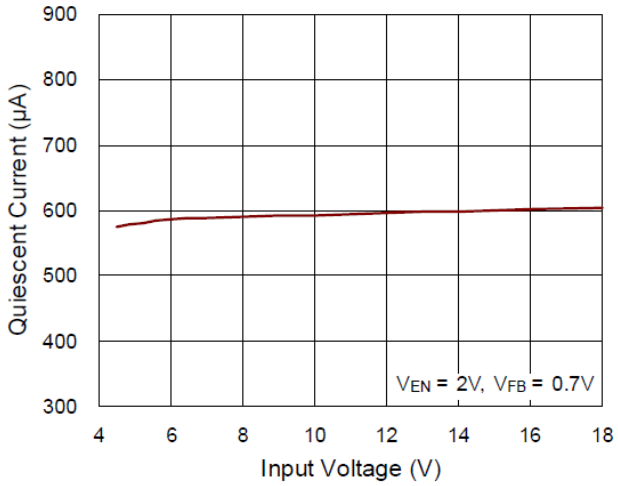
### Shutdown Quiescent Current vs. Input Voltage



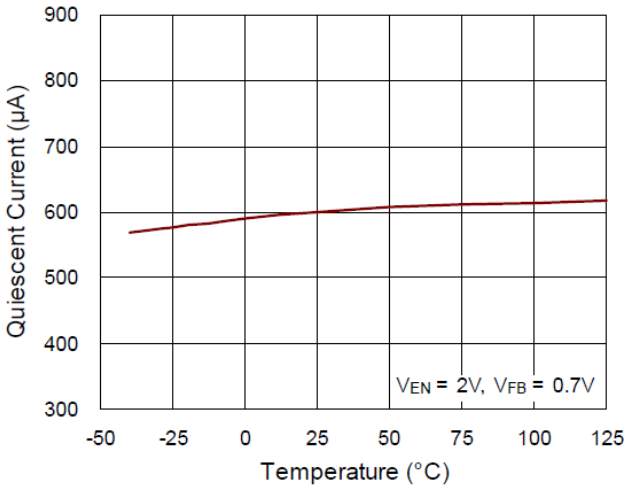

### Shutdown Quiescent Current vs. Temperature



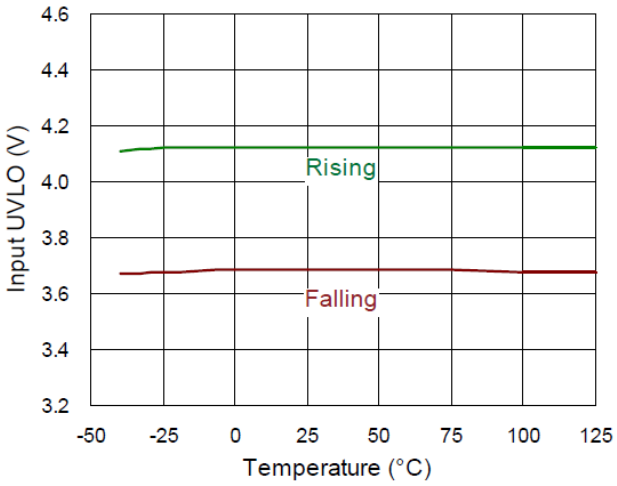

### Quiescent Current vs. Input Voltage



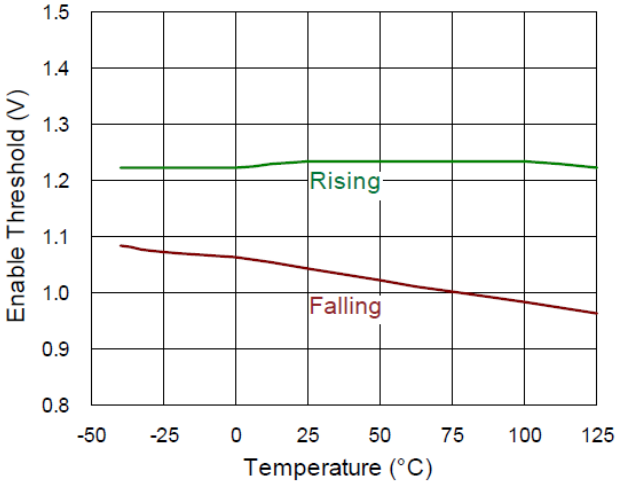

### Quiescent Current vs. Temperature



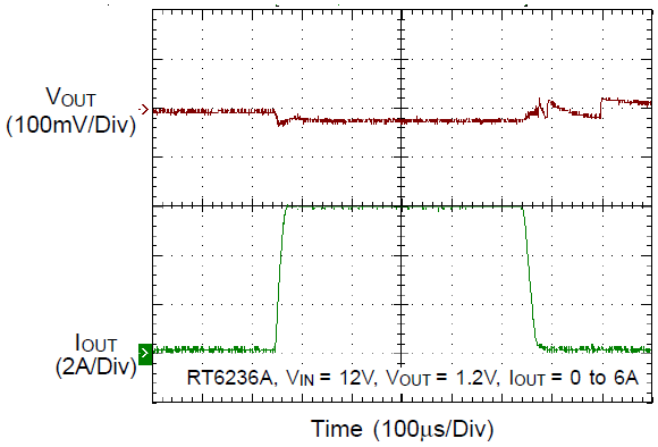

### Input UVLO vs. Temperature



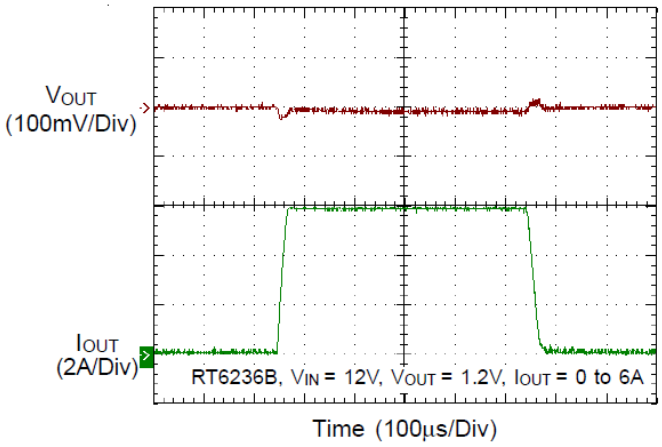

### Enable Threshold vs. Temperature



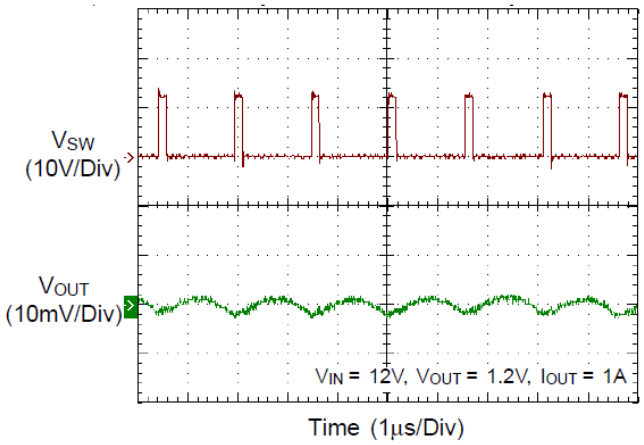
### Load Transient Response



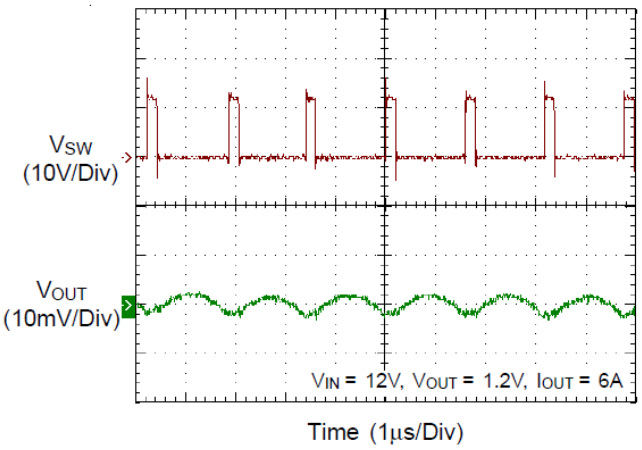

### Load Transient Response



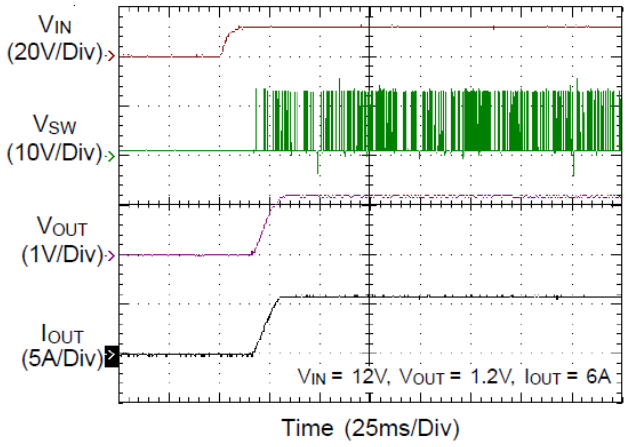

### Voltage Ripple



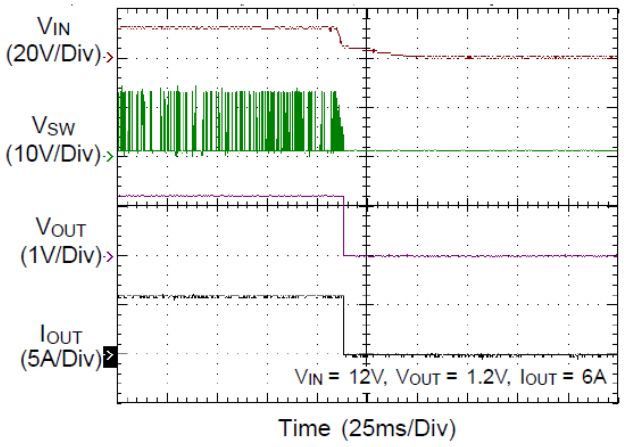

### Voltage Ripple



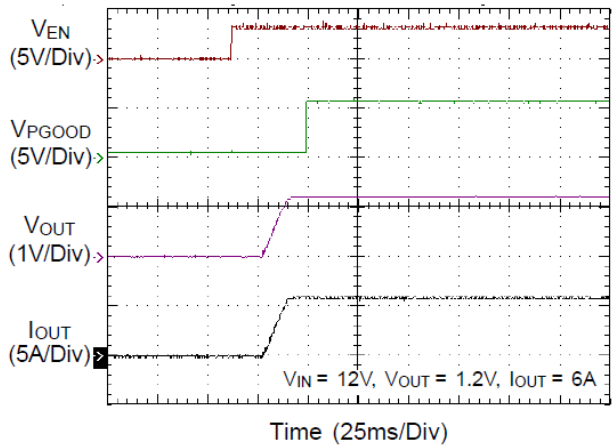

### Power On from Input Voltage



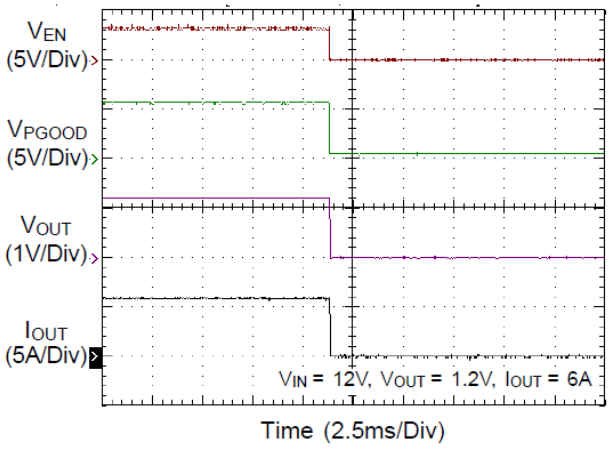

### Power Off from Input Voltage



Power On from Enable Voltage




Power Off from Enable Voltage



# 15 Operation

The RT6236A/B are high-performance 650kHz 6A step-down regulators with internal power switches and synchronous rectifiers. they feature an Advanced Constant On-Time (ACOT®) control architecture that provides stable operation with ceramic output capacitors without the need for complicated external compensation, among other benefits. The ACOT® control mode also provide fast transient response, especially for low output voltages and low duty cycles.

The input voltage range is from 4.5V to 18V, and the output voltage is adjustable from 0.7V to 8V. The proprietary ACOT® control scheme improves upon other constant on-time architectures, achieving a nearly constant switching frequency across line, load, and output voltage ranges. The RT6236A/B are optimized for ceramic output capacitors. Since there is no internal clock, response to transients is nearly instantaneous and the inductor current can ramp up quickly to maintain output regulation without large bulk output capacitance.

## 15.1 Constant On-Time (COT) Control

The core component of any COT architecture is the on-time one-shot. Each on-time is a predetermined "fixed" period that is triggered by a feedback comparator. This robust arrangement has high noise immunity and is ideal for low duty cycle applications. After the on-time one-shot period, there is a minimum off-time period before any further regulation decisions are considered. This arrangement prevents the need to make any decisions during the noisy time periods just after switching events, when the switching node (SW) rises or falls. Because there is no fixed clock, the high-side switch can turn on almost immediately after load transients, and further switching pulses can ramp the inductor current higher to meet load requirements with minimal delays.

Traditional current mode or voltage mode control schemes typically require monitoring of the feedback voltage, current signals (also for current limit), and internal ramps and compensation signals, to determine the optimal timing for turning off the high-side switch and turning on the synchronous rectifier. Accurately measuring these small signals in a switching environment can be challenging just after switching large currents. This makes those architectures problematic at low duty cycles and with suboptimal board layouts.

Because no switching decisions are made during noisy time periods, COT architectures are preferred in low duty cycles and noisy applications. However, traditional COT control schemes have disadvantages that limit their use in many situations. Many applications require a known switching frequency range to avoid interference with other sensitive circuits. True constant on-time control, where the on-time is actually fixed, results in a variable switching frequency. In a step-down converter, the duty cycle is proportional to the output voltage and inversely proportional to the input voltage. Therefore, if the on-time is fixed, the off-time (and therefore the frequency) must change in response to changes in input or output voltage.

Modern pseudo-fixed frequency COT architectures greatly enhance the performance of COT by making the one-shot on-time proportional to VOUT and inversely proportional to VIN. In this way, an on-time is chosen as approximately what it will be for an ideal fixed-frequency PWM in similar input/output voltage conditions. Although this represents a substantial improvement, the switching frequency still varies considerably across line and load conditions due to losses in the switches and inductor, and other parasitic effects.

Another challenge with many COT architectures is their dependence on adequate ESR in the output capacitor, making it difficult to use highly desirable, small, cost-effective ceramic capacitors, which typically have low-ESR. Most COT architectures use AC current feedback from the output capacitor, generated by the inductor current passing through the ESR, to function a current mode control system. However, when using ceramic capacitors, the inductor current feedback is often too small to keep stability in the control loop, like a current mode system with no current feedback.

### 15.2 ACOT® Control Architecture

Making the on-time proportional to VOUT and inversely proportional to VIN is not sufficient to achieve consistent frequency behavior for several reasons. Firstly, voltage drops across the MOSFET switches and the inductor cause the effective input voltage that is lower than the measured input voltage and the effective output voltage is higher than the measured output voltage. As the load changes, the switch voltage drops, causing a switching frequency variation with the load current. Also, at light loads, if the inductor current becomes negative, the switch dead-time between the turn-off of the synchronous rectifier and the turn-on of the high-side switch allows the switching node to rise to the input voltage. This increases the effective on time and causes the switching frequency to drop noticeably.

One way to reduce these effects is to monitor the actual switching frequency and compare it with the desired range. An additional advantage of this approach is that it eliminates the need to sense the actual output voltage, potentially saving one pin connection. ACOT® technology employs this method by measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

For optimal stability when using low-ESR ceramic capacitors, ACOT® uses a virtual inductor current ramp generated by the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR.

The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

### 15.3 ACOT® One-Shot Operation

The RT6236A/B control algorithm is straightforward. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, and the on-time one-shot is triggered, provided that the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. During the on-time one-shot, the high-side switch turns on, and the inductor current ramps up linearly. After the on-time period, the high-side switch turns off, and the synchronous rectifier turns on, causing the inductor current to ramp down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching period, allowing the feedback voltage and current sense signals to settle. The minimum off-time is kept short (230ns typically) to enable rapidly repeated on-times, which can raise the inductor current quickly when needed.

### 15.4 Discontinuous Operating Mode (RT6236A Only)

After soft-start, the RT6236A operates in a fixed frequency mode to minimize interference and noise problems. The RT6236A uses variable-frequency discontinuous switching at light loads to enhance efficiency. During the discontinuous switching, the on-time is immediately increased to add "hysteresis" to discourage the IC from switching back to continuous switching unless the load increases substantially.

The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced to the duration required for 650kHz switching, encouraging the circuit to remain in continuous conduction mode and preventing repetitive transitions between continuous switching and discontinuous switching.

### 15.5 Current Limit

The RT6236A/B current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between the source and drain of the synchronous rectifier. If the inductor current exceeds the current limit, the on-time one-shot is inhibited (mask the high-side signal) until the inductor current ramps down below the current limit. Thus, only when the inductor current is well below the current limit is another on time permitted. This arrangement prevents the average output current from greatly exceeding the guaranteed current limit value, as typically occurs with other valley-type current limits. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output undervoltage

protection level, the IC will stop switching (see Output Overvoltage Protection and Undervoltage Protection).

### 15.6 Output Overvoltage Protection and Undervoltage Protection

If the output voltage $V_{OUT}$ rises above the regulation level and lower 1.2 times regulation level, the high-side switch naturally remains off, and the synchronous rectifier turns on. For the RT6236B, if the output voltage remains high, the synchronous rectifier remains on until the inductor current reaches the low-side current limit. If the output voltage still remains high, the IC's switches ensure that the synchronous rectifier remains on and the high-side MOS stays off, operating at typical 500kHz switching protection frequency. If the inductor current reaches the low-side current limit, the synchronous rectifier will turn off until the next protection clock cycle. If the output voltage exceeds the OVP trip threshold (1.25 times regulation level) for longer than 10μs (typical), the IC's output Overvoltage Protection (OVP) is triggered, and the RT6236BL chip enters latch mode.

For the RT6236A, if the output voltage $V_{OUT}$ rises above the regulation level but is lower than 1.2 times the regulation level, the high-side switch naturally remains off, and the synchronous rectifier turns on until the inductor current reaches zero. If the output voltage remains high, the IC's switches remain off. If the output voltage exceeds the OVP trip threshold (1.25 times the regulation level) for longer than 10μs (typical), the IC's OVP is triggered, and the RT6236AL chip enters latch mode.

The RT6236A/B also includes output Undervoltage Protection (UVP). If the output voltage drops below the UVP trip threshold for longer than 250μs (typical), the IC's UVP is triggered, Causing the chip to enter either latch or hiccup mode (see Hiccup Mode).

### 15.7 Hiccup Mode

The RT6236AH/BH uses hiccup mode for UVP. When the protection function is triggered, the IC will shut down for a period of time and then attempt to recover automatically. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, resuming normal operation as soon as UVP is removed. During hiccup mode, the shutdown time is determined by the capacitor at SS. A 2μA current source discharges $V_{SS}$ from its starting voltage (normally $V_{PVCC}$). The IC remains shut down until $V_{SS}$ reaches 0.2V, about 10ms for a 3.9nF capacitor. At that point, the IC begins to charge the SS capacitor at 6μA, initiating a normal start-up sequence. If the fault remains, the UVP protection will be enabled when $V_{SS}$ reaches 2.2V (typical). The IC will then shut down again and discharge the SS capacitor from the 2.2V level, taking about 4ms for a 3.9nF SS capacitor.

### 15.8 Latch-Off Mode

The RT6236AL/BL uses latch-off mode OVP and UVP. When the protection function is triggered, the IC will shut down in Latch-Off Mode. The IC stops switching, leaving both switches open, and is latched off. To restart operation, toggle EN or cycle the power to the IC off and then on again.

### 15.9 Shut-Down, Start-Up, and Enable (EN)

The enable input (EN) has a logic-low level of 0.4V. When $V_{EN}$ is below this level, the IC enters shutdown mode, and the supply current drops to less than 10μA. When $V_{EN}$ exceeds its logic-high level of 2V, the IC becomes fully operational.

Between these two levels, there are two thresholds (1.2V typical and 1.4V typical). When $V_{EN}$ exceeds the lower threshold, the internal bias regulators begin to function, and the supply current increases above the shutdown current level. Switching operation begins when $V_{EN}$ exceeds the upper threshold. Unlike many competing devices, EN is a high-voltage input that can be safely connected to VIN (up to 18V) for automatic start-up.

### 15.10 Input Undervoltage-Lockout

In addition to the enable function, the RT6236A/B features an Undervoltage-Lockout (UVLO) function that monitors the internal linear regulator output (VIN). To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when VIN drops below the UVLO-falling threshold. The IC resumes switching when VIN exceeds the UVLO-rising threshold.

### 15.11 Soft-Start (SS)

The RT6236A/B soft-start uses an external pin (SS) to clamp the output voltage and allow it to slowly rise. After $V_{EN}$ is high and VIN exceeds its UVLO threshold, the IC begins to source 6μA from the SS pin. An external capacitor at SS is used to adjust the soft-start timing. Use the equation below to determine the minimum capacitance required to avoid UV occurrence.

$$T = \frac{C_{OUT} \times V_{OUT} \times 0.6 \times 1.2}{(I_{LIM} - \text{Load Current}) \times 0.8}$$

$$C_{SS} \geq \frac{T \times 6\mu A}{V_{REF}}$$

Do not leave SS unconnected. During start-up, while the SS capacitor charges, the RT6236A/B operates in discontinuous switching mode with very small pulses. This prevents negative inductor currents and keeps the circuit from sinking current. Therefore, the output voltage may be pre-biased to a positive level before start-up. Once the $V_{SS}$ ramp charges enough to raise the internal reference above the feedback voltage, switching will begin, and the output voltage will smoothly rise from the pre-biased level to its regulated level. After $V_{SS}$ rises above about 2.2V, output overvoltage and undervoltage protections are enabled, and the RT6236A/B transitions to continuous-switching operation.

### 15.12 Internal Regulator (PVCC)

An internal linear regulator (PVCC) generates a 5V supply from VIN. The 5V supply powers the internal control circuits, such as the internal gate drivers, PWM logic, reference, analog circuitry, and other blocks. A 1μF ceramic capacitor for decoupling and stability is required.

### 15.13 PG Comparator

PG is an open-drain output controlled by a comparator connected to the feedback signal. If FB exceeds 90% of the internal reference voltage or an OVP event is cleared, PG will be in a high impedance state. Otherwise, the PG output is connected to GND.

### 15.14 External Bootstrap Capacitor ($C_{BOOT}$)

Connect a 0.1μF low ESR ceramic capacitor between BOOT and SW. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET switch.

In some cases, such as when the duty ratio is higher than 65% application or the input voltage is lower than 5.5V, it is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement. The bootstrap diode can be a low-cost option such as the IN4148 or BAT54. The external 5V source can be a fixed 5V input from the system or a 5V output from the RT6236A/B. Note that the external boot voltage must be lower than 5.5V.

### 15.15 Over-Temperature Protection

The RT6236A/B includes an Over-Temperature Protection (OTP) circuitry to prevent overheating caused by

excessive power dissipation. The OTP will shut down the switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling to keep the junction temperature below 150 °C.

# 16 Application Information

(Note 6)

## 16.1 Inductor Selection

Selecting an inductor involves specifying its inductance and its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best balance of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and can improve the circuit's transient response. However, they increase the inductor ripple current and output voltage ripple, and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required. Additionally, the transient response will be slower as more time is required to change the current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current ($\Delta I_L$) that is about 20% to 50% of the desired full output load current. To calculate the approximate inductor value, select the input and output voltages. the switching frequency ($f_{SW}$), the maximum output current ($I_{OUT(MAX)}$), and estimate $\Delta I_L$ as a percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current ($\Delta I_L$) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are the minimum requirements. In some application, to maintain control of the inductor current during overload and short circuit conditions, it may be desirable to have current ratings up to the current limit value. However, the IC's output undervoltage shutdown feature makes this unnecessary for most applications.

$I_{L(PEAK)}$ should not exceed the minimum value of the IC's upper current limit level, or the IC may not be able to meet the desired output current. If necessary, reduce the inductor ripple current ($\Delta I_L$) to increase the average inductor current (and the output current) while ensuring that $I_{L(PEAK)}$ does not exceed the upper current limit level.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For minimize inductor core losses, a ferrite core is usually the best choice. Although a shielded core type may be larger or more expensive, it will likely result in fewer EMI and other noise problems.

Considering the Typical Application Circuit for a 1.2V output at 6A with an input voltage of 12V, and using an inductor ripple of 1.2A (20%), the calculated inductance value is:

$$L = \frac{1.2 \times (12 - 1.2)}{12 \times 650kHz \times 1.2A} = 1.38\mu H$$

The ripple current was selected to be 1.2A. As long as we use the calculated 1.5μH inductance, this should be the actual ripple current amount. The ripple current and required peak current are as follows:

$$\Delta I_L = \frac{1.2 \times (12 - 1.2)}{12 \times 650kHz \times 1.5\mu H} = 1.108A$$

$$\text{and } I_{L(PEAK)} = 6A + \frac{1.108A}{2} = 6.554A$$

For the 1.5μH value, the inductor's saturation and thermal rating should exceed at least 6.554A. For more conservative, the rating for the inductor saturation current must be equal to or greater than the switch current limit of

the device, rather than the inductor peak current.

### 16.2 Input Capacitor Selection

The input filter capacitors are necessary to smooth out the switched current drawn from the input power source and to reduce voltage ripple on the input. The actual capacitance value is less important than the RMS current rating (and voltage rating, of course). The RMS input ripple current ($I_{RMS}$) is a function of the input voltage, output voltage, and load current:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. However, caution is needed when these capacitors are used at the input of circuits supplied by a wall adapter or other supply connected through long, thin wires. Current surges through the inductive wires can induce ringing at the RT6236A/B input, potentially causing large, damaging voltage spikes at VIN. If this phenomenon is observed, some bulk input capacitance may be required. Ceramic capacitors (to meet the RMS current requirement) can be placed in parallel with other types such as tantalum, electrolytic, or polymer (to reduce ringing and overshoot).

Choose capacitors rated at higher temperatures than required. Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application. The typical operating circuit uses two 10μF and one 0.1μF low ESR ceramic capacitors on the input.

### 16.3 Output Capacitor Selection

The RT6236A/B are optimized for ceramic output capacitors, and the best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

### 16.4 Output Ripple

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

For the Typical Application Circuit with a 1.2V output and an inductor ripple of 1.108A, using 3 x 22μF output capacitors each with about 5mΩ ESR (including PCB trace resistance), the components of the output voltage ripple are as follows:

$$V_{RIPPLE(ESR)} = 1.108A \times 5m\Omega = 5.54mV$$

$$V_{RIPPLE(C)} = \frac{1.108A}{8 \times 66\mu F \times 650kHz} = 3.23mV$$

$$V_{RIPPLE} = 6mV + 3.23mV = 9.23mV$$

### 16.5 Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT® transient response is very quick, and output transients are usually small.

However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's 650kHz switching frequency.

However, some modern digital loads can exhibit nearly instantaneous load changes. The following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components: the voltage steps caused by the output capacitor's ESR, and the voltage sag, and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor:

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit. However, we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as follows:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times \left(V_{IN(MIN)} \times D_{MAX} - V_{OUT}\right)}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

For the Typical Application Circuit for a 1.2V output, the circuit has an inductor of 1.5μH and 3 x 22μF output capacitance with 5mΩ ESR each. The ESR step is 6A x 1.67mΩ = 10mV, which is small, as expected. The output voltage sag and soar in response to full 0A-6A-0A instantaneous transients are:

$$t_{ON} = \frac{1.2V}{12V \times 650kHz} = 153ns$$

$$\text{and } D_{MAX} = \frac{153ns}{153ns + 230ns} = 0.399$$

where 230ns is the minimum off time.

$$V_{SAG} = \frac{1.5\mu H \times (6A)^2}{2 \times 66\mu F \times (12V \times 0.399 - 1.2V)} = 114mV$$

$$V_{SOAR} = \frac{1.5\mu H \times (6A)^2}{2 \times 66\mu F \times 1.2V} = 341mV$$

The voltage sag is about 9.5% of the output voltage, and the voltage soar is a full 28.42% of the output voltage. The ESR step is negligible here but it does partially add to the soar when using higher-ESR output capacitors.

The voltage soar is typically much worse than the sag in high-input, low-output step-down converters because the high input voltage demands a large inductor value, which stores lots of energy that is transferred into the output if the load stops drawing current. Also, for a given inductor, the soar for a low output voltage is a greater voltage change and an even higher percentage of the output voltage.

Any voltage sag is always short-lived, as the circuit quickly sources current to regain regulation within a few switching cycles. With the RT6236B, any overshoot transient is also typically short-lived since the converter will sink current, reversing the inductor current sharply until the output reaches regulation again. The RT6236A operates in discontinuous mode at light loads and prevents sinking current, so for that IC, the output voltage will soar until load current or leakage brings the voltage down to normal.

Most applications never experience instantaneous full load steps, and the RT6236A/B high switching frequency and fast transient response can easily control voltage regulation at all times. Also, since both sag and soar are proportional to the square of the load change, if load steps are reduced to 1A (from the 6A examples previously mentioned), the voltage changes will be reduced by a factor of almost ten. For these reasons, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitors (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, always calculate the soar to ensure that overvoltage protection will not be triggered. Undervoltage is unlikely since the threshold is very low (60%), that function has a long delay (250μs), and the IC will quickly return the output to regulation. Overvoltage protection has a minimum threshold of 120% and a short delay of 10μs, and can actually be triggered by incorrect component choices, particularly for the RT6236A, which does not sink current.

### 16.6 Feed-Forward Capacitor ($C_{ff}$)

The RT6236A/B are optimized for ceramic output capacitors and low duty cycle applications. However, for high-output voltages with high feedback attenuation, the circuit's response can become over-damped, slowing transient response. In high-output voltage circuits ($V_{OUT}$ > 3.3V), the transient response can be improved by adding a small "feed-forward" capacitor ($C_{ff}$) across the upper FB divider resistor (Figure 1). This increases the circuit's Q and reduces damping, thereby speeding up the transient response without affecting the steady-state stability of the circuit. Choose a suitable capacitor value by using the following steps:

- Determine the bandwidth (BW) by the quickest method to perform a transient response from no load to full load. Confirm the damping frequency. The damping frequency is equivalent to BW.

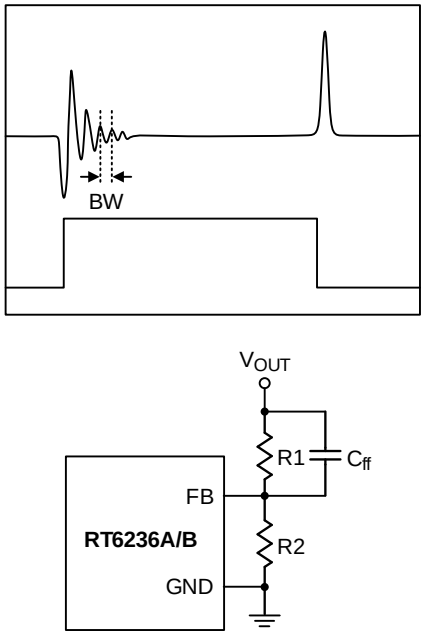



Figure 1.$C_{ff}$ Capacitor Setting

- $C_{ff}$ can be calculated using the following equation:

$$C_{ff} = \frac{1}{2 \times 3.1412 \times R1 \times BW \times 0.8}$$

### 16.7 Soft-Start (SS)

The RT6236A/B soft-start function uses an external capacitor at SS to adjust the soft-start timing according to the following equation:

$$t\ (ms) = \frac{C_{SS}\ (nF) \times 0.7V}{I_{SS}\ (\mu A)}$$

To determine the minimum capacitance required to avoid UV occurrences, refer to the following equation:

$$T = \frac{C_{OUT} \times V_{OUT} \times 0.6 \times 1.2}{(I_{LIM} - \text{Load Current}) \times 0.8}$$

$$C_{SS} \geq \frac{T \times 6\mu A}{V_{REF}}$$

Do not leave SS unconnected.

### 16.8 Enable Operation (EN)

For automatic start-up, the low-voltage EN pin can be connected to VIN through a 100kΩ resistor. Its large hysteresis band makes EN useful for simple delay and timing circuits. EN can be externally pulled to VIN by adding a resistor-capacitor delay ($R_{EN}$ and $C_{EN}$ in Figure 2). Calculate the delay time using EN's internal threshold where switching operation begins.

An external MOSFET can be added to implement digital control of EN when no system voltage above 2V is available (Figure 3). In this case, a 100kΩ pull-up resistor, $R_{EN}$, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling the circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input undervoltage lockout threshold (Figure 4).

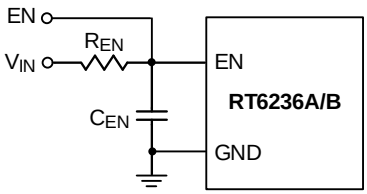



Figure 2. External Timing Control

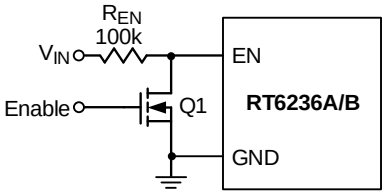



Figure 3. Digital Enable Control Circuit

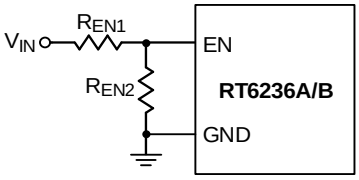



Figure 4. Resistor Divider for Lockout Threshold Setting

### 16.9 Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground, with the midpoint connected to FB. The output voltage is set according to the following equation:

$V_{OUT}$ = 0.7V x (1 + R1 / R2)

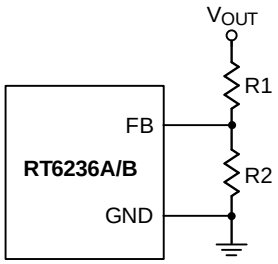



Figure 5. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up, and calculate R1 as follows:

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

### 16.10 External BOOT Bootstrap Diode

When the input voltage is lower than 5.5V, it is recommended to add an external bootstrap diode between VIN (or VINR) and the BOOT pin to enhance the internal MOSFET switch and improve efficiency. The bootstrap diode can be a low-cost option such as 1N4148 or BAT54.

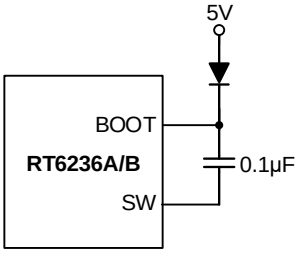



Figure 6. External Bootstrap Diode

### 16.11 External BOOT Capacitor Series Resistance

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Most EMI occurs during switch turn-on, as $V_{SW}$ rises rapidly. During switch turn-off, SW is discharged relatively slowly by the inductor current during the dead time between high-side and low-side switch on-times. In some cases, it is desirable to reduce EMI further at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<47Ω) resistor between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and the rise of $V_{SW}$ rise. To remove the resistor from the capacitor charging path (avoiding poor enhancement due to undercharging the BOOT capacitor), use the external diode shown in Figure 6 to charge the BOOT capacitor and place the resistance between BOOT and the capacitor/diode connection.

### 16.12 PVCC Capacitor Selection

Decouple PVCC to GND with a 1µF ceramic capacitor. It is recommended to use high-grade dielectric (X7R or X5R) ceramic capacitors, due to their stable temperature and bias voltage characteristics.

### 16.13 Thermal Considerations

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and the difference between junction and ambient temperature. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout-dependent. For the UQFN-13JL 2x3 (FC) package, the thermal resistance, $\theta_{JA}$, is 64.8°C/W on a standard four-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (125°C – 25°C) / (64.8°C /W) = 1.54W for UQFN-13JL 2x3 (FC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

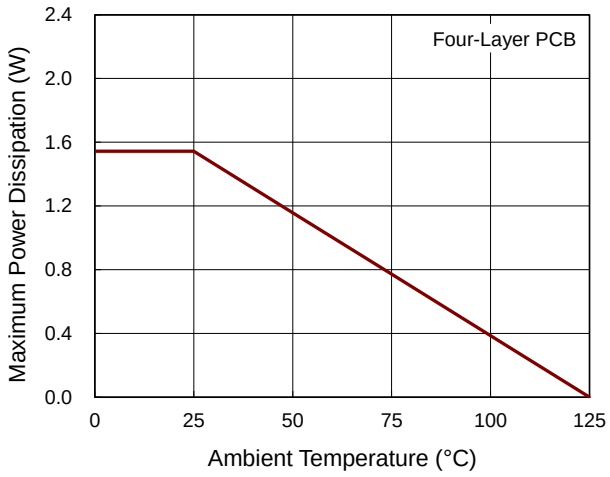



Figure 7. Derating Curve of Maximum Power Dissipation

### 16.14 Layout Consideration

- Follow the PCB layout guidelines for optimal performance of the device.
- Keep the traces of the main current paths as short and wide as possible.
- Place the input capacitor as close as possible to the VIN and VIN pins.
- The SW node is with a high-frequency voltage swing and should be kept to a small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect the feedback network behind the output capacitors. Keep the loop area small and place the feedback components near the device.
- Connect all analog grounds to a common node, and then connect the common node to the power ground behind the output capacitors.
- An example of a PCB layout guide is shown in Figure 8 for reference.

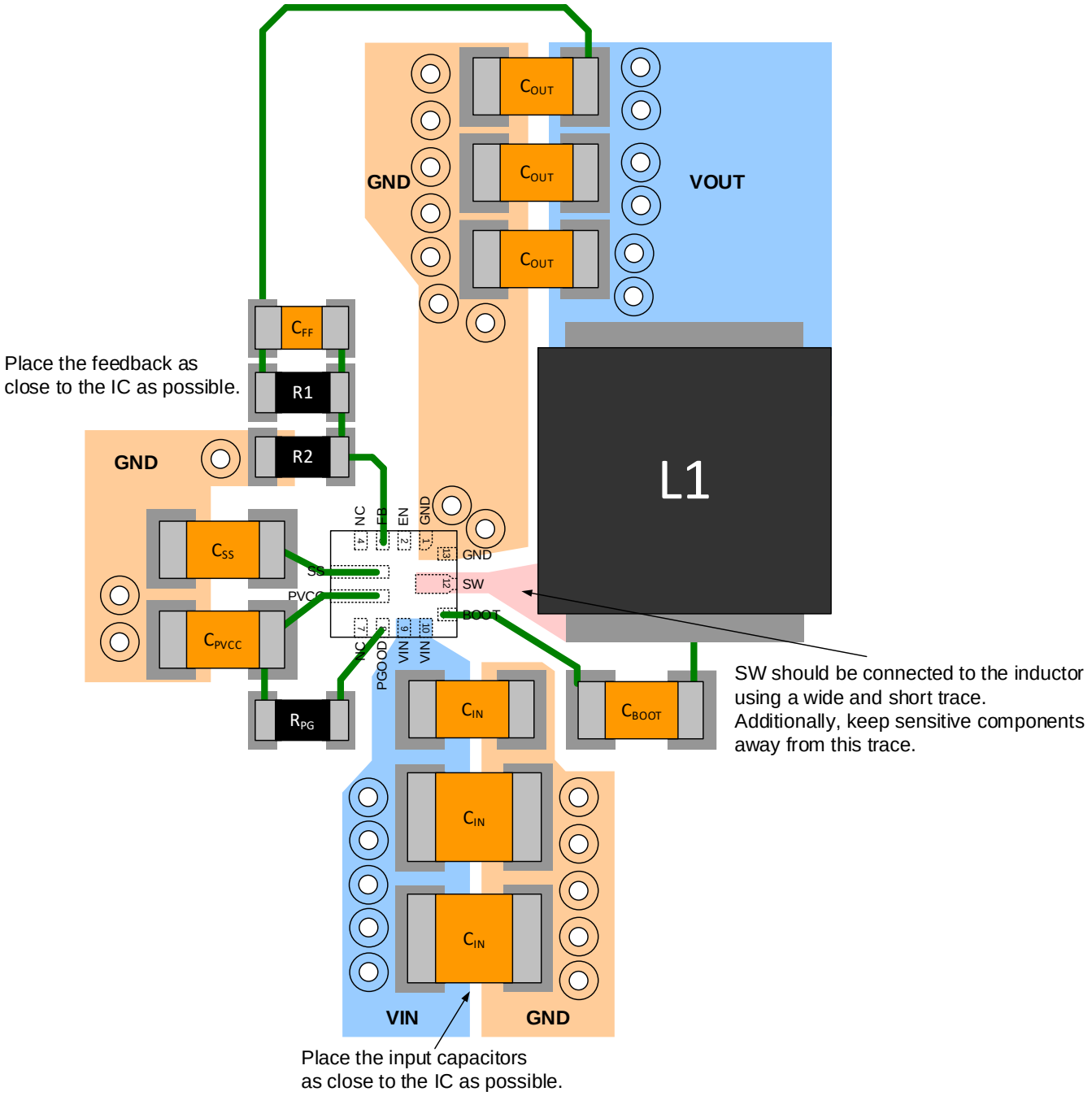
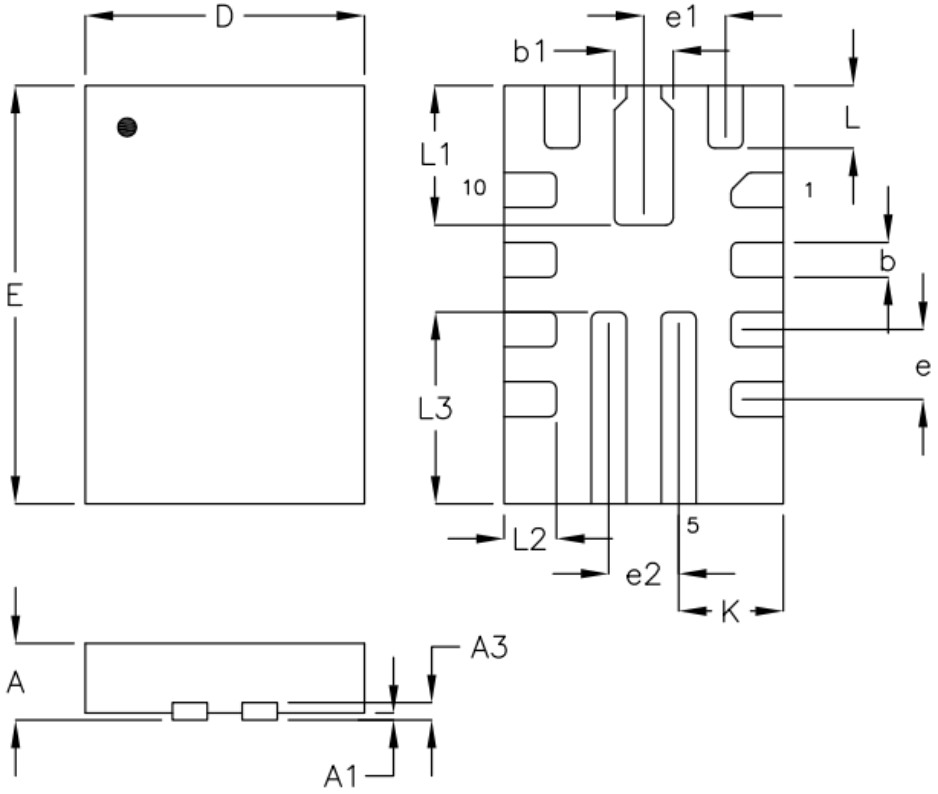



Figure 8. PCB Layout Guide

**Note 6.** The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

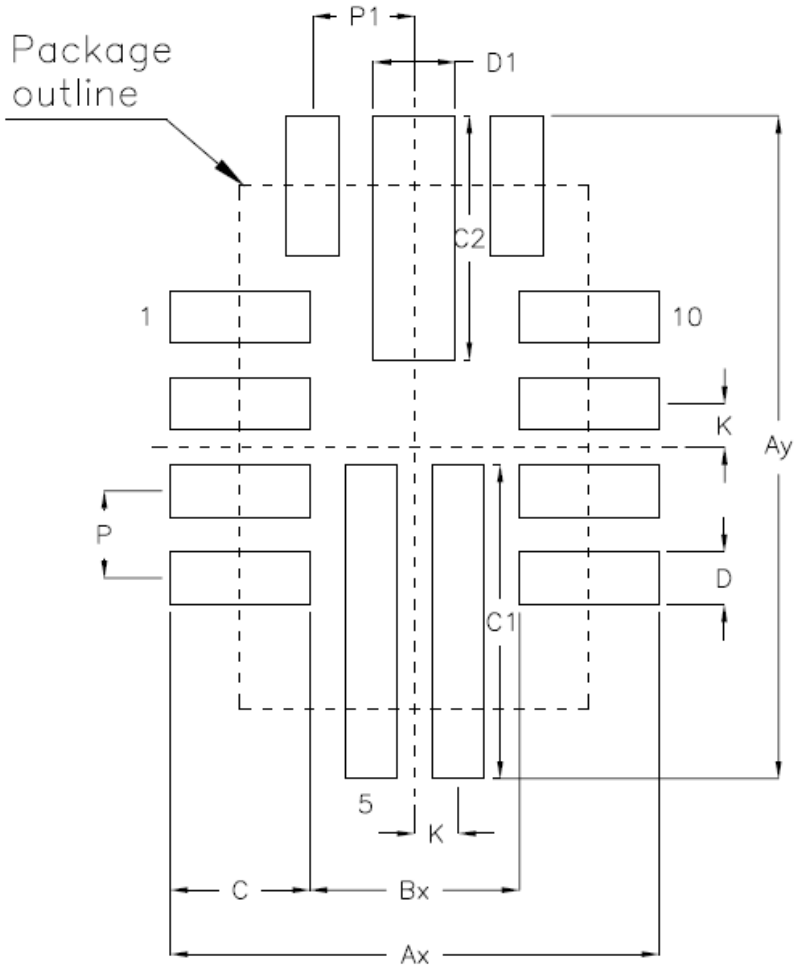
## 17 Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.100 | 0.152 | 0.004 | 0.006 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| b1 | 0.370 | 0.470 | 0.015 | 0.019 |
| D | 1.900 | 2.100 | 0.075 | 0.083 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| K | 0.750 | | 0.030 | |
| e | 0.500 | | 0.020 | |
| e1 | 0.585 | | 0.023 | |
| e2 | 0.500 | | 0.020 | |
| L | 0.400 | 0.500 | 0.016 | 0.020 |
| L1 | 0.950 | 1.050 | 0.037 | 0.041 |
| L2 | 0.325 | 0.425 | 0.013 | 0.017 |
| L3 | 1.325 | 1.425 | 0.052 | 0.056 |

**U-Type 13JL QFN 2x3 (FC) Package**

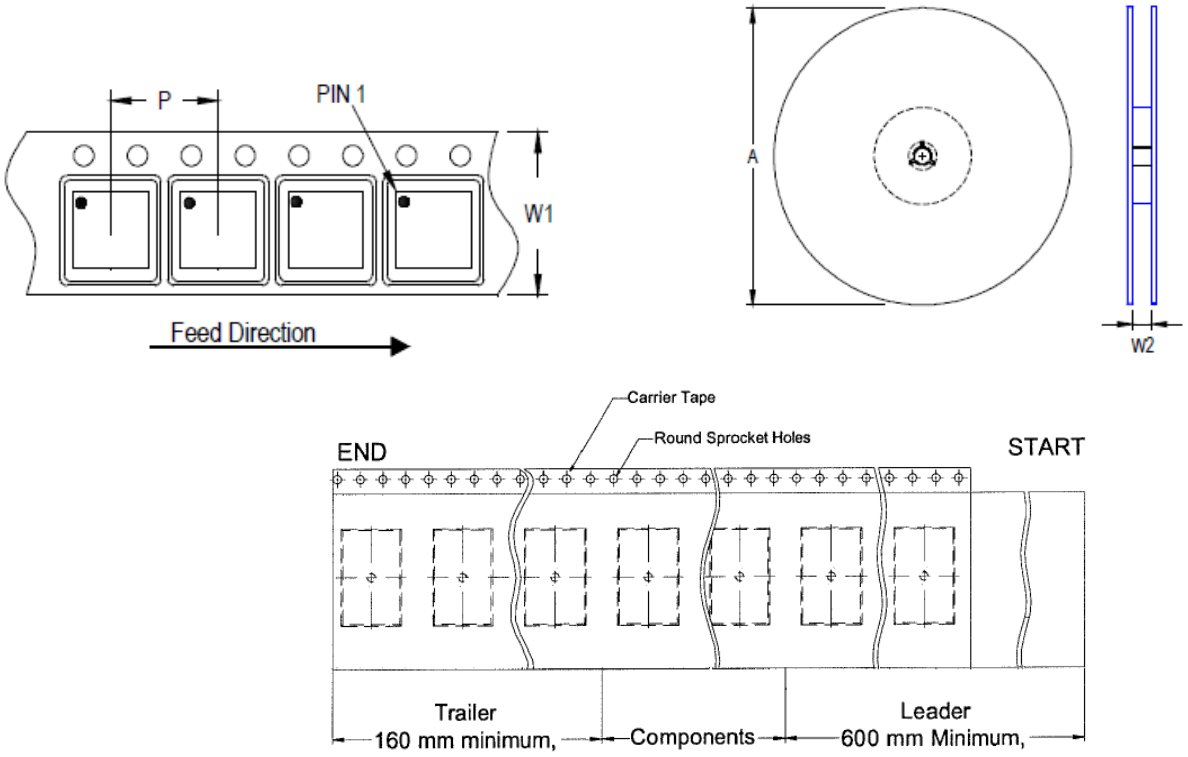
## 18 Footprint Information



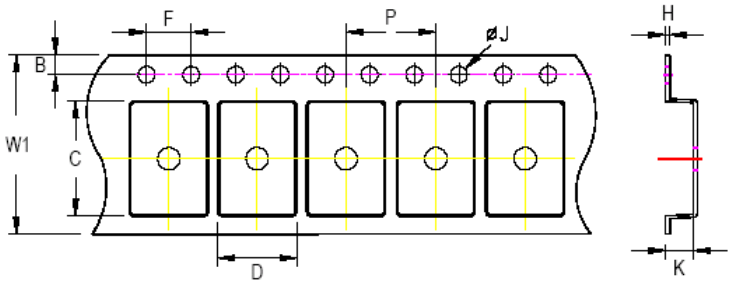

| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | | | Tolerance |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P | P1 | Ax | Bx | Ay | C*10 | C1*2 | C2 | D*12 | D1 | K | |
| UQFN2x3-13J(FC) | 13 | 0.500 | 0.585 | 2.800 | 1.200 | 3.800 | 0.800 | 1.800 | 1.400 | 0.300 | 0.470 | 0.250 | ±0.050 |

# 19 Packing Information

## 19.1 Tape and Reel Data




| Package Type | Tape Size (W1) (mm) | Pocket Pitch (P) (mm) | Reel Size (A) | | Units per Reel | Trailer (mm) | Leader (mm) | Reel Width (W2) Min./Max. (mm) |
|---|---|---|---|---|---|---|---|---|
| | | | (mm) | (in) | | | | |
| (V, W) QFN/DFN 2x3 | 12 | 8 | 180 | 7 | 1,500 | 160 | 600 | 12.4/14.4 |




**C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:**

**- For 12mm carrier tape: 0.5mm max.**

| Tape Size | W1 | P | | B | | F | | ØJ | | K | | H |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Max. |
| 12mm | 12.3mm | 7.9mm | 8.1mm | 1.65mm | 1.85mm | 3.9mm | 4.1mm | 1.5mm | 1.6mm | 1.0mm | 1.3mm | 0.6mm |

### 19.2 Tape and Reel Packing

| Step | Photo/Description | Step | Photo/Description |
|---|---|---|---|
| 1 |  Reel 7” | 4 |  3 reels per inner box **Box A** |
| 2 |  HIC & Desiccant (1 Unit) inside | 5 |  12 inner boxes per outer box |
| 3 |  Caution label is on backside of Al bag | 6 |  Outer box **Carton A** |

| Container / Package | Reel | | Box | | | Carton | | |
|---|---|---|---|---|---|---|---|---|
| | Size | Units | Item | Reels | Units | Item | Boxes | Unit |
| (V, W) QFN & DFN 2x3 | 7” | 1,500 | Box A | 3 | 4,500 | Carton A | 12 | 54,000 |
| | | | Box E | 1 | 1,500 | For Combined or Partial Reel. | | |

### 19.3 Packing Material Anti-ESD Property

| Surface Resistance | Aluminum Bag | Reel | Cover tape | Carrier tape | Tube | Protection Band |
|---|---|---|---|---|---|---|
| $\Omega/cm^2$ | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** |

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## 20 Datasheet Revision History

| Version | Date | Description | Item |
|---|---|---|---|
| 04 | 2024/7/17 | Modify | *Simplified Application Circuit on page 1*<br>*General Description on page 1*<br>*Features on page 1*<br>*Ordering Information on page 1*<br>*Pin Configuration on page 4*<br>*Functional Pin Description on page 4*<br>*Functional Block Diagram on page 5*<br>*Electrical Characteristics on page 7, 8*<br>*Typical Application Circuit on page 9*<br>*Application Information on page 27*<br>*Footprint Information on page 29*<br>*Packing Information on page 30, 31, 32*<br>- Added packing information |