1.8V to 5.5V, 0.6A/1A, 2.3μA I_Q Step-Down Converter in 0.35mm Pitch WCSP Package

1 General Description

The RT5716 is a high switching frequency synchronous step-down converter with a quiescent current of 2.3μA. The device uses Ripple-Based Constant-On-Time (RBCOT) control to enhance load and line transient response, optimizing performance over a wide range of loads and output capacitors.

The RT5716 has an input voltage range from 1.8V to 5.5V, making it suitable for battery applications. It provides 16 selectable output voltage levels by connecting a resistor between RSEL/MODE pin and GND. The Pulse Frequency Modulation (PFM) design maintains high efficiency during light loads. While at higher load conditions, the device automatically switches to PWM. The device can deliver up to 1A loading current. In shutdown mode, the supply current is typically 55nA, which is excellent for reducing power consumption.

The RT5716 is available in TWL-CSP-6B 0.69x1.04 (BSC) and WDFN-6L 1.5x1.5 (FC) packages, which are the smallest packages for small-size applications.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT5716□-□□□

Packing
A: Default Code

OCP and Frequency Select
(Refer to Functional Table)

Output Voltage Combination
(Refer to Functional Table)

Package Type(1)
P: TWL-CSP-6B 0.69x1.04 (BSC)
FN: WDFN-6L 1.5x1.5 (FC) (W-Type)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

3 Features

- **4MHz Switching Frequency**
- **2.3μA Operating Quiescent Current**
- **Input Voltage Range: 1.8V to 5.5V**
- **16 Selectable Output Voltages by RSEL/MODE Pin and Fixed Output Voltage Without RSEL Setting**
- **RBCOT Control for Transient Response**
- **PFM and Force Pulse Width Modulation (FPWM) Mode**
- **Output Voltage Discharge**
- **OCP, OTP, and UVLO Protection**
- **Support up to 1A Loading Current**

4 Applications

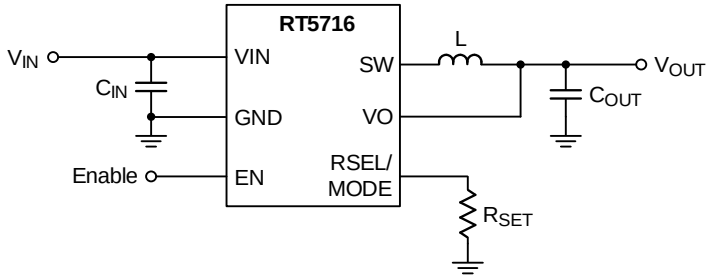
- Hand-Held Devices
- PCB Area Limited Applications
- Asset Tracking Devices
- Battery Powered Equipment
- Wearable Devices
- Internet of Things

5 Marking Information

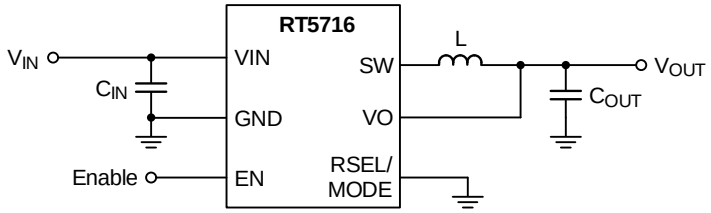
For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 Simplified Application Circuit

6.1 Adjustable VOUT by RSET Setting



6.2 Fixed VOUT



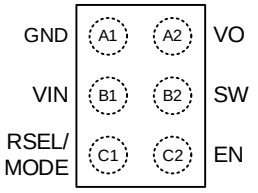
7 Functional Table

Output Voltage Setting Range		OCP and Frequency Select	
A	Output-1, 0.4V to 3.3V	A	OCP Select 1 = 1.2A, Frequency Select 1 = 4MHz
B	Output-2, 0.4V to 0.775V in 25mV steps	B	OCP Select 2 = 1.7A, Frequency Select 1 = 4MHz
C	Output-3, 0.8V to 1.55V in 50mV steps	C	OCP Select 1 = 1.2A, Frequency Select 1 = 1.5MHz
D	Output-4, 1.8V to 3.3V in 100mV steps	D	OCP Select 2 = 1.7A, Frequency Select 1 = 1.5MHz

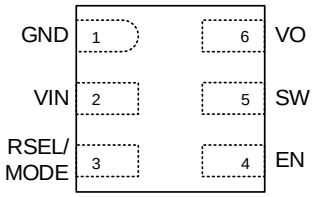
Table of Contents

8 Pin Configuration

(TOP VIEW)



TWL-CSP-6B 0.69x1.04 (BSC)

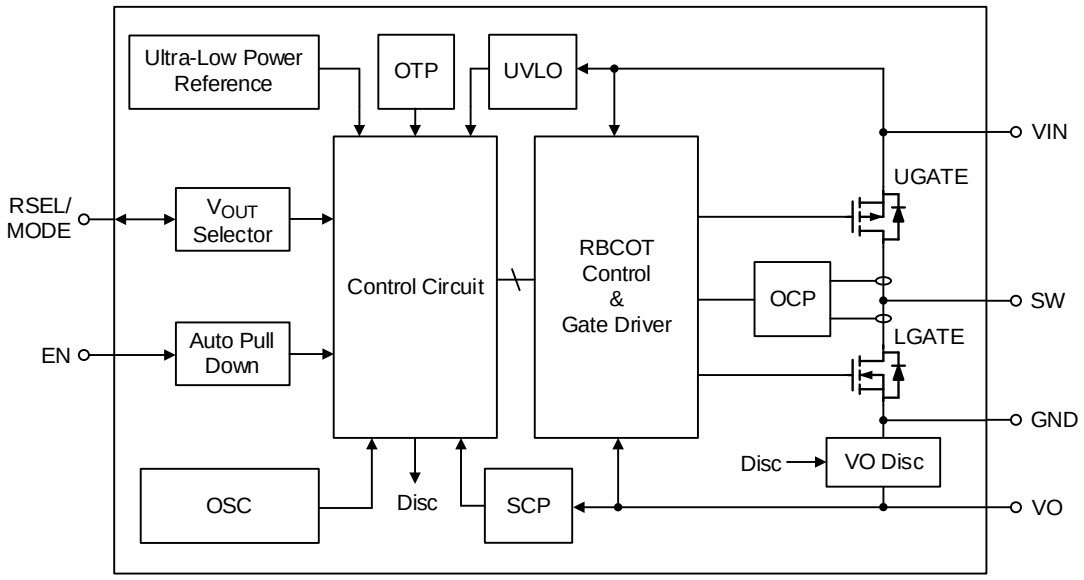


WDFN-6L 1.5x1.5 (FC)

9 Functional Pin Description

Pin No.		Pin Name	Pin Function
TWL-CSP-6B 0.69x1.04 (BSC)	WDFN-6L 1.5x1.5 (FC)		
A1	1	GND	Device ground pin. This pin should be connected to input and output capacitors with the shortest path.
A2	6	VO	Output voltage feedback pin. This pin should be connected close to the output capacitor terminal for better voltage regulation. A ceramic capacitor of sufficient value should be connected to this pin with the shortest possible path.
B1	2	VIN	Supply input. A ceramic capacitor of sufficient value should be connected to this pin with the shortest possible path.
B2	5	SW	This pin is the connection between two build-in switches in the chip, which should be connected to the external inductor. The inductor should be connected to this pin with the shortest path.
C1	3	RSEL/ MODE	Connecting a resistor between RSEL/MODE and GND sets the VOUT level when the converter is enabled. Once the VOUT level has been decided, RSEL/MODE pin operates as an input. Pull low for PFM operation during light load and pull it high for FPWM operation. (There is no additional current path or capacitance greater than 30pF to GND during resistor-to-digital conversion.)
C2	4	EN	Chip enable input pin. High level voltage enables the device while low level voltage turns the device off. This pin must be terminated.

10 Functional Block Diagram



11 Absolute Maximum Ratings

(Note 2), (Note 3)

- VIN, VO, RSEL/MODE, EN ---------- –0.3V to 6V
- SW (DC) ---------- –0.3V to V_{IN} + 0.3V
- SW(AC), less than 10ns while switching ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C

  TWL-CSP-6B 0.69x1.04 (BSC) ---------- 1.03W

  WDFN-6L 1.5x1.5 (FC) ---------- 0.69W
- Package Thermal Resistance (Note 4)

  TWL-CSP-6B 0.69x1.04 (BSC), θ_{JA} ---------- 96.8°C/W

  WDFN-6L 1.5x1.5 (FC), θ_{JA} ---------- 145.34°C/W

  WDFN-6L 1.5x1.5 (FC), θ_{JC} ---------- 16.73°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)

  HBM (Human Body Model) ---------- ±2kV

  CDM (Charged Device Model) ---------- ±500V

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. The operating voltage for RSEL/MODE is recommended to be lower than the input voltage.

Note 4. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 6)

Recommended Operating Conditions		Min	Typ	Max	Unit
V_{IN}	Supply voltage, V_{IN}	1.8	--	5.5	V
I_{OUT}	Output current, $V_{IN} \geq$ 2.3V, RT5716X-XB, RT5716X-XD	--	--	1	A
I_{OUT}	Output current, V_{IN} < 2.3V, RT5716X-XB, RT5716X-XD	--	--	0.7	A
I_{OUT}	Output current, RT5716X-XA, RT5716X-XC	--	--	0.6	A
L	Effective inductance, RT5716X-XA, RT5716X-XB	0.33	0.47	1.2	µH
C_{OUT}	Effective output capacitance, RT5716X-XA, RT5716X-XB	2	--	26	µF
L	Effective inductance, RT5716X-XC, RT5716X-XD	0.7	1	1.2	µH
C_{OUT}	Effective output capacitance, RT5716X-XC, RT5716X-XD	--	10	--	µF
C_{IN}	Effective input capacitance	0.5	4.7	--	µF
$C_{RSEL/MODE}$	External parasitic capacitance at the RSEL/MODE pin	--	--	30	pF

Recommended Operating Conditions		Min	Typ	Max	Unit
R_{SET}	Resistance range for external resistor at RSEL/MODE pin (E96 1% Resistor Values)	10	--	249	kΩ
	External resistor tolerance E96 series at RSEL/MODE pin	--	--	1%	--
	E96 resistor series temperature coefficient (TCR)	–200	--	200	ppm/°C
T_A	Operating ambient temperature range	–40	--	85	°C
T_J	Operating junction temperature range	–40	--	125	°C

Note 6. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(V_{IN} = 3.6V, C_{IN} = 4.7μF, C_{OUT} = 4.7μF x 2, L = 0.47μH, T_J = –40°C to 125°C, typical values are at T_J = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Buck Regulator						
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising, T_J = –40°C to 125°C (Note 7)	--	1.7	1.8	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}	V_{IN} falling, T_J = –40°C to 125°C (Note 7)	--	1.65	1.75	V
Undervoltage-Lockout Deglitch Time	$t_{DEGLITCH\_UVLO}$		--	32	--	μs
Quiescent Current into VIN Pin (Switching)	$I_{Q\_VIN\_SW}$	EN = V_{IN}, I_{OUT} = 0A, V_{OUT} = 1.2V, RSEL/MODE = GND	--	2.5	--	μA
Quiescent Current (Force PWM Mode)	$I_{Q\_VIN\_PWM}$	EN = V_{IN}, I_{OUT} = 0A, V_{OUT} = 1.2V, RSEL/MODE = V_{IN} (after start-up)	--	8	--	mA
Quiescent Current into VIN Pin (Non-Switching)	$I_{Q\_VIN\_NSW}$	EN = V_{IN}, I_{OUT} = 0A, V_{OUT} = 1.2V, T_J = –40°C to 85°C (Note 7), RSEL/MODE = GND	--	2.3	3.7	μA
Shutdown Current	I_{SHDN}	EN = GND, shutdown current into V_{IN} RSEL/MODE = GND, T_J = –40°C to 85°C (Note 7)	--	55	250	nA
Bias Current into VO Pin	I_{BIAS_VO}	EN = V_{IN}, V_{OUT} = 1.2V, (internal 8M resistor divider), T_J = –40°C to 85°C (Note 7)	--	100	400	nA
Switching Frequency	f_{SW}	EN = V_{IN}, I_{OUT} = 0A, V_{OUT} = 1.8V, RSEL/MODE = V_{IN} (after start-up)	--	4	--	MHz
Positive Inductor Peak Current Limit	I_{LIM_PEAK}	1.8V ≤ V_{IN} ≤ 5.5V, OCP Select 1 = 1.2A, T_J = –40°C to 125°C (Note 7)	1.02	1.2	1.38	A
		1.8V ≤ V_{IN} ≤ 5.5V, OCP Select 2 = 1.7A, T_J = –40°C to 125°C (Note 7)	1.44	1.7	1.96	
Positive Inductor Valley Current Limit	I_{LIM_VALLEY}	1.8V ≤ V_{IN} ≤ 5.5V, OCP Select 1 =1.2A, T_J = –40°C to 125°C (Note 7)	0.73	0.86	0.99	A
		1.8V ≤ V_{IN} ≤ 5.5V, OCP Select 2 = 1.7A, T_J = –40°C to 125°C (Note 7)	1.15	1.36	1.57	
Negative Inductor Peak Current Limit	$I_{LIM\_PEAK\_NEG}$	1.8V ≤ V_{IN} ≤ 5.5V	--	–1	--	A

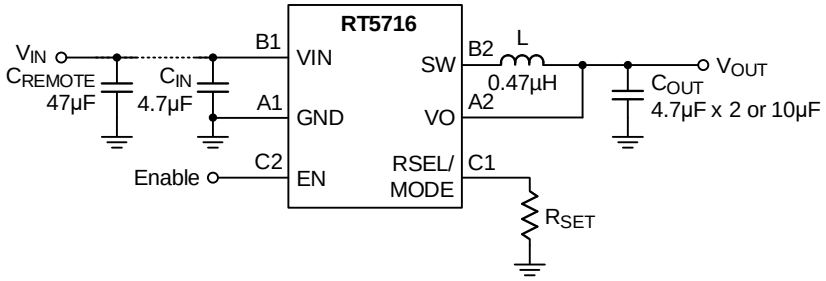
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit Propagation Delay	t_{DLY_LIM}		--	50	--	ns
Leakage Current into the SW Pin	I_{SW_LK}	V_{SW} = 1.2V, T_J = –40°C to 85°C (Note 7)	--	10	25	nA
On-Resistance of High-Side MOSFET	R_{ON_H}	T_J = –40°C to 125°C (Note 7)	--	120	170	mΩ
On-Resistance of Low-Side MOSFET	R_{ON_L}	T_J = –40°C to 125°C (Note 7)	--	80	115	mΩ
Minimum On-Time	t_{ON_MIN}	V_{IN} = 5.5V, V_{OUT} = 0.4V	--	40	--	ns
Minimum Off-Time	t_{OFF_MIN}	V_{IN} = 3.6V, V_{OUT} = 3.3V	--	40	--	ns
Output Discharge Resistance	R_{DISCHG}	EN = GND, I_{VOS} = –10mA into the VO pin, T_J = –40°C to 85°C (Note 7)	--	7	11	Ω
Output Voltage Accuracy	V_{OUT_ACC}	PFM mode, V_{OUT} ≤ 1.5V, I_{OUT} = 1mA, T_J = –40°C to 85°C (Note 7)	--	±22.5	--	mV
		PFM mode, V_{OUT} > 1.5V, I_{OUT} = 1mA, T_J = –40°C to 85°C (Note 7)	--	±1.5	--	%
		FPWM mode, V_{OUT} ≤ 1.5V, I_{OUT} = 0mA, T_J = –40°C to 125°C (Note 7)	--	±22.5	--	mV
		FPWM mode, V_{OUT} > 1.5V, I_{OUT} = 0mA, T_J = –40°C to 125°C (Note 7)	--	±1.5	--	%
Load Regulation	V_{LOAD_REG}	V_{IN} = 3.6V, V_{OUT} = 1.2V, FPWM, I_{OUT} = 0A to 1A (Note 7) (For TWL-CSP package)	--	±1	--	%
		V_{IN} = 3.6V, V_{OUT} = 1.2V, FPWM, I_{OUT} = 0A to 1A (Note 7) (For WDFN package)	--	±2	--	
Line Regulation	V_{LINE_REG}	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.2V, I_{OUT} = 0mA, FPWM (Note 7)	--	±1	--	%
Auto Bypass Mode Leave Detection Threshold	V_{TH_100+}	Rising V_{IN}, 100% mode is left with V_{IN} = V_{OUT} + V_{TH_100+}	--	250	--	mV
Auto Bypass Mode Enter Detection Threshold	V_{TH_100-}	Falling V_{IN}, 100% mode is entered with V_{IN} = V_{OUT} + V_{TH_100-}	--	190	--	mV
Over-Temperature Protection	T_{OTP}	V_{IN} = 3.6V, V_{OUT} = 1.2V	--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Timing						
Regulator Start-Up Delay Time	t_{DLY_SU}	V_{IN} = 3.6V, EN = GND to V_{IN}, V_{OUT} starts switching, T_J = –40°C to 125°C (Note 7)	--	500	1100	µs
Soft-Start Time	t_{SS}	From V_{OUT} = 0V to 95% of V_{OUT} nominal, T_J = –40°C to 125°C (Note 7)	--	120	500	µs
V_{OUT} Level Setup Time	t_{SU_VOUT}	To setup V_{OUT} level ready	--	400	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Input (EN and RSEL/MODE Inputs)						
Input Voltage Logic High	V_{IH}	V_{IN} = 1.8V to 5.5V, T_J = –40°C to 125°C (Note 7)	0.8	--	--	V
Input Voltage Logic Low	V_{IL}	V_{IN} = 1.8V to 5.5V, T_J = –40°C to 125°C (Note 7)	--	--	0.4	V
RSEL/MODE Pin Input Bias Current	I_{IN_MODE}	V_{IN} = 5.5V, EN = high, T_J = –40°C to 125°C (Note 7)	--	10	25	nA
EN Pin Leakage Current	I_{EN_LK}	T_J = –40°C to 85°C (Note 7), EN = high	--	10	25	nA
Internal Pull-Down Resistance	R_{PD}	E_N pin to GND	--	500	--	kΩ

Note 7. This specification is guaranteed by design.

14 Typical Application Circuit

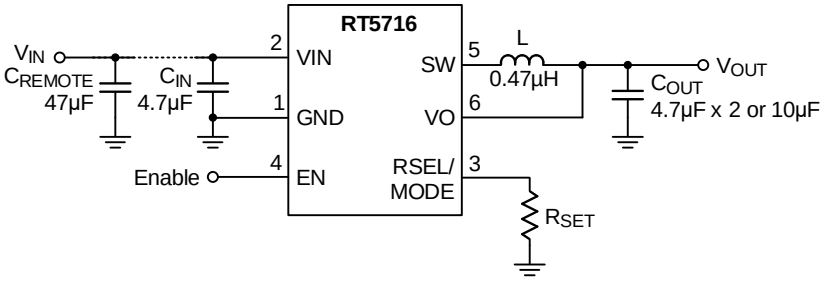
14.1 TWL-CSP-6B 0.69x1.04 (BSC)



Reference	Part Number	Value	Package	Manufacturer
CIN	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
COUT	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
	GRM155R60J106ME15D	10µF/6.3V/X5R	0402	Murata
CREMOTE (Note 8)	GRM21BR60J476ME11L	47µF/6.3V/X5R	0805	Murata
L (For 1.5MHz)	DFE201610E-1R0M=P2	1µH	0806	Murata
L (For 4MHz)	DFE18SANR47MG0L	0.47µH	0603	Murata
RSET	Resistor E96 series 1%, TC ±200ppm	See Table 1. Output Voltage Setting	--	--

Note 8. CREMOTE is an additional input capacitor that is not essential for normal operation. However, it can be utilized to minimize input voltage ripple.

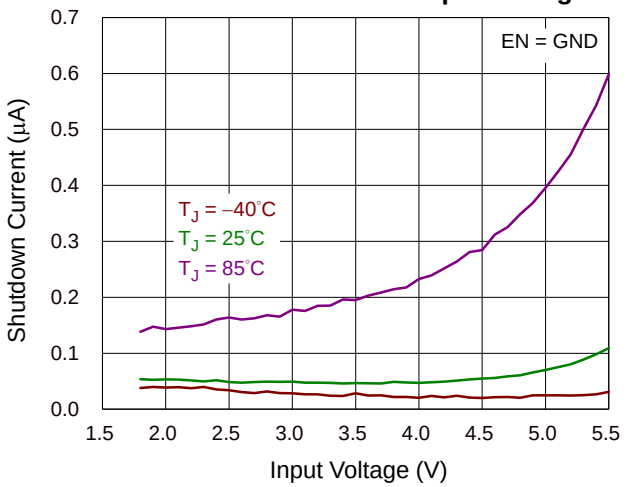
14.2 WDFN-6L 1.5x1.5 (FC)



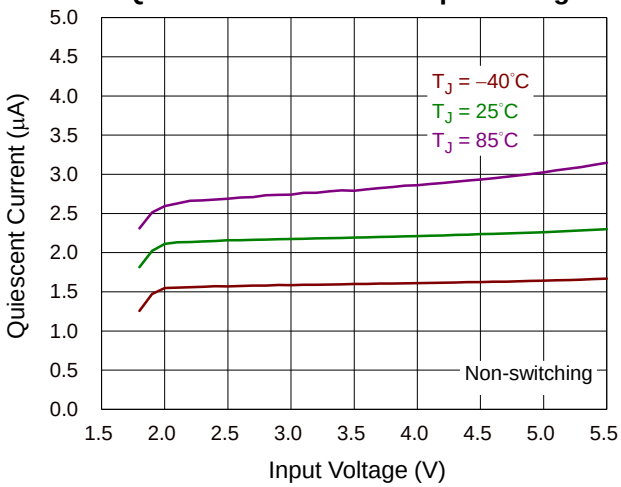
Reference	Part Number	Value	Package	Manufacturer
CIN	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
COUT	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
	GRM155R60J106ME15D	10µF/6.3V/X5R	0402	Murata
CREMOTE (Note 8)	GRM21BR60J476ME11L	47µF/6.3V/X5R	0805	Murata
L (For 1.5MHz)	DFE201610E-1R0M=P2	1µH	0806	Murata
L (For 4MHz)	DFE18SANR47MG0L	0.47µH	0603	Murata
RSET	Resistor E96 series 1%, TC ±200ppm	See Table 1. Output Voltage Setting	--	--

15 Typical Operating Characteristics

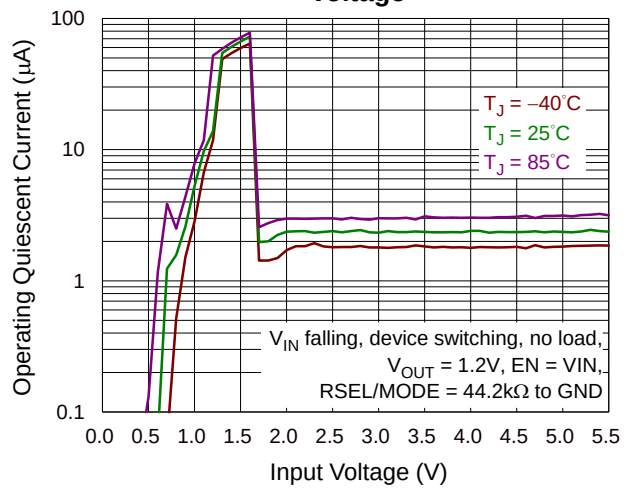
Shutdown Current vs. Input Voltage



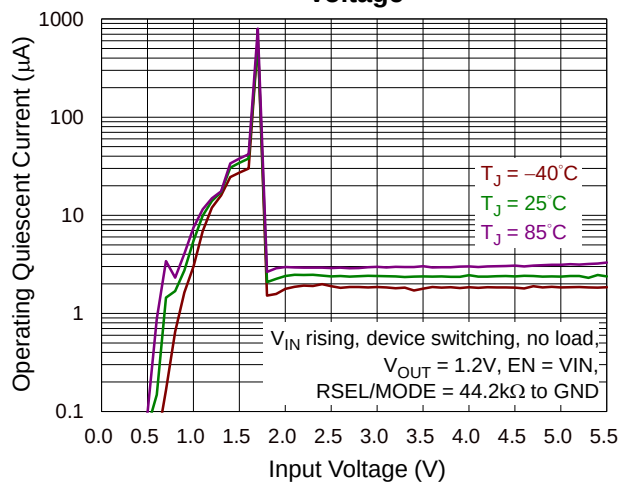
Quiescent Current vs. Input Voltage



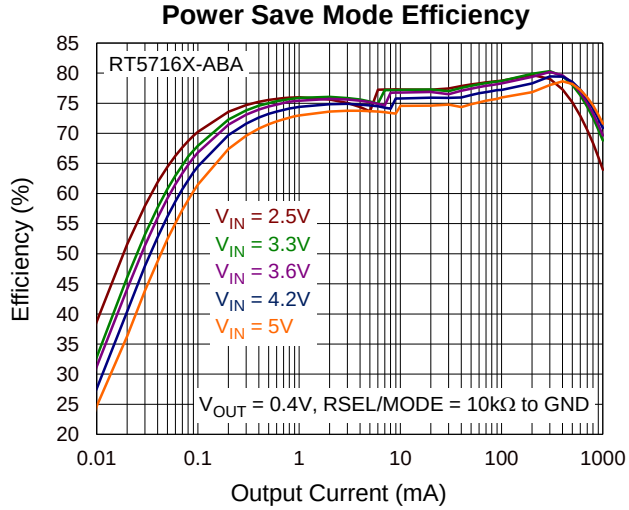
Operating Quiescent Current vs. Input Voltage



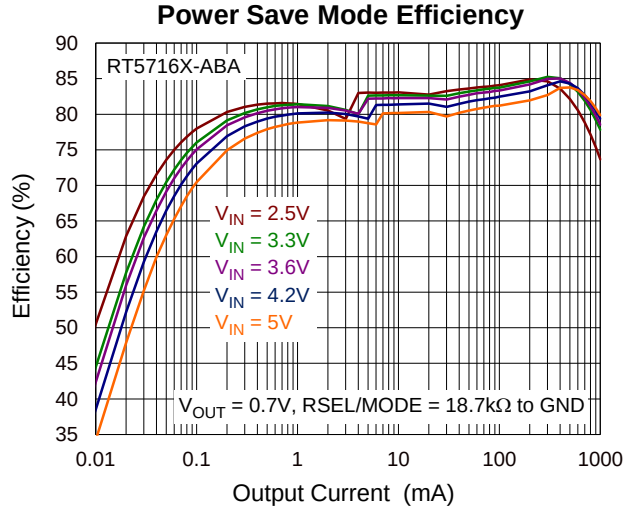
Operating Quiescent Current vs. Input Voltage



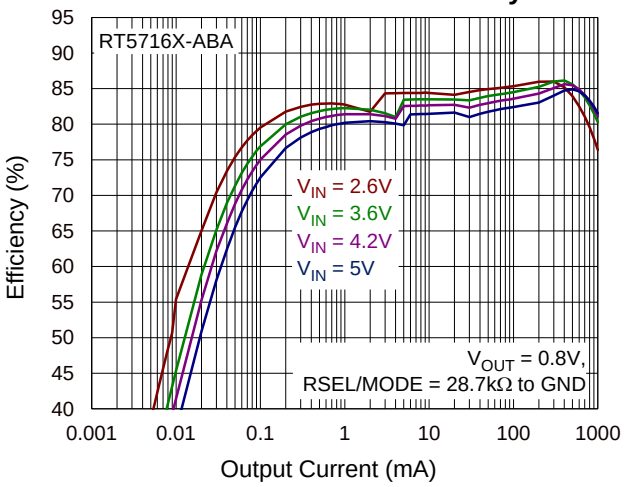
Power Save Mode Efficiency



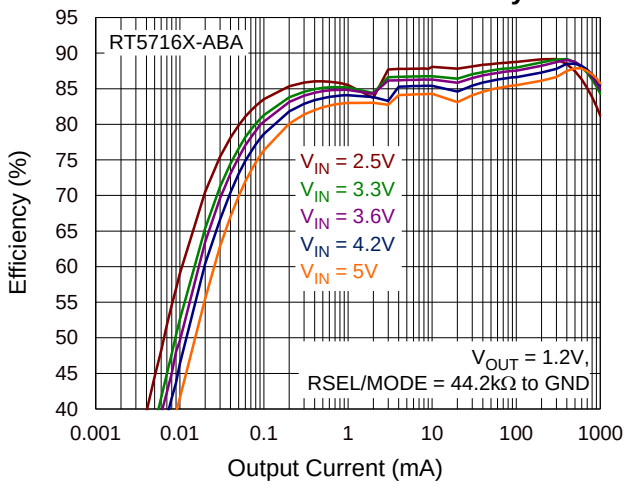
Power Save Mode Efficiency



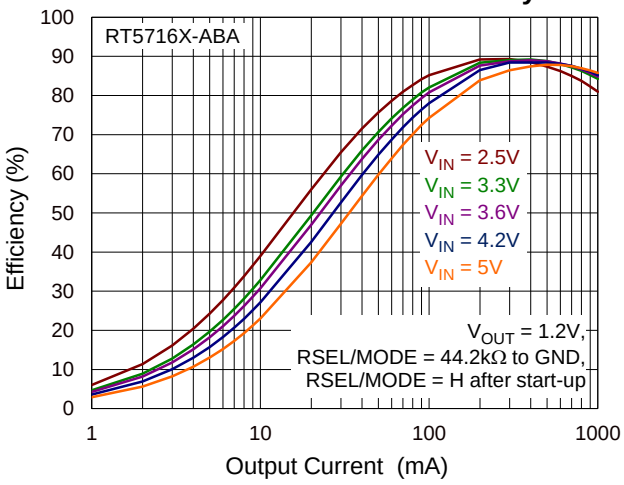
Power Save Mode Efficiency



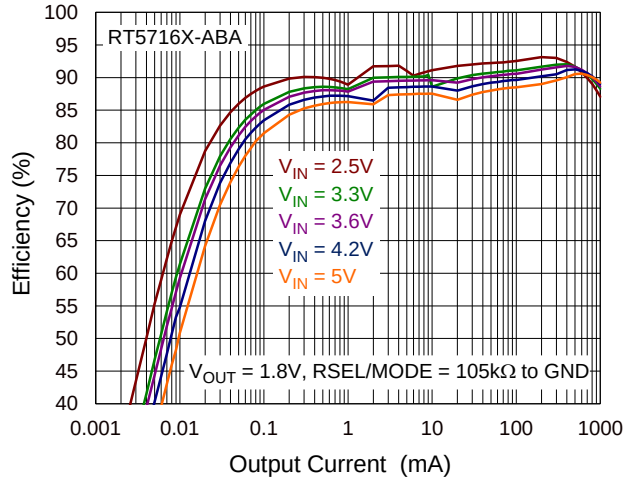
Power Save Mode Efficiency



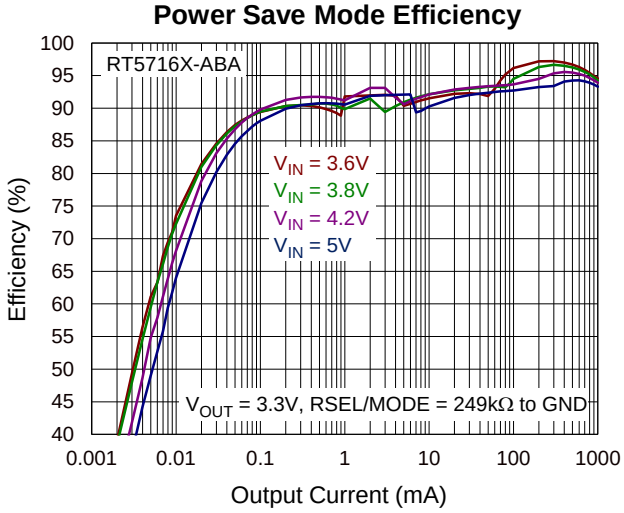
Forced PWM Mode Efficiency



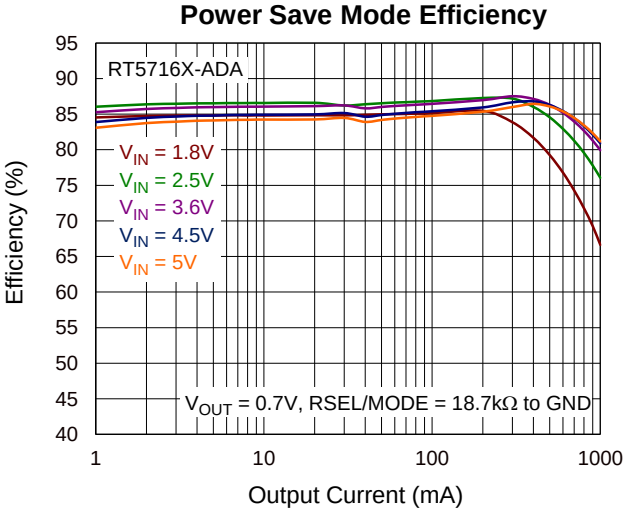
Power Save Mode Efficiency



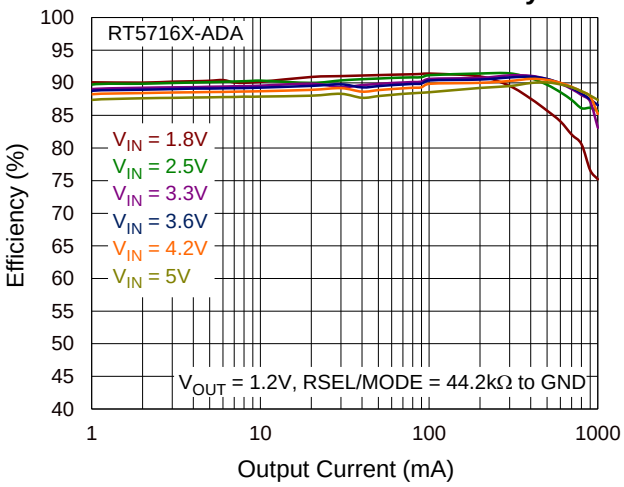
Power Save Mode Efficiency



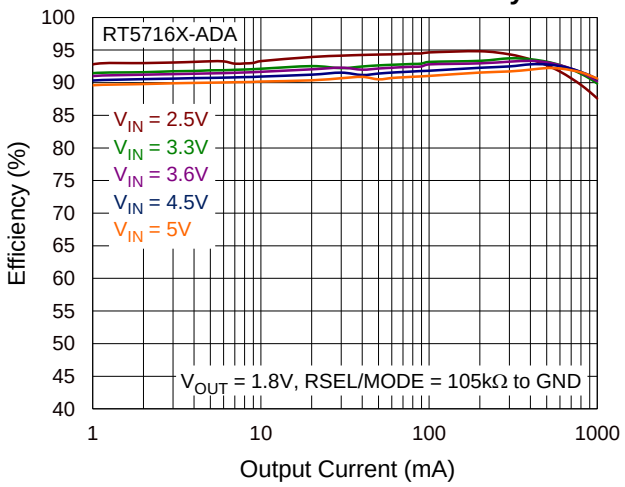
Power Save Mode Efficiency



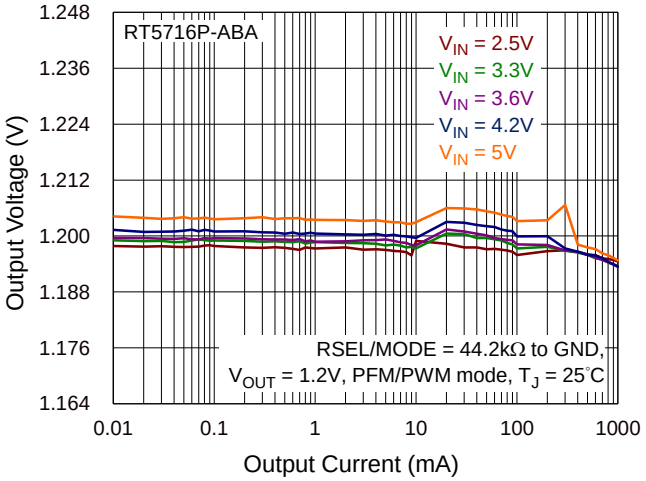
Power Save Mode Efficiency



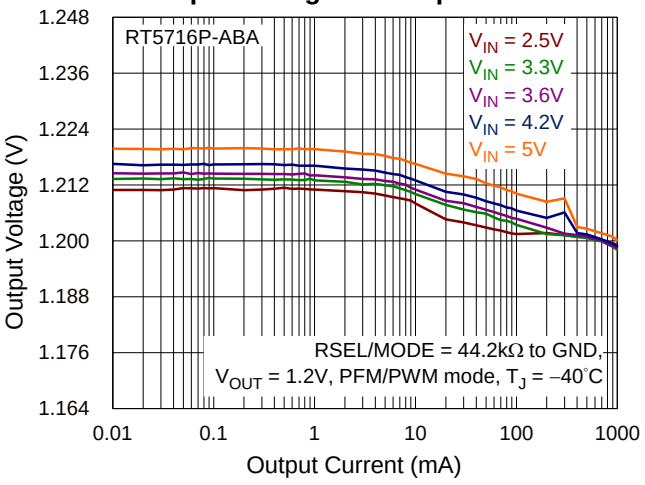
Power Save Mode Efficiency



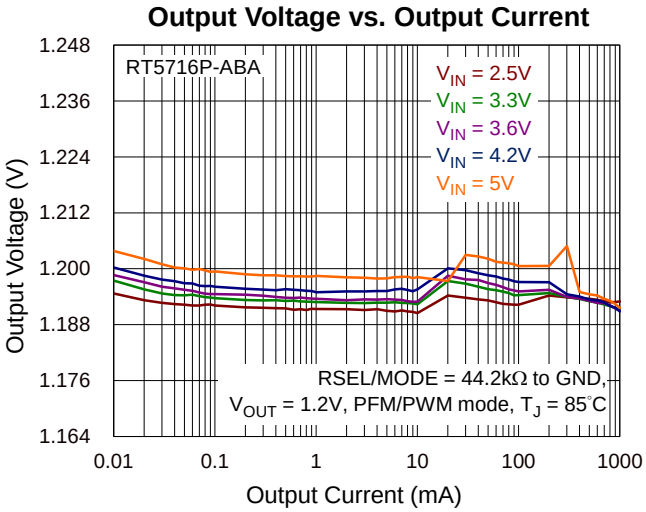
Output Voltage vs. Output Current



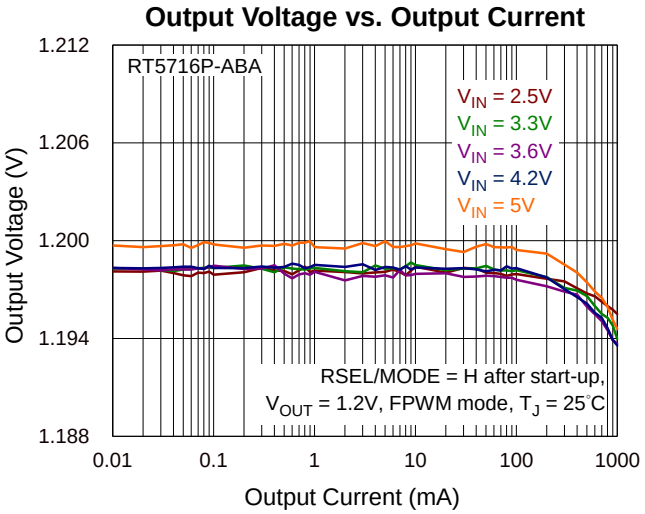
Output Voltage vs. Output Current



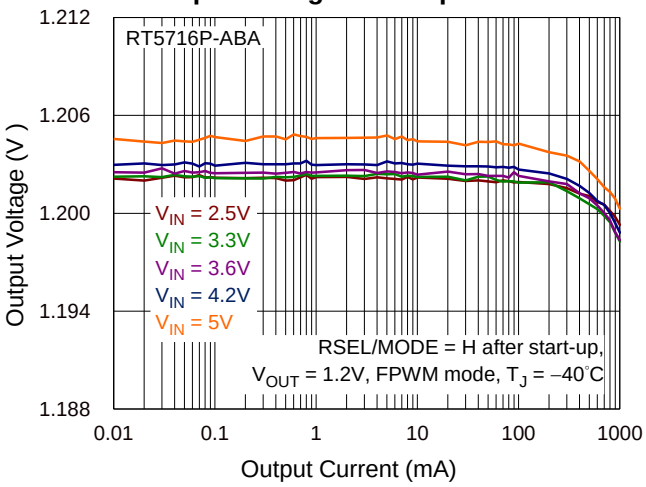
Output Voltage vs. Output Current



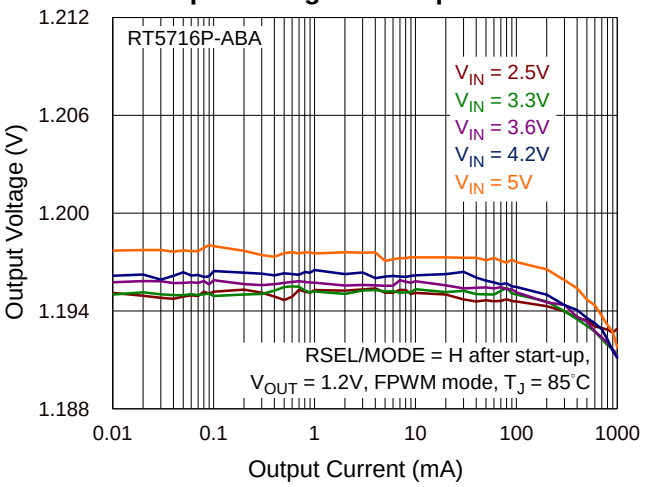
Output Voltage vs. Output Current



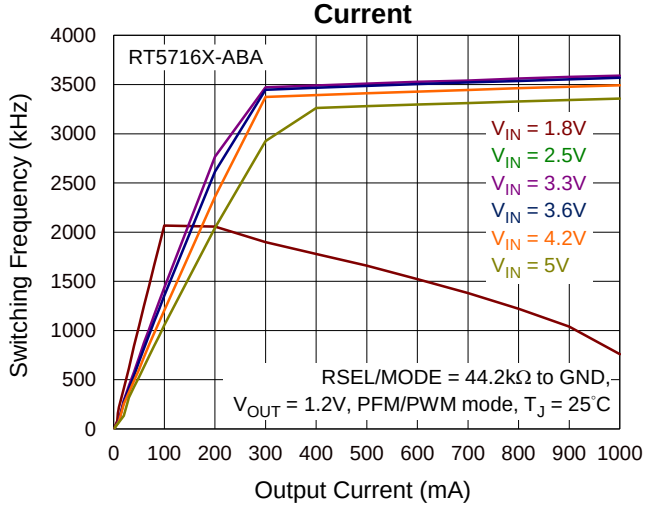
Output Voltage vs. Output Current



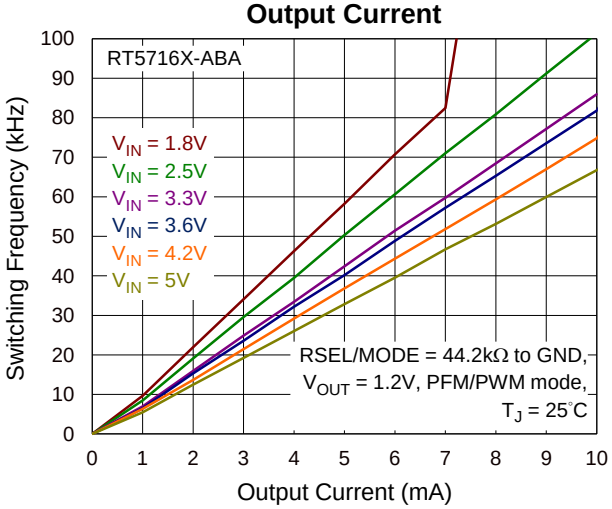
Output Voltage vs. Output Current



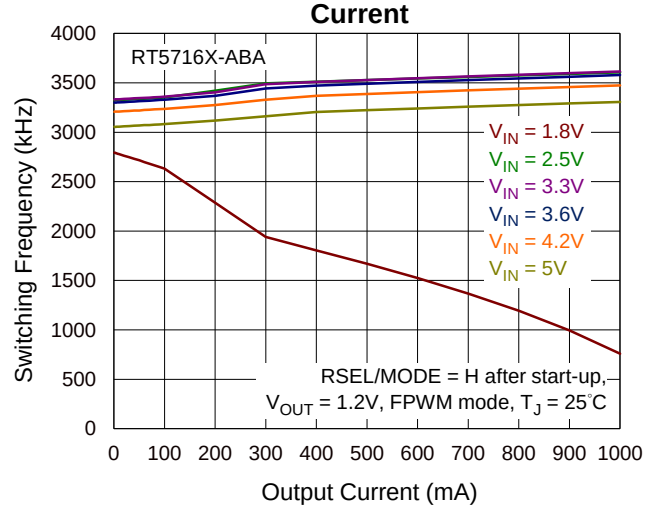
Switching Frequency vs. Output Current



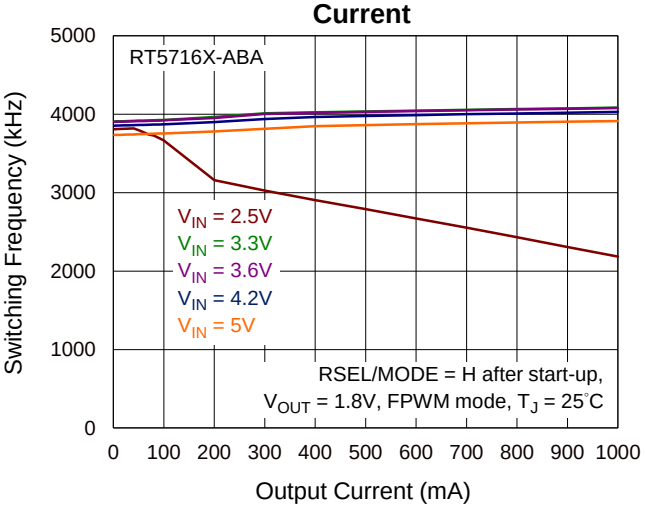
Switching Frequency (Zoom In) vs. Output Current



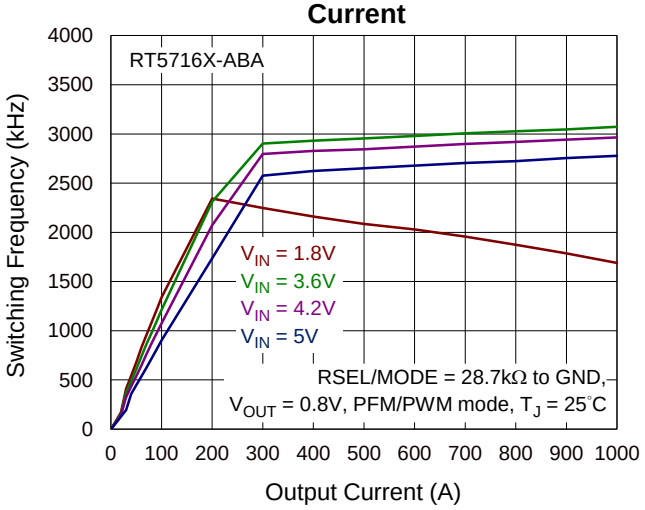
Switching Frequency vs. Output Current



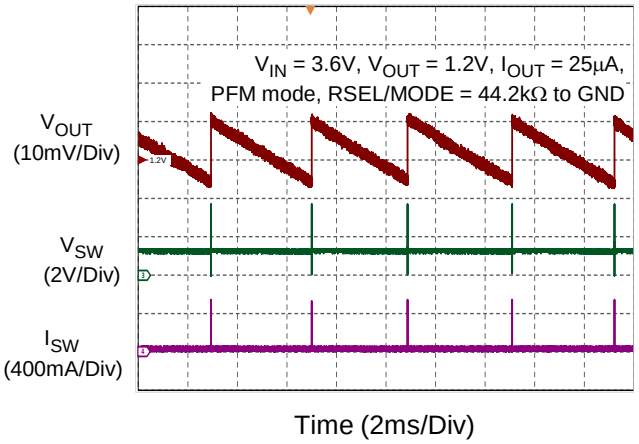
Switching Frequency vs. Output Current



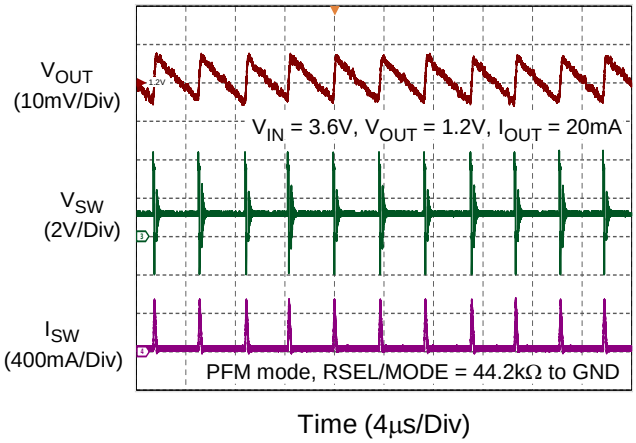
Switching Frequency vs. Output Current



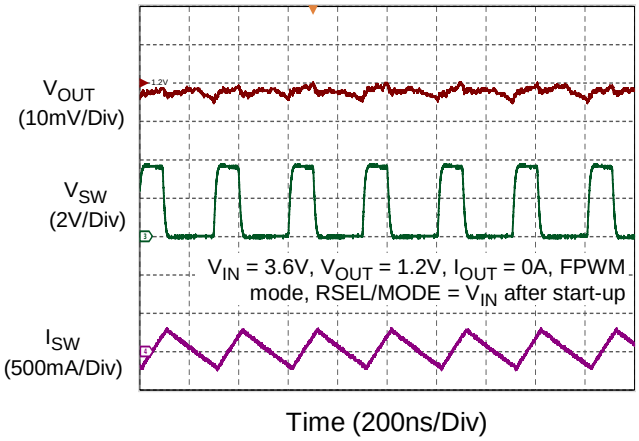
Typical Operation Power Save Mode



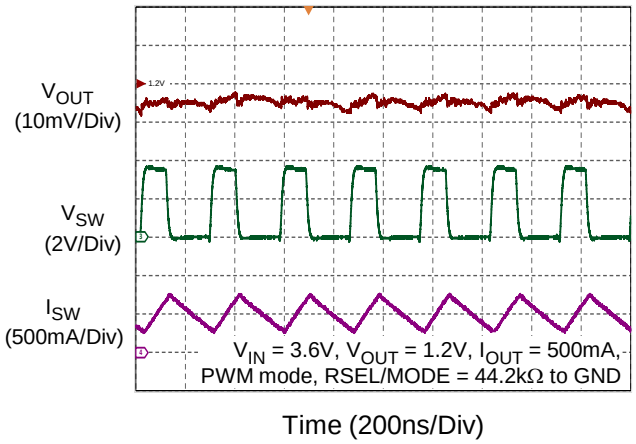
Typical Operation Power Save Mode



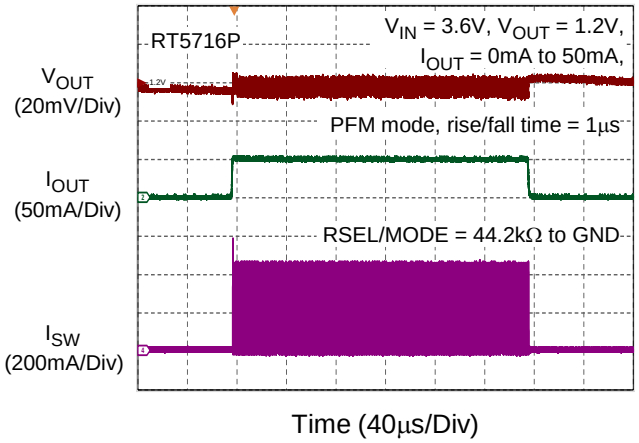
Typical Operation Forced PWM Mode



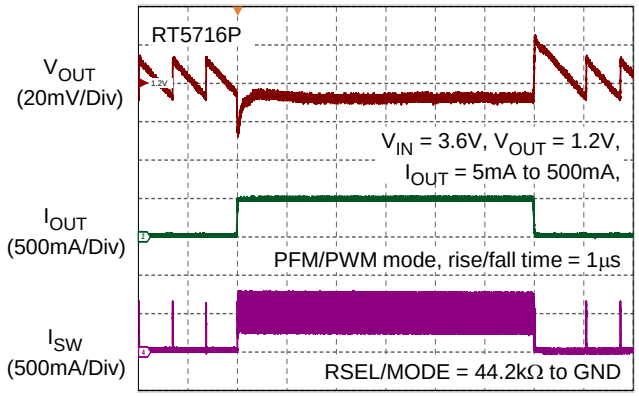
Typical Operation PWM Mode



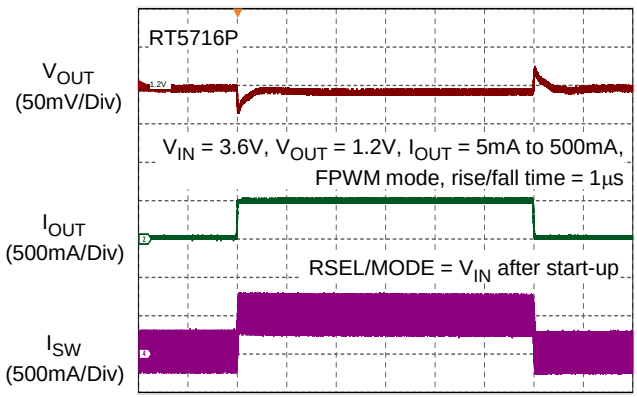
Load Transient Power Save Mode



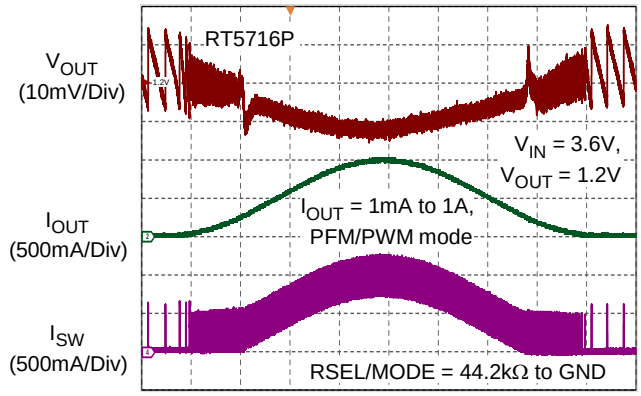
Load Transient Power Save Mode



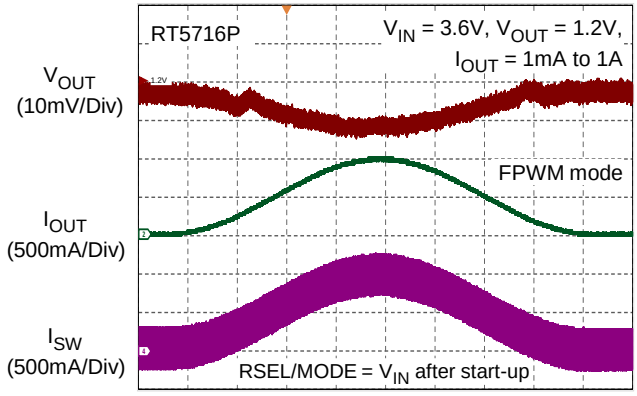
Load Transient Forced PWM Mode



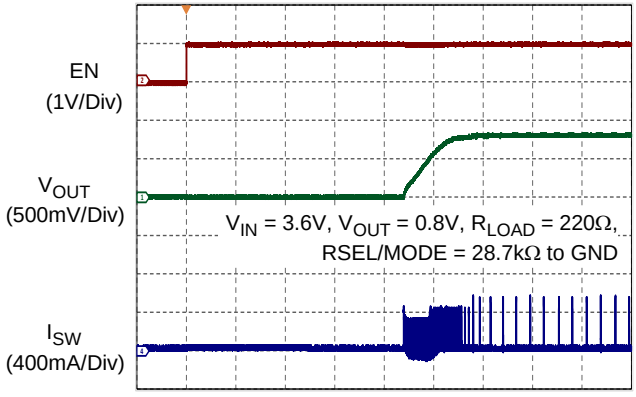
AC Load Sweep Power Save Mode



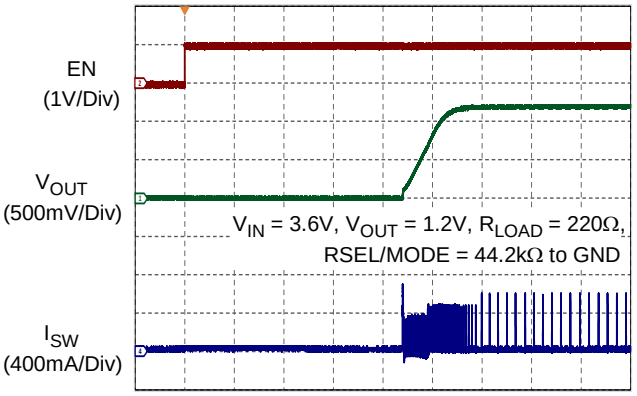
AC Load Sweep Forced PWM Mode



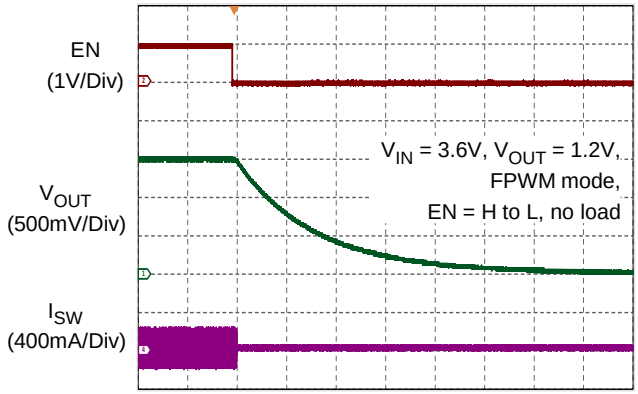
Start-Up



Start-Up



Output Discharge



16 Operation

The RT5716 is a high switching frequency synchronous step-down converter, with an input voltage range from 1.8V to 5.5V. It provides 16 selectable output voltage levels by connecting a resistor between RSEL/MODE pin and GND. The PFM design maintains high efficiency during light loads. While at higher load conditions, the device automatically switches to PWM. In shutdown mode, the device is disabled, which is excellent for reducing power consumption. To prevent damaging by abnormal operations, the protection mechanisms include Undervoltage-Lockout (UVLO), Over-Temperature Protection (OTP), and Overcurrent Protection (OCP).

16.1 Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the logic-high threshold, the IC enters normal operation. When the EN pin is set to low, the device transitions to shutdown mode. In shutdown mode, the converter stops switching, the internal control circuitry turns off, and the discharge function is triggered.

The EN low level time must be longer than 200μs for the internal circuit reset time.

16.2 Undervoltage-Lockout Protection (UVLO)

To protect the chip from operating at insufficient supply voltage, UVLO is required. When the input voltage is lower than the UVLO falling threshold, the device will be locked out.

16.3 100% Duty Cycle Operation

The converter enters 100% duty cycle operation once the input voltage decreases and the difference between the input and output voltage is lower than V_{TH_100-}. The output voltage follows the input voltage minus the voltage drop across the internal P-MOSFET and the inductor. Once the input voltage increases and reaches the 100% mode exit threshold, V_{TH_100+}, the converter returns to normal switching operation. See Figure 1.

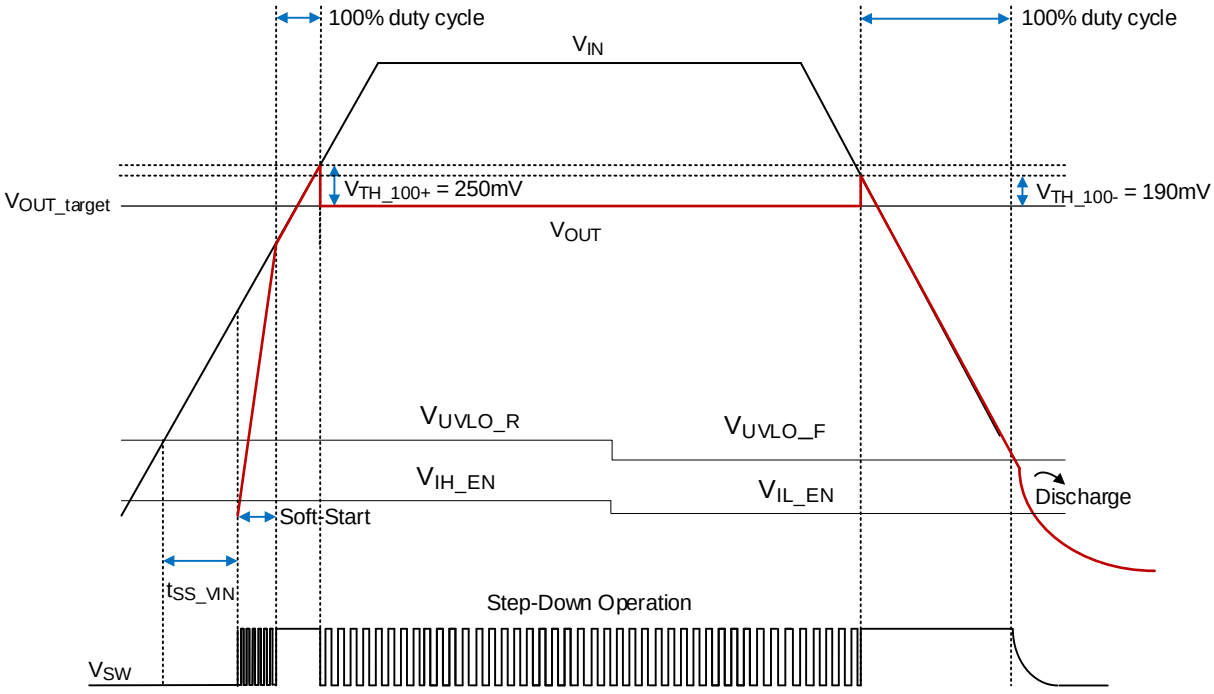


Figure 1. Auto Bypass Mode

16.4 Over-Temperature Protection (OTP)

When the junction temperature exceeds the OTP threshold, the IC will shut down the switching operation. Once the junction temperature cools down and falls below the OTP lower threshold, the converter will automatically resume switching.

16.5 Overcurrent Protection and Short Circuit Protection

The OCP and SCP functions are implemented by high-side MOSFET and low-side MOSFET. When the inductor current reaches the peak current-limit threshold, the high-side MOSFET will be turned off. The low-side MOSFET turns on to discharge the inductor current until it falls below the valley current-limit threshold. After peak current limit triggered, the maximum inductor current is determined by the inductor current rising rate and the response delay time of the internal network.

During the OCP and SCP period, the output voltage drops below the set threshold (0.2V typical), and the current limit value is reduced to a low current limit level to lower the device loss, reduce the heat and prevent further damage to the chip.

Due to internal propagation delay (t_{DLY_LIM} = 50ns), the actual inductor current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{Current\ limit\ peak} = I_{LIM\_PEAK} + \frac{(V_{IN}-V_{OUT})}{L} \times t_{DLY\_LIM}$$

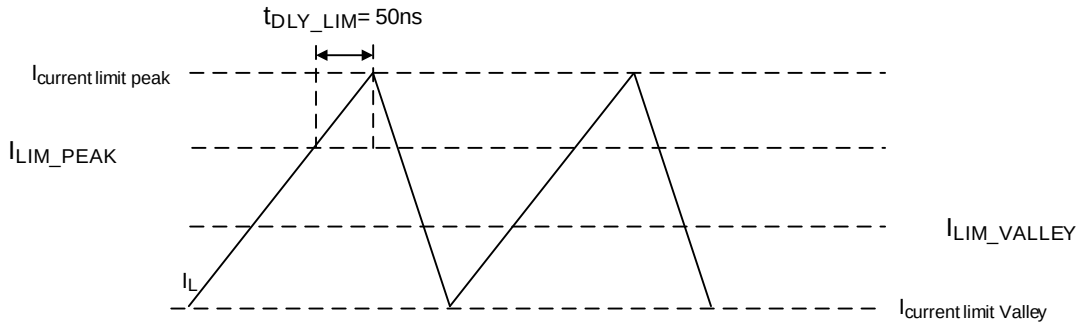


Figure 2. Current Limit

16.6 Pulse Frequency Modulation and Ton Extend Mode

In PFM mode, the converter does not switch at a fixed frequency as it does in PWM mode. Instead, it detects the voltage of VOUT. When the voltage is lower than the set value, the high-side MOSFET turns on. The turn-on time of the high-side MOSFET is calculated based on the frequency, VIN, and VOUT. After the high-side MOSFET turns off, the low-side MOSFET turns on until the inductor current reaches zero.

PFM operation reduces the converter's switching frequency to very low values, typically down to a few kilohertz, during light load conditions. This reduction in switching frequency helps minimize switching losses, significantly increasing the light load efficiency of the converter. Furthermore, in the RT5716X-XAA and RT5716X-XBA at ultra-light load, the high-side MOSFET on-time is extended to further reduce the switching frequency and improve overall efficiency.

16.7 Output Voltage Selection

The RT5716 provides one fixed and 16 selectable levels of V_{OUT} which can be set with a single external resistor connected between the RSEL/MODE pin and GND. The V_{OUT} level selector circuit starts to detect the value of the resistor once the converter is enabled, and the control circuitry is powered up. The V_{OUT} level is set during the V_{OUT} level setup time (t_{SU_VOUT}).

Table 1. Output Voltage Setting

Type	Output-1 (V)	Output-2 (V)	Output-3 (V)	Output-4 (V)	RSEL (kΩ) (Note 9)		
Level	0.4V to 3.3V	0.4V to 0.775V	0.8V to 1.55V	1.8V to 3.3V	Min	Typ	Max
0	3.3	0.7	1.2	1.8	Connected to GND (No resistor needed)		
1	0.4	0.4	0.8	1.8	9.9	10	10.1
2	0.58	0.425	0.85	1.9	12	12.1	12.2
3	0.6	0.45	0.9	2	15.2	15.4	15.6
4	0.7	0.475	0.95	2.1	18.5	18.7	18.9
5	0.75	0.5	1	2.2	23.5	23.7	23.9
6	0.8	0.525	1.05	2.3	28.4	28.7	29
7	1.1	0.55	1.1	2.4	36.1	36.5	36.9
8	1.2	0.575	1.15	2.5	43.8	44.2	44.6
9	1.3	0.6	1.2	2.6	55.6	56.2	56.8
10	1.5	0.625	1.25	2.7	67.4	68.1	68.8
11	1.6	0.65	1.3	2.8	85.7	86.6	87.5
12	1.8	0.675	1.35	2.9	104	105	106.1
13	1.9	0.7	1.4	3	131.7	133	134.3
14	2.5	0.725	1.45	3.1	160.4	162	163.6
15	3	0.75	1.5	3.2	203	205	207.1
16	3.3	0.775	1.55	3.3	≥249	≥249	≥249

Note 9. 6 resistor series, 1% accuracy, temperature coefficient better than or equal to ±200 ppm/°C.

17 Application Information

(Note 10)

The basic RT5716 application circuit is shown in the Typical Application Circuit. This section discusses the external component selection and the considerations of practical applications by referring to the electrical characteristics.

17.1 Inductor Selection

The recommended power inductor is 0.47μH for I_{OUT} = 600mA and I_{OUT} = 1A. The inductor saturation current rating needs to be carefully chosen to follow the overcurrent protection design considerations. In applications, it is necessary to select an inductor with low DCR to provide good performance and efficiency.

17.2 C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2 x V_{OUT}, where I_{RMS} = I_{OUT}/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. It is advisable to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

17.3 Output Voltage in PFM Mode

Since the RT5716 adopts valley control in PFM mode, which means that the switching node (SW) starts to switch when the output voltage drops to the valley voltage (see Figure 3), the average output voltage ($VOUT_{avg}$) can be calculated by Equation 1:

$$V_{OUT\_avg} = V_{OUT\_valley} + \frac{1}{2} V_{OUT\_ripple} \quad (1)$$

where V_{OUT_valley} is the valley voltage, and V_{OUT_ripple} is the output voltage ripple.

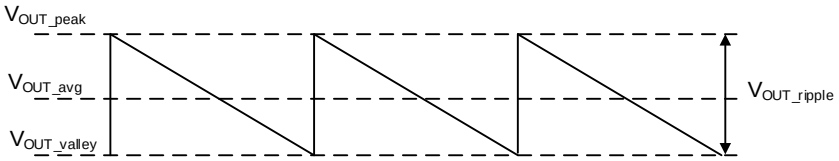


Figure 3. Output Voltage Waveform

The output voltage ripple originates from the excessive charge, ΔQ, stored in the inductor (see Figure 4) and ΔQ can be calculated by Equation 2:

$$\Delta Q = \frac{1}{2} \times \Delta i_L \times t \times k \quad (2)$$

where Δi_L is the inductor current ripple, t is the switching period in CCM operation and k is a coefficient dependent on the nominal switching frequency. Since the on-time of the high-side MOSFET will be extended when the nominal switching frequency is 4MHz, k will be 1.4; however, it will be disabled when the nominal switching frequency is 1.5MHz, resulting in k being 1.

The inductor current ripple can be obtained by Equation 3:

$$\Delta i_L = \frac{V_{IN} - V_{OUT}}{L} \times t_1 \quad (3)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, and t_1 is the on-time of high-side MOSFET. t_1 can be calculated by Equation 4:

$$t_1 = \frac{V_{OUT}}{V_{IN}} \times t \times k \quad (4)$$

The output voltage ripple can be calculated by Equation 5:

$$VOUT_{ripple} = \frac{\Delta Q}{C_{OUT}} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT} \times t^2 \times k^2}{2 \times V_{IN} \times L \times C_{OUT}} \quad (5)$$

where t is 250ns. When f_{SW} is 4 MHz; t is 660ns when f_{SW} is 1.5MHz.

Since the valley voltage is fixed, the average output voltage depends on the output voltage ripple. Additionally, the larger the output capacitance, the smaller the output voltage ripple. As a result, the average output voltage with larger output capacitance is lower due to the reduced voltage ripple, compared to the average output voltage with smaller output capacitance.

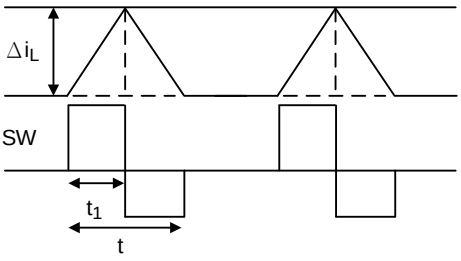


Figure 4. Inductor Current in DCM Mode

17.4 Power Sequence

There are three common power-on device scenarios:

1. EN is pulled high after VIN has been established.
2. EN and VIN are established at same time.
3. VIN is pulled high after EN has been established.

There will be two types of boot-up times. One is to enable the system after VIN has been established, and after a period of t_{SS_EN}, the device boots up. The other is that EN has been established before VIN is pulled high, and after a period of delay, the device boots up.

There are two common power-off scenarios:

1. When VIN is at a high level, the EN is pulled low, and the device is powered off by EN.

2. When VIN is pulled low, the device is powered off by UVLO after t_{UVLO_DT}. In this case, a slew rate of > 600μs is recommended when VIN is powered off.

To ensure that the device boots up as shown in Figure 5, it is recommended to power VIN from 0V and have a 100ms interval between each power-up.

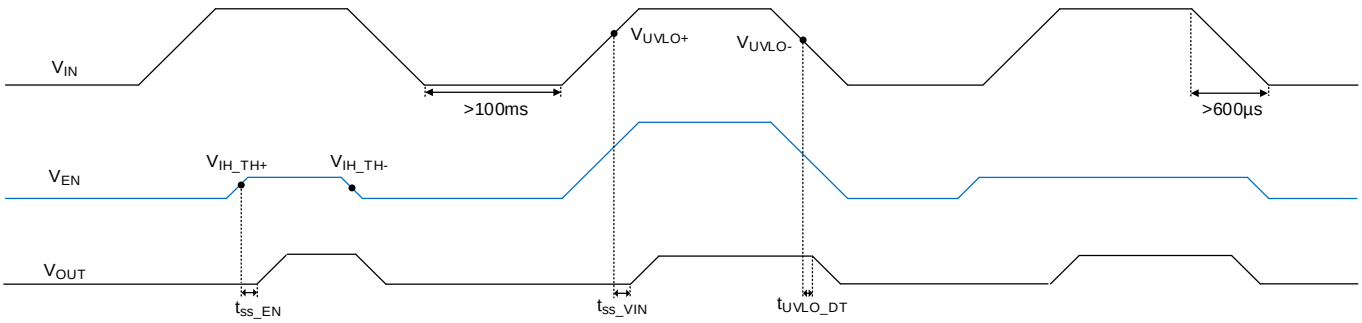


Figure 6. Power-On/Off Sequence

17.5 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a TWL-CSP-6B 0.69x1.04 (BSC) package, the thermal resistance, θ_{JA}, is 96.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WDFN-6L 1.5x1.5 (FC) package, the thermal resistance, θ_{JA}, is 145.34°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (96.8°C/W) = 1.03W for a TWL-CSP-6B 0.69x1.04 (BSC) package.

$P_{D(MAX)}$ = (125°C - 25°C) / (145.34°C/W) = 0.69W for a WDFN-6L 1.5x1.5 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

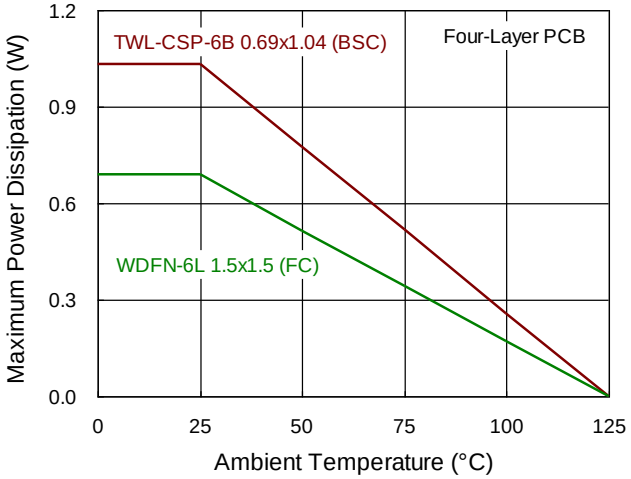


Figure 3. Derating Curves of Maximum Power Dissipation

17.6 Layout Considerations

For high-frequency switching power supplies, the PCB layout is crucial to get good regulation, high efficiency and stability. The following guidelines can help achieve a better PCB layout.

- For good regulation, place the power components as close as possible. The traces should be wide and short, especially for the high-current loop.
- Shorten the SW node trace length and make it wide.

Table 2. Protection Trigger Condition and Behavior

Protection Type	Threshold Refer to Electrical Characteristics	Protection Method	Reset Method
Positive Inductor Peak Current Limit for I_{OUT} = 1.2A	I_{SW} > 1.2A (Typical)	Turn off UG MOS	I_{SW} < 0.86A (Typical)
Positive Inductor Peak Current Limit for I_{OUT} = 1.7A	I_{SW} > 1.7A (Typical)		I_{SW} < 1.36A (Typical)
UVLO	V_{IN} < V_{UVLO_F} (Typical)	Shutdown	V_{IN} > V_{UVLO_R} (Typical)
OTP	T_J > 150°C (Typical)	Shutdown	T_J < 130°C (Typical)

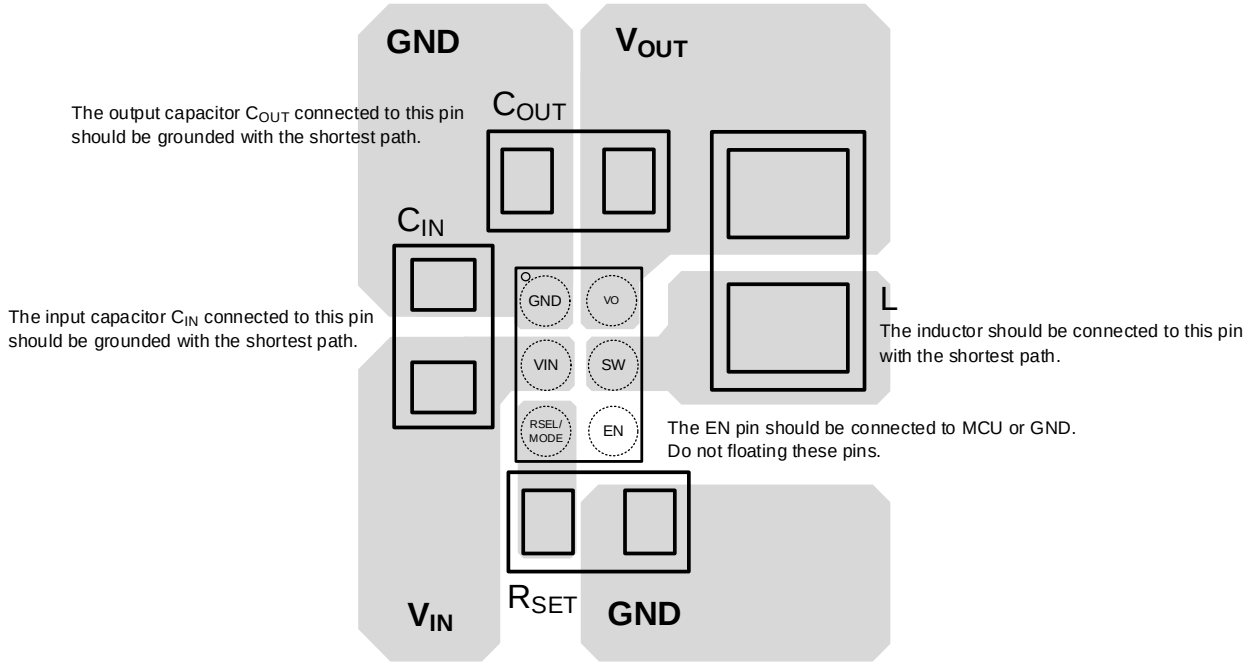


Figure 7. PCB Layout Guide for TWL-CSP-6B 0.69x1.04 (BSC) Package

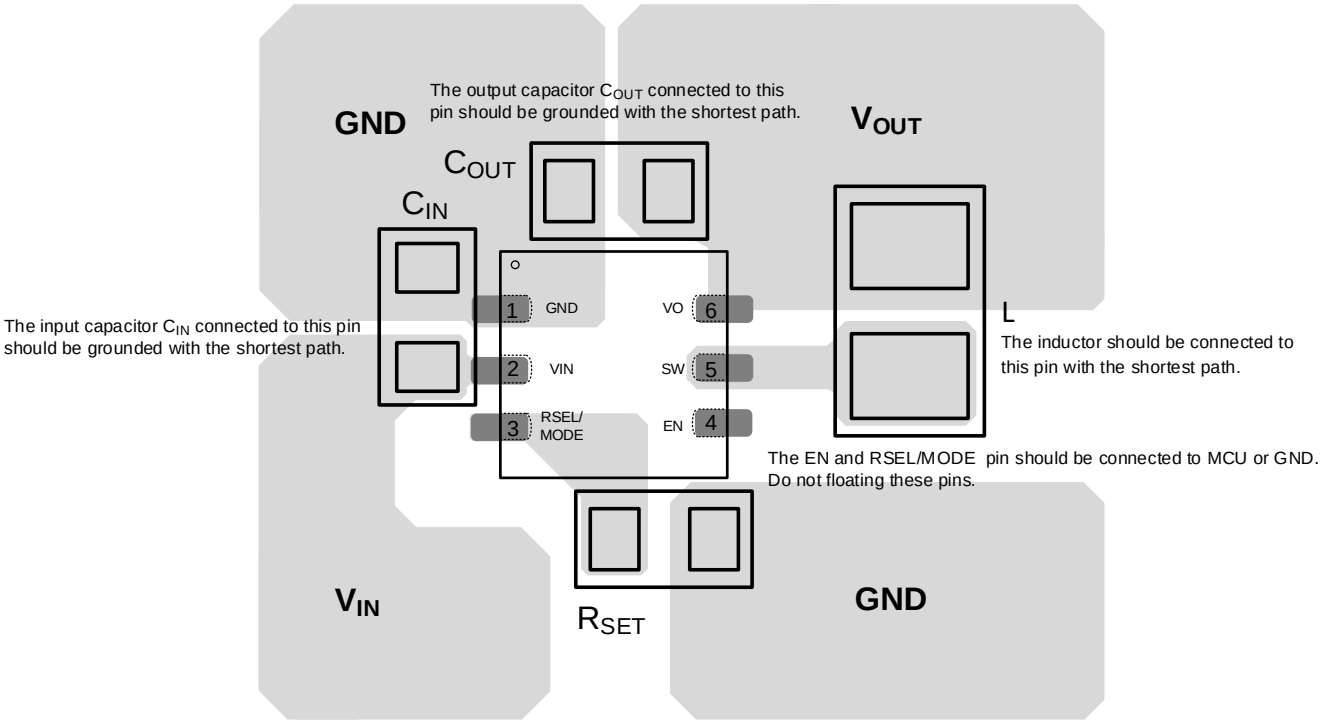
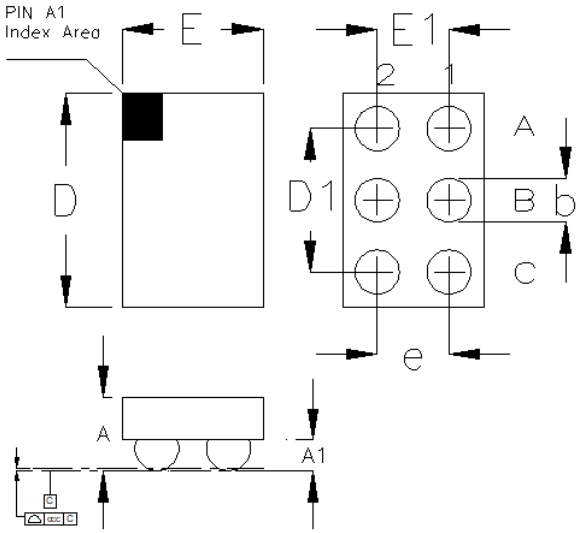


Figure 8. PCB Layout Guide for WDFN-6L 1.5x1.5 (FC) Package

Note 10. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension

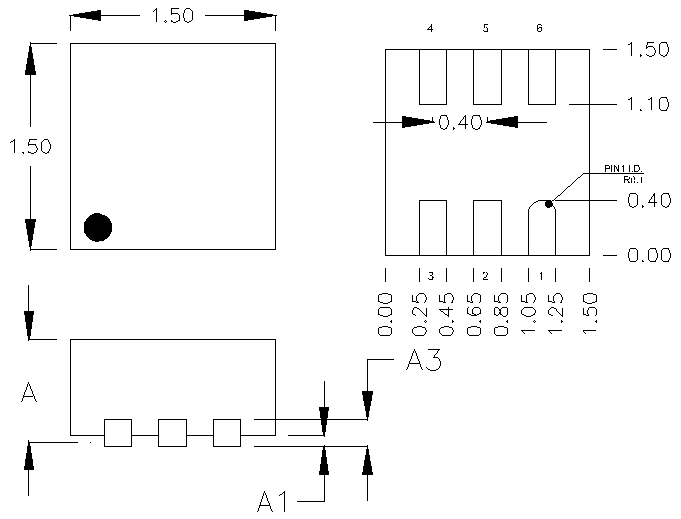
18.1 TWL-CSP-6B 0.69x1.04 (BSC)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.320	0.400	0.013	0.016
A1	0.120	0.180	0.005	0.007
b	0.190	0.240	0.007	0.009
D	1.010	1.070	0.040	0.042
D1	0.700		0.028	
E	0.660	0.720	0.026	0.028
E1	0.350		0.014	
e	0.350		0.014	
ccc	0.020		0.001	

6B TWL-CSP 0.69x1.04 Package

18.2 WDFN-6L 1.5x1.5 (FC)

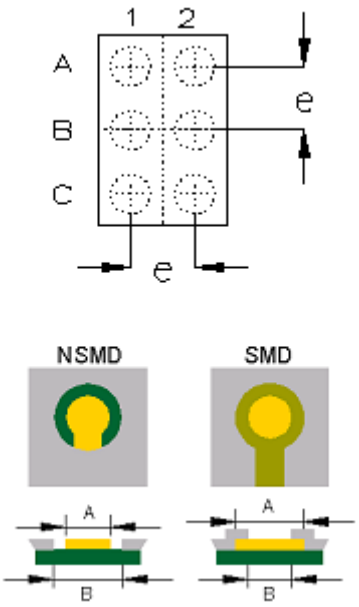


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

W-Type 6L DFN 1.5x1.5 Package (FC)

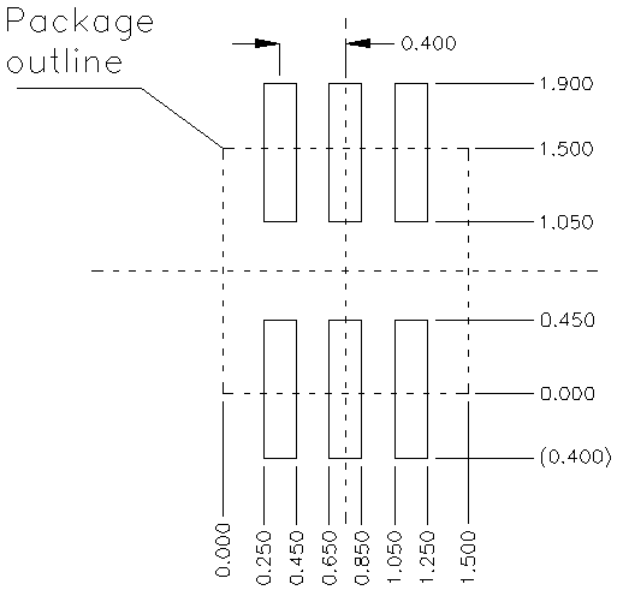
19 Footprint Information

19.1 TWL-CSP-6B 0.69x1.04 (BSC)



Package	Number of Pins	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
TWL-CSP0.69x1.04-6	6	NSMD	0.350	0.200	0.300	±0.025
		SMD		0.230	0.200	

19.2 WDFN-6L 1.5x1.5 (FC)

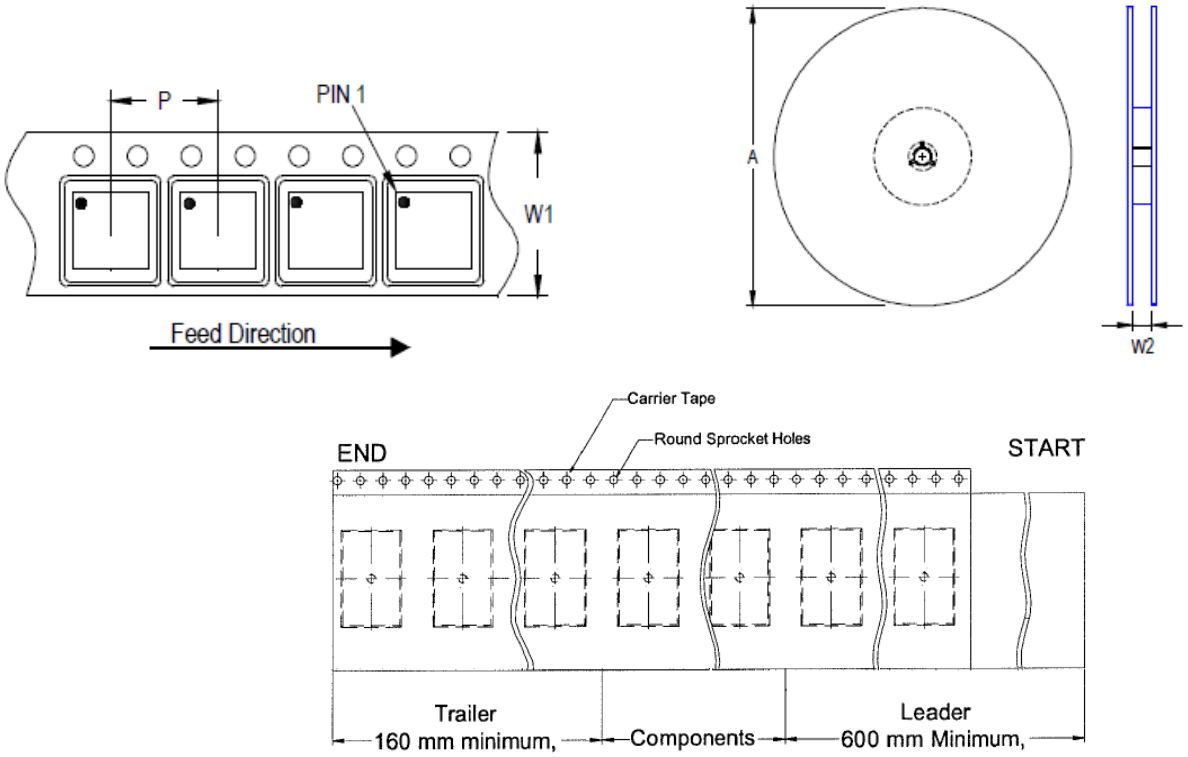


Package	Number of Pin	Tolerance
V/W/U/XDFN1.5x1.5-6(FC)	6	±0.05 mm

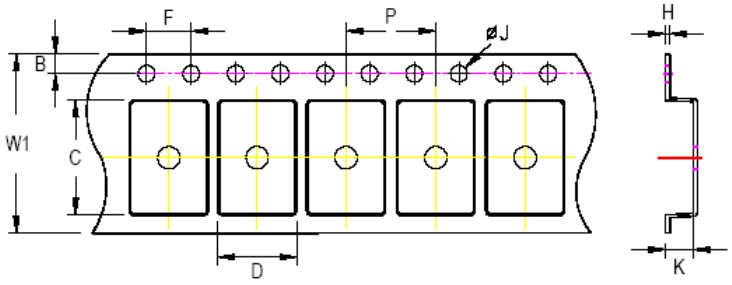
20 Packing Information

20.1 Tape and Reel Data

20.1.1 TWL-CSP-6B 0.69x1.04 (BSC)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 0.69x1.04	8	4	180	7	3,000	160	600	8.4/9.9

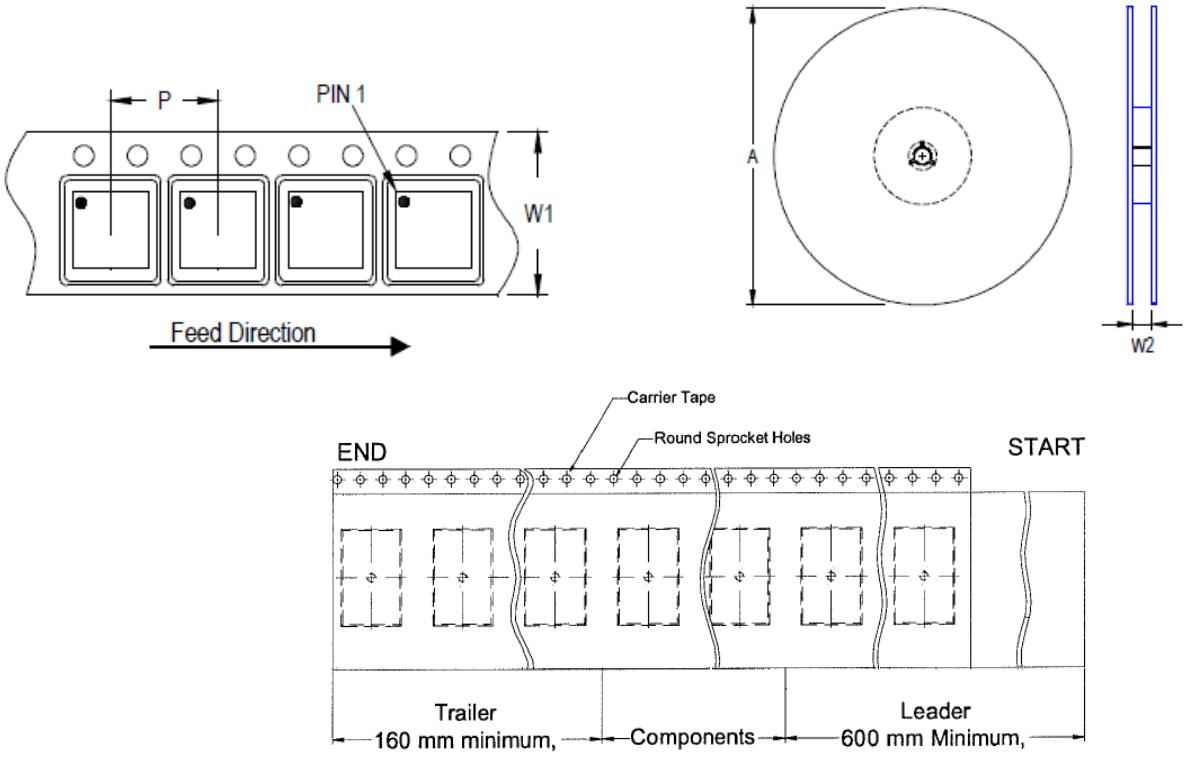


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

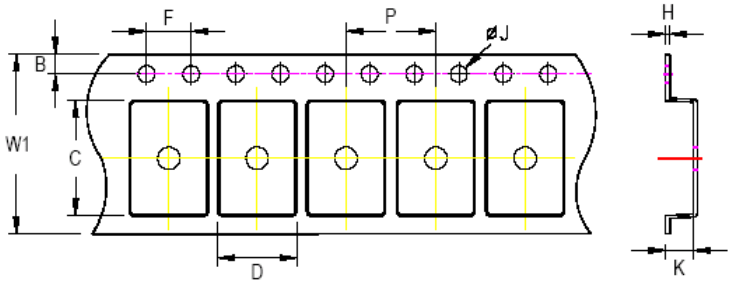
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.47mm	0.53mm	0.6mm

20.1.2 WDFN-6L 1.5x1.5 (FC)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 1.5x1.5	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.05mm	1.25mm	0.6mm

20.2 Tape and Reel Packing

20.2.1 TWL-CSP-6B 0.69x1.04 (BSC)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 0.69x1.04	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

20.2.2 WDFN-6L 1.5x1.5 (FC)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 1.5x1.5	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

21 Datasheet Revision History

Version	Date	Description	Item
00	2024/2/5	Final	
01	2024/10/17	Modify	*General Description on page 1* - Modified the notation of PFM *Ordering Information on page 1* - Updated description - Added note *Features on page 1* - Modified the notation of PSM and FPWM *Applications on page 1* - Removed Portable Information *Functional Table on page 2* - Added 1.5MHz option *Functional Pin Description on page 4* - Modified the description of the VO and VIN pins *Recommended Operating Conditions on page 6* - Updated the content *Electrical Characteristics on page 7, 8* - Modified the spec of Shutdown Current and Bias Current into VO Pin - Modified the test conditions of Load Regulation - Added the spec of Regulator Start-Up Delay Time *Typical Application Circuit on page 10, 11* - Added 1.5MHz option *Typical Operating Characteristics on page 13, 14* - Added 1.5MHz option *Operation on page 19, 20* - Modified the description of Section 16.4 and 16.6 *Application Information on page 22, 23, 24, 26* - Added Section 17.3 and 17.4 - Updated declaration *Packing Information on page 31, 32, 33, 34* - Updated packing information