1.8V to 5.5V, 0.6A/1A, 2.3μA IQ Step Down Converter 6-Pin, 0.35mm Pitch WCSP Package

General Description

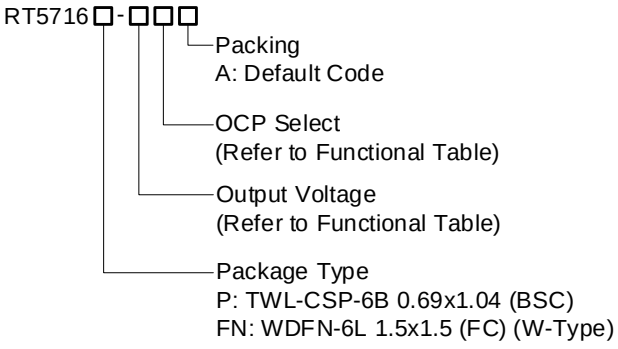
The RT5716 is a high switching frequency synchronous step-down converter with a quiescent current of 2.3μA. The device uses RBCOT (Ripple-Based Constant-On-Time) control to enhance load/line transient response to be optimized over a wide range of loads and output capacitors.

The RT5716 input voltage range is from 1.8V to 5.5V, making it suitable for battery applications. It provides 16 selectable output voltage levels by connecting the resistor between RSEL/MODE pin and GND. The PFM design can maintain high efficiency during the light load. At higher load conditions, the device automatically switches to PWM. The device can deliver up to 0.6/1A loading current. In shutdown mode, the supply current is typically 55nA, excellent in reducing power consumption.

The RT5716 is available in TWL-CSP-6B 0.69x1.04 (BSC) and WDFN-6L 1.5x1.5 (FC) packages that have the smallest packages for small size applications.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

Ordering Information



Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Features

- **4MHz Switching Frequency**
- **2.3μA Operating Quiescent Current**
- **Input Voltage Range: 1.8V to 5.5V**
- **16 Selectable Output Voltages by RSEL/MODE Pin and Fixed Output Voltage Without RSEL Setting**
- **RBCOT Control for Transient Response**
- **Selectable PSM and FPWM Mode**
- **Output Voltage Discharge**
- **OCP, OTP and UVLO Protection**
- **0.6A or 1A Loading Current**

Applications

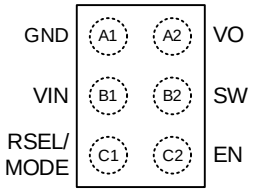
- Hand-Held Devices
- Portable Information
- Asset Tracking Devices
- Battery Powered Equipment
- Wearable Devices
- Internet of Things

Marking Information

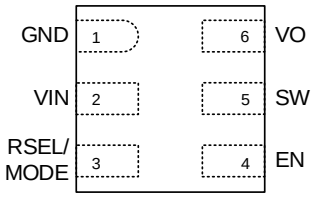
For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configuration

(TOP VIEW)



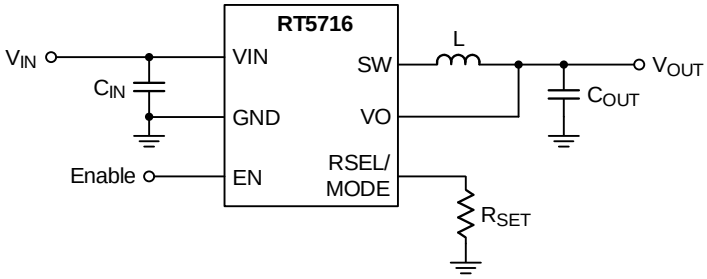
TWL-CSP-6B 0.69x1.04 (BSC)



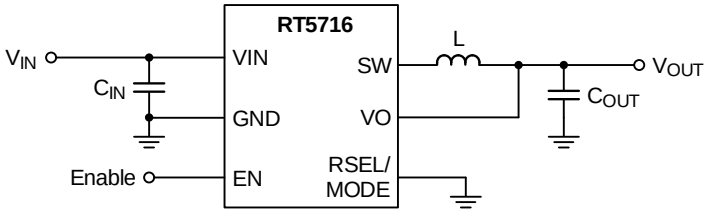
WDFN-6L 1.5x1.5 (FC)

Simplified Application Circuit

Adjustable V_{OUT} by RSET Setting



Fixed V_{OUT}



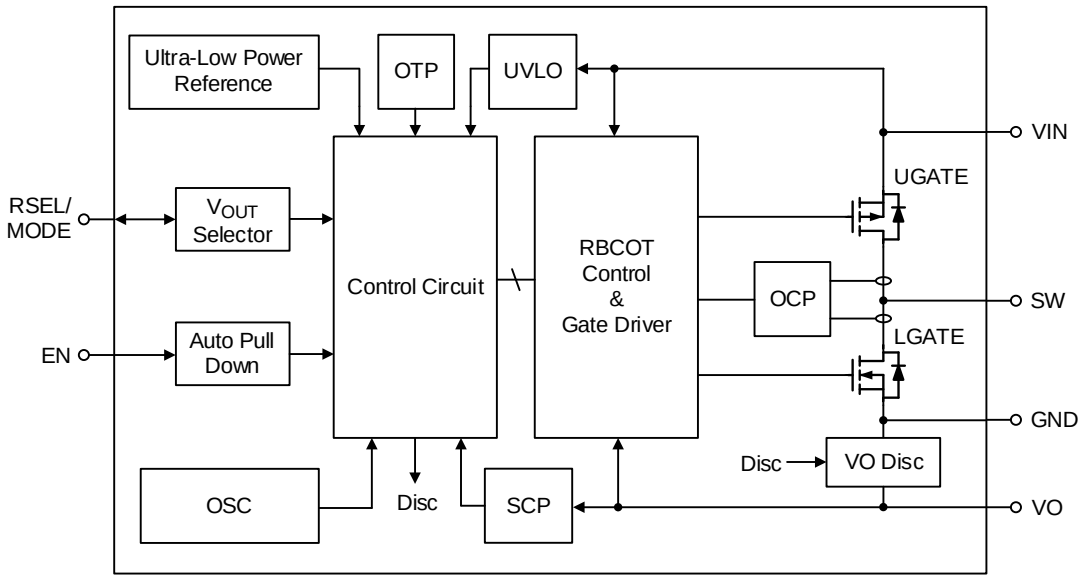
Functional Table

Output Voltage Setting Range		OCP Select	
A	Output-1, 0.4V to 3.3V	A	OCP Select 1 = 1.2A
B	Output-2, 0.4V to 0.775V in 25mV steps	B	OCP Select 2 = 1.7A
C	Output-3, 0.8V to 1.55V in 50mV steps		
D	Output-4, 1.8V to 3.3V in 100mV steps		

Functional Pin Description

Pin No.		Pin Name	Pin Function
TWL-CSP-6B 0.69x1.04 (BSC)	WDFN-6L 1.5x1.5 (FC)		
A1	1	GND	Device ground pin. This pin should be connected to input and output capacitors with the shortest path.
A2	6	VO	Output voltage feedback pin. This pin should be connected close to the output capacitor terminal for better voltage regulation. A minimum of 2μF and type 9.4μF ceramic capacitor should be connected to this pin with the shortest path.
B1	2	VIN	Supply input. A minimum of 0.5μF and type 4.7μF ceramic capacitor should be connected to this pin with the shortest path.
B2	5	SW	This pin is the connection between two build-in switches in the chip, which should be connected to the external inductor. The inductor should be connected to this pin with the shortest path.
C1	3	RSEL/ MODE	Connecting a resistor between RSEL/MODE and GND sets the VOUT level when the converter is enabled. Once the VOUT level has been decided, RSEL/MODE pin operates as an input. Pull low for PSM operation and pull high for FPWM operation. (There is no additional current path or capacitance greater than 30pF to GND during resistor-to-digital conversion.)
C2	4	EN	The chip enable input pin controls the operation of the device. When a high level voltage is applied, it enables the device, and when a low level voltage is applied, it turns the device off. It is important to ensure that this pin is properly terminated to ensure reliable operation.

Functional Block Diagram



Operation

The RT5716 is a high switching frequency synchronous step-down converter; the input voltage range is from 1.8V to 5.5V and it provides 16 selectable output voltage levels by connecting the resistor between RSEL/MODE pin and GND. The PFM design can maintain high efficiency during the light load. At higher load conditions the device automatically switches to PWM. In shutdown mode, the device is disabled, excellent in reducing power consumption. To prevent the device from being damaged by abnormal operations, the protection mechanisms include Undervoltage Lockout (UVLO), Over-Temperature Protection (OTP) and Overcurrent Protection (OCP).

Enable

The device can be enabled or disabled by the EN pin. When the EN pin is above the threshold for logic high, the IC enters normal operation. When the EN pin is set to low, the device transitions to shutdown mode. In this mode, the converter stops switching, the internal control circuitry turns off, and the discharge function is triggered.

EN low level time must larger than 200μs for internal circuit reset time.

UVLO Protection

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage is lower than the UVLO falling threshold voltage, the device will be lockout.

100% Duty Cycle Operation

The converter enters 100% duty cycle operation once the input voltage decreases and the difference voltage between input and output is lower than V_{TH_100-}. The output voltage follows the input voltage minus the voltage drop across the internal P_MOSFET and the inductor. Once the input voltage increases and trips the 100% mode exit threshold, V_{TH_100+}, the converter goes back to normal switching again. See Figure 1.

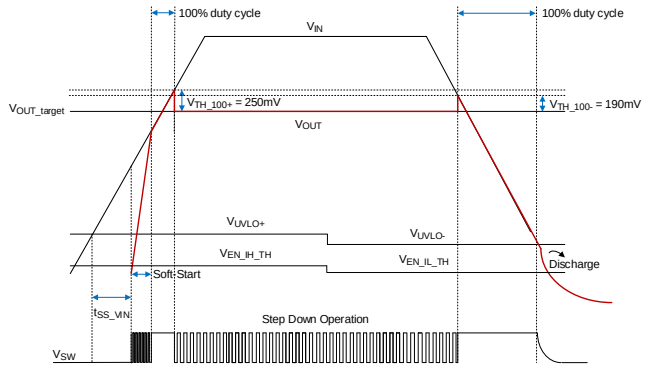


Figure 1. Auto Bypass Mode

Over-Temperature Protection

When the junction temperature exceeds the OTP threshold value, the IC will shut down the switching operation. Once the junction temperature cools down and is lower than the OTP lower threshold, the converter will automatically resume switching. To prevent V_{OUT} from increasing by 0.2V to 0.5V when the ambient temperature reaches above 85°C and V_{OUT} is less than 1.8V, it is recommended to draw a load of at least 300nA.

Overcurrent Protection and Short Circuit Protection

The OCP and SCP function is implemented by high-side MOSFET and low-side MOSFET. When the inductor current reaches the peak current-limit threshold, the high-side MOSFET will be turned-off. The low-side MOSFET turns on to discharge the inductor current until the inductor current trips below the valley current-limit threshold. After peak current limit triggered, the max inductor current is decided by the inductor current rising rate and the response delay time of the internal network.

During OCP and SCP period, the output voltage drops below the setting threshold (typ. 0.2V) and the current limit value is reduced to low current limit level for lowering the devices loss, reducing the heat and preventing further damage of the chip.

Due to internal propagation delay ($t_{I\_LIM\_DELAY}$ = 100ns), the actual inductor current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{Current\ limit\ peak} = I_{Peak\ current\ limit\ leavel} + \frac{(V_{IN}-V_{OUT})}{L} \times t_{I\_LIM\_DELAY}$$

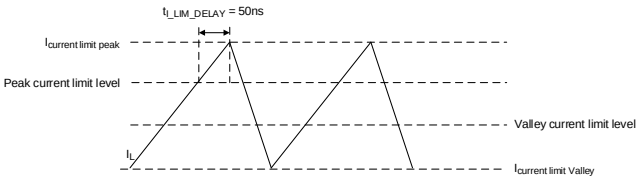


Figure 2. Current Limit

Pulse Frequency Modulation and Ton Extend Mode

Buck converters with enhanced light load efficiency will reduce their switching frequency at light load.

In PFM mode, the low-side MOSFET is switched off when the inductor current reaches zero, and the switch node floats until the next time the high-side MOSFET is switched on.

PFM operation reduces the converter's switching frequency to very low values, typically down to a few kilohertz, during light load conditions. This reduction in switching frequency helps minimize switching losses, significantly increasing the light load efficiency of the converter.

Furthermore, at ultra-light load, the high-side MOSFET on time is extended to further reduce the switching frequency and improve overall efficiency.

Output Voltage Selection

The RT5716 provides 1 fixed and 16 different levels of V_{OUT} which can be set with a single external resistor connected between the RSEL/MODE pin and GND. The V_{OUT} level selector circuit starts to detect the value of the resistor once the converter has been enabled and the control circuitry is powered up. The V_{OUT} level is set once during the V_{OUT} level setup time (t_{RSEL}) of the device.

Table 1. Output Voltage Setting

Type	Output-1 (V)	Output-2 (V)	Output-3 (V)	Output-4 (V)	RSEL (kΩ) *		
Level	0.4V to 3.3V	0.4V to 0.775V	0.8V to 1.55V	1.8V to 3.3V	Min	Nom	Max
0	3.3	0.7	1.2	1.8	Connected to GND (No resistor needed)		
1	0.4	0.4	0.8	1.8	9.9	10	10.1
2	0.58	0.425	0.85	1.9	12	12.1	12.2
3	0.6	0.45	0.9	2	15.2	15.4	15.6
4	0.7	0.475	0.95	2.1	18.5	18.7	18.9
5	0.75	0.5	1	2.2	23.5	23.7	23.9
6	0.8	0.525	1.05	2.3	28.4	28.7	29
7	1.1	0.55	1.1	2.4	36.1	36.5	36.9
8	1.2	0.575	1.15	2.5	43.8	44.2	44.6
9	1.3	0.6	1.2	2.6	55.6	56.2	56.8
10	1.5	0.625	1.25	2.7	67.4	68.1	68.8
11	1.6	0.65	1.3	2.8	85.7	86.6	87.5
12	1.8	0.675	1.35	2.9	104	105	106.1
13	1.9	0.7	1.4	3	131.7	133	134.3
14	2.5	0.725	1.45	3.1	160.4	162	163.6
15	3	0.75	1.5	3.2	203	205	207.1
16	3.3	0.775	1.55	3.3	≥249	≥249	≥249

*: E96 resistor series, 1% accuracy, temperature coefficient better or equal than ±200 ppm/°C.

Absolute Maximum Ratings (Note 1) (Note 2)

- VIN, VO, RSEL/MODE, EN ---------- –0.3V to 6V
- SW (DC) ---------- –0.3V to V_{IN} + 0.3V
- Power Dissipation, P_D @ T_A = 25°C

  TWL-CSP-6B 0.69x1.04 (BSC) ---------- 1.03W

  WDFN-6L 1.5x1.5 (FC) ---------- 0.69W
- Package Thermal Resistance (Note 3)

  TWL-CSP-6B 0.69x1.04 (BSC), θ_{JA} ---------- 96.8°C/W

  WDFN-6L 1.5x1.5 (FC), θ_{JA} ---------- 145.34°C/W

  WDFN-6L 1.5x1.5 (FC), θ_{JC} ---------- 16.73°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- ±2kV

  CDM (Charged Device Model) ---------- ±500V

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. The operating voltage for RSEL/MODE is recommended to be lower than the input voltage.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

Recommended Operating Conditions (Note 5)

- Supply Input Voltage ---------- 1.8V to 5.5V
- Output Current ($V_{IN} \geq$ 2.3V), I_{OUT}

  for RT5716-AB, RT5716-BB, RT5716-CB, RT5716-DB ---------- 1A (Max.)
- Output Current (V_{IN} < 2.3V), I_{OUT}

  for RT5716-AB, RT5716-BB, RT5716-CB, RT5716-DB ---------- 0.7A (Max.)
- Output Current, I_{OUT}

  for RT5716-AA, RT5716-BA, RT5716-CA, RT5716-DA ---------- 0.6A (Max.)
- Effective Inductance, L ---------- 0.33µH to 1.2µH
- Effective Inductance, L ---------- 0.47µH (Typ.)
- Effective Min. Input Capacitance, C_{IN_MIN} ---------- 0.5µF
- Effective Typ. Input Capacitance, C_{IN_TYP} ---------- 4.7µF
- Effective Output Capacitance, C_{OUT} ---------- 2µF to 26µF
- External Max. Parasitic Capacitance at RSEL/MODE Pin ---------- 30pF

- Resistance Range for External Resistor at RSEL/MODE Pin
  (E96 1% Resistor Values), R_{SET} ---------- 10kΩ to 249kΩ
- External Resistor Tolerance E96 Series at RSEL/MODE Pin, R_{SET} ---------- 1%
- E96 Resistor Series Temperature Coefficient (TCR), R_{SET} ---------- –200ppm/°C to 200ppm/°C
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{IN} = 3.6V, C_{IN} = 4.7μF, C_{OUT} = 4.7μF x 2, L = 0.47μH, T_J = –40°C to 125°C, typical values are at T_J = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BUCK Regulator						
Undervoltage Lockout Rising Threshold	V_{UVLO+}	V_{IN} rising, T_J = –40°C to 125°C (Note 6)	--	1.7	1.8	V
Undervoltage Lockout Falling Threshold	V_{UVLO-}	V_{IN} falling, T_J = –40°C to 125°C (Note 6)	--	1.65	1.75	V
Undervoltage Lockout Deglitch Time	t_{UVLO_DT}		--	32	--	μs
Quiescent Current into VIN Pin (Switching)	I_{Q_IN-SW}	EN = V_{IN}, I_{OUT} = 0A, V_{OUT} = 1.2V, RSEL/MODE = GND	--	2.5	--	μA
Quiescent Current (Force PWM Mode)	I_{Q_PWM}	EN = V_{IN}, I_{OUT} = 0A, V_{OUT} = 1.2V, RSEL/MODE = V_{IN} (after start-up)	--	8	--	mA
Quiescent Current into VIN Pin (Non-Switching)	$I_{Q\_IN-NONSW}$	EN = V_{IN}, I_{OUT} = 0A, V_{OUT} = 1.2V, T_J = –40°C to 85°C (Note 6), RSEL/MODE = GND	--	2.3	3.7	μA
Shutdown Current	I_{SHDN}	EN = GND, shutdown current into V_{IN} RSEL/MODE = GND, T_J = –40°C to 85°C (Note 6)	--	55	290	nA
Bias Current into VO Pin	I_{IN_VOS}	EN = V_{IN}, V_{OUT} = 1.2V, (internal 8M resistor divider), T_J = –40°C to 85°C (Note 6)	--	400	520	nA
Switching Frequency	f_{SW}	EN = V_{IN}, I_{OUT} = 0A, V_{OUT} = 1.8V, RSEL/MODE = V_{IN} (after start-up)	--	4	--	MHz
Positive Inductor Peak Current Limit	I_{CL_pk}	1.8V ≤ V_{IN} ≤ 5.5V, OCP Select 1 = 1.2A, T_J = –40°C to 125°C (Note 6)	1.02	1.2	1.38	A
		1.8V ≤ V_{IN} ≤ 5.5V, OCP Select 2 = 1.7A, T_J = –40°C to 125°C (Note 6)	1.44	1.7	1.96	
Positive Inductor Valley Current Limit	I_{CL_valley}	1.8V ≤ V_{IN} ≤ 5.5V, OCP Select 1 =1.2A, T_J = –40°C to 125°C (Note 6)	0.73	0.86	0.99	A
		1.8V ≤ V_{IN} ≤ 5.5V, OCP Select 2 = 1.7A, T_J = –40°C to 125°C (Note 6)	1.15	1.36	1.57	
Negative Inductor Peak Current Limit	$I_{CL\_N\_pk}$	1.8V ≤ V_{IN} ≤ 5.5V	--	–1	--	A
Current Limit Propagation Delay	$t_{I\_LIM\_DELAY}$		--	50	--	ns

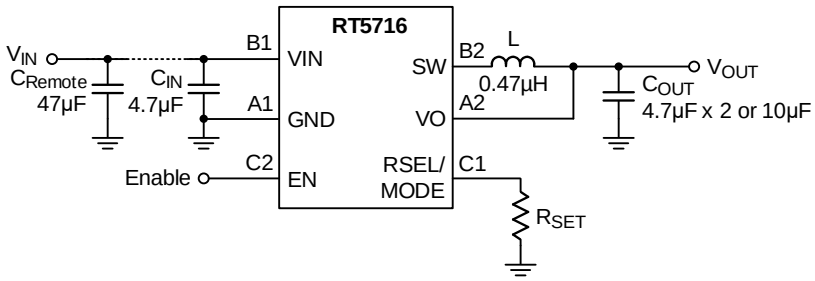
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Leakage Current into SW Pin	I_{LKG_SW}	V_{SW} = 1.2V, T_J = –40°C to 85°C (Note 6)	--	10	25	nA
UGATE R_{ON}	R_{ON_HG}	T_J = –40°C to 125°C (Note 6)	--	120	170	mΩ
LGATE R_{ON}	R_{ON_LG}	T_J = –40°C to 125°C (Note 6)	--	80	115	mΩ
Minimum On Time	t_{MIN_ON}	V_{IN} = 5.5V, V_{OUT} = 0.4V	--	40	--	ns
Minimum Off Time	t_{MIN_OFF}	V_{IN} = 3.6V, V_{OUT} = 3.3V	--	40	--	ns
Output Discharge Resistance	R_{DIS}	EN = GND, I_{VOS} = –10mA into the VO pin, T_J = –40°C to 85°C (Note 6)	--	7	11	Ω
Output Voltage Accuracy	V_{OUT_ACC}	PFM mode, V_{OUT} ≤ 1.5V, I_{OUT} = 1mA, T_J = –40°C to 85°C (Note 6)	--	±22.5	--	mV
		PFM mode, V_{OUT} > 1.5V, I_{OUT} = 1mA, T_J = –40°C to 85°C (Note 6)	--	±1.5	--	%
		FPWM mode, V_{OUT} ≤ 1.5V, I_{OUT} = 0mA, T_J = –40°C to 125°C (Note 6)	--	±22.5	--	mV
		FPWM mode, V_{OUT} > 1.5V, I_{OUT} = 0mA, T_J = –40°C to 125°C (Note 6)	--	±1.5	--	%
Load Regulation	V_{LOAD_REG}	V_{IN} = 3.6V, V_{OUT} = 1.2V, FPWM, I_{OUT} = 0A to 1A, T_J = –40°C to 85°C (Note 6) (For TWL-CSP package)	--	±1	--	%
		V_{IN} = 3.6V, V_{OUT} = 1.2V, FPWM, I_{OUT} = 0A to 1A, T_J = –40°C to 85°C (Note 6) (For WDFN package)	--	±2	--	
Line Regulation	V_{LINE_REG}	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.2V, I_{OUT} = 0mA, FPWM, T_J = –40°C to 85°C (Note 6)	--	±1	--	%
Auto Bypass Mode Leave Detection Threshold	V_{TH_100+}	Rising V_{IN}, 100% mode is left with V_{IN} = V_{OUT} + V_{TH_100+}	--	250	--	mV
Auto Bypass Mode Enter Detection Threshold	V_{TH_100-}	Falling V_{IN}, 100% mode is entered with V_{IN} = V_{OUT} + V_{TH_100-}	--	190	--	mV
Over-Temperature Protection	T_{OTP}	V_{IN} = 3.6V, V_{OUT} = 1.2V	--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Timing						
Regulator Start-Up Delay Time	t_{SS_EN}	V_{IN} = 3.6V, EN = GND to V_{IN}, V_{OUT} starts switching, T_J = –40°C to 125°C (Note 6)	--	500	1100	μs
Soft-Start Time	t_{SS}	From V_{OUT} = 0V to 95% of V_{OUT} nominal, T_J = –40°C to 125°C (Note 6)	--	120	500	μs
V_{OUT} Level Setup Time	t_{RSEL}	To setup V_{OUT} level ready	--	400	--	μs
Logic Input (EN and RSEL/MODE Inputs)						
High Level Input Voltage	V_{IH_TH}	V_{IN} = 1.8V to 5.5V, T_J = –40°C to 125°C (Note 6)	0.8	--	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low Level Input Voltage	V_{IL_TH}	V_{IN} = 1.8V to 5.5V, T_J = –40°C to 125°C (Note 6)	--	--	0.4	V
RSEL/MODE Pin Input Bias Current	I_{IN_MODE}	V_{IN} = 5.5V, EN = high, T_J = –40°C to 125°C (Note 6)	--	10	25	nA
EN Pin Leakage	EN_{LK}	T_J = –40°C to 85°C (Note 6), EN = high	--	10	25	nA
Internal Pull-Down Resistance	R_{PD}	EN pin to GND	--	500	--	kΩ

Note 6. This specification is guaranteed by design.

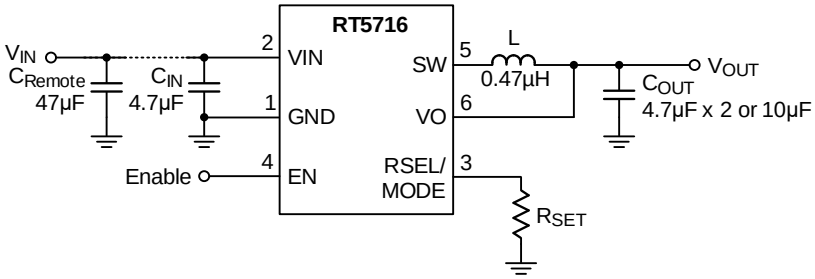
Typical Application Circuit

For TWL-CSP-6B 0.69x1.04 (BSC) Package



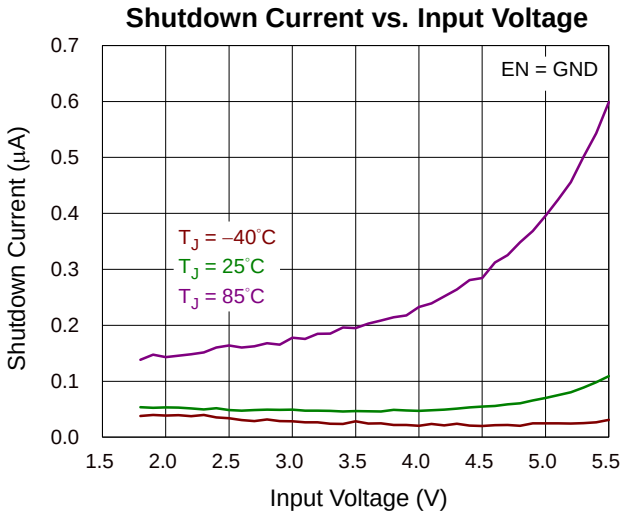
Reference	Part Number	Value	Package	Manufacturer
CIN	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
COUT	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
	GRM155R60J106ME15D	10µF/6.3V/X5R	0402	Murata
CRemote	GRM21BR60J476ME11L	47µF/6.3V/X5R	0805	Murata
L	DFE18SANR47MG0L	0.47µH	0603	Murata
RSET	Resistor E96 series 1%, TC ±200ppm	See Table 1. Output Voltage Setting	--	--

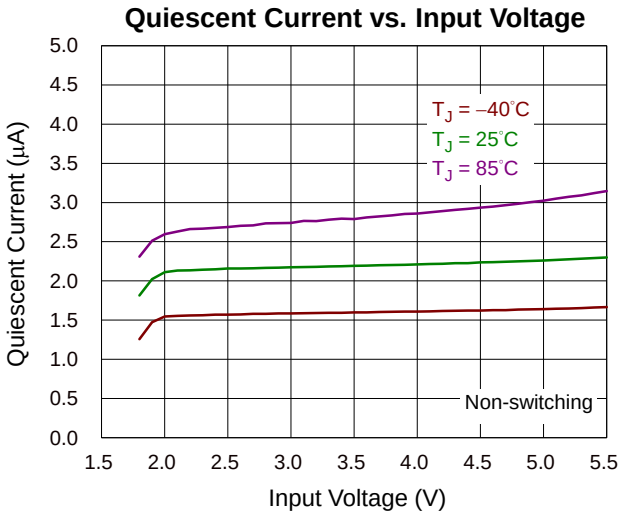
For WDFN-6L 1.5x1.5 (FC) Package

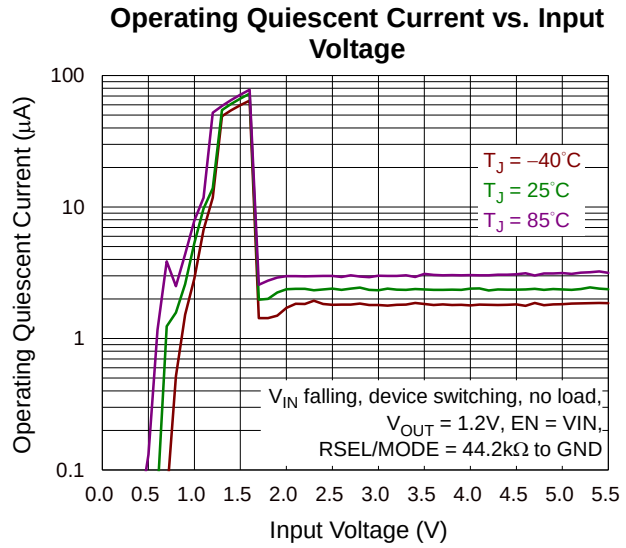


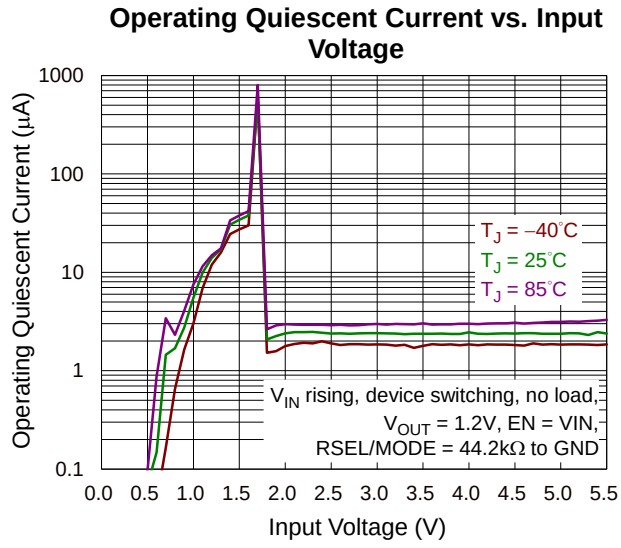
Reference	Part Number	Value	Package	Manufacturer
CIN	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
COUT	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
	GRM155R60J106ME15D	10µF/6.3V/X5R	0402	Murata
CRemote	GRM21BR60J476ME11L	47µF/6.3V/X5R	0805	Murata
L	DFE18SANR47MG0L	0.47µH	0603	Murata
RSET	Resistor E96 series 1%, TC ±200ppm	See Table 1. Output Voltage Setting	--	--

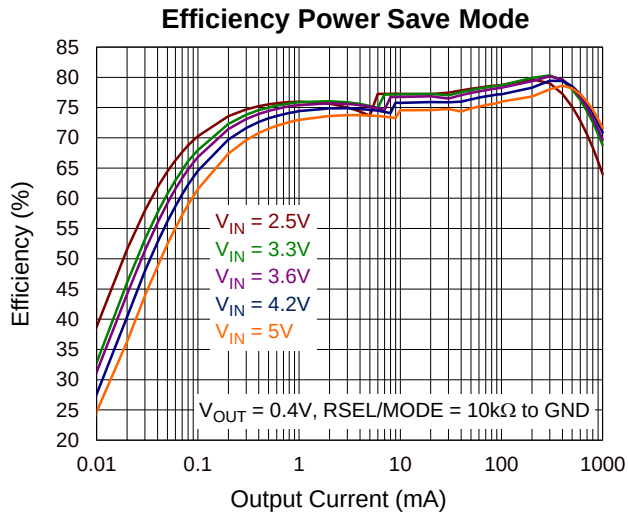
Typical Operating Characteristics

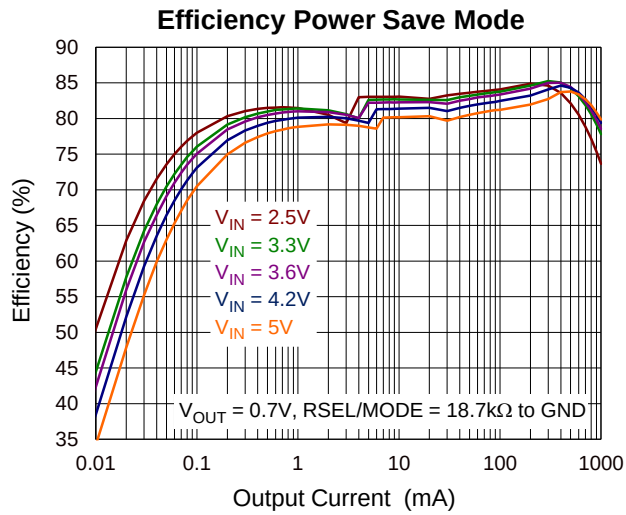




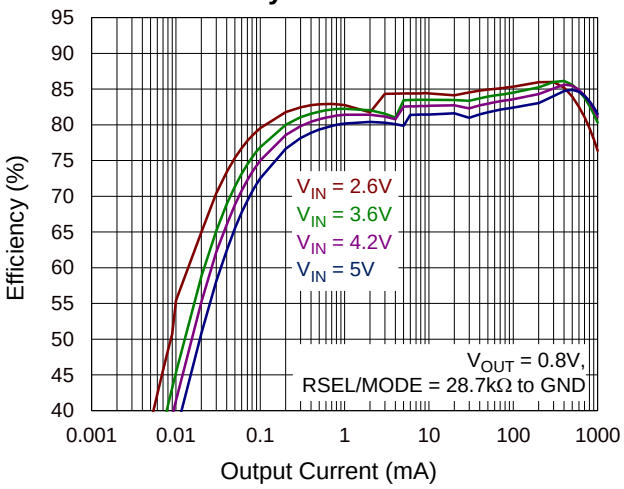




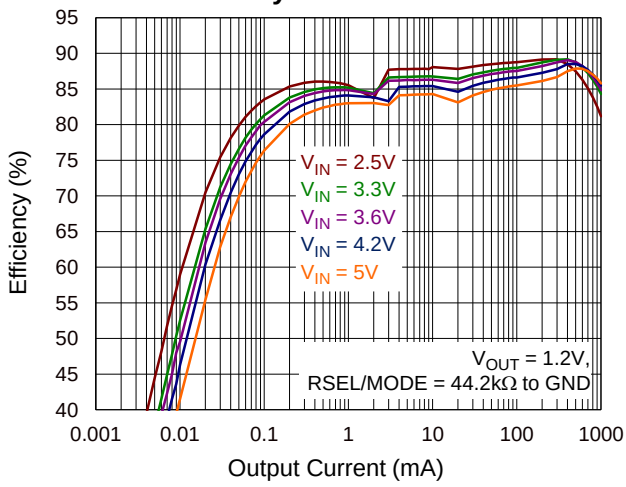




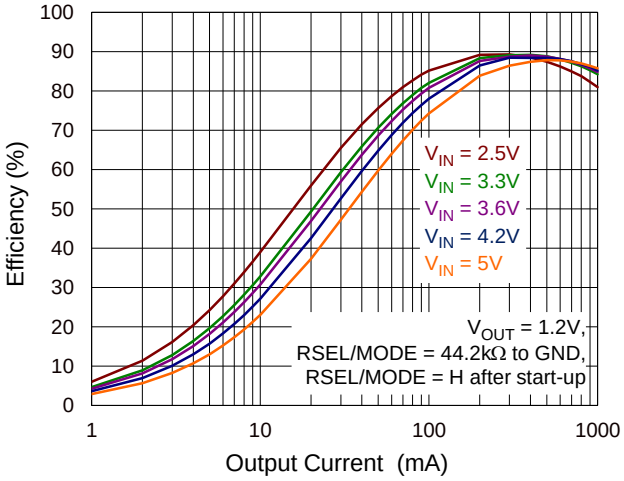
Efficiency Power Save Mode



Efficiency Power Save Mode



Efficiency Forced PWM Mode



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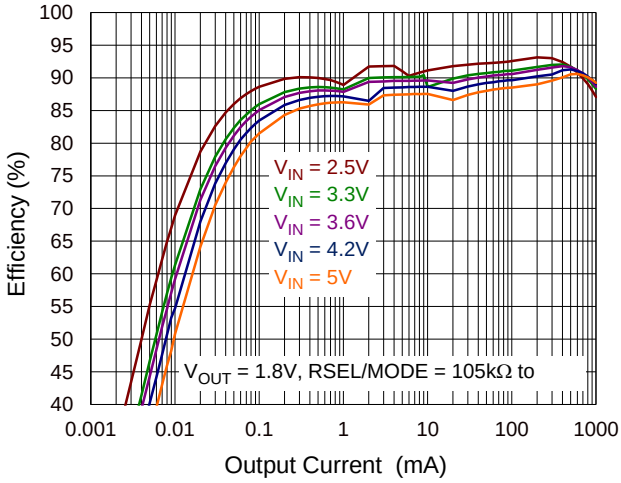

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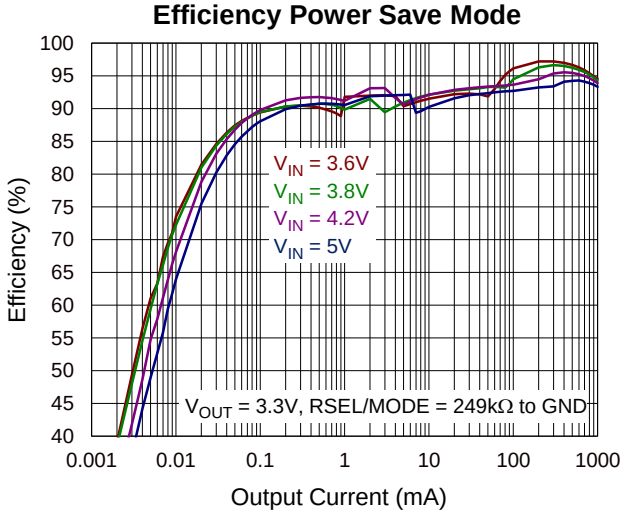
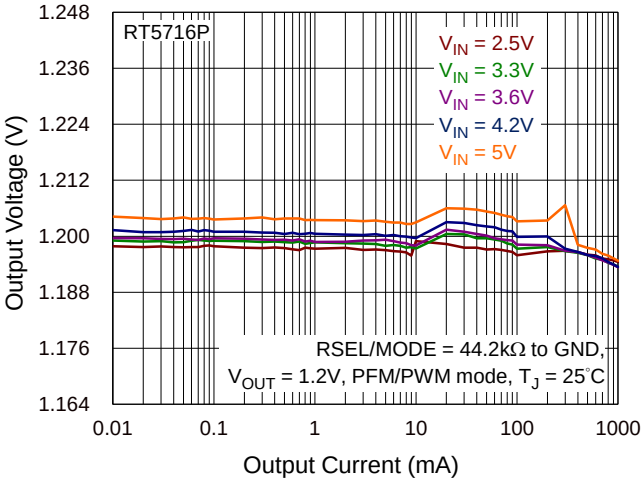
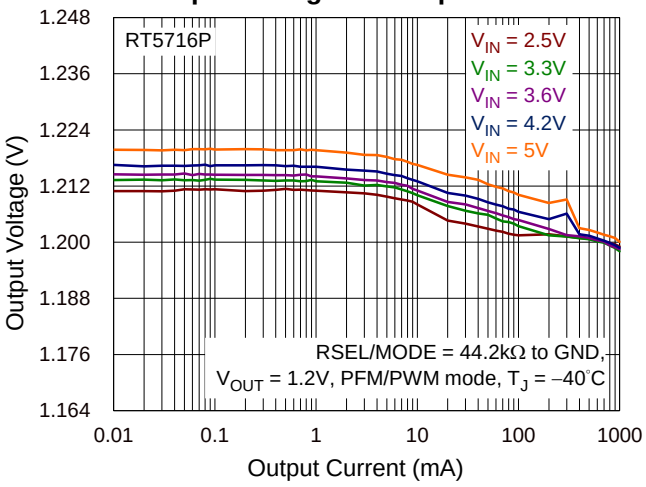


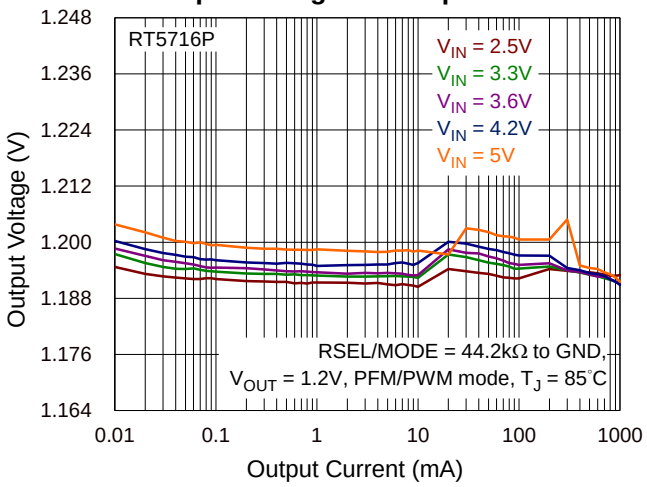
Output Voltage vs. Output Current



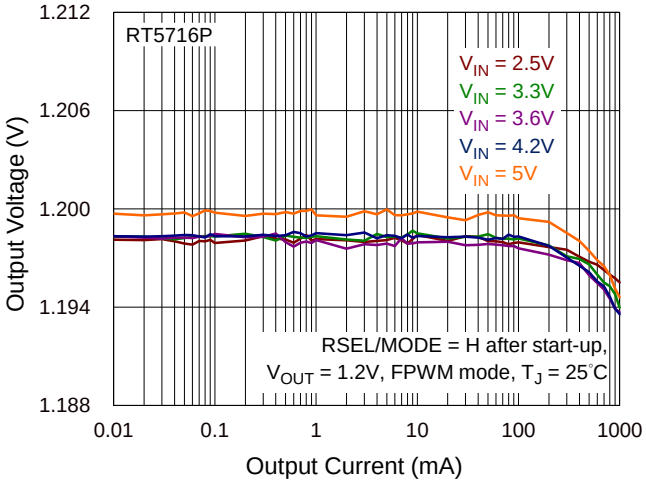
Output Voltage vs. Output Current



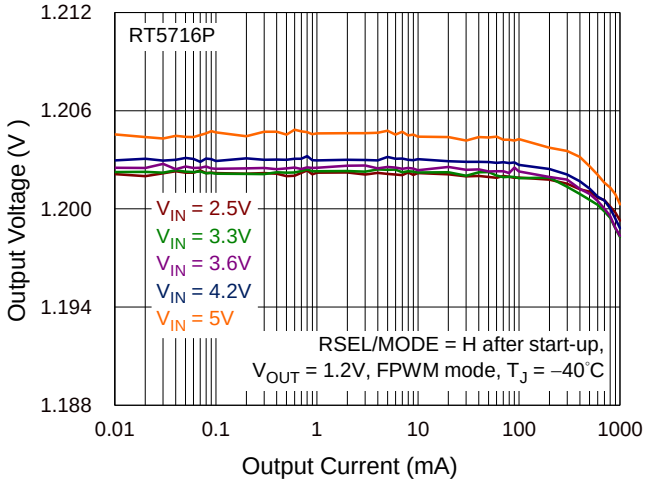
Output Voltage vs. Output Current



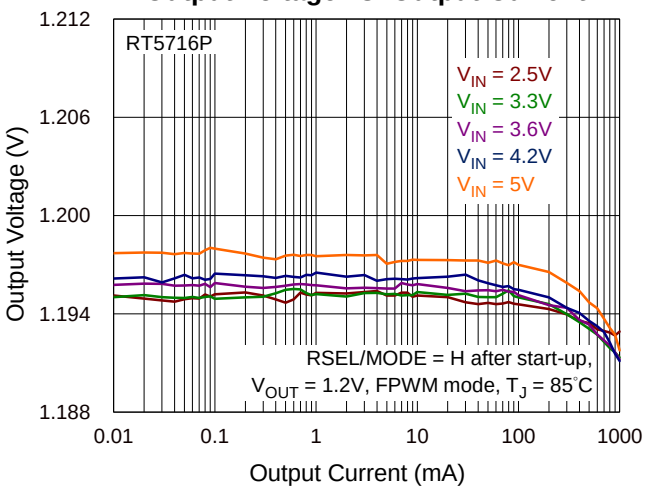
Output Voltage vs. Output Current



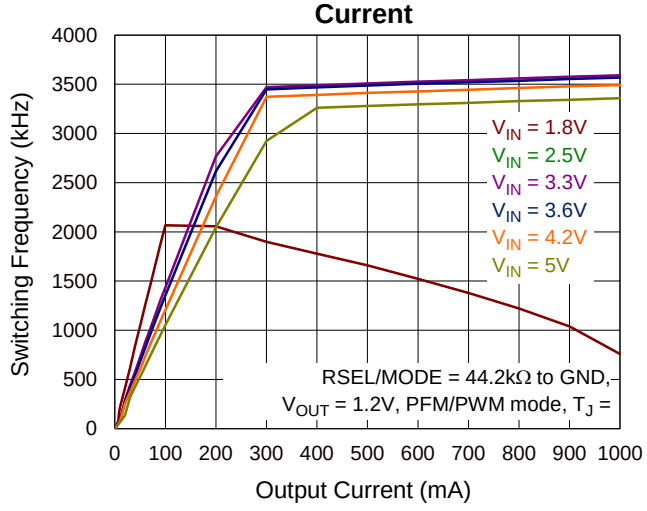
Output Voltage vs. Output Current



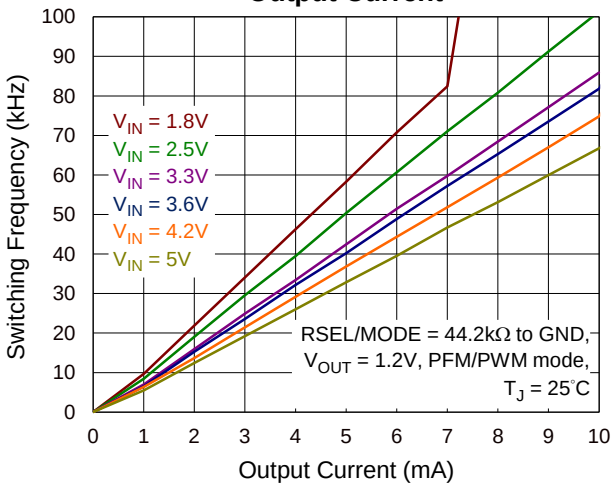
Output Voltage vs. Output Current



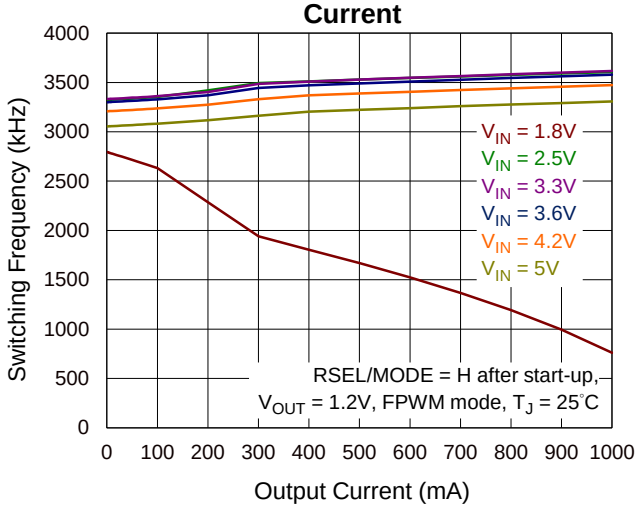
Switching Frequency vs. Output Current



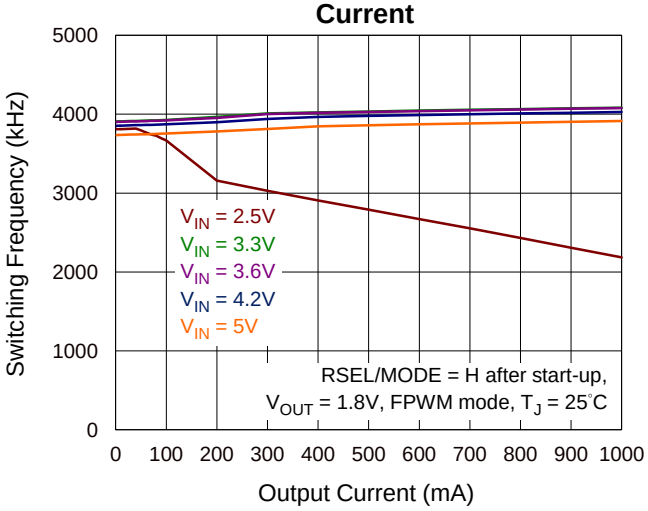
Switching Frequency (Zoom In) vs. Output Current



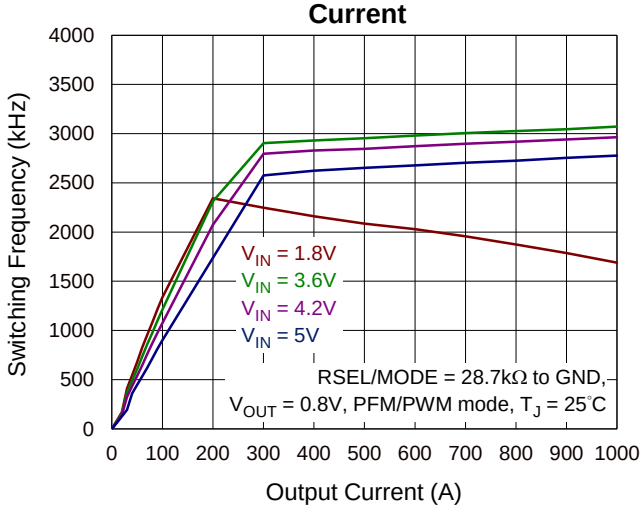
Switching Frequency vs. Output Current



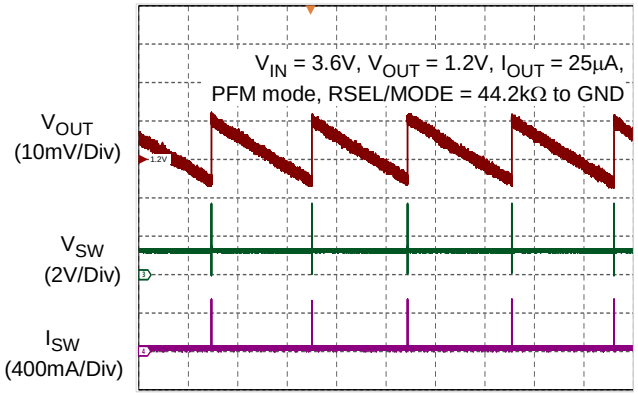
Switching Frequency vs. Output Current



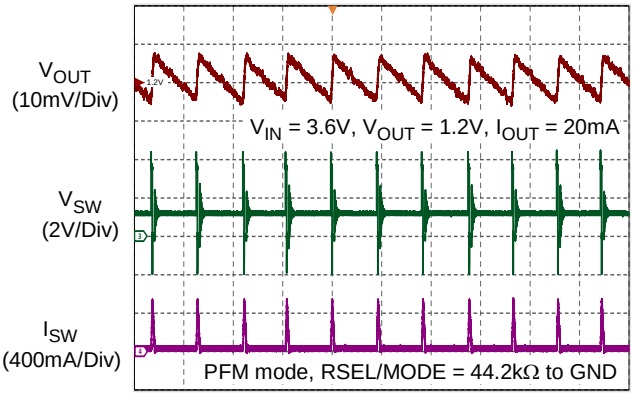
Switching Frequency vs. Output Current



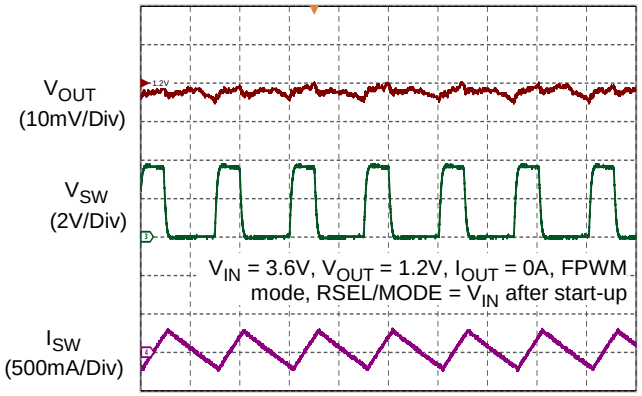
Typical Operation Power Save Mode



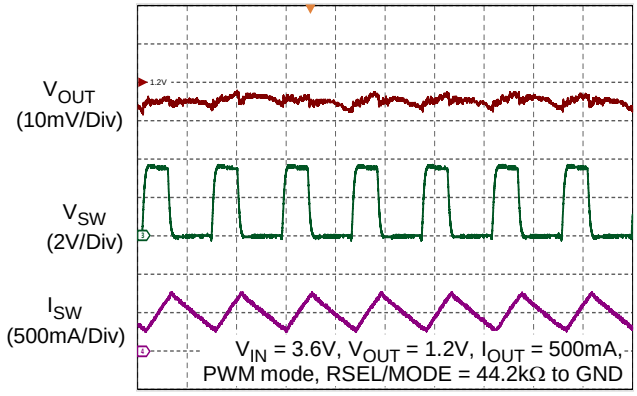
Typical Operation Power Save Mode



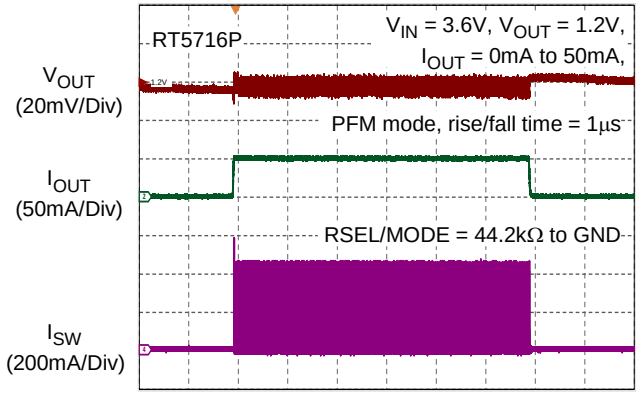
Typical Operation Forced PWM Mode



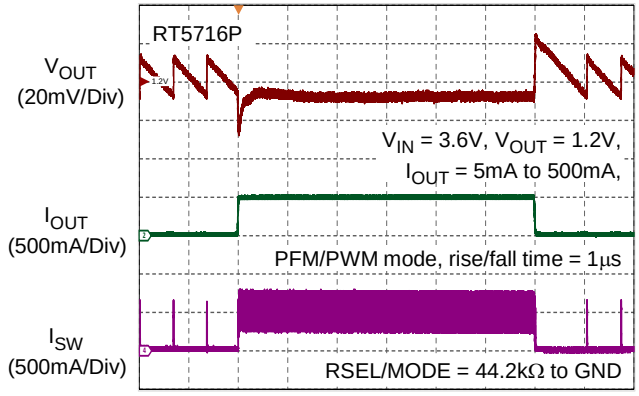
Typical Operation PWM Mode



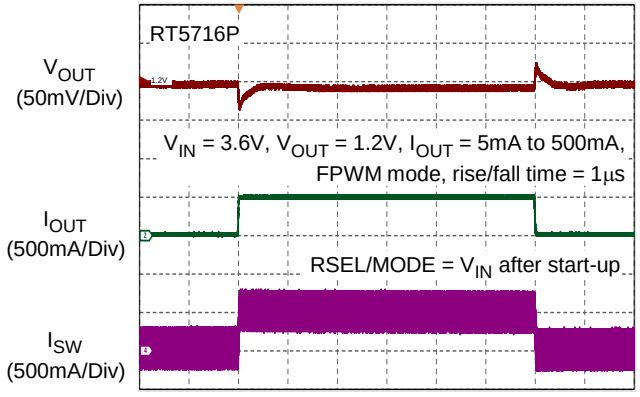
Load Transient Power Save Mode



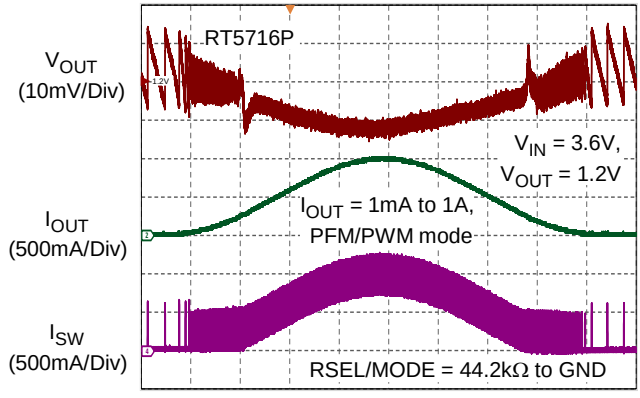
Load Transient Power Save Mode



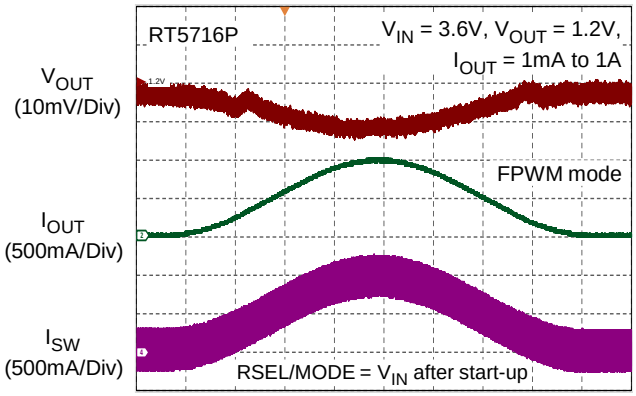
Load Transient Forced PWM Mode



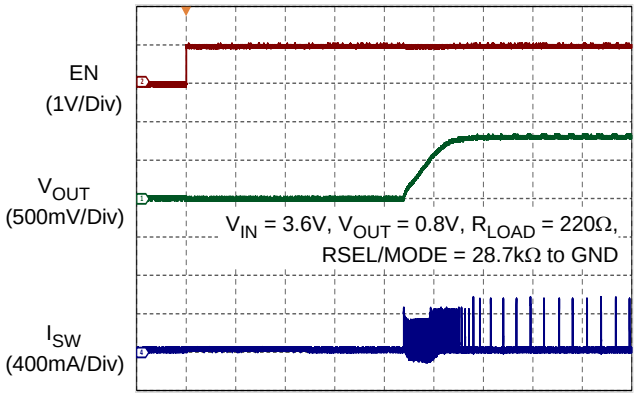
AC Load Sweep Power Save Mode



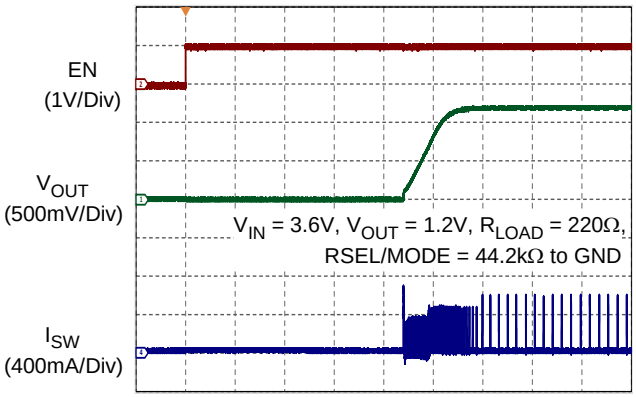
AC Load Sweep Forced PWM Mode



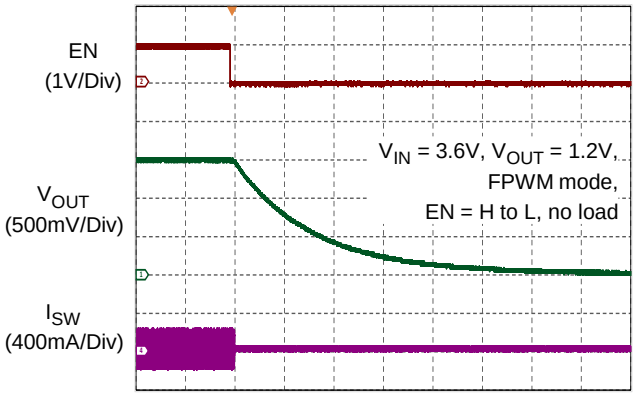
Start-Up



Start-Up



Output Discharge



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The basic RT5716 application circuit is shown in Typical Application Circuit. Application Information discusses the external component selection and the considerations of practical applications by referring to the electrical characteristics.

Inductor Selection

The recommended power inductor is 0.47μH for I_{OUT} = 600mA and I_{OUT} = 1A. The inductor saturation current rating needs to take care to choose follow overcurrent protection design consideration. In applications, it needs to select an inductor with the low DCR to provide good performance and efficiency.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2 x V_{OUT}, where I_{RMS} = I_{OUT}/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. To choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a TWL-CSP-6B 0.69x1.04 (BSC) package, the thermal resistance, θ_{JA}, is 96.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WDFN-6L 1.5x1.5 (FC) package, the thermal resistance, θ_{JA}, is 145.34°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (96.8°C/W) = 1.03W for a TWL-CSP-6B 0.69x1.04 (BSC) package.

$P_{D(MAX)}$ = (125°C - 25°C) / (145.34°C/W) = 0.69W for a WDFN-6L 1.5x1.5 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

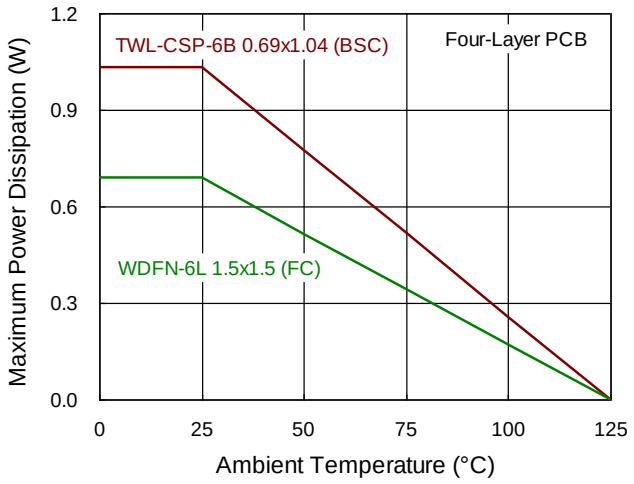


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

For high frequency switching power supplies, the PCB layout is important to get good regulation, high efficiency and stability. The following descriptions are the guidelines for better PCB layout.

- For good regulation, place the power components as close as possible. The traces should be wide and short enough especially for the high-current loop.
- Shorten the SW node trace length and make it wide.

Table 2. Protection Trigger Condition and Behavior

Protection Type	Threshold Refer to Electrical Spec.	Protection Method	Reset Method
Positive Inductor Peak Current Limit for I_{OUT} = 1.2A	I_{SW} > 1.2A (Typ.)	Turn off UG MOS	I_{SW} < 0.86A (Typ.)
Positive Inductor Peak Current Limit for I_{OUT} = 1.7A	I_{SW} > 1.7A (Typ.)		I_{SW} < 1.36A (Typ.)
UVLO	V_{IN} < V_{UVLO-} (Typ.)	Shutdown	V_{IN} > V_{UVLO+} (Typ.)
OTP	T_J > 150°C (Typ.)	Shutdown	T_J < 130°C (Typ.)

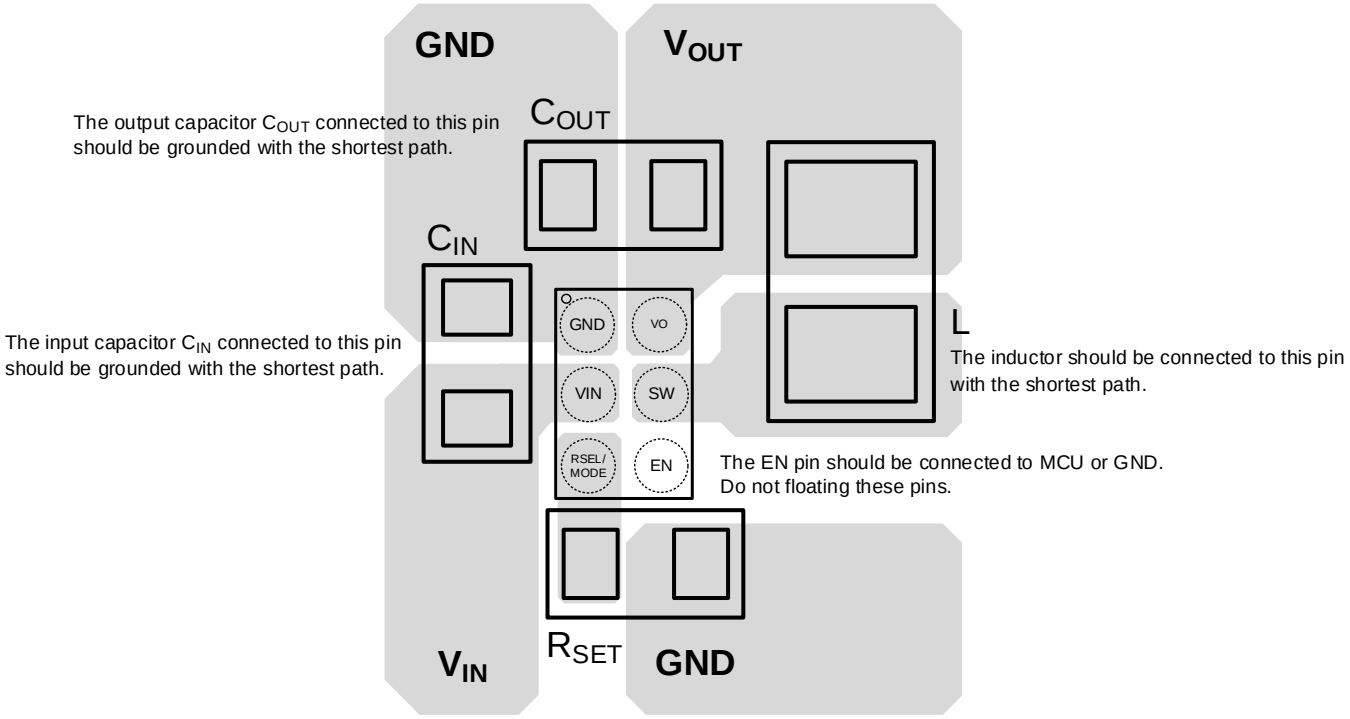


Figure 4. PCB Layout Guide for TWL-CSP-6B 0.69x1.04 (BSC) Package

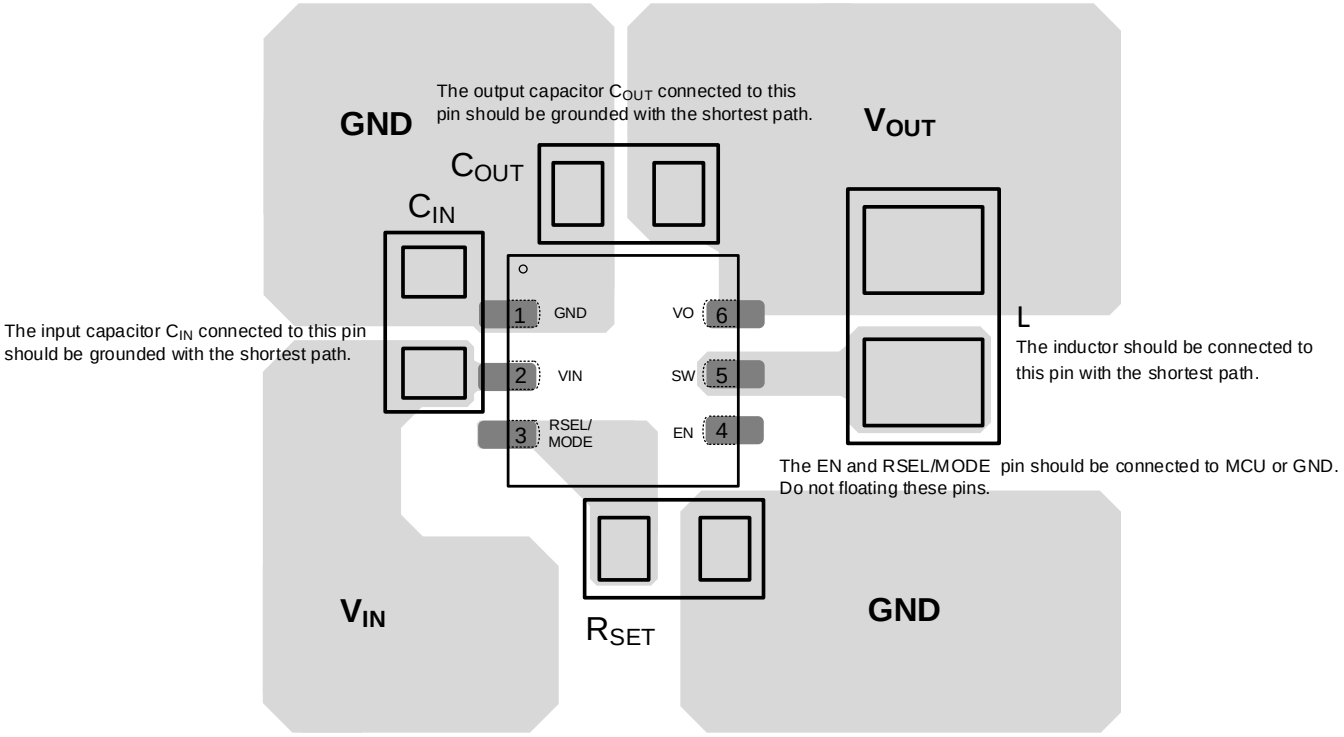
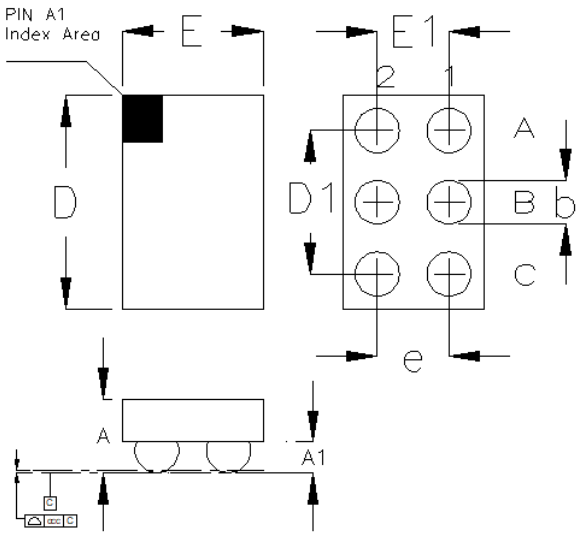


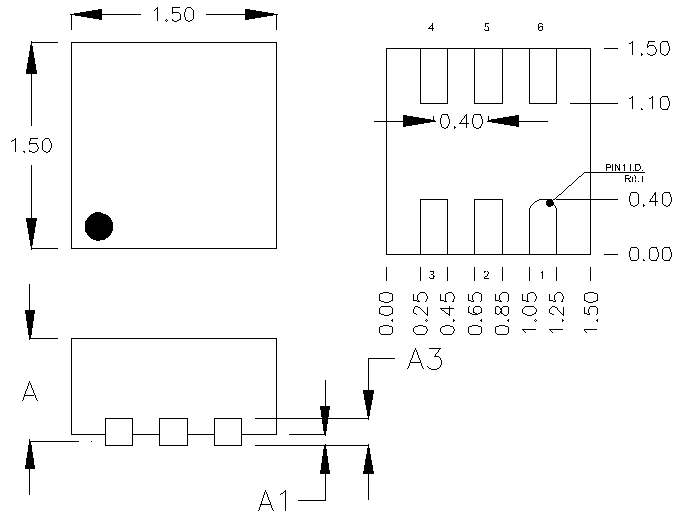
Figure 5. PCB Layout Guide for WDFN-6L 1.5x1.5 (FC) Package

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.320	0.400	0.013	0.016
A1	0.120	0.180	0.005	0.007
b	0.190	0.240	0.007	0.009
D	1.010	1.070	0.040	0.042
D1	0.700		0.028	
E	0.660	0.720	0.026	0.028
E1	0.350		0.014	
e	0.350		0.014	
ccc	0.020		0.001	

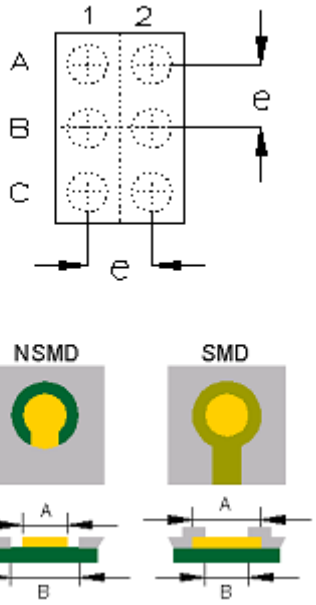
6B TWL-CSP 0.69x1.04 Package



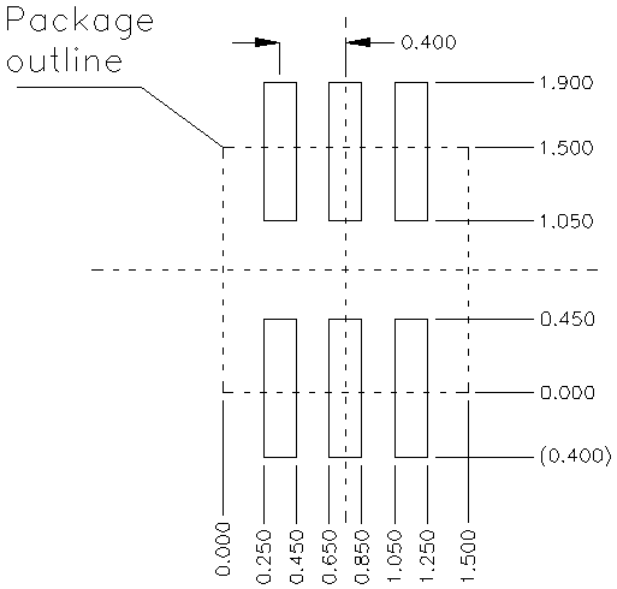
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

W-Type 6L DFN 1.5x1.5 Package (FC)

Footprint Information



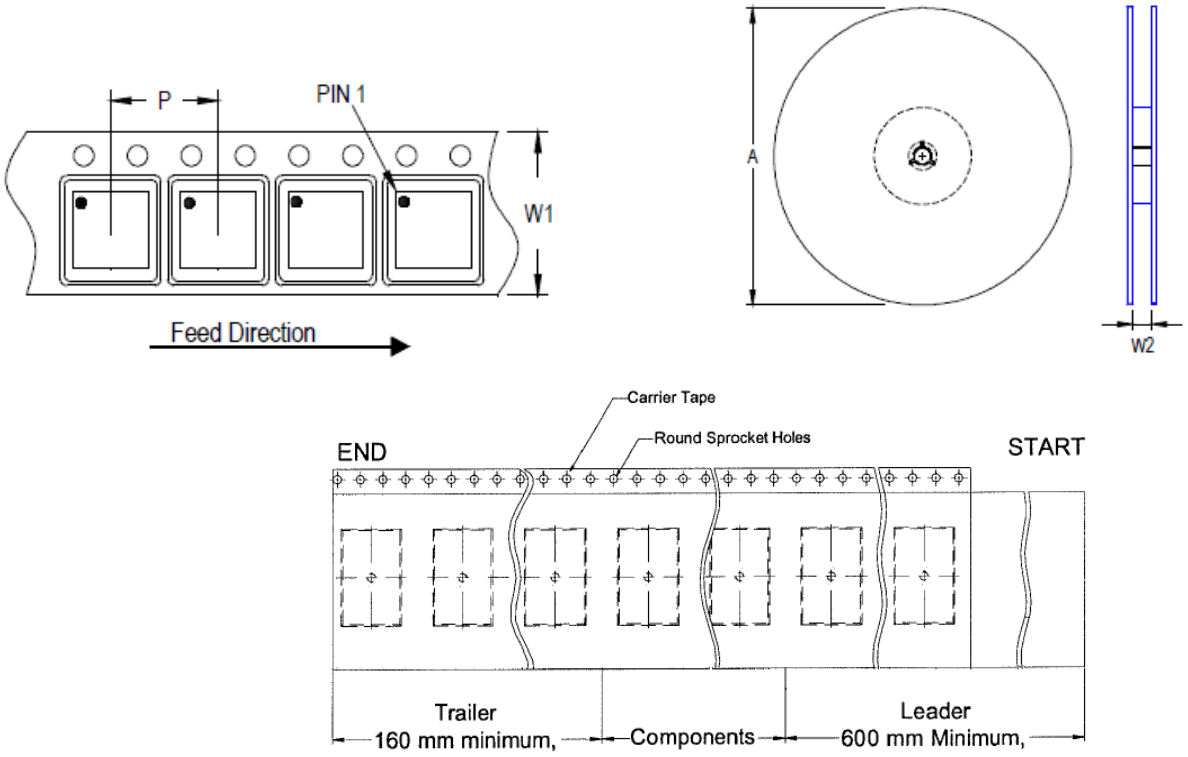
Package	Number of Pins	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
TWL-CSP0.69x1.04-6	6	NSMD	0.350	0.200	0.300	±0.025
		SMD		0.230	0.200	



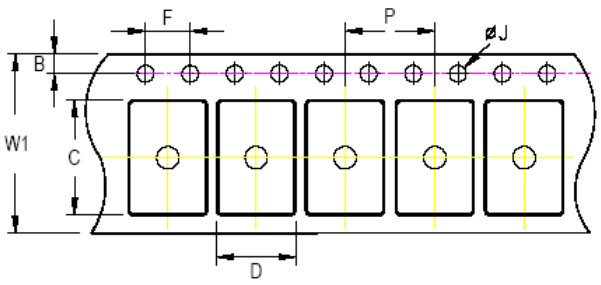
Package	Number of Pin	Tolerance
V/W/U/XDFN1.5x1.5-6(FC)	6	±0.05 mm

Packing Information

Tape and Reel Data - WL-CSP 0.69x1.04



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 0.69x1.04	8	4	180	7	3,000	160	600	8.4/9.9

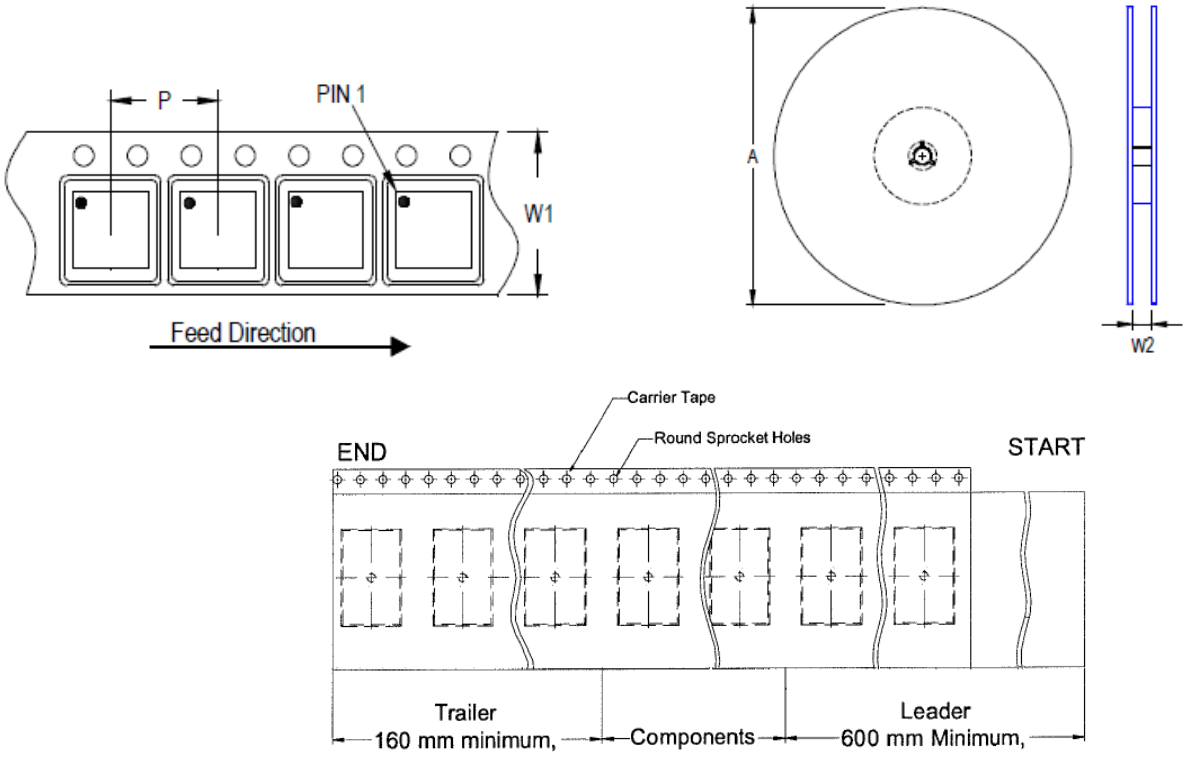


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

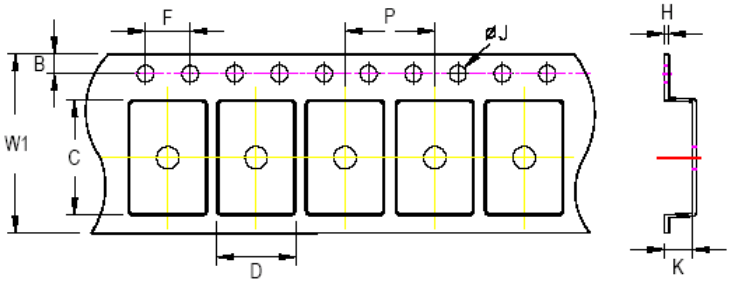
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Data - QFN & DFN 1.5x1.5



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 1.5x1.5	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing - WL-CSP 0.69x1.04

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
WL-CSP 0.69x1.04	7”	3,000	Box A	18.3*18.3*8.0	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	1	3,000	For Combined or Partial Reel.			

Tape and Reel Packing - QFN & DFN 1.5x1.5

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN & DFN 1.5x1.5	7”	2,500	Box A	18.3*18.3*8.0	3	7,500	Carton A	38.3*27.2*38.3	12	90,000
			Box E	18.6*18.6*3.5	1	2,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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Datasheet Revision History

Version	Date	Description	Item
00	2024/2/5	Final	