Audio Amplifier with IV Sense

General Description

The RT5510 is a boosted BTL class-D amplifier with V/I sensing. A built-in DC-DC step-up converter is used to provide efficient power for class-D amplifier with multi-level class-G operation. The digital audio interface supports I^2S, left-justified, right-justified, TDM and DSP A/B format for audio in with a data out used for chip information like voltage sense and current sense, which are able to be monitored via DATAO through proper register setting.

Ordering Information

RT5510□

└ Package Type
WSC : WL-CSP-30B 2.25x2.60 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

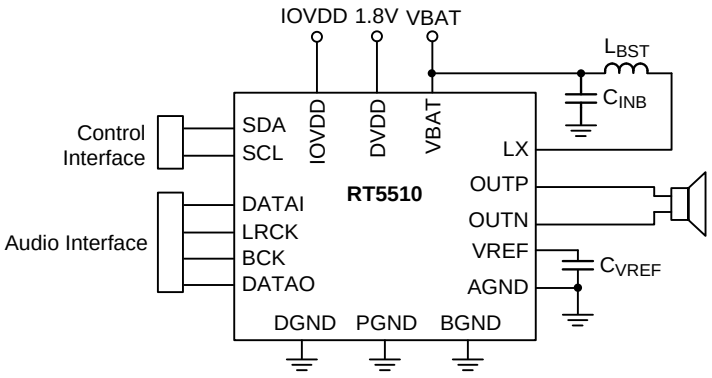
Applications

- Smart Phone
- Tablet

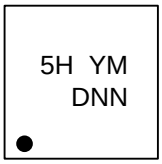
Features

- **Class-D Speaker AMP**
  - **4.8W Output Power @ 9.5V, 8Ω Load, THD < 1%**
  - **6.5W Output Power @ 9.5V, 4Ω Load, THD < 1%**
  - **0/3/6/9/12/15/18dB Boost Gain**
  - **20μV Output Noise**
  - **Add DRE to Reduce Output Noise**
- **Boost Converter**
  - **Adaptive Boost for Speaker, Boost from Battery Supply Up to Programmed Voltage, Max 9.5V**
  - **Accurate Input Current Limit**
  - **Analog Part : Current Sense, Slope Compensation, Feedback ADC**
  - **Alternate Mode Supported**
  - **Digital Part : Voltage Loop and End-Point Prediction in Boost Mode**
- **Digital**
  - **Digital Audio Interface Support I^2S, Left-Justified, Right-Justified, TDM and DSPA/B**
  - **Flexible Interrupt Controller**
  - **Clip Control (Battery Safeguard) to Prevent Drawing Larger Current from Battery When Low VBAT**
  - **Watchdog to Monitor Application Process Status and Shutdown the System**
  - **Volume Control**
- **RoHS Compliant and Halogen Free**

Simplified Application Circuit



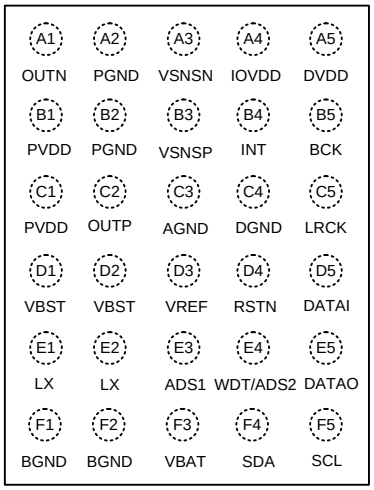
Marking Information



5H : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



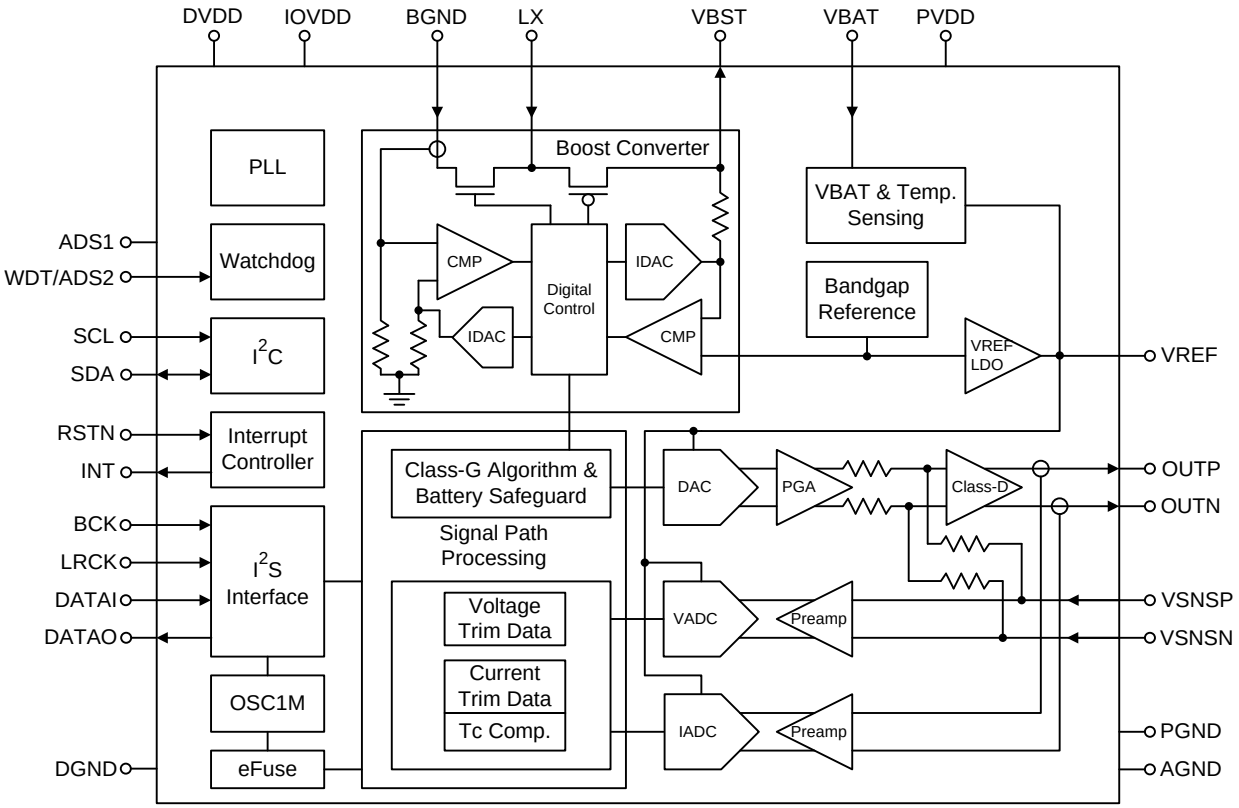
WL-CSP-30B 2.25x2.60 (BSC)

Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
A1	OUTN	O	Class-D inverting output.
A2, B2	PGND	P	Power ground.
A3	VSNSN	I	Voltage sense negative input.
A4	IOVDD	P	Digital I/O supply voltage. A 0.1μF external capacitor is required.
A5	DVDD	P	Digital supply voltage. A 0.1μF external capacitor is required.
B1, C1	PVDD	P	Class-D supply voltage. Voltage is provided by VBST pin. A 22μF external capacitor is required.
B3	VSNSP	I	Voltage sense positive input.
B4	INT	O	Interrupt output.
B5	BCK	I	I^2S interface bit clock data input.
C2	OUTP	O	Class-D non-inverting output.
C3	AGND	G	Analog ground.
C4	DGND	G	Digital ground.
C5	LRCK	I	I^2S interface word select data input.
D1, D2	VBST	O	Boost converter output voltage.
D3	VREF	P	Reference voltage output. A 1μF external capacitor is required.
D4	RSTN	I	Hardware reset input, high active. Normally keep low level, go high level for hardware reset.
D5	DATAI	I	I^2S interface digital audio data input.
E1, E2	LX	P	Boost converter switch input node.
E3	ADS1	I	Address select input 1.

Pin No.	Pin Name	Type	Pin Function
E4	WDT/ADS2	I	Watchdog input/Address select 2. The RT5510 will latch the level of WDT/ADS2 once 768μs after the edge of RSTN pin or analog POR goes from low to high or software reset from high to low for address select function.
E5	DATAO	O	I^2S interface digital audio data output.
F1, F2	BGND	G	Boost converter ground.
F3	VBAT	P	Battery supply voltage. Connect 2.7V to 5.5 V battery supply. A 0.1μF external capacitor is required.
F4	SDA	I/O	I^2C interface data input, Open drain structure. A 4.7kΩ external pull-up resistor is required.
F5	SCL	I	I^2C interface clock input, Open drain structure. A 4.7kΩ external pull-up resistor is required.

Functional Block Diagram



Operation

Class-D Audio Amplifier

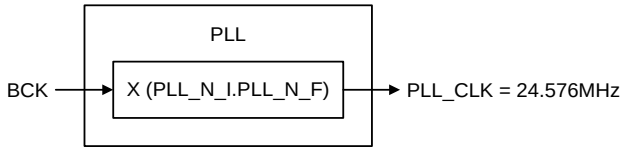
The RT5510 is a 9.5V boosted class-D audio amplifier capable of delivering up to 4.8Wrms output power into an 8Ω speaker at a supply voltage of 3.6V. The audio amplifier features low noise (20μVrms). Signal gains are configurable through analog (D_SPK_BOOST[2:0] 0 to 18dB, 3dB/step) and digital (VOLUME[7:0] 12 to −115.5dB, −0.5dB/step) circuits.

Over-current protection with threshold of 3A is also implemented in the high efficiency bridge-tied-load (BTL) devices to provide additional protection alongside the current limit of boost converter. The 3-level PWM scheme supports filter less speaker drive.

PLL

The on-chip PLL generates the 24.576MHz clock as the internal operating clock source. The PLL uses the BCK of I^2S interface as the reference clock and the programmability of the PLL allows the support of various sample rate of audio data, like 8k / 11.025k / 12k / 16k / 22.05k / 24k / 32k / 44.1k / 48k / 88.2k / 96kHz. Combining PLL_N_I and PLL_N_F forms an unsigned number in u13.16 format, which specifies the ratio of 24.576MHz clock over the reference clock, BCK.

$$PLL\_CLK = BCK \times (PLL\_N\_I + \frac{PLL\_N\_F}{2^{16}})$$



Over-Voltage Protection

The over-voltage (OV) protection detects whether the PVDD voltage exceeds 11.5V to 12.5V. If the OV flag is raised, analog circuits will be shut down. System will check the PVDD voltage and update the status every 200ms.

Over-Current Protection

The over-current protection can detect the over-current fault on class-D. The fault on the class-D which causes a large current over 3A triggers the OC flag to the digital control system and disables the analog blocks by 200ms. After 200ms cooling time, the OC protection detects the current again to determinate if the OC event is finished.

Under-Voltage Protection

The under-voltage protection can detect the under-voltage fault on power supply VBAT. The UV flag is triggered when VBAT is lower than UVLO, then digital control system disables the analog blocks by 200ms. After 200ms cooling time, the UV protection detects the voltage again to determinate if the UV event is finished.

Over-Temperature Protection

The over-temperature protection can detect the over-temperature fault on the chip. The OT protection is triggered when temperature sensed by TEMP sense is higher than 150°C, then the digital control system disables the analog blocks by 200ms. After 200ms cooling time, the OT protection detects the temperature again to determinate if the OT event is finished with the hysteresis threshold 120°C.

VBAT Sense

The VBAT sense monitors the battery voltage between the range from 2V to 6.375V with 8bit resolution, the output is shown in the register " 0x48 VBAT" with the equation battery voltage (V) = VBAT code (DEC) / 40.

Temp. Sensing

Temperature sense monitors the temperature of the chip with the range between −40°C to 175°C with 9-bit resolution, the output is shown in the register "VPTAT" with the equation code = temperature (K) = temperature (°C) + 273.

Absolute Maximum Ratings (Note 1)

- VBST, PVDD ---------- –0.3 to 13V
- OUTP, OUTN, LX, VSNSP, VSNSN ---------- –0.3V to 13V
- VBAT, IOVDD ---------- –0.3V to 6V
- DVDD, VREF ---------- –0.3V to 2.5V
- LRCK, BCK, DATAI, DATAO, ADS1, WDT/ADS2 ---------- –0.3V to (IOVDD + 0.3V)
- SCL, SDA, INT ---------- –0.3V to 6V
- RSTN ---------- –0.3V to (IOVDD + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-30B 2.25x2.60 (BSC) ---------- 3.44W
- Package Thermal Resistance (Note 2)
  WL-CSP-30B 2.25x2.60 (BSC), θ_{JA} ---------- 29°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- VBAT ---------- 2.7V to 5.5V
- DVDD ---------- 1.71V to 2V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(VBAT = 3.6V, Data bit = 24 bits, BCK mode = 64fs, SR = 48kHz, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Digital I/O Voltage	I_{OVDD}		1.71	1.8	3.6	V
Digital Supply Voltage	DVDD		1.71	1.8	2	V
Speaker Amp Supply Voltage	PVDD		2.7	3.6	9.5	V
Battery Supply Voltage	V_{BAT}		2.7	3.6	5.5	V
UVLO for VBAT	UVLO		2.1	2.3	2.4	V
Iq, Boost in Battery Mode (Note 5)	I_{Q_VBAT}	VBAT and LX	1	3	5	mA
	I_{Q_DVDD}		9	12	15	
ISD on VBAT	I_{SD_VBAT}	DVDD = 1.8V	0	0.5	1	μA
ISD on DVDD	I_{SD_DVDD}	VBAT = 2.7 to 5.5V, DVDD = 1.8V, BCK = LRCK = DAI = 0V	0	4	20	μA
ILEAK in Shipping Mode	I_{LEAK}	VBAT = 4.2V, DVDD = 0V	0	0.5	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System Efficiency	η	P_O = 2.5W, including DC to DC converter, 100Hz audio signal	76	80	84	%
Over-Temperature Protection	OTP		--	150	--	°C
Over-Temperature Protection Hysteresis	ΔOTP		--	30	--	°C
Boost						
Boost Output Voltage	VBST		2.7	--	9.5	V
VBST Accuracy	ΔVBST		–0.1	--	0.1	V
Class-D						
Maximum Output Power	P_O	1kHz, PVDD = 3.6V, 8Ω load, 1% THD + N	0.6	0.65	0.7	W
		1kHz, PVDD = 9.5V, 8Ω load, 1% THD + N	4.7	4.8	4.9	
		1kHz, PVDD = 9.5V, 4Ω load @ 1% THD + N, VBAT = 4.2V	--	6.5	--	
Output Offset Voltage	Vos		0	1	3	mV
Output Noise	Vn	A-weighting	15	20	25	μV
Signal to Noise Ratio	SNR	PVDD = 9.5V, THD + N < 1%, Gain = 15dB, A-weighting	107	109	111	dB
Dynamic Range	DR	–60dBFS, 1kHz, A-weighting, Gain = 15dB	107	109	111	dB
Total Harmonic Distortion + Noise	THD+N	1kHz, P_O = 350mW, 8Ω load	–90	–70	–50	dB
Power Supply Rejection Ratio	$PSRR_{VBAT}$	217Hz, VBAT ripple = 200mVpp	70	80	95	dB
Over-Current Protection of Speaker	OCP_SPK	OUTP/OUTN short to PVDD or PGND, or OUTP short to OUTN	2.7	3	3.3	A
Over-Voltage Protection	OVP		11.5	12	12.5	V
Current Sense						
Resolution			--	16	--	Bits
Accuracy		1A Ipeak, 25°C, PVDD = 3.6 to 9.5V	–3	--	3	%
Temperature Variation		1A Ipeak, 25 to +85°C, PVDD = 3.6 to 9.5V	–5	--	5	%
Signal to Noise Ratio	SNR		65	70	75	dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_O = 3W	–50	–45	–40	dB
Current Sense Full Scale		Peak current which will give full scale digital output	–3	--	3	A
Current Sense Gain Linearity		f = 1kHz from 50mAp to 1Ap	–1.5	--	1.5	%
Voltage Sense						
Resolution			--	16	--	Bits
Accuracy		8V peak voltage	–3	--	3	%
Signal to Noise Ratio	SNR	A-weighting	77	82	87	dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_O = 3W	–60	–55	–50	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Sense Full scale			–12	--	12	V
Voltage Sense Gain linearity		f = 1kHz from 0.4Vp to 8Vp	--	1	--	%
Battery Sense						
Resolution			--	8	--	Bits
Voltage Resolution			–50	--	50	mV
Full Scale Input Voltage			--	6.375	--	V
Accuracy		VBAT = 3.6V	–1	--	1	%
VREF LDO						
Voltage			--	1.5	--	V
Output Capacitor		Output is stable	0.5	1	2.5	μF
I^2C Interface Electrical Characteristics (Note 6)						
SDA, SCL Input Threshold	V_{IH}		0.7 x DVDD	--	--	V
	V_{IL}		--	--	0.3 x DVDD	
Pull-Down Current	I_{FO2}		--	2	--	μA
Digital Output Low (SDA)	V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency	f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3	--	--	μs
Hold Time After (Repeated) Start Condition	$t_{HD,STA}$		0.6	--	--	μs
Repeated Start Condition Setup Time	$t_{SU,STA}$		0.6	--	--	μs
Stop Condition Time	$t_{SU,STD}$		0.6	--	--	μs
Data Hold Time	$t_{HD,DAT (OUT)}$		225	--	--	ns
Input Data Hold Time	$t_{HD,DAT (IN)}$		0	--	900	ns
Data Setup Time	$t_{SU,DAT}$		100	--	--	ns
Clock Low Period	t_{LOW}		1.3	--	--	μs
Clock High Period	t_{HIGH}		0.6	--	--	μs
Clock Data Falling Time	t_F		20	--	300	ns
Clock Data Rising Time	t_R		20	--	300	ns
Spike Suppression Time	t_{SP}		--	--	50	ns
I^2S Interface Electrical Characteristics (Note 6)						
High-Level Input Voltage	V_{IH}		0.7 x DVDD	--	--	V
Low-Level Input Voltage	V_{IL}		--	--	0.3 x DVDD	V
Setup Time, LRCK to SCLK Rising Edge	t_{su1}		10	--	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Hold Time, LRCK from SCLK Rising Edge	t_{h1}		10	--	--	ns
Setup Time, SDIN to SCLK Rising Edge	t_{su2}		10	--	--	ns
Hold Time, SDIN from SCLK Rising Edge	t_{h2}		10	--	--	ns
Rise/fall Time for SCLK/LRCLK	t_r		--	--	8	ns

Note 1. Continuously stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

Note 6. Guaranteed by design.

Typical Application Circuit

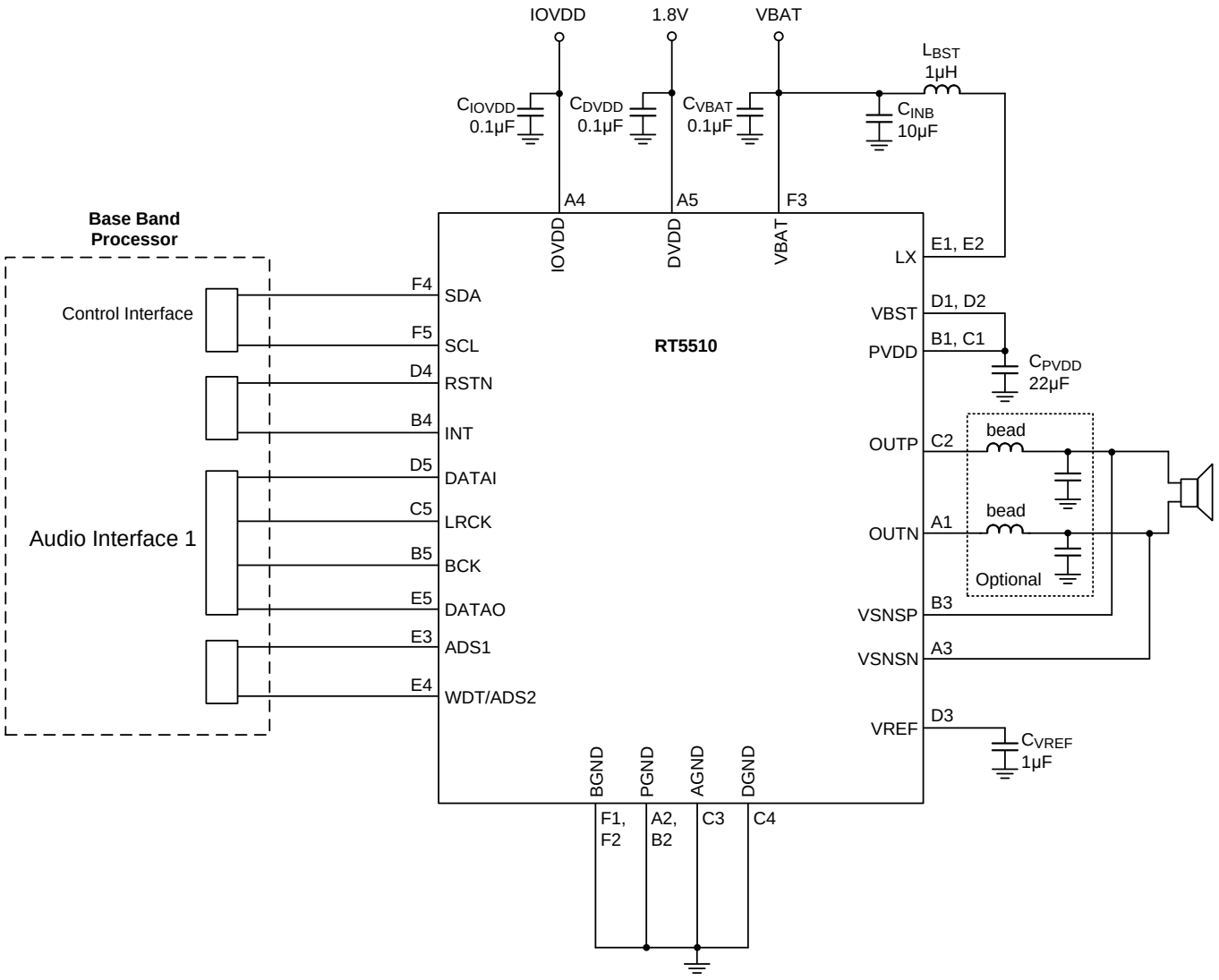
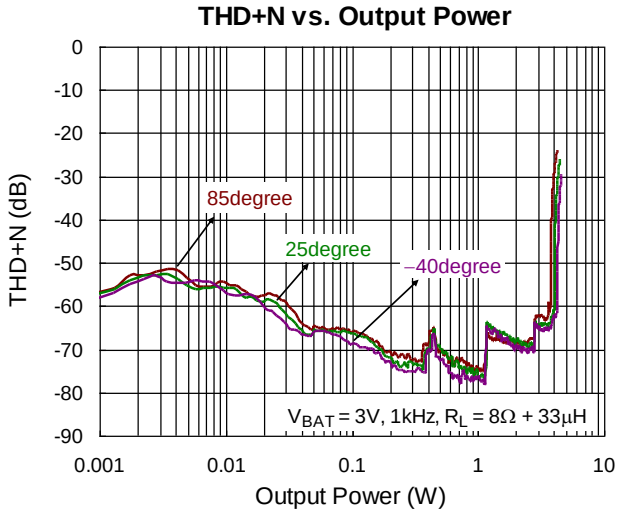
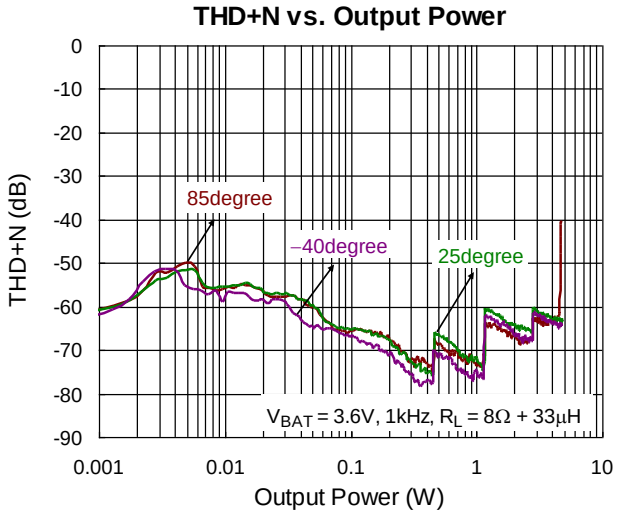


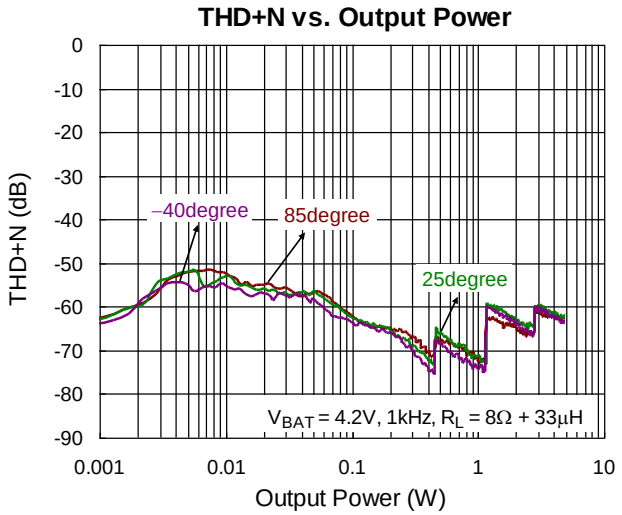
Table 1. Recommended Components Information

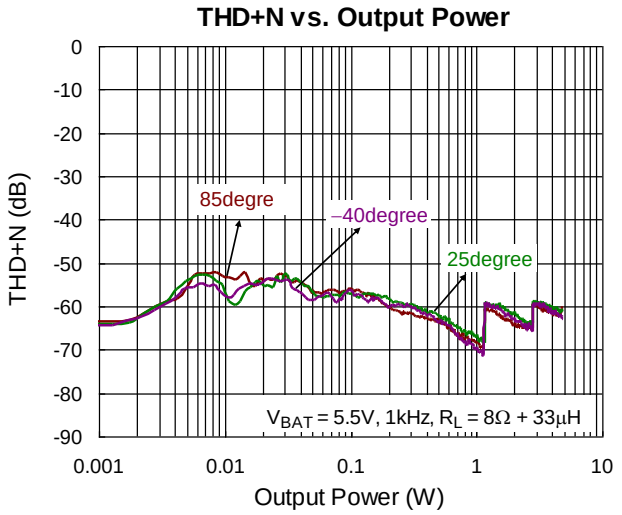
Reference	Part Number	Description	Package	Manufacturer
C_{INB}	GRM155R61A106ME11D	10µF/10V/X5R	0402	muRata
C_{PVDD}	GRM219R61C226ME15L	22µF/16V/X5R	0805	muRata
C_{PVDD}	GRM187R61A226ME15D	22µF/10V/X5R	0603	muRata
L_{BST}	CIGT252010EH1R0MNE	1µH, 4.7A, 30mΩ, ±20%	2.5x2x1.2mm	Samsung

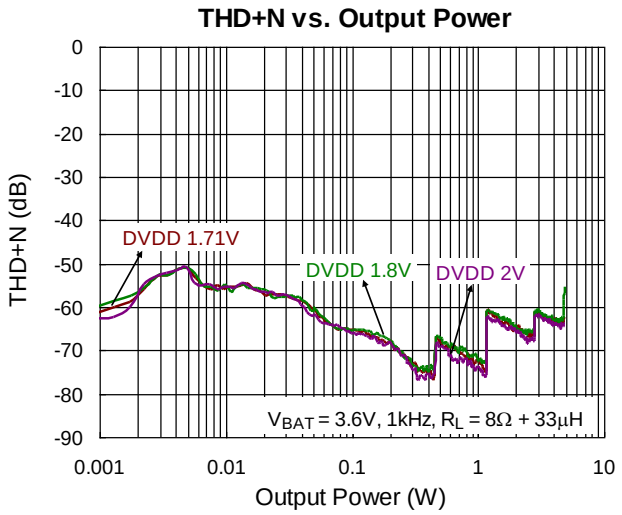
Typical Operating Characteristics

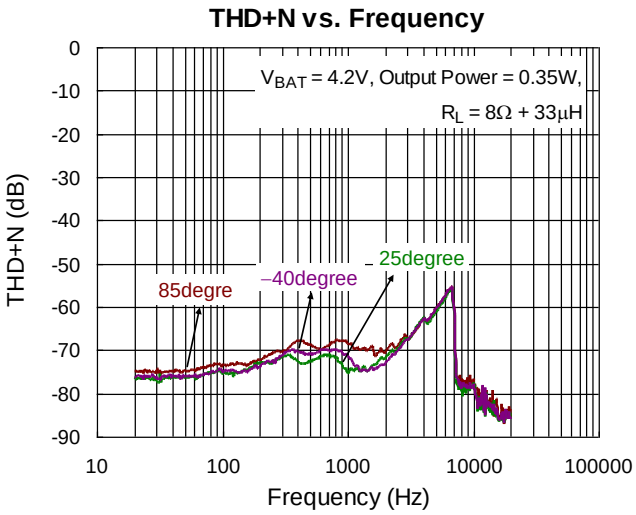




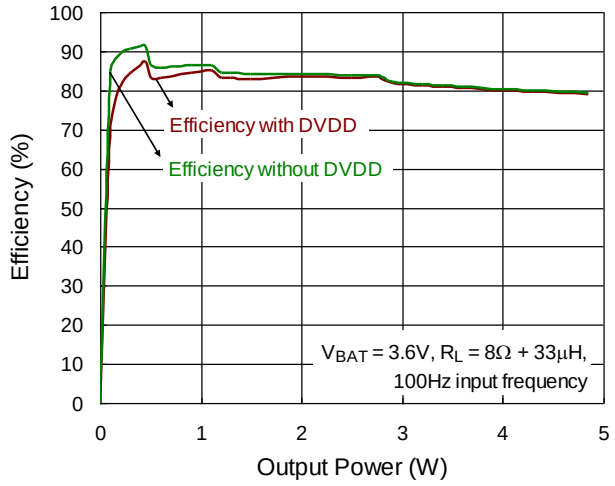




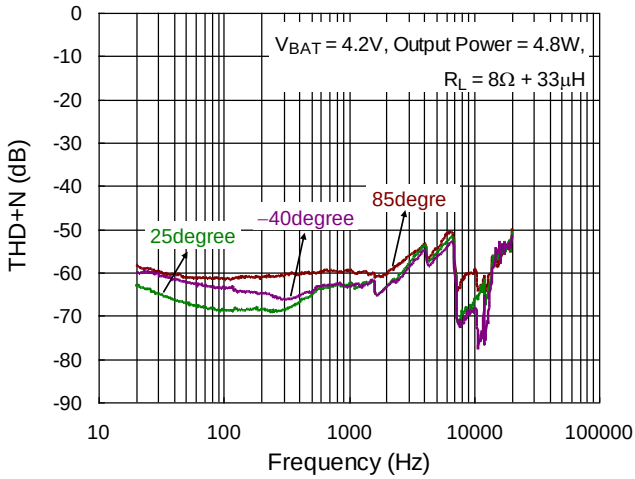




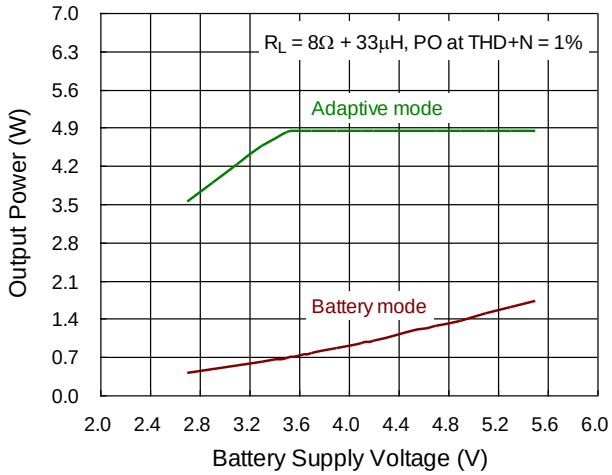
Efficiency vs. Output Power



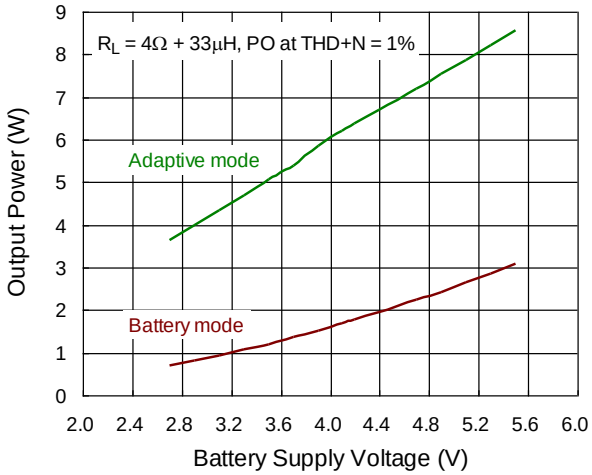
THD+N vs. Frequency



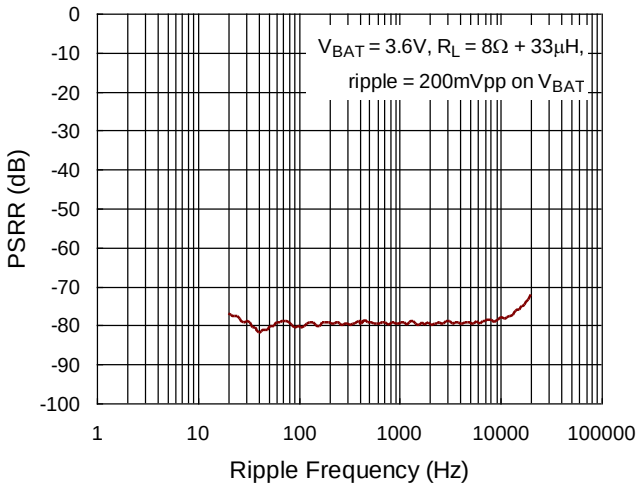
Output Power vs. Battery Supply Voltage



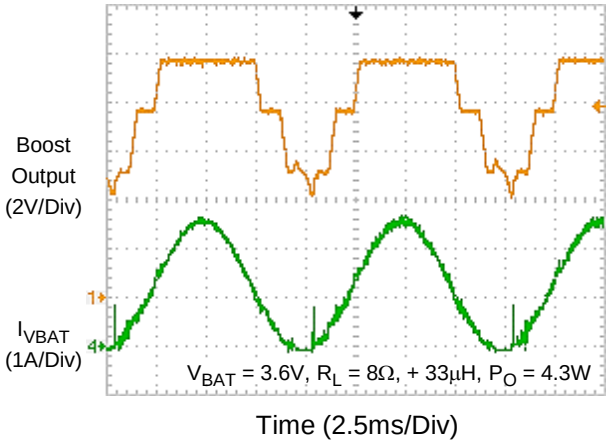
Output Power vs. Battery Supply Voltage



PSRR



Boost Change Mode Behavior



I²C Interface

Device Addressing

The RT5510 supports I²C control interface. The default device address is accessed via ADS1 pin and WDT/ADS2 pin, see Table 2. Address selection via ADS1 pin and WDT/ADS2 pin with four separate address are supported for stereo mode application. The levels on ADS1 pin and WDT/ADS2 pin determine the values of bits 1 and 2, respectively. Note that the RT5510 always monitors the level of ADS1 to change its I²C ID, but the RT5510 will latch the level of WDT/ADS2 once 768μs after the edge of RSTN pin or analog POR goes from low to high or software reset from high to low.

Table 2. Address Selection Via Pins ADS1 and WDT/ADS2

WDT/ADS2 Pin (V)	ADS1 Pin (V)	Address	Function (bit 0)
0	0	0110100x (34H)	0 : write, 1 : read
0	DVDD	0110101x (35H)	0 : write, 1 : read
DVDD	0	0110110x (36H)	0 : write, 1 : read
DVDD	DVDD	0110111x (37H)	0 : write, 1 : read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 = LSB
0	1	1	0	1	WDT/ADS2	ADS1	Bit 0 = LSB

I²C bus wiring is very simple. Only two signal lines SDA (Serial Data Line, Data or address signal) and SCL (Serial Clock Line, Clock signal) are used to perform serial communication between integrated circuits in the system.

The corresponding I²C communication pins in the RT5510 are SDA and SCL.

Typical I²C format is (Start)-[Slave Address]-[Register Address]-[Data]-(Stop). After writing the slave address first, it needs to be written again to specify the register address for reading and writing. The start and stop conditions of I²C are determined by the SDA transition state, while SCL is at logic high level. When SCL is high, the SDA transition from high to low is Start condition. Otherwise, SDA transition from low to high is Stop condition. The I²C Bus protocol stipulates that in addition to the start signal and the stop signal, all signal transmissions are fixed in groups of 8 bits (1 Byte), and the MSB is sent first. After each group (8 bits) signal is sent, the sender needs to read an ACK bit (acknowledged) that the receiver responds. ACK low indicates that the data has been received. ACK is an important basis for judging whether the communication between Master/Slave is normal. For valid I²C data read or write, SDA must keep the signal stable and can't change state when SCL is high in order to correctly read (latch) the data. SDA only allows transitions when SCL is low level.

The serial interface also supports single-byte and multiple-byte read/write function. Please refer to the next paragraph for the RT5510 Read / Write function description.

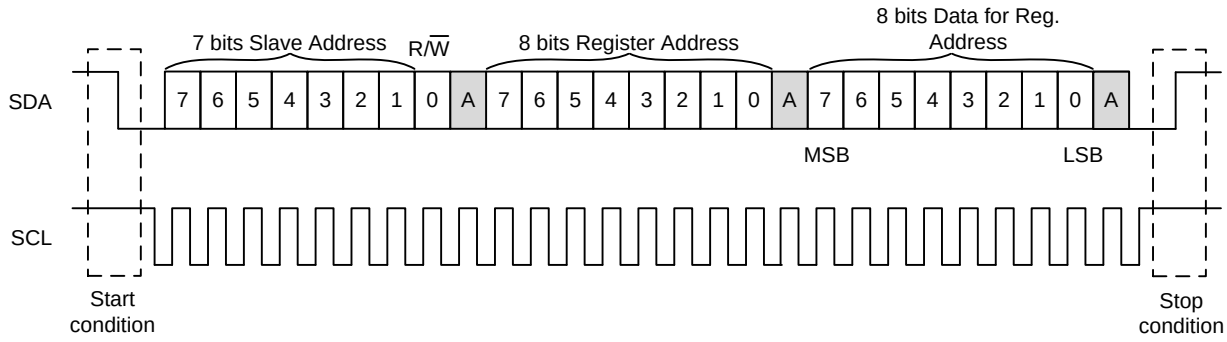


Figure 1. Typical I²C Format

Read and Write Function

The RT5510 single-byte data-read function format is shown in Figure 2.

Data transfer is initiated when the master device transmits a start condition: SDA is pulled low while SCL stays high, followed by the slave address. The data is sampled when SCL rises for the first bit. The read/write bit is set to 0 to declare the RT5510 address byte to be read. After slave device address and the read/write bit, the RT5510 device responds an acknowledge bit. In second step, the master device sends the RT5510 internal memory address to be read and the RT5510 responds with an acknowledge bit. Then the master device sends start condition again followed by setting the RT5510 device address and read/write bit to 1, and the RT5510 device responds an acknowledge bit. (Setting the read/write bit to 1 represents read internal memory address data.)

The RT5510 sends out data from the register to read. After receiving register data, the master device replies no-acknowledge bit (SDA go high) to indicate that it has not continued to read the data. Then master device sends stop condition (when SDA is pulled high while SCL is high) to complete the single-byte data reading function.

About read multiple data byte, the format is the same as reading a single data byte, and the only difference is the data byte amount sent form slave device. The master device replies with an acknowledge bit after receiving each data byte. After the RT5510 sends the last data byte, the master device replies no-acknowledge bit and transmits a stop condition.

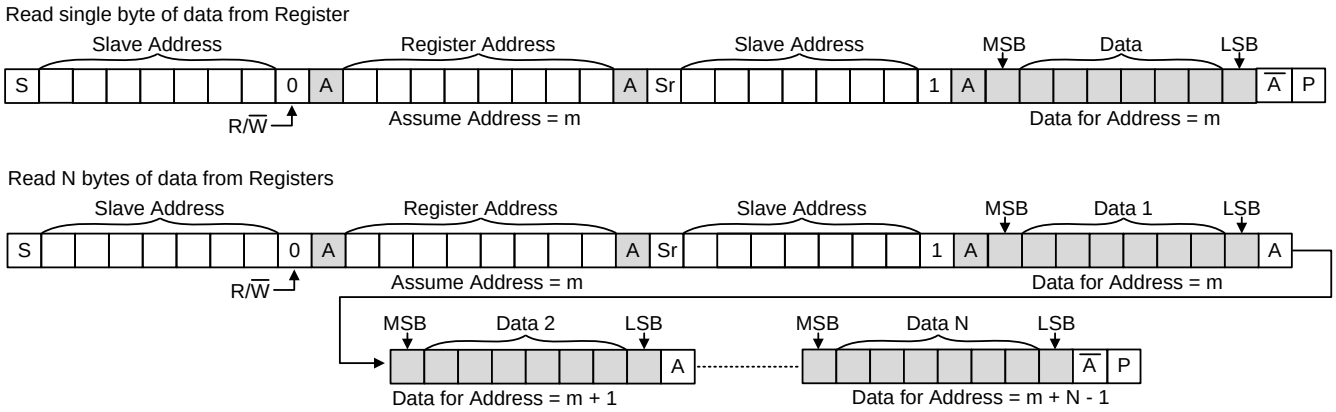


Figure 2. Single-byte and Multiple-byte I²C Read Format

The RT5510 single-byte data-write function format is shown in Figure 3.

Data transfer is initiated when the master device transmit a start condition: SDA is pulled low while SCL stays high, followed by the slave address. The data is sampled when SCL rises for the first bit. The read/write bit is set to 0 to declare the RT5510 address byte to be write. After slave device address and the read/write bit, the RT5510 device responds an acknowledge bit. In second step, the master device sends the RT5510 internal memory address to be written and the RT5510 responds with an acknowledge bit. Then master device sends out data to write in RT5510 internal memory address. After receiving register data, the RT5510 replies an acknowledge bit to indicate that the data is received. Then master device sends stop condition (when SDA is pulled high while SCL is high) to complete the single-byte data write function.

About write multiple data byte, the format is the same as write a single data byte, and the only difference is the data byte amount sent form master device. The slave device replies with an acknowledge bit after receiving each data byte. After the RT5510 receives the last data byte, the RT5510 replies an acknowledge bit and master device transmits a stop condition.

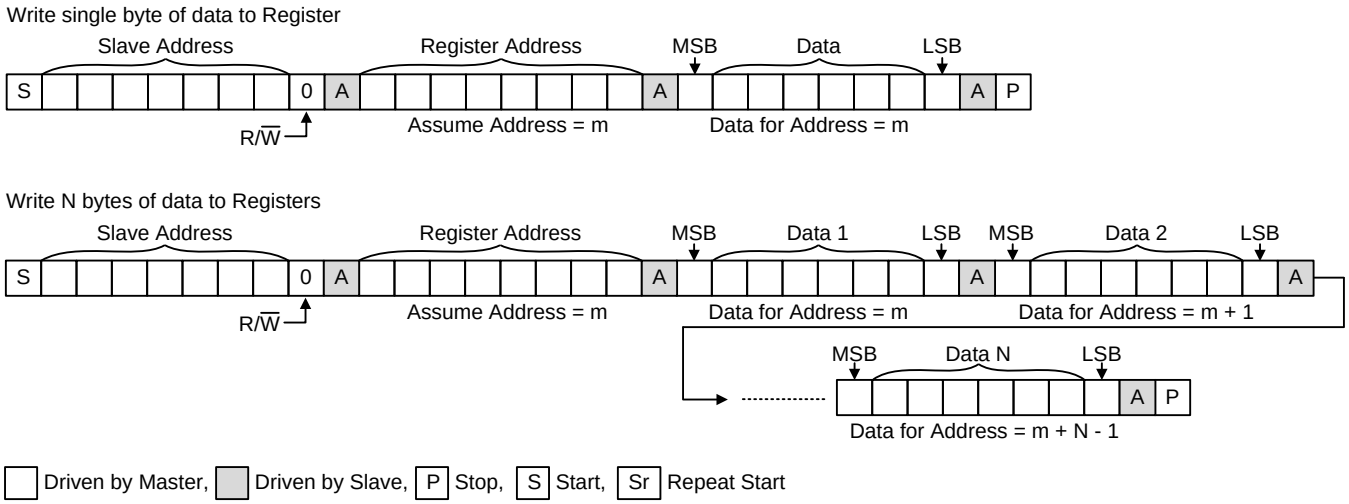


Figure 3. Single-byte and Multiple-byte I^2C Format

I²C Waveform Information

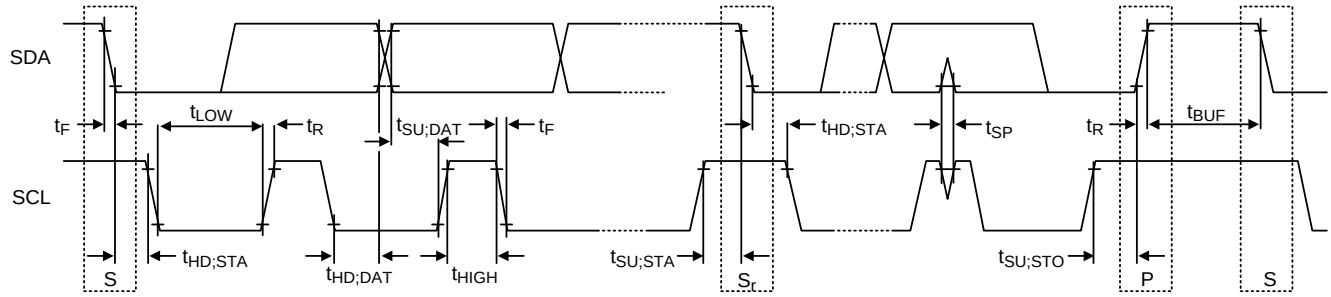


Figure 4. Timing Diagram of I²C Interface

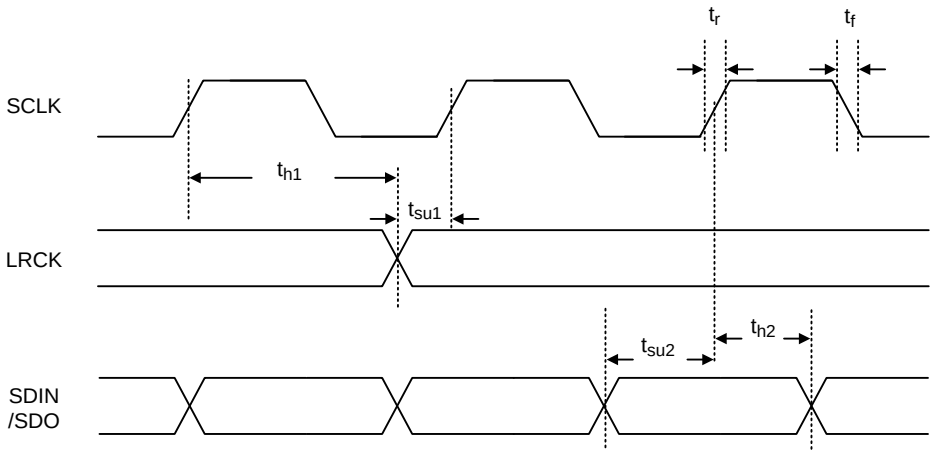


Figure 5. Timing Diagram of Slave Mode I²S Interface

Operation Mode Modes

The RT5510 can operate in four different modes which are power-down/suspend/operating/fault. Internal functional block operational status in different modes is depicted in Figure 6.

Mode / Blk	PWDN	SUSP	OP	FAULT
PLL	✕	○	○	○
I^2C	○	○	○	○
I^2S	✕	✕	○	○
AMP	✕	✕	○	✕

○ : Normal operation

✕ : Power down

Figure 6. Operation Mode

Mode	Condition	Description
Power-down	PWDN = 1	1. When PWDN is set to 1, chip will enter power-down mode. 2. Power consumption is minimum and PWM outputs are floating. 3. I^2C bus remains awake. 4. I^2S path is disable.
Suspend	BCK/SR invalid	1. Chip will enter suspend mode. 2. Most of the data path are off, and PWM outputs are floating. 3. I^2C bus remains awake. 4. PLL keeps in free-run mode and CK1M is used to monitor BCK/SR on I^2S bus to see if they are correct.
Operating	BCK & SR valid PWDN = 0 AMPE = 1	1. If set PWDN/AMPE at register 0x03 as condition, chip will enter operating mode when BCK and sampling rate are valid.
Fault	OV/OT/OC/UV = 1	1. Chip enters fault mode when an error event of physical protection mechanisms occurs (OCP/OVP/UVP/OTP). 2. The boost and AMP are OFF. 3. The system exits from Fault mode after the protection event released for a checking cycle of about 200ms.

Mode Transition

The state machine of mode transition is shown in Figure 7. After power on, the control bit will always be reset to PWDN mode.

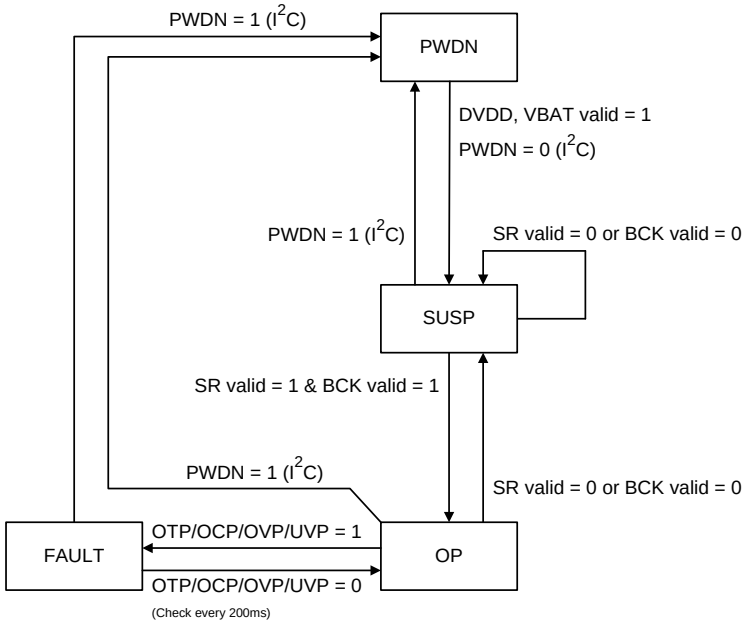


Figure 7. Mode Transition

Power ON/OFF Sequence

The power on sequence is shown in Figure 8. After power is valid, two groups of control signals should be set.

I2C : PWDN and AMPE should be programmed. These two bits can be programmed by single command since they are at the same byte address.

I2S : BCK should be valid on the specified interface.

If the PWDN is set to 0 before the BCK is valid, it will go to SUSP mode automatically. The output of amplifier will be valid after entering OP mode Signal ramp up will always be implemented when the mode transits from PWDN or SUSP mode to OP mode.

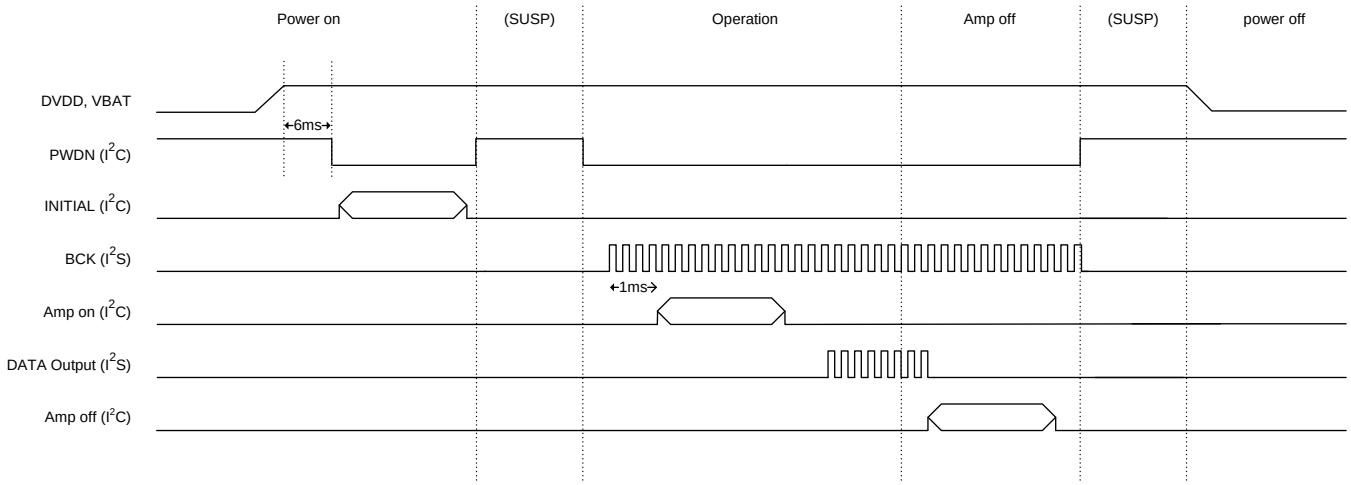


Figure 8. Power ON/OFF Sequence

I²S Mode Change without PWDN

When I²S mode change, like BCK and LRCK frequency relationship, the chip will not be shut down. If the clock source from I²S changes, I²S invalid is detected. In this case, soft muting is implemented before entering Amp off situation. In the opposite situation, if the clock source from I²S is detected valid again, signal ramp up is implemented at the start after it enters the operating mode.

The above procedure is shown in Figure 9 and ramp is setting by register 0x 28 bit [2:0].

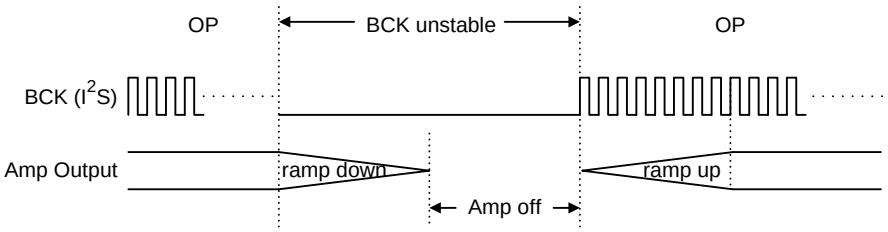


Figure 9. I²S Mode Change without PWDN

Table 3. Ramp Control Setting

Register	Bits	Bits Name	Description
0x28	2:0	VOLCTRL	Ramp control when new volume setting is different from old setting : 000 : No ramp up/down (default) 001 : 0.5db per sample 010 : 0.5db per 2 samples 011 : 0.5dB per 4 samples 100 : 0.5dB per 8 samples 101 : 0.5dB per 16 samples 110 : 0.5dB per 32 samples 111 : 0.5dB per 64 samples

Data (I^2S) Interface

Data Format

The I^2S formats supported by the RT5510 are listed below :

Table 4. Data Format List

Interface	Data Format	BCK Frequency
I^2S Standard	up to 16bit	32fs
I^2S Standard	up to 24bit	48fs
I^2S Standard	up to 24bit	64fs
Left-justified	up to 16bit	32fs
Left-justified	up to 24bit	48fs
Left-justified	up to 24bit	64fs
Right-justified (16-bit)	16bit	32fs
Right-justified (16-bit)	16bit	48fs
Right-justified (16-bit)	16bit	64fs
Right-justified (18-bit)	18bit	48fs
Right-justified (18-bit)	18bit	64fs
Right-justified (20-bit)	20bit	48fs
Right-justified (20-bit)	20bit	64fs
Right-justified (24-bit)	24bit	48fs
Right-justified (24-bit)	24bit	64fs
TDM 8-slot	64bit	64fs
TDM 16-slot	128bit	128fs
TDM 32-slot	256bit	256fs

fs : 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz

I^2S Sampling Rate

I^2S can support sampling rate of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz.

Output Path

DATAO uses BCK as the reference clock to transmit selected data. The LRCK is treated as channel select for I^2S mode and frame synchronizer in TDM mode.

The Digital Audio interface supports I^2S and TDM formats at various sample rates from 8kHz to 96kHz. The interface is compliant with all I^2S interface configurations and supports a wide range of TDM interface configurations (up to 16-channel at fs = 48kHz). The LSB and MSB must be supported. The signal name is defined as :

1. IMON : The current sense signal.
2. VMON : The voltage sense signal.
3. VBAT : The voltage sense for battery.
4. VTEMP : The temperature sense of chip.

5. SPKPROT_GAIN : The gain of safeguard for speaker protection.

When only one smart PA is connected, I²S bus is recommended. At this situation, signal sequence should be VMON, VTEMP, VBAT, IMON and SPKPROT_GAIN. The SDI signal is only 16bit available for each channel.

The sequence is shown as below :

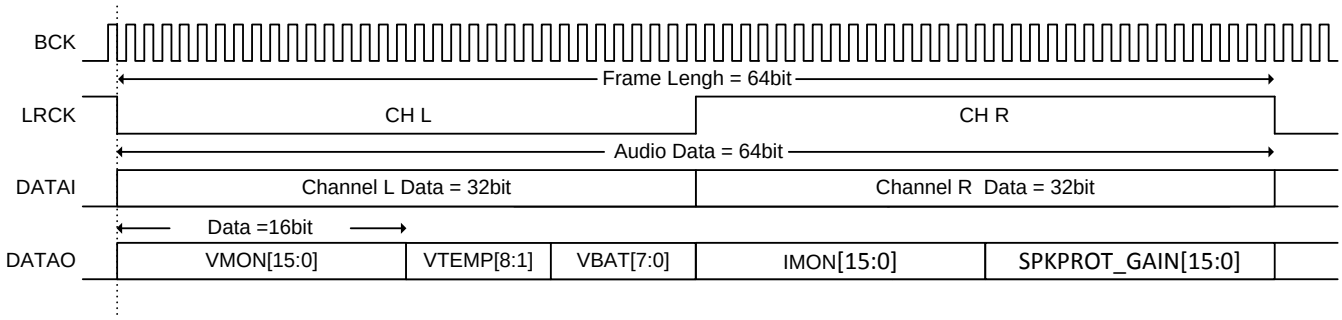


Figure 10. Only One Smart PA I²S Left-Justified Format

When two smart PA is connected and the I²S is used, the VTEMP, VBAT and SPKPROT_GAIN signal must be disabled. The SDI signal is only 16bit available for each channel.

The sequence is shown as below :

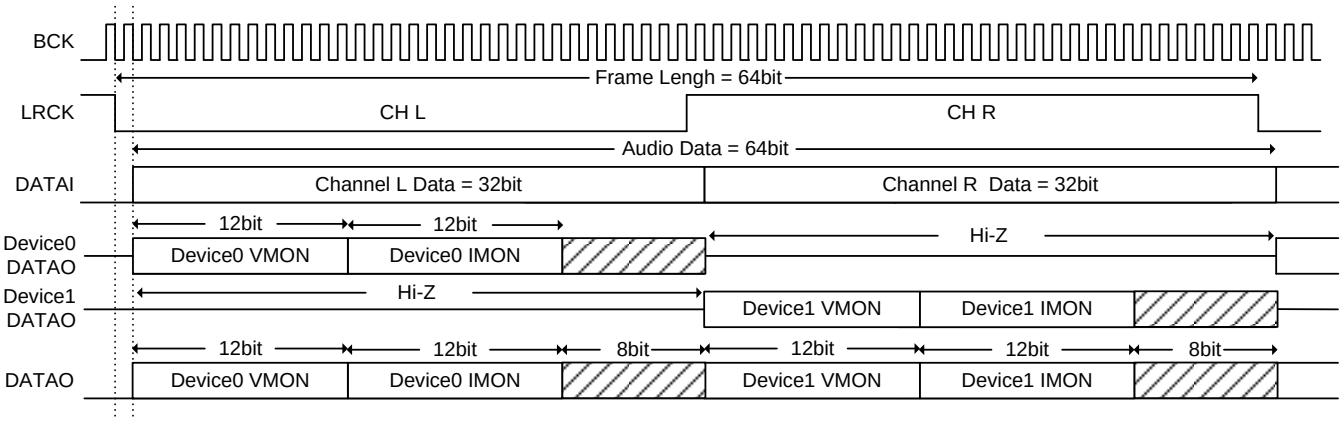


Figure 11. Two Smart PA I²S Standard Format

TX Data Structuring in I²S Mode

Table 5. TX Data Structuring in I²S Mode

I²SDOLS I²SDORS	Left Channel				Right Channel	
	bit 0-7	bit 8-15	bit 16-23	bit 24-31	bit 0-15	bit 16-31
000	VMON[15:0]		VTEMP[8:1]	VBAT[7:0]	IMON[15:0]	SPKPROT_GAIN[15:0]
001	DAC_BIQ[23:0]			8'h0	{DC_CUT_DATA[25:0], 8'h0}	
010	Hi-Z[31:0]				VMON[15:4]	IMON[15:4] 8'h00
011	VMON[15:4]	IMON[15:4]		8'h0	Hi-Z[31:0]	

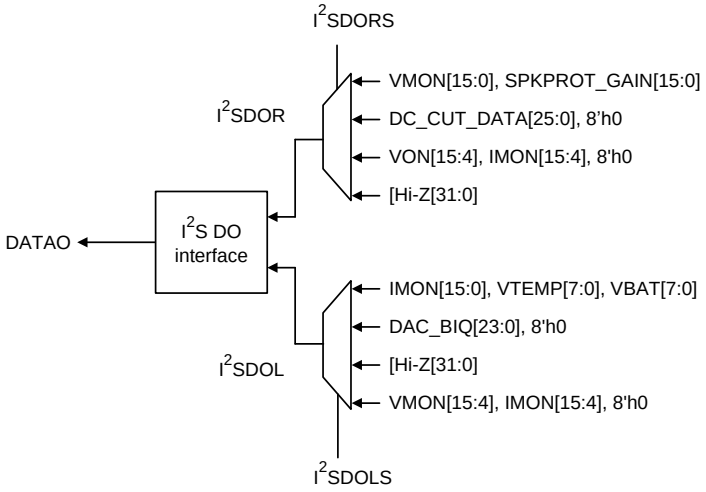


Figure 12. I²S Output Mux

When two smart PA is connected and TDM mode is used. At this mode, the frame length should be set to 128bit. The SDI signal is only 16bit available for each channel. The minimum LRCK length is 2 BCK length.

The sequence is shown as below :

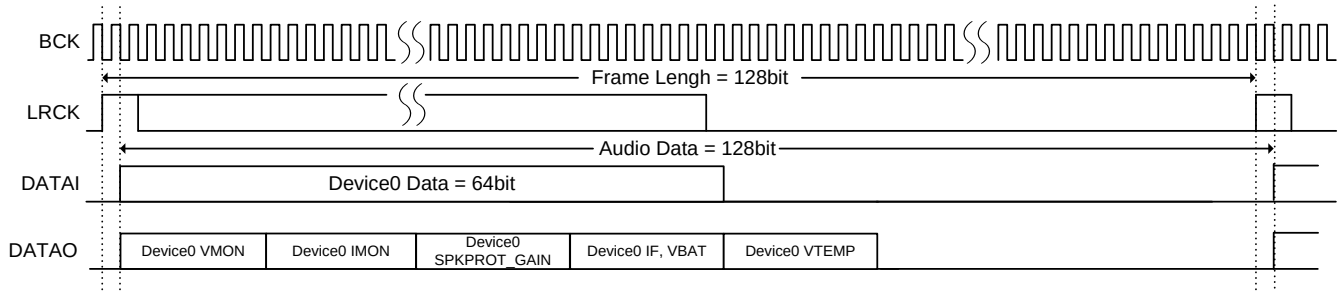


Figure 13. One Smart PA TDM Standard Format

The TDM_TX_LOC register indicates the starting slot to put the data stream on SDOUT pin and the TDM_TX_LEN whose unit is byte (slot) determines how many bytes will be transmitted. Please refer to the TX Data Structuring in I²S Mode section.

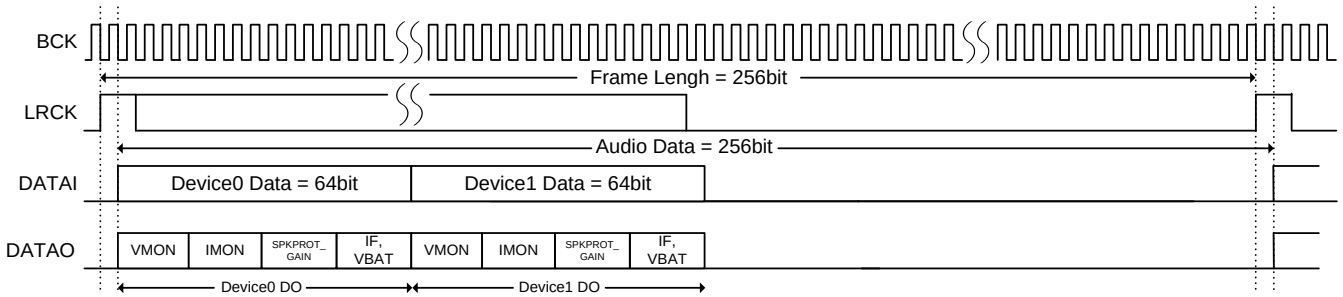
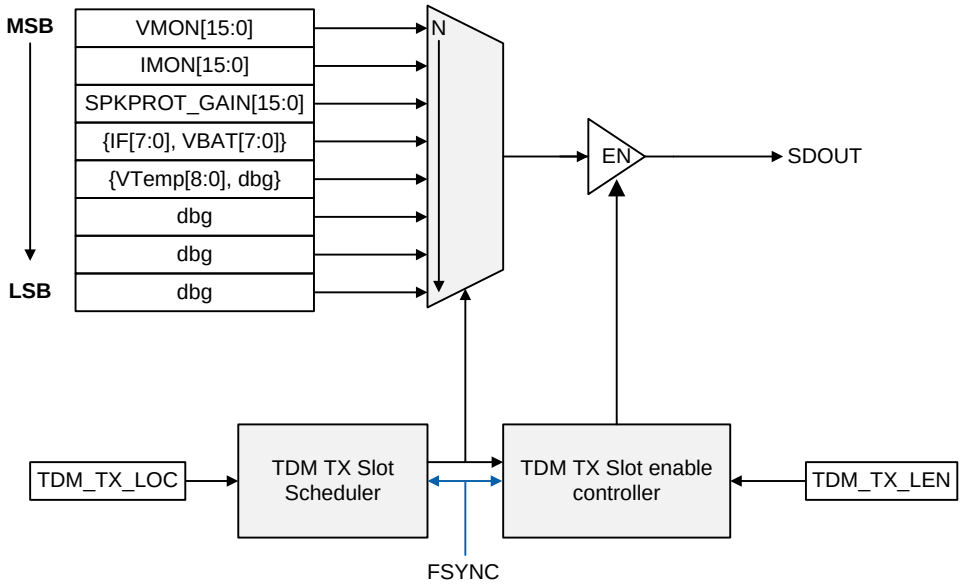


Figure 14. Two Smart PA TDM Standard Format

TX Data Structuring in TDM Mode

The RT5510 can transmit {VMON[15:0], IMON[15:0], SPKPROT_GAIN[15:0], IF[7:0], VBAT[7:0], VTemp[8:0], dbg[54:0]} to I^2S SDOUT in TDM mode. The TDM_TX_LOC register indicates the starting slot to put the data stream on SDOUT pin. The sequence of data stream in TDM mode is {VMON[15:0], IMON[15:0], SPKPROT_GAIN[15:0], IF[7:0], VBAT[7:0], VTemp[8:0], dbg[54:0]} and MSB-first. The TDM_TX_LEN whose unit is byte (slot) determines how many bytes will be transmitted, from MSB to the (TDM_TX_LEN)th slot. The rest of slots outside of the transmitted data stream shall be keep Hi-Z.



* IF[7:0] is the register 0x05 interrupt flag.

* dbg is only for testing.

Figure 15. TX Data Structuring in TDM Mode

RX Data in TDM Mode

The data in the TDM stream that is allocated for assignment to the internal data registers is extracted using the TDM_RX_LOC and TDM_RX_LEN controls. Data is extracted MSB-first, starting at the TDM_RX_LOC location and placing it into its respective internal data register. This process continues until TDM_RX_LEN bits are extracted from the TDM stream or another data extraction begins.

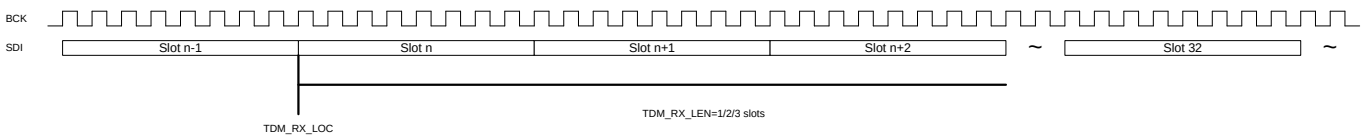


Figure 16. RX Data Structuring in TDM Mode

Application Information

Watchdog

When enable, the watchdog block monitors the edge-to-edge period of the watchdog input signal. If the period between edges is greater than the watchdog timer setting, the watchdog input signal is invalid. It means the protection algorithm is no longer function normally. The boost and speaker amplifier should be automatically disable to prevent damage. When the period between edges of watchdog input signal becomes less than the timer setting, the boost and speaker amplifier will be automatically enable. Please refer to Table 6.

Table 6. Amp Behavior Configuration at Watchdog Timeout

Name	Description
WD_RESP = 00	The Amp neither mutes nor shut down when the watchdog is triggered. The boost converter's output voltage is not affected.
WD_RESP = 01	The Amp shuts down immediately and the output transition is Hi-Z. The boost converter ramps down to VBAT then enters bypass mode.
WD_RESP = 10	The Amp mutes according to the configuration of VOLCTRL, instant mute or soft mute. The boost converter ramps down to VBAT then enters bypass mode.
WD_RESP = 11	Signal in is multiplied by WD_RP when watchdog timeout is happened, instead of R_VOLUME.

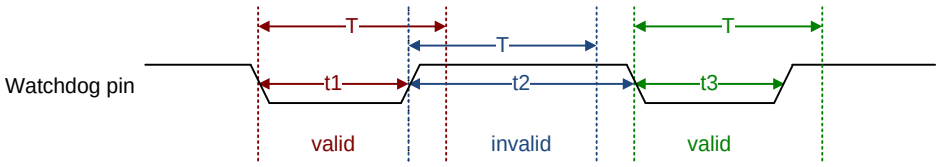


Figure 17. Watchdog Timeout Edge Rate Configuration

In the Figure 17, the period t1 between edges is less the timer setting T. The watchdog input signal is valid, so the chip keeps functioning normally. However, in the next period, t2 is larger than T. The watchdog input signal becomes invalid and the boost and speak amplifier are turned off. In the following period, t3 turns to be less than T. Then, the boost and speaker amplifier are turned on again.

Boost Mode and Signal Tracking Behavior

The RT5510 boost converter has three modes of operation : battery mode, fixed mode and adaptive mode. The operating mode is usually set to adaptive mode for optimum efficiency. Please refer to below table to set the operating mode :

Table 7. Boost Mode Selection

Register	Bits	Bits Name	Description
0x40	1:0	BST mode	00 : Disable (default) 01 : Battery mode 10 : Fixed mode 11 : Adaptive mode

According to the I²S input signal change, the RT5510 boost class-G algorithm can determine the voltage required by the speaker output signal to achieve the best efficiency.

The boost algorithm calculates the voltage of the speaker output signal and compares it with the threshold voltage of the boost converter change mode to determine whether the boost converter output voltage needs to be changed. The boost converter has up to three output voltage configurations that can be set by the user.

When the boost converter is configured in adaptive mode, the speaker output signal is lower than threshold 3 voltage. The boost converter is bypassed and supplied directly to the load by the battery. When the speaker output signal is higher than threshold 3 voltage, boost converter enable and the boost output is set to target 3 voltage. This is for the speaker output signal to have a margin and avoid the phenomenon of clipping. In the same way, when the speaker output signal is higher than threshold 2 voltage, boost converter enables and the boost output is set to target 2 voltage. The boost converter has a maximum configurable voltage of 9.5V.

When estimating the voltage drop of the output signal, the Boost algorithm is compared to the threshold voltage to determine whether to change the output voltage of the boost converter.

When the Boost algorithm determines that the speaker output signal is lower than the threshold 1 voltage, the boost converter output voltage has a hold time of 500μs to maintain the original output voltage to ensure that the signal becomes larger again. After the hold time, the boost converter reduces the output voltage to the target 2 voltage. In the same way, the speaker output signal is below the threshold 3 voltage. After the hold time, the boost converter reduces the output voltage and is configured to bypass, supplying the load energy directly from the battery.

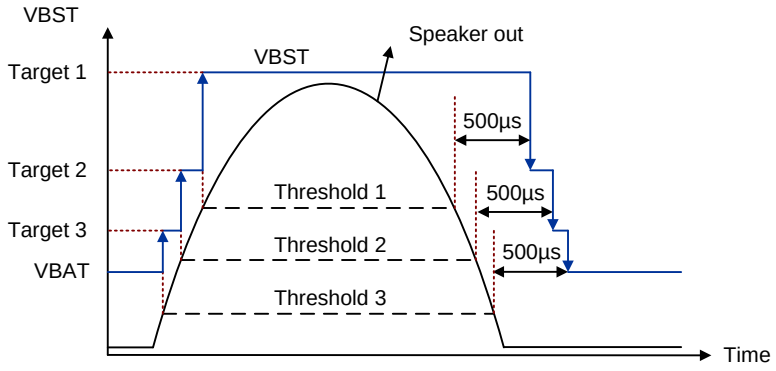


Figure 18. Boost Behavior

The RT5510 I²S input signal is converted and processed by the DAC to a speaker output with a delay time of approximately 430μs. The boost algorithm calculates the voltage of the speaker output signal from I²S to directly control the boost converter output voltage. This means that the boost output voltage is 430μs faster than the speaker output signal. This ensures that the speaker output signal gets enough voltage level from boost converter.

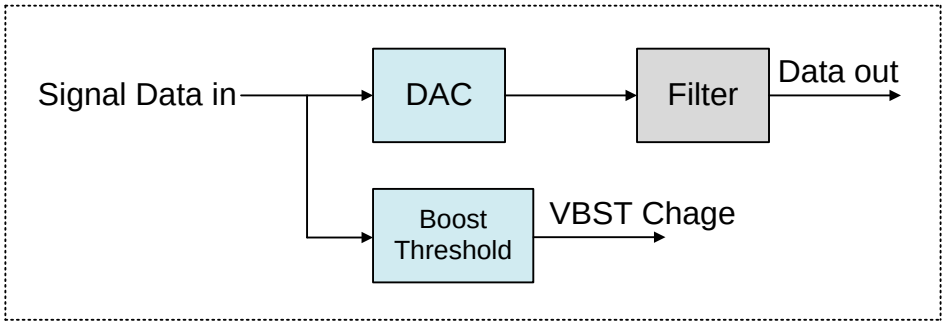


Figure 19. DAC and Processing Time

Boost output voltage and change mode threshold register are shown in below table. BST_TH indicates the threshold at which the boost converter changes the output voltage, and BST_THT indicates the target voltage to be outputted by the boost converter.

Table 8. Boost Output Voltage and Change Mode Threshold

Register	Bits	Bits Name	Description
0x41	11:6	BST_THT1	VBST target in fixed mode or highest VBST target in adaptive mode 000000 : Disabled 000001 to 100001 : 2.9 + BST_THT1 x 0.2V e.g. 000001 : 3.1V, 100001 : 9.5V (default) 100010 to 111111 : Reserved
	5:0	BST_TH1	Boost threshold for BST_THT1 000000 : Disabled 000001 to 100001 : 1.3+ BST_TH1 x 0.2V e.g. 000001 : 1.5V, 100001 : 7.9V 011011 : 6.7V (default) 100010 to 111111 : Reserved
0x42	11:6	BST_THT2	Middle VBST target in adaptive mode 000000 : Disabled 000001 to 100001 : 2.9 + BST_THT2 x 0.2V e.g. 000001 : 3.1V, 100001 : 9.5V 010111 : 7.5V (default) 100010 to 111111 : Reserved
	5:0	BST_TH2	Boost threshold for BST_THT2 000000 : Disabled 000001 to 100001 : 1.3+ BST_TH2 x 0.2V e.g. 000001 : 1.5V, 100001 : 7.9V 001111 : 4.3V (default) 100010 to 111111 : Reserved

Register	Bits	Bits Name	Description
0x43	11:6	BST_THT3	Lowest VBST target in adaptive mode 000000 : Disabled 000001 to 100001 : 2.9 + BST_THT3 x 0.2V e.g. 000001 : 3.1V, 100001 : 9.5V 001011 : 5.1V (default) 100010 to 111111 : Reserved
	5:0	BST_TH3	Boost threshold for BST_THT3 000000 : Disabled 000001 to 100001 : 1.3+ BST_TH3 x 0.2V e.g. 000001 : 1.5V, 100001 : 7.9V 000111 : 2.7V (default) 100010 to 111111 : Reserved

Boost Current Limit

The RT5510 boost converter has a configurable current limit function. The default current limit is 4A. This setting can meet the application of R_L = 8Ω and output 4.8W. This limit value can be set lower according to the selected inductor. Please refer to Table 9 to set the required limit value. If the CC_MAX set value is small, the output power will be limited. The CC_MAX value from 0000000 to 0110100 and 1111110 to 1111111 are not allowed for use.

Table 9. Boost Current Limitation

Register	Bits	Bits Name	Description
0x45	6:0	CC_MAX	0110101 : 2A 1000011 : 2.5A 1010001 : 3A 1011111 : 3.5A 1100111 : 4A (default) 1101111 : 4.5A 1111101 : 5A

Clip Control

When the battery voltage is low, playing music causes an instantaneous voltage drop of the battery voltage, which may cause the system to malfunction or restart.

To avoid similar issue, the RT5510 has built-in battery sense and safeguard features. By detecting the battery voltage, the safeguard function is activated when VBAT is low. The RT5510 class-D output voltage upper limit is controlled according to the set clip slope. When the output voltage is lower than the upper limit of clip slop, the class-D output voltage will not be attenuated. When the class-D output voltage exceeds the upper limit of clip slop, the safeguard will start to attenuate the gain and cause the class-D output voltage to drop to the upper limit of the clip slop set value. In the working range of the safeguard function, the upper limit of the class-D output voltage is dynamic and vary with battery voltage. When the battery voltage is reduced, the class-D output voltage will decay. Since the output voltage is lower, the current consumption is reduced, the battery voltage doesn't have excessive voltage drop when playing music.

To enable the safeguard function on the RT5510, it can be set by the register 0x30 bit 0 setting1 (Enable clip means safeguard function enable). If register 0x30 bit 0 setting is 0, the RT5510 does not execute safeguard, then the excessive output signal will be clipped according to the set clip control parameter.

Table 10. Safeguard Function Mode Selection

Register	Bits	Bits Name	Description
0x30	0	CLPE	0 : Disable 1 : Enable clip (default)

The safeguard is executed according to the parameter of the clip control. Clip control related parameters are VBCPS (Battery Clip Threshold), CPSLP (Clip Slope), MINCLS (Minimum Battery Clip Threshold, VOMIN).

In addition to the above parameters, the user can configure battery voltage recovery hysteresis, rate of VO threshold recovery when VBAT returns and rate of VO threshold drops when VBAT is low, making the operation more flexible.

The clip control is shown in Figure 20.

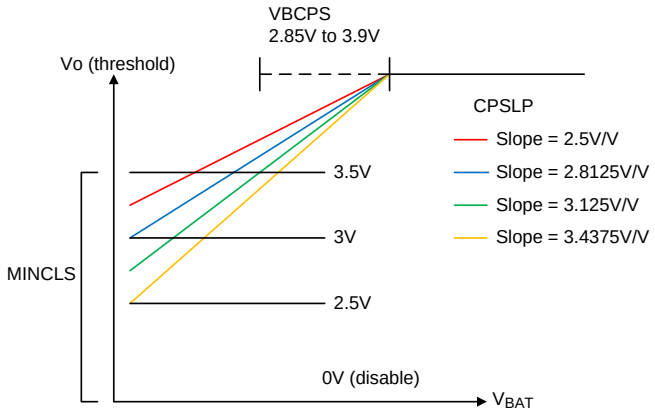


Figure 20. Clip Control

The slope of clip threshold (Vo/VBAT) can be set by CPSLP from 2.5V/V to 3.4375V/V. A Vo stop point (0, 2.5V, 3V or 3.5V) for clip threshold can be set via MINCLS. The output voltage drop will stops at this point. The clip threshold is calculated through the following equation :

ClipThres = SIGMAX – (VBCPS – VBAT) x CPSLP for clip threshold ≥ MINCLS

ClipThres = MINCLS for clip threshold ≤ MINCLS

The detail function is shown below, the dropping rate of threshold can be set via CLIPDR register.

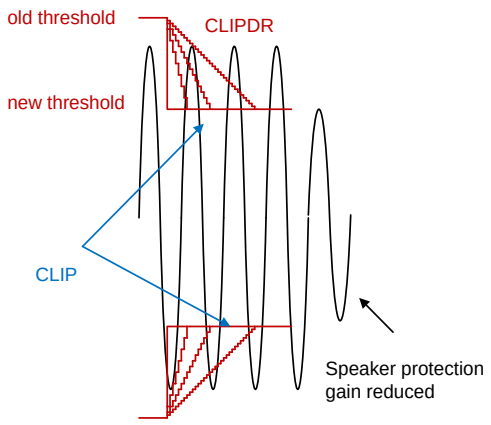


Figure 21. Safeguard Function Gain Reduced

If battery voltage returns to a hysteresis level, ClipThres will increase by a rate of CLIPRR to a certain level which is defined by VBCPS, CPSLP and VBAT. The battery voltage hysteresis can be set via BVHYS register.

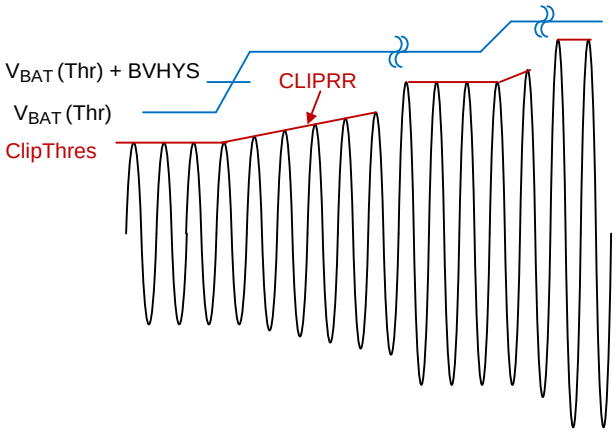


Figure 22. Clip Threshold Depend on VBAT

Hard Clipping

When Hard clip is enabled (Register 0x24 bit 8), if the digital signal is larger than HARD_CLIP_TH, the signal will be clamped to HARD_CLIP_TH.

Table 11. Hard Clipping

Register	Bits	Bits Name	Description
0x24	8	HARD_CLIP_EN	0 : Disable hard clipping 1 : Enable hard clipping (default)
	7:0	HARD_CLIP_TH	Hard clip threshold if HARD_CLIP_EN = 1 downward, 12 to –115.5dB in –0.5dB step, (default 00000000 = 12dB) e.g. 00000001 = 11.5dB

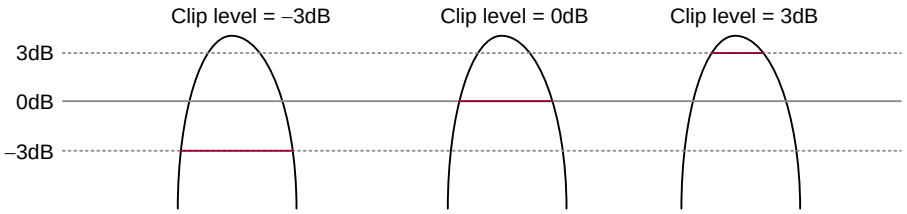


Figure 23. Signal Hard Clipping

DRE

In the signal path, the noise floor of SPK output is related to the analog gain. If decreasing the analog gain, the noise floor decreases, and vice versa. However, increasing the digital gain will not affect the noise floor. To help eliminating unwanted low level noise caused by analog circuit when incoming signal is below a certain threshold, a DRE technique is used. The DRE, Dynamic Range Expansion, stands for expanding the dynamic range of a signal. Any signal before entering analog circuit below the threshold is expanded by the specified ratio, and also the analog end is compressed by the inverse of this ratio.

The function block is depicted as below. DRE controller will monitor the signal and check if it is smaller than the threshold. If the signal is continuously smaller than the threshold for a certain time, the digital gain will be raised to current analog gain and the analog gain will be reduced to 0dB to keep the overall path gain unchanged.

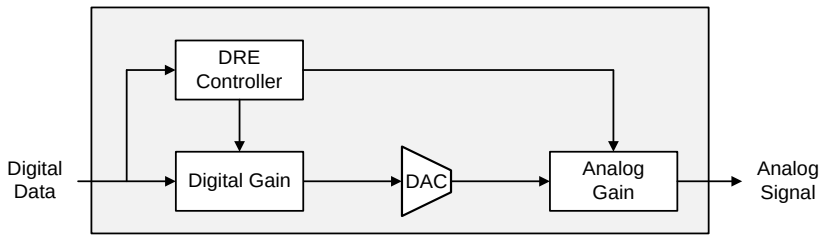


Figure 24. DRE Function Block

There are some parameters necessary to be configured before enabling DRE. The Threshold, (0x69), is the trigger point to enter or leave DRE. Before entering DRE, the Hold Time, (0x68[2:1]), is the time before starting to find zero cross point when signal < Threshold is triggered. In Zero crossing stage, the Hold Time is also used to timeout this stage if no zero cross is detected. The Coarse delay, (0x6B[4:0]), is used to delay the gain-changing time of digital and analog end after finding zero cross stage. The gain-changing time for digital, (0x6A[9:0]), and analog end, (0x6A[29:20]), can be both fine-tuned to compensate the path delay from digital end to analog end. During DRE, if any signal is detected as larger than Threshold, it is going to leaving DRE after zero cross point is detected or Hold Time is expired. Also, the Coarse delay, Analog fine delay and Digital fine delay are applied to compensate the path delay between digital end and analog end.

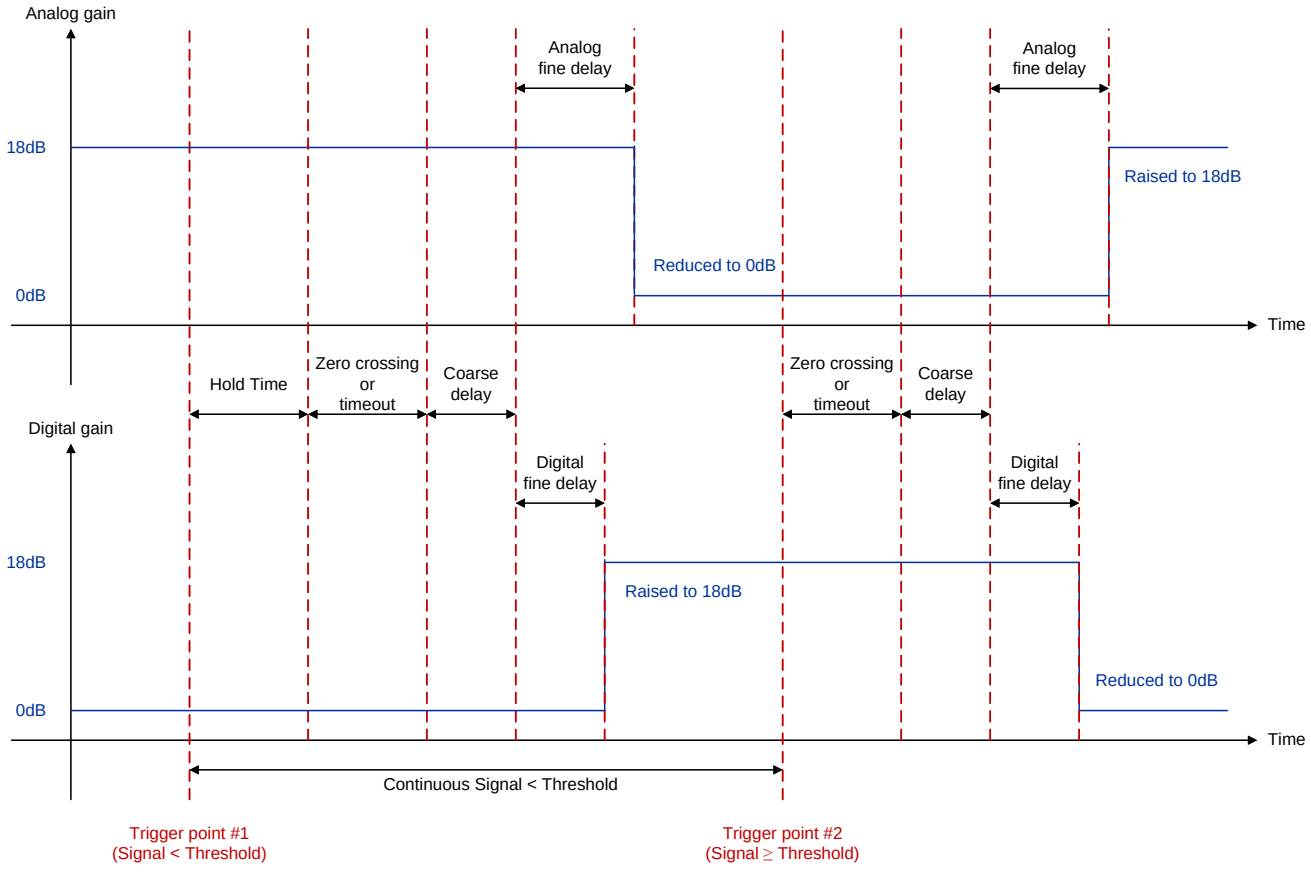


Figure 25. DRE Function Sequence

V/I Sensing

The RT5510 has built-in voltage and current sensing to monitor speaker behavior in real time. The VSNSP and VSNSN pins are speaker voltage sensing application and it should be connected after ferrite bead filter. In addition to getting the output voltage on speaker, the V-Sense connections can eliminate output trace and ferrite bead filter resistance IR drop between output pin to V-Sense terminal. The voltage sense monitors the speaker load voltage signal via an amplifier and an A/D converter. The current sense monitors the speaker load current with a small resistor, this signal via an amplifier and an A/D converter. Both signal output are pin DATAO.

This feature can be set to disable in the register 0xA3 bit'[3:2] to reduce the quiescent current. Please refer to Table 12.

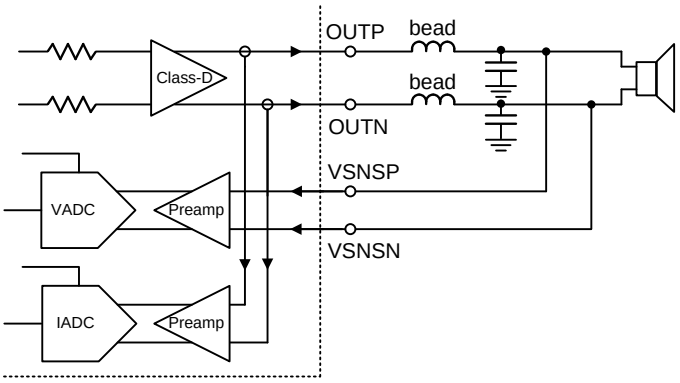


Figure 26. Voltage and Current Setting Monitor Structure

Table 12. V/ I Sense ADC

Register	Bits	Bits Name	Description
0xA3	3	D_CSADC_EN	Current sense ADC 0 : Disable 1 : Enable (default)
	2	D_VSADC_EN	Voltage sense ADC 0 : Disable (default) 1 : Enable

Users can use the algorithm and the RT5510 to reach speaker protection.

If the system has a speaker protection algorithm, the voltage and current sensing data can be used to achieve speaker excursion and temperature protection. Regarding the temperature protection of the speaker, the speaker resistance can be estimated by voltage and current sensing data, and the temperature of the speaker is calculated from the temperature coefficient of resistance of the coil material. Current sensing data obtains the current variation to estimate the speaker excursion.

Boost Capacitor Selection

The RT5510 VBAT power is from battery in real cell phone, and the trace is not shortest and battery provide to other device on phone mother board. The current peak drop and voltage ripple is predictable on VBAT pin. In order to reduce the ripple from battery and boost converter, the boost input voltage should be stable. Place a 10μF ceramic capacitor close to the VBAT pin and inductor. For cell phone applications, ceramic capacitor has small size and low ESR. Choose X5R or X7R temperature characteristic to keep capacitance in higher temperature.

When select capacitor, users have to ensure the DC bias characteristics in component datasheet, it will show the capacitance reduction percentage from rating. It is suggested to choose capacitor voltage rating at least 2x the maximum DC voltage application range to avoid capacitance reduction. For boost VBST = 9.5V application, a 10μF for input capacitor and a 100nF for DVDD decoupling capacitor are recommended.

Boost output capacitor is important for supply Class-D amplifier PVDD power. This capacitor can reduce boost output voltage ripple and keep the boost output voltage stable. If the output capacitance drops to low, the supply power PVDD for class-D amplifier will be too low and get worst performance.

The output ripple can be determined as following equation :

$$\Delta V_{OUT} = \frac{D \times I_{OUT} \times T_S}{\eta \times C_{OUT}} + \left(\frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D \times T_S}{2 \times L_{Boost}}\right) \times r_{C\_esr}$$

Boost capacitor connected to BST is important for stability. The CPVDD capacitance is changed by DC bias. When select capacitor, please notice the DC bias characteristics. The recommended minimum CPVDD capacitance is 6μF for 3.6W output power, 8μF for 4.3W output power, and 10μF for 5W output power.

Boost Inductor Selection

Small size and better efficiency are the major concerns for portable devices, such as the RT5510 is used for mobile phone. The inductor should have low core loss at 1MHz (Min.) and low DCR for better efficiency.

The maximum current of inductor is highly depends on the speaker impedance which determines the output current of the boost converter. The inductor saturation current rating should be considered to cover the inductor peak current which can be approximated by the following equation :

$$I_{L\_max} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} + \frac{V_{IN} \times D \times T_S}{2 \times L_{Boost}}$$

The following is the inductor selection reference. The recommended typical inductance is 1μH for the RT5510 boost converter. Inductor selection must consider the saturation current and DC resistance specifications. The rating inductance might be reduced by inductor current and heat, please refer to the inductance decrease current and temperature rise current in inductor datasheet. Therefore, please note the input current limit, and don't let the inductor into saturation state. For system efficiency, it is suggested to choose a low DC resistance component.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature TJ(MAX), listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-30B 2.25x2.60 (BSC) package, the thermal resistance, θ_{JA}, is 22.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (29°C/W) = 3.44W for a WL-CSP-30B 2.25x2.60 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 27 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

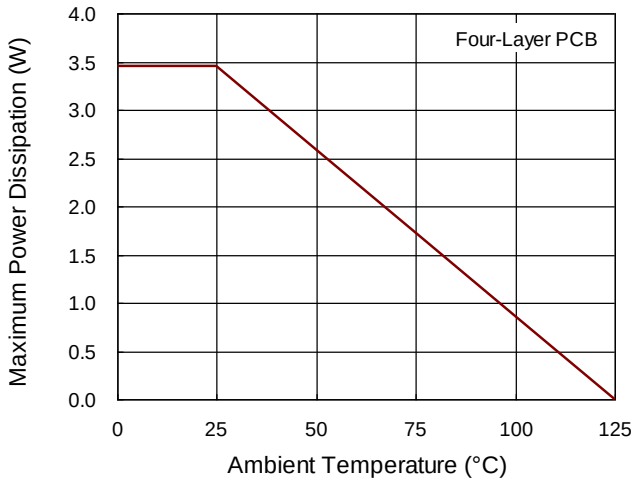
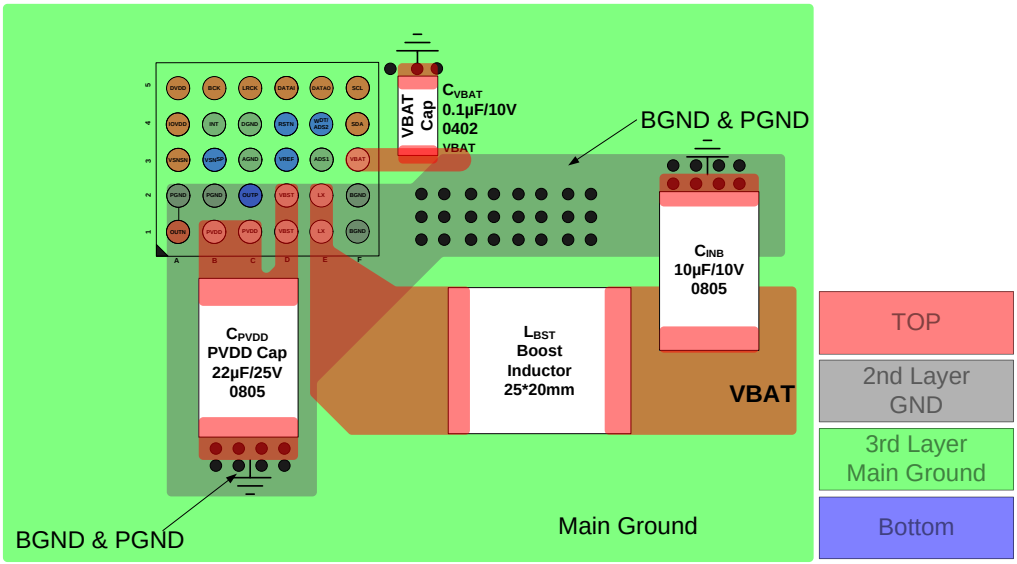


Figure 27. Derating Curve of Maximum Power Dissipation

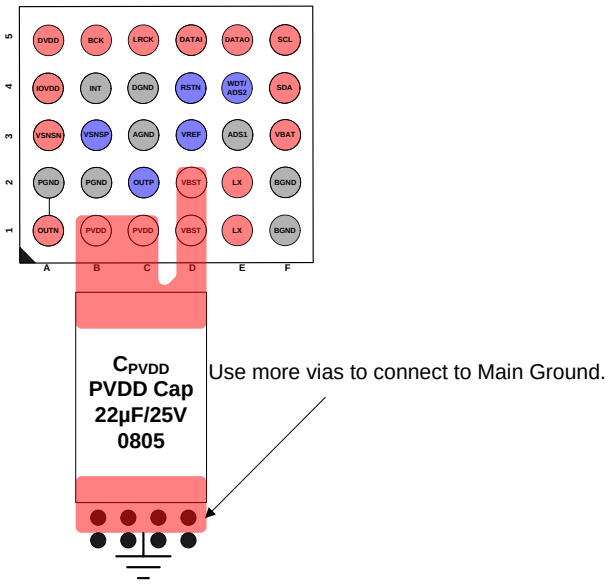
Layout Considerations

For the best performance of the RT5510, the below PCB layout guidelines including the below items must be strictly followed.

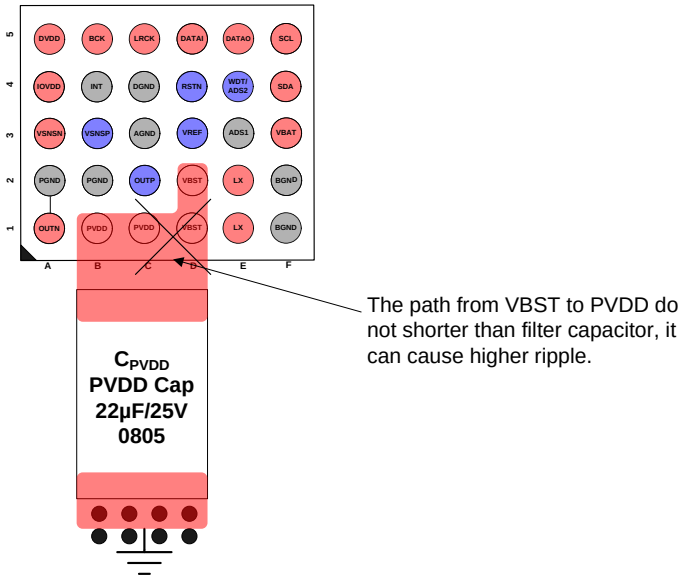
- VBAT connect to LX through the boost inductor. Place the inductor as close as possible to the chip with 80 mil width at least. The shorter and wider trace provides lower parasitic inductance and resistance for achieving better efficiency. The VBAT pin only consumes few micro amperes for internal analog circuit, so the trace with 6 mil width is enough for VBAT of the RT5510. The VBAT capacitor handling high noisy current for boost circuit, please connect it to BGND and PGND first for shorten the current path and minimize the influence to digital circuit.



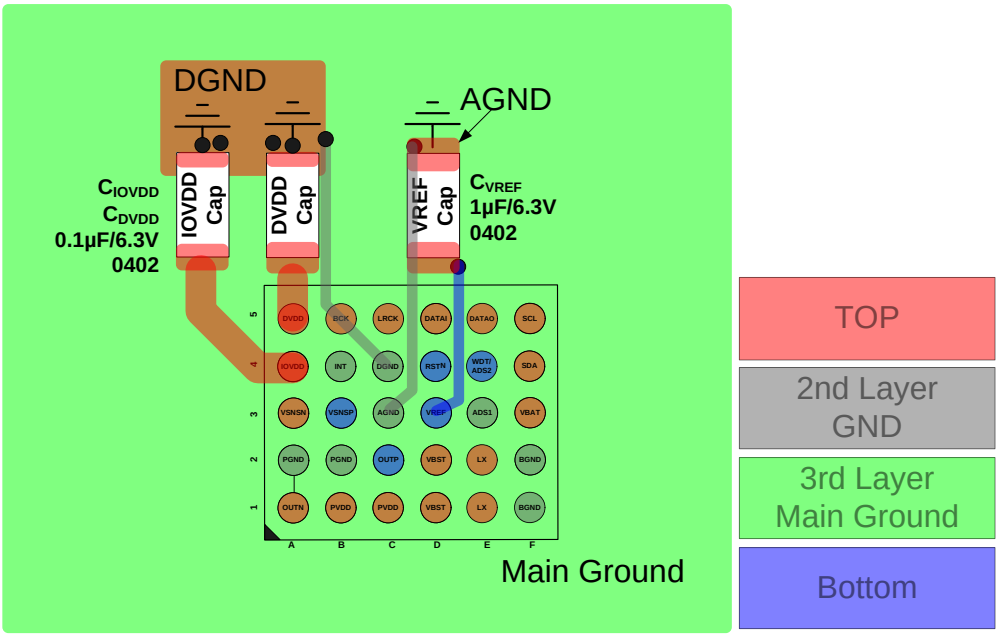
- Place the filter capacitor as close as possible to the VBST pin, then use shortest trace to link the capacitors and the trace width is 20mil at least. Use more vias to connect to main ground to reduce parasitic inductance and resistance.



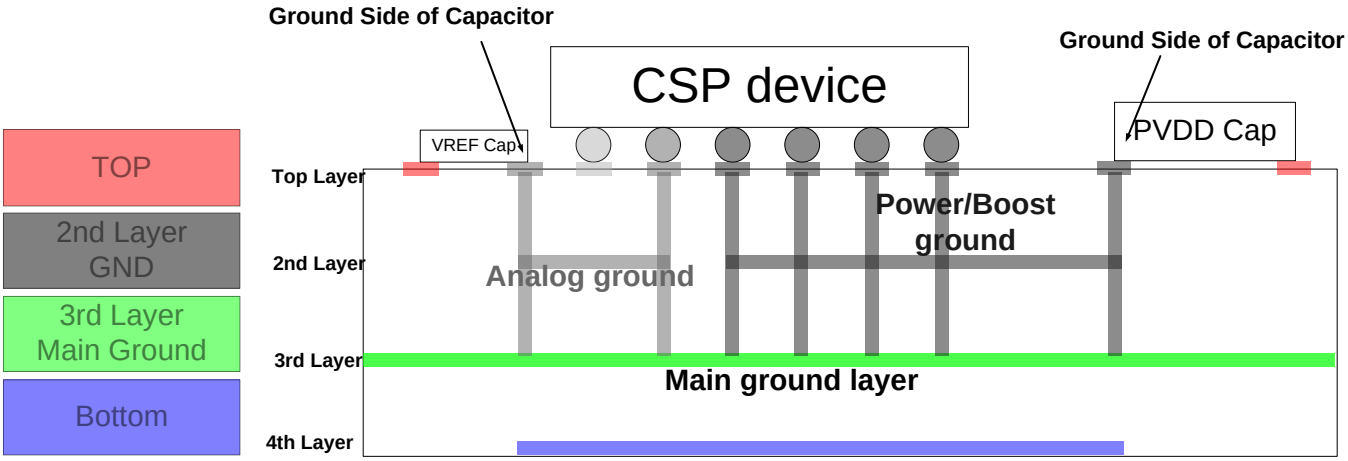
- Connect PVDD to the VBST filter capacitor from an independent path to make sure the voltage feed into PVDD is well filtered. The shortest path may bypass the filter capacitor so that causes higher voltage ripple than expected on PVDD.



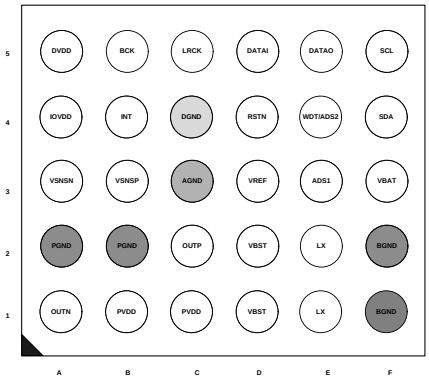
- For achieving good audio quality, the ground connection of decoupling capacitors (IOVDD and DVDD caps) should be linked to DGND first before going to main ground. Identically the VREF decoupling capacitor ground connection should be linked to AGND first before going to main ground. The trace width of IOVDD, DVDD and VREF are 6 mil at least.

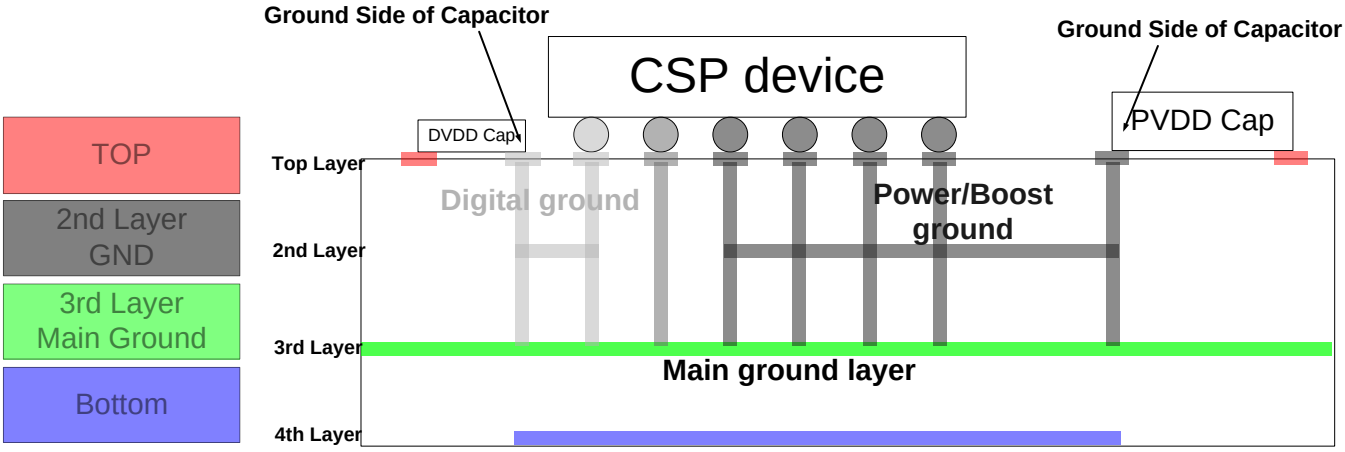


- Separate three ground planes (PGND and BGND, DGND and AGND) to isolate the noisy ground from other sensitive grounds and route the shortest path for high current return from Power/Boost ground plane before connecting to main ground to make sure the digital and analog circuit get a sufficient clean ground before influence by noisy high current path.



Analog ground:
- Dedicate a GND plane or trace to isolate other noisy ground.
- GND side of VREF decoupling capacitor should be connected to AGND first before going to main ground or connect to main ground directly from GND side of capacitor.

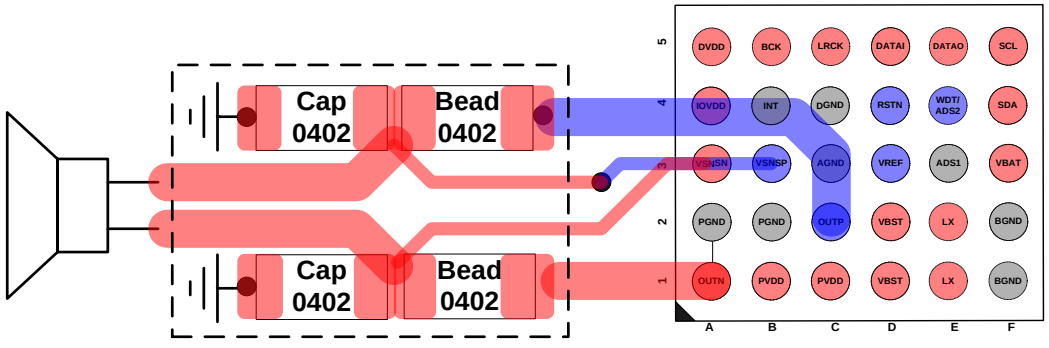




Power and Boost ground :
- Dedicate a GND plane to isolate the noisy ground from other sensitive grounds.
- Use multiple vias to connect main ground.

Digital ground :
- Dedicate a GND plane or trace to isolate other noisy ground.
- GND side of DVDD decoupling capacitor should be connected to DGND first before going to main ground or connect to main ground directly from GND side of capacitor.

- The traces of OUTA and OUTB should be kept equal width and length. When using the ferrite bead filter, it should be placed close to chip for better EMI performance. For achieving good accuracy for speaker protection, route separates trace from VSNSP and VSNSN to SPK side.



The RT5510 layout suggestion for 4 layers evaluation board is shown in Figure 28.

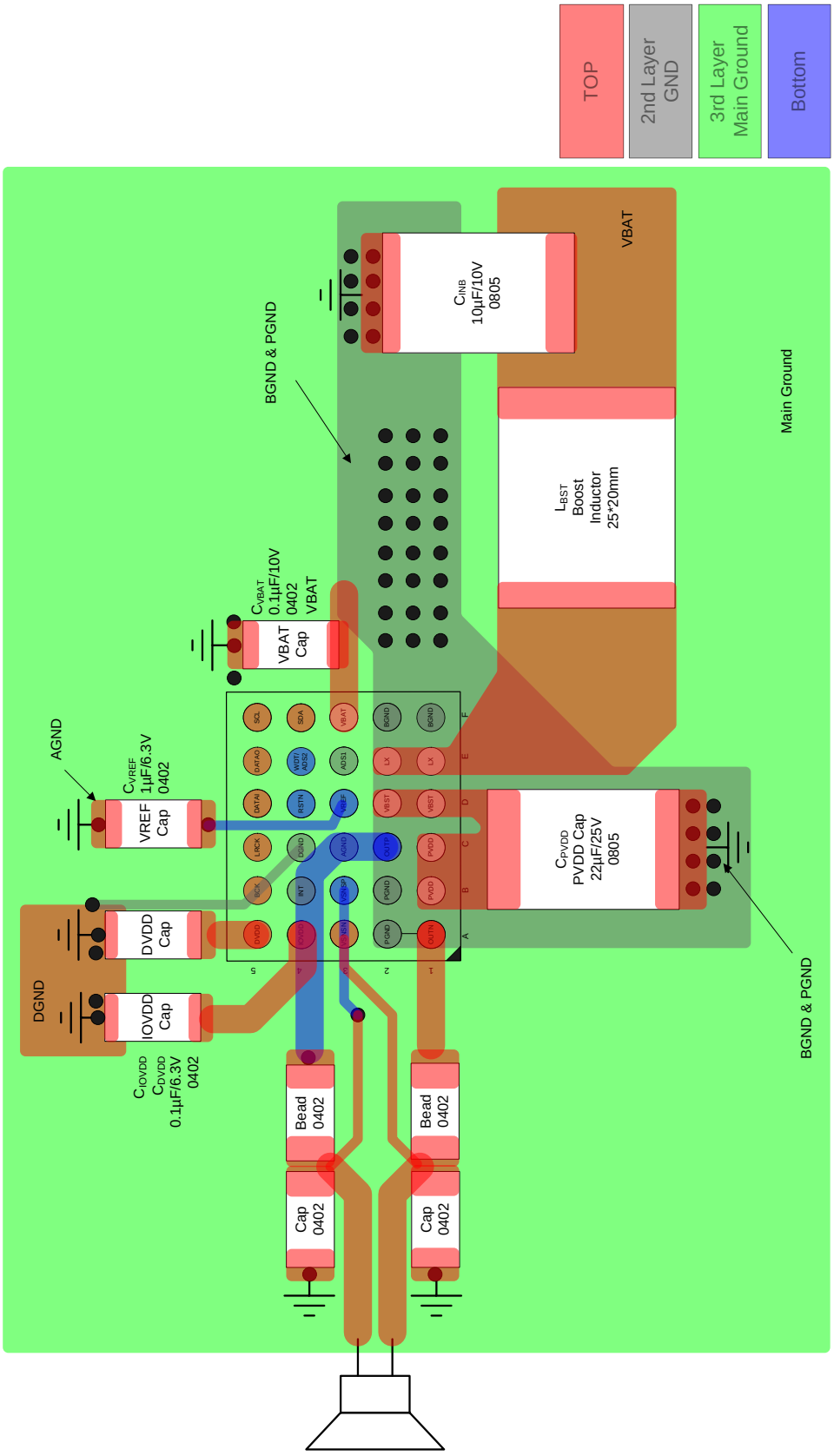


Figure 28. Suggested 4 Layers PCB Layout

Register Table

Registers Description

Address	Byte	Bits	Bits Name	Default	Type	Description
0x00	2	15:12	Reserved	0000	R	Reserved
		11:8	DEVICE_ID	0000	R/W	Device ID
		7:0	CHIP_ID[7:0]	11100000	R	Chip Revision ID E0 : First version E1 : 2nd version E2 : 3rd version …..
0x01	1	7:5	Reserved	000	R	Reserved
		4	PLL_LOCK	0	R	0 : PLL is locked to BCK (default) 1 : PLL is unlocked to BCK
		3	BCK_CLOCK_STABLE	0	R	0 : BCK rate stable (default) 1 : BCK rate unstable
		2	BCK_VALID	0	R	0 : BCK stable and match with BCK_MODE setting (default) 1 : BCK unstable and miss match with BCK_MODE setting
		1	BCK_LOSS	0	R	0 : BCK no loss(default) 1 : BCK loss
		0	LRCK_LOSS	0	R	0 : LRCK no loss(default) 1 : LRCK loss
0x03	1	7	SW_RESET	0	R/W	0 : Chip doesn't Software reset (default) 1 : Chip reset by Software reset
		6:4	Reserved	000	R	Reserved
		3	AMPDS	0	R/W	Soft off mode enable 0 : Enter soft mode before off mode (enable ramp control) (default) 1 : Enter off mode directly (disable ramp control)
		2	AMPE	0	R/W	Class-D enable 0 : Disable Class-D (default) 1 : Enable Class-D
		1	SPKM	0	R/W	0 : Unmute (default) 1 : Force speaker mute (with ramp control)
		0	PWDN	1	R/W	Chip power down control 0 : Chip enable 1 : Chip power down (default)

Address	Byte	Bits	Bits Name	Default	Type	Description
0x04	1	7	IF_WDT_EN	1	R/W	0 : Watchdog interrupt disable 1 : Watchdog interrupt enable (default)
		6	IF_BCK_STABLE_EN	1	R/W	0 : BCK un-stable interrupt disable 1 : BCK un-stable interrupt enable (default)
		5	IF_PLL_LOCK_EN	1	R/W	0 : PLL unlock interrupt disable 1 : PLL unlock interrupt enable (default)
		4	IF_UV_EN	1	R/W	0 : Under-voltage interrupt disable 1 : Under-voltage interrupt enable(default)
		3	IF_OV_EN	1	R/W	0 : Over-voltage interrupt disable 1 : Over-voltage interrupt enable (default)
		2	IF_OCP_EN	1	R/W	0 : AMP NMOS or PMOS over-current interrupt disable 1 : AMP NMOS or PMOS over-current interrupt enable (default)
		1	IF_BST_OC_EN	1	R/W	0 : Boost over-current interrupt disable 1 : Boost over-current interrupt enable (default)
		0	IF_OT_EN	1	R/W	0 : Over-temperature interrupt disable 1 : Over-temperature interrupt enable (default)
0x05	1	7	IF_WDT	0	R/W1C	Watchdog interrupt flag, write 1 to clear 0 : Chip operating mode (default) 1 : Interrupt flag = 1, WDT invalid
		6	IF_BCK_STABLE	0	R/C	BCK un-stable interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, BCK un-stable
		5	IF_PLL_LOCK	0	R/C	PLL unlock interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, PLL unlock
		4	IF_UV	0	R/C	Under-voltage interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs
		3	IF_OV	0	R/C	Over-voltage interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs
		2	IF_OCP	0	R/C	AMP NMOS or PMOS over-current interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs
		1	IF_BST_OC	0	R/C	Boost over-current interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs
		0	IF_OT	0	R/C	Over-temperature interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs

Address	Byte	Bits	Bits Name	Default	Type	Description
0x06	1	7:0	CRC8	00000000	R/W	I^2C write data checksum
0x09	1	7:6	Reserved	00	R	Reserved
		5	D_UVP_FLAG	0	R	Battery voltage under threshold 0 : Normal (default) 1 : Over threshold, protection occurs
		4	D_OVP_FLAG	0	R	Class-D amplifier supply voltage (VDDP) over threshold 0 : Normal (default) 1 : Over threshold, protection occurs
		3	OCPP_FLAG	0	R	Class-D output stage high-side OC flag 0 : Normal (default) 1 : Over threshold, protection occurs
		2	OCPN_FLAG	0	R	Class-D output stage low-side OC flag 0 : Normal (default) 1 : Over threshold, protection occurs
		1	D_OCP_FLAG	0	R	Boost Converter current over threshold 0 : Normal (default) 1 : Over threshold, protection occurs
		0	D_OTP_FLAG	0	R	Class-D amplifier temperature over threshold 0 : Normal (default) 1 : Over threshold, protection occurs

Address	Byte	Bits	Bits Name	Default	Type	Description
0x10	1	7:6	AUD_BIT	00	R/W	00 : 24bits (default) 01 : 20bits 10 : 18bits 11 : 16bits
		5:3	BCK_MODE	010	R/W	If MODE_DET_EN = 1, the detected BCK mode is read out If MODE_DET_EN = 0, the BCK_MODE is written to indicate the BCK mode 000 : 32fs 001 : 48fs 010 : 64fs (default) 011 : 96fs 100 : 128fs 101 : 256fs Others : Not support
		2:0	SR_MODE	011	R/W	If MODE_DET_EN = 1, the detected SR is read out If MODE_DET_EN = 0, the SR_MODE is written to indicate the sampling rate 000 : 32k 001 : Not support 010 : 96k/88.2k 011 : 48k/44.1k (default) 100 : 16k 101 : 24k/22.05k 110 : 8k 111 : 12k/11.025k

Address	Byte	Bits	Bits Name	Default	Type	Description
0x11	1	7	I^2S_LOSS_DET_EN	1	R/W	0 : Disable BCK/LRCK LOSS auto-detect 1 : Enable BCK/LRCK LOSS auto-detect (default)
		6	BCK_STABLE_CHK_EN	1	R/W	0 : Disable BCK stable and valid check 1 : Enable BCK stable and valid check (default)
		5	MODE_DET_EN	1	R/W	0 : Disable sampling rate auto-detect and write SR_MODE/BCK_MODE to indicate the sampling rate and BCK mode 1 : Enable SR & BCK mode auto-detect and read SR_MODE/BCK_MODE will return the detection result (default)
		4	DSP_MODE_SEL	0	R/W	0 : DSP mode A (default) 1 : DSP mode B
		3	TDM_OFFSET	0	R/W	The number of bits between the frame sync signal transitioning and data being driven on the data line 0 : The first data can be sampled at the first BCK rising edge after FSYNC rising edge (default) 1 : The first data can be sampled at the second BCK rising edge after FSYNC rising edge
		2:0	AUD_FMT	000	R/W	000 : I^2S (default) 001 : Left justify mode 010 : Right justify mode 011 : DSP mode 100 : 8 TDM slots (slot #0 to slot #7) 101 : 16 TDM slots (slot #0 to slot #15) 110 : 32 TDM slots (slot #0 to slot #31) 111 : Reserved

Address	Byte	Bits	Bits Name	Default	Type	Description
0x12	1	7:6	I^2SLRS	01	R/W	Audio input selection 00 : Left channel 01 : (Left + Right)/2 (default) 10 : Right channel 11 : Reserved
		5:3	I^2SDOLS	000	R/W	DATAO left channel output selection 000 : {IMON[15:0], VTEMP[7:0], VBAT[7:0]} (default) 001 : {DAC_BIQ[23:0], 8'h0} 010 : {[Hi-Z[31:0]} 011 : {VMON[15:0], IMON[15:0]} 100 : {DC_CUT_DATA[25:0], 6'h0} 101 : {SAFE_DATA_OUT[19:0], 12'h0} 110 : {DF_DATA_OUT[21:0], 10'h0} 111 : {DF_DATA_OUT_HC[21:0], 10'h0}
		2:0	I^2SDORS	000	R/W	DATAO right channel output selection 000 : {VMON[15:0], SPKPROT_GAIN[15:0]} (default) 001 : {DC_CUT_DATA[25:0], 8'h0} 010 : {VON[15:0], IMON[15:0]} 011 : {[Hi-Z[31:0]} 100 : {SAFE_DATA_OUT[19:0], 12'h0} 101 : {DF_DATA_OUT[21:0], 10'h0} 110 : {DF_DATA_OUT_HC[21:0], 10'h0} 111 : {DF_DATA_OUT_IN[21:0], 10'h0}
0x13	1	7:6	TDM_RX_LEN	10	R/W	RX length control 00 : 1 slot (8bits) 01 : 2 slot (16bits) 10 : 3 slot (24bits) (default) 11 : Reserved
		5	Reserved	0	R	Reserved
		4:0	TDM_RX_LOC	00000	R/W	RX location control, indicate which slot the data MSB is loaded in 00000 : Slot 0 (default) 00001 to 11110 : Slot 1 to Slow30 11111 : Slot 31

Address	Byte	Bits	Bits Name	Default	Type	Description
0x14	2	15:13	Reserved	000	R	Reserved
		12:8	TDM_TX_LEN	00000	R/W	TX length control, indicate how many bytes should be transmitted from slot TDM_TX_LOC 00000 : TX disable (default) 00001 : TX length 1 slots 00010 : TX length 2 slots 00001 to 10000 : TX length 1 to 16 slots Others : Reserved
		7	TDM_TEST_EN	0	R/W	0 : TDM TX debug data test mode disable (default) 1: TDM TX debug data test mode enable
		6:5	Reserved	00	R	Reserved
		4:0	TDM_TX_LOC	00000	R/W	TX location control, indicate which slot the data MSB is loaded in 00000 : Slot 0 (default) 00001 to 11110 : Slot 1 to Slow30 11111 : Slot 31
0x18	1	7:3	Reserved	00000	R	Reserved
		2	HPF_VS_EN	1	R/W	0 : Disable HPF for voltage sense 1 : Enable HPF for voltage sense (default)
		1	HPF_IS_EN	1	R/W	0 : Disable HPF for current sense 1 : Enable HPF for current sense (default)
		0	HPF_AUD_IN_EN	1	R/W	0 : Disable HPF for audio in 1 : Enable HPF for audio in (default)

Address	Byte	Bits	Bits Name	Default	Type	Description
0x20	1	7	WD_EN	1	R/W	0 : Disable watchdog 1 : Enable watchdog (default)
		6	Reserved	0	R	Reserved
		5:4	WD_TIMEOUT_SEL	10	R/W	Configure the minimum edge rate (rising or falling) of WDT pin, if violated, WD_RESP will be triggered 00 : At least one edge occurs every 5ms 01 : At least one edge occurs every 20ms 10 : At least one edge occurs every 35ms (default) 11 : At least one edge occurs every 50ms
		3:2	Reserved	00	R	Reserved
		1:0	WD_RESP	10	R/W	If watchdog timeout happened, WD_RESP will guide the behavior of AMP 00 : The Amp neither mutes nor shut down when the watchdog is triggered. The boost converter's output voltage is not affected. 01 : The Amp shuts down immediately and the output transition is Hi-Z. The boost converter ramps down to VBAT then enters bypass mode. 10 : The Amp mutes according to the configuration of VOLCTRL, instant mute or soft mute. The boost converter ramps down to VBAT then enters bypass mode. (default) 11 : Signal in is multiplied by WD_RP when watchdog timeout is happened, instead of R_VOLUME.
0x21	1	7:0	WD_RP	00101000	R/W	Volume during watchdog timeout, downward, 12 to –115.5dB in –0.5dB step, (default 00101000 = –8dB) e.g. 00000000 = 12dB Equation : Volume = (WD_RP (DEC) x –0.5dB) + 12dB
0x24	2	15:9	Reserved	0000000	R	Reserved
		8	HARD_CLIP_EN	1	R/W	0 : Disable hard clipping 1 : Enable hard clipping(default)
		7:0	HARD_CLIP_TH	00000000	R/W	Hard Clip threshold if HARD_CLIP_EN = 1 Downward, 12 to –115.5dB in –0.5dB step, (default 00000000 = 12dB) e.g. 00000001 = 11.5dB Equation : Hard Clip threshold = (HARD_CLIP_TH (DEC) x –0.5dB) + 12dB

Address	Byte	Bits	Bits Name	Default	Type	Description
0x28	1	7:3	Reserved	00000	R	Reserved
		2:0	VOLCTRL	000	R/W	Ramp control when new volume setting is different from old setting : 000 : No ramp up/down (default) 001 : 0.5dB per sample 010 : 0.5dB per 2 samples 011 : 0.5dB per 4 samples 100 : 0.5dB per 8 samples 101 : 0.5dB per 16 samples 110 : 0.5dB per 32 samples 111 : 0.5dB per 64 samples
0x29	1	7:0	VOLUME	00011000	R/W	Volume, downward 12 to –115.5dB in –0.5dB step, (default 00011000 = 0dB) e.g. 00000000 = 12dB Equation : Digital volume = (VOLUME (DEC) x –0.5dB) + 12dB
0x30	1	7:4	Reserved	0000	R	Reserved
		3:1	VBCPS	001	R/W	Clip threshold setting 000 : 3.9V 001 : 3.75V (default) 010 : 3.6V 011 : 3.45V 100 : 3.3V 101 : 3.15V 110 : 3V 111 : 2.85V
		0	CLPE	1	R/W	0 : Disable clip 1 : Enable clip (default)

Address	Byte	Bits	Bits Name	Default	Type	Description
0x31	2	15:14	CLIPRR	00	R/W	Rate of Vo threshold recover when VBAT return 00 : Increase by 1/8 of original Vo per 1s (default) 01 : Increase by 1/8 of original Vo per 1.5s 10 : Increase by 1/8 of original Vo per 2s 11 : Increase by 1/8 of original Vo per 2.5s
		13:12	CLIPDR	00	R/W	Rate of Vo threshold drop when VBAT is low 00 : 1/16 of original per sample (default) 01 : 1/8 of original Vo 10 : 1/4 of original Vo 11 : 1 step to target
		11:10	BVHYS	00	R/W	Battery voltage recovery hysteresis 00 : Battery voltage + 0.05 (default) 01 : Battery voltage + 0.1 10 : Battery voltage + 0.15 11 : Battery voltage + 0.2
		9:0	CPSLP	1000000000	R/W	Clip slope setting : For example, set clip slope = 12, signal path gain = 11.1 CPSLP value (DEC) = Clip slope × 256 / Signal path gain CPSLP value (Bin) = 0100010100 CPSLP value (Bin) =1000000000 (default), the Clip slope is 22.2.
0x32	2	15:0	VOMIN	16'h1DDD	R/W	Minimum Clip threshold converted from (V) For example, set minimum clip threshold = 2.85V, signal path gain = 11.1 VOMIN (DEC) = 2.85 × 32768 / Signal path gain VOMIN (HEX) = 20DD Set VOMIN = 1DDD (default), signal path gain = 11.1, minimum clip threshold = 2.59V.
0x3F	1	7:3	Reserved	00000	R	Reserved
		2:0	T0_SEL	000	R/W	The selection of T0, 22 to 29°C 000 : 22°C (default) 001 : 23°C 010 : 24°C 011 : 25°C 100 : 26°C 101 : 27°C 110 : 28°C 111 : 29°C

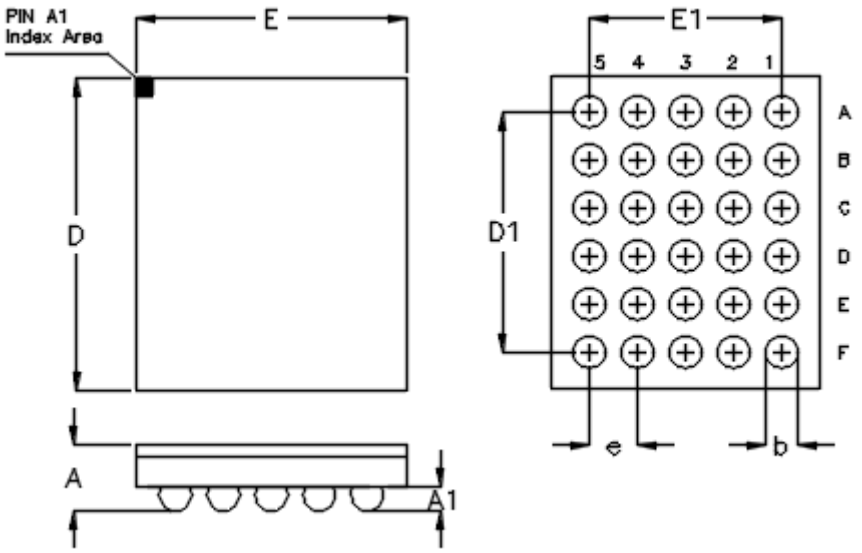
Address	Byte	Bits	Bits Name	Default	Type	Description
0x40	1	7:6	BST_TOT	01	R/W	Level timeout time in adaptive mode : 00 : 500μs 01 : 1ms (default) 10 : 2ms 11 : 4ms
		5:4	SLEW_RATE	01	R/W	VBST slew rate when using boost mode : 00 : 2.5mV/μs 01 : 5mV/μs (default) 10 : 10mV/μs 11 : 20mV/μs
		3	PSM_EN	1	R/W	0 : Disable PSM 1 : Enable PSM (default)
		2	DCM_EN	1	R/W	0 : Disable DCM 1 : Enable DCM (default)
		1:0	BST_MODE	00	R/W	Boost mode 00 : Disable (default) 01 : Battery 10 : Fixed 11 : Adaptive
0x41	2	15:12	Reserved	0000	R	Reserved
		11:6	BST_THT1	100001	R/W	VBST target in fixed mode or highest VBST target in adaptive mode 000000 : Disabled 000001 to 100001 : 2.9 + BST_THT1 x 0.2V e.g. 000001 : 3.1V, 100001 : 9.5V (default), 100010 to 111111 : Reserved
		5:0	BST_TH1	011011	R/W	Boost threshold for BST_THT1 000000 : Disabled 000001 to 100001 : 1.3 + BST_TH1 x 0.2V e.g. 000001 : 1.5V, 100001 : 7.9V, 011011 : 6.7V (default), 100010 to 111111 : Reserved
0x42	2	15:12	Reserved	0000	R	Reserved
		11:6	BST_THT2	010111	R/W	Middle VBST target in adaptive mode 000000: Disabled 000001 to 100001 : 2.9 + BST_THT2 x 0.2V e.g. 000001 : 3.1V, 100001 : 9.5V, 010111 : 7.5V (default), 100010 to 111111 : Reserved
		5:0	BST_TH2	001111	R/W	Boost threshold for BST_THT2 000000 : Disabled 000001 to 100001 : 1.3 + BST_TH2 x 0.2V e.g. 000001 : 1.5V, 100001 : 7.9V, 001111 : 4.3V (default) 100010 to 111111 : Reserved

Address	Byte	Bits	Bits Name	Default	Type	Description
0x43	2	15:12	Reserved	0000	R	Reserved
		11:6	BST_THT3	001011	R/W	Lowest VBST target in adaptive mode 000000 : Disabled 000001 to 100001 : 2.9 + BST_THT3 x 0.2V e.g. 000001 : 3.1V, 100001 : 9.5V, 001011 : 5.1V (default), 100010 to 111111 : Reserved
		5:0	BST_TH3	000111	R/W	Boost threshold for BST_THT3 000000 : Disabled 000001 to 100001 : 1.3 + BST_TH3 x 0.2V e.g. 000001 : 1.5V, 100001 : 7.9V, 000111 : 2.7V (default), 100010 to 111111 : Reserved
0x45	1	7	Reserved	0	R	Reserved
		6:0	CC_MAX	1100111	R/W	The IDAC1 peak value 0110101 : 2A 1000011 : 2.5A 1010001 : 3A 1011111 : 3.5A 1100111 : 4A (default) 1101111 : 4.5A 1111101 : 5A
0x46	1	7	Reserved	0	R	Reserved
		6	OTP_MODE	0	R/W	0 : Digital OTP to trigger auto-recovery (default) 1 : Analog OTP flag to trigger auto-recovery
		5	BST_OCP_MODE	1	R/W	0 : Boost digital OCP if OCP_PROT_EN = 1 1 : Boost Analog OCP for limit PWM duty (without OCP) (default)
		4	AMP_OCP_PROT_EN	1	R/W	0 : Disable speaker OCP protection 1 : Enable speaker OCP protection (default)
		3	OVP_PROT_EN	1	R/W	0 : Disable OVP protection 1 : Enable OVP protection (default)
		2	UVP_PROT_EN	1	R/W	0 : Disable UVP protection 1 : Enable UVP protection (default)
		1	BST_OCP_PROT_EN	1	R/W	0 : Disable boost OCP protection 1 : Enable boost OCP protection (default)
		0	OTP_PROT_EN	1	R/W	0 : Disable OTP protection 1 : Enable OTP protection (default)

Address	Byte	Bits	Bits Name	Default	Type	Description
0x47	2	15:9	Reserved	0000000	R	Reserved
		8:0	VPTAT	000000000	R	VPTAT code (DEC) = Chip temperature (°C) + 273°C e.g. VPTAT code = 100101010, VPTAT code (DEC) = 298, chip temperature = 25°C
0x48	1	7:0	VBAT	00000000	R	Battery voltage (V) = VBAT code (DEC) / 40 e.g. 10100000 = 160 (DEC), Battery voltage = 160 / 40 = 4V
0x68	1	7:5	Reserved	000	R	Reserved
		4	Time out_disable	0	R/W	0 : Enter DRE if timeout to find zero crossing (default) 1 : Not enter DRE if timeout to find zero crossing
		3	DRE_method_sel	0	R/W	0 : Enter DRE at zero crossing (default) 1 : Enter DRE if signal < threshold
		2:1	DRE_HOLD_SEL	10	R/W	Hold time before entering DRE 00 : 16ms 01 : 32ms 10 : 64ms (default) 11 : 128ms
		0	DRE_EN	1	R/W	0 : Disable DRE 1 : Enable DRE (default)
0x69	1	7:0	DRE_THDMODE	01000000	R/W	Threshold = 20log (DRE_THDMODE (DEC) × 2 ^ (–11)), DRE_THDMODE= –30.1dB (default)

Address	Byte	Bits	Bits Name	Default	Type	Description
0xA3	1	7:5	D_SPK_BOOST[2:0]	101	R/W	Class-D gain control [000:110] = 0 to 18dB, 3dB per step 000 : 0dB 001 : 3dB 010 : 6dB 011 : 9dB 100 : 12dB 101 : 15dB (default) 110 : 18dB Others : Reserved
		4	Reserved	0	R	Reserved
		3	D_CSADC_EN	1	R/W	Current sense ADC 0 : Disable 1 : Enable (default)
		2	D_VSADC_EN	0	R/W	Voltage sense ADC 0 : Disable (default) 1 : Enable
		1	D_SPK_DC_TRACE_EN	1	R/W	SPK DC-TRACE enable 0 : Disable 1 : Enable (default)
		0	D_EN_TRIWAVE	1	R/W	Enable triangle wave generator 0 : Disable 1 : Enable (default)

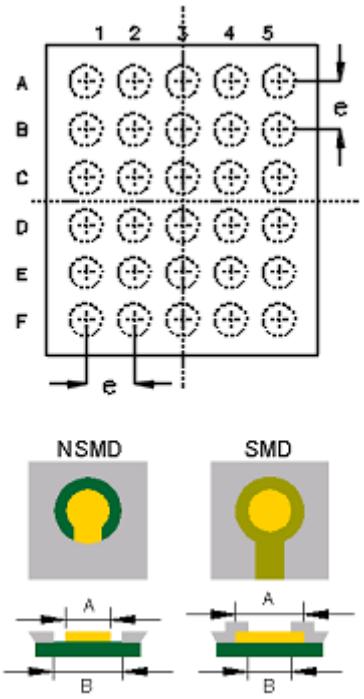
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.560	2.640	0.101	0.104
D1	2.000		0.079	
E	2.210	2.290	0.087	0.090
E1	1.600		0.063	
e	0.400		0.016	

30B WL-CSP 2.25x2.60 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.25x2.60-30(BSC)	30	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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