RICHTEK®

RT5147

Power Management Unit Total Power Solution for SSD

1 General Description

The RT5147 provides a highly-integrated multi-channel system power management solutions designed to fulfill the performance, efficiency, and feature requirements of SSD applications.

It features four buck regulators and two LDOs, delivering multiple output voltages to accommodate various applications with different Voltage Identification (VID) requirements. The power-on sequence is configurable, offering enhanced flexibility for system design.

Additionally, the RT5147 is equipped with 8 configurable GPIO pins to meet diverse system hardware control requirements. These GPIOs can be programmed for a variety of functions, including PWRDIS/ Sleep/ Deep Sleep settings for PMIC state machine control, Enable/Disable settings for Buck1 and Buck2, VID control settings for Buck3 and Buck4, nRESET pin functionality to monitor PMIC power good status, and configuration as External Enable (External_EN) and External Power Good (External_PG) signals. Furthermore, the GPIOs support three-state configuration through the I^2C interface when operating in the normal mode. The RT5147 is designed to operate within a recommended junction temperature range of –40°C to 125°C, and an ambient temperature range of –40°C to 85°C.

2 Applications

- SSD

3 Marking Information

3T: Product Code
XXYY: Wafer ID with Check Sum
CCC-RRR: IC Coordinate (X, Y)
YMDAN: Date Code

4 Features

- **Input Supply Voltage Range: 2.7V to 3.7V**
- **Highly Efficient Programmable Regulators**
  - **BUCK 1: 1.7V to 2.9V, 20mV per step; 4A**
  - **BUCK 2: 0.5V to 1.3V, 10mV per step; 2A**
  - **BUCK 3: 0.5V to 1.3V, 10mV per step; 4A**
  - **BUCK 4: 0.9V to 2.0V, 10mV per step; 2A**
  - **LDO 1: 1.0V to 2.7V, 50mV per step; 400mA**
  - **LDO 2: 1.0V to 2.7V, 50mV per step; 400mA**
- **Configurable Outputs**
  - **±1.5% Feedback Voltage Accuracy for Full Temperature Range (–40°C to 125°C)**
  - **DVS Change for All Bucks via I^2C Interface**
  - **Enable Time for All VRs**
  - **Soft-Start Time for All VRs**
  - **Selectable Switching Frequency for Every Buck Rail**
- **Input OV/UV Warning Indication and Fault Protection**
- **Output OV/UV/OC Fault Protection**
- **Over-Temperature Protection**
- **Diode Emulation Mode for Light-Load and High Efficiency Operation**
- **Buck2 and Buck3 Support DVS without I^2C Command at Sleep Mode**
- **Non-Volatile Register Configurability**
- **I^2C Interface 400kHz/1MHz/3.4MHz**
- **8 Multi-Function GPIOs for Control and Command Unit**
  - **nRESET_N for ASIC**
  - **IRQ_N Interrupt Flag**
  - **PWRDIS, SLEEP1, SLEEP2**
  - **Enable/Disable Settings for Buck1 and Buck2**
  - **2 Sets of EXT_EN_I and EXT_EN_O**
  - **SYSMON Can Only be Set by GPIO5**
  - **Buck1/2/3/4 and LDO1/2 Selection by GPIOx**

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5 Ordering Information

RT5147□- 01

Revision Code

Package Type(1)

WSC: WL-CSP-36B 2.66x2.70 (BSC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

Part Number Version Table

Part Number	GPIOx Status	VIN (V)	VOUT (V)						
			BUCK1 (B1)	BUCK2 (B2)	BUCK3 (B3)	B2/B3	BUCK4 (B4)	LDO1 (L1)	LDO2 (L2)
				Normal	Normal	Sleep			
RT5147WSC-01	H	3.3	PLSW	BUCK = 0.91	BUCK = 0.78	BUCK = 0.68	BUCK = 1.1	LDO = 1.8	LDO = 1.8
	Hi-Z	3.3	BUCK = 2.5	BUCK = 0.91	BUCK = 0.78	BUCK = 0.68	BUCK = 1.2	LDO = 1.8	X
	L	3.3	BUCK = 2.5	BUCK = 0.91	BUCK = 1.2	BUCK = 0.68	BUCK = 1.2	LDO = 2.5	PLSW

Note 2.

(1) GPIO2 controls BUCK1 and BUCK2, GPIO3 controls BUCK3, GPIO4 controls BUCK4 and LDO1, and GPIO6 controls LDO2.

(2) PLSW = P-type Load Switch.

6 Simplified Application Circuit

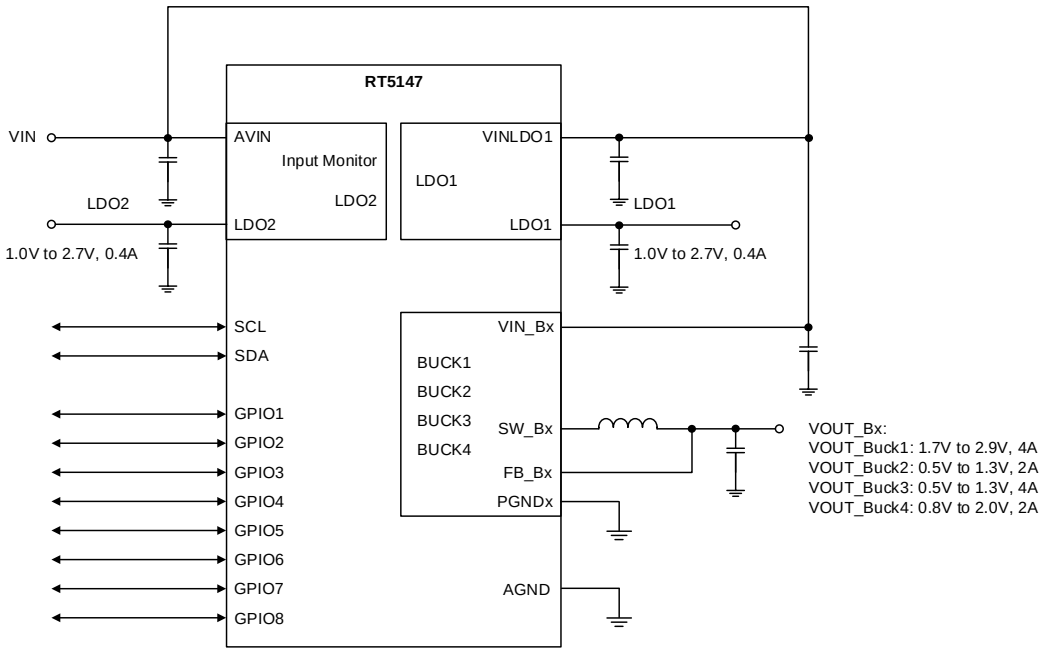

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Table of Contents

1 General Description ---- 1
2 Applications ---- 1
3 Marking Information ---- 1
4 Features ---- 1
5 Ordering Information ---- 2
6 Simplified Application Circuit ---- 2
7 Pin Configuration ---- 4
8 Functional Pin Description ---- 4
9 Functional Block Diagram ---- 7
10 Absolute Maximum Ratings ---- 8
11 Recommended Operating Conditions ---- 8
12 Electrical Characteristics ---- 9
13 Typical Application Circuit ---- 24
14 Typical Operating Characteristics ---- 25
15 Operation ---- 29
15.1 Buck Converter ---- 29
15.2 Buck Overcurrent Limiter (OCL) ---- 29
15.3 Buck Undervoltage Protection (UVP) ---- 29
15.4 Buck Overvoltage Protection (OVP) ---- 29
15.5 Linear Dropout Regulator (LDO) ---- 29
15.6 Over-Temperature Protection (OTP) ---- 29
15.7 GPIO1 ---- 29
15.8 GPIO2 ---- 30
15.9 GPIO3 ---- 30
15.10 GPIO4 ---- 31
15.11 GPIO6 ---- 31
15.12 GPIO5/7/8 ---- 31
16 Application Information ---- 33
16.1 Bucker Converter ---- 33
16.2 Inductor Selection ---- 33
16.3 C_{IN} and C_{SYS} Selection ---- 34
16.4 C_{OUT} Selection ---- 35
16.5 Overcurrent Limit (OCL) ---- 36
16.6 Undervoltage Protection (UVP) ---- 36
16.7 Overvoltage Protection (OVP) ---- 36
16.8 AVIN Overvoltage Protection (AVIN OVP) ---- 36
16.9 AVIN Undervoltage-Lockout (AVIN UVLO) ---- 37
16.10 Over-Temperature Protection (OTP) ---- 37
16.11 Protection Functions ---- 37
16.12 Rails Configuration ---- 37
16.13 I^2C Interface ---- 38
16.14 State Machine ---- 39
16.15 Sequence Diagram ---- 41
16.16 TIME_SLOT, ON_DLY, WAKE_UP_DLY, and OFF_DLY ---- 45
16.17 B1/B2_EN ---- 46
16.18 VOUT_LOW ---- 46
16.19 EXT_ENx_O ---- 46
16.20 SYSMON, SYSWARN and POK_OV ---- 47
16.21 AVIN_OV and AVIN UVLO ---- 47
16.22 Status and Flag ---- 47
16.23 nIRQ (Negative Interrupt Request) ---- 47
16.24 Power Disable (PWRDIS) ---- 48
16.25 B2/B3_DVS_EN_SLEEPx ---- 48
16.26 Thermal Considerations ---- 49
16.27 Layout Considerations ---- 50
17 Functional Register Description ---- 51
17.1 Registers Configuration ---- 54
18 Outline Dimension ---- 105
19 Footprint Information ---- 106
20 Packing Information ---- 107
20.1 Tape and Reel Data ---- 107
20.2 Tape and Reel Packing ---- 108
20.3 Packing Material Anti-ESD Property ---- 109
21 Datasheet Revision History ---- 110

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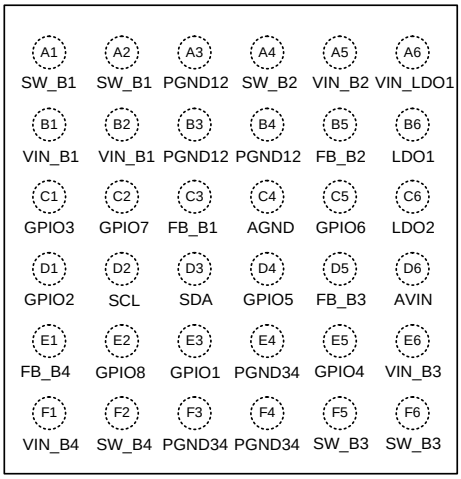
7 Pin Configuration

(TOP VIEW)



WL-CSP-36B 2.66x2.70 (BSC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, A2	SW_B1	Switch node of Buck1. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect these pins to the output inductor and keep the sensitive trace and signals away.
A3, B3, B4	PGND12	Power stage ground for Buck1 and Buck2. This is the ground return path for the low-side power MOSFETs and drivers of Buck1 and Buck2. To minimize the parasitic impedance and thermal resistance, it is essential to directly solder this ground to a large PCB Power Ground (PGND) plane and to incorporate thermal vias beneath the PGND pin.
A4	SW_B2	Switch node of Buck2. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.
A5	VIN_B2	Buck2 Input voltage pin. It is internally connected to the source terminal of Buck2 high-side MOSFET. It is necessary to connect a ceramic capacitor (C = 10μF/0603) as close as possible from the VIN_B2 pin to the PGND12 pin.
A6	VIN_LDO1	LDO1 input supply. It is necessary to connect a ceramic capacitor (C = 2.2μF/0402) as close as possible from the VIN_LDO1 pin to the PGND pin.
B1, B2	VIN_B1	Buck1 input voltage pins are internally connected to the source terminal of Buck1 high-side MOSFET. It is necessary to connect a ceramic capacitor (C = 10μF/0603) as close as possible from the VIN_B1 pin to the PGND12 pin.
B5	FB_B2	Buck2 feedback sense for output regulation. It is used to detect output voltage status for OVP, UVP, and Power Good of Buck2. Connect it to the Buck2 output capacitor.
B6	LDO1	LDO1 output. To ensure stability of the LDO, it is recommended to connect the pin to a ceramic capacitor (C = 2.2μF/0402).
C1	GPIO3	By default, GPIO3 is set as an EXT_EN1_O output pin with an Open Drain configuration, which requires the use of an external pull-up resistor. Once the AVIN voltage exceeds the UVLO threshold, the user can select GPIO3 to perform one of the other nine available functions.

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Pin No.	Pin Name	Pin Function
C2	GPIO7	By default, GPIO7 serves as a PWRDIS (Power Disable) input pin with an open drain configuration, which requires the use of an external pull-up resistor. Once the AVIN voltage exceeds the UVLO threshold, the user can select GPIO7 to perform one of the other nine available functions.
C3	FB_B1	Buck1 feedback sense for output regulation. It is used to detect output voltage status for OVP, UVP, and Power Good of Buck1. Connect it to the Buck1 output capacitor.
C4	AGND	Ground of internal analog circuitry. AGND must be connected to the PGND plane through a single point.
C5	GPIO6	By default, GPIO6 is set as an EXT_EN1_O output pin with an open drain configuration, which requires the use of an external pull-up resistor. Once the AVIN voltage exceeds the UVLO threshold, the user can select GPIO6 to perform one of the other nine available functions.
C6	LDO2	LDO2 output. To ensure stability of the LDO, it is recommended to connect it to a ceramic capacitor (C = 2.2μF/0402).
D1	GPIO2	By default, GPIO2 is set as an EXT_EN1_O output pin with an open drain configuration, which requires the use of an external pull-up resistor. Once the AVIN voltage exceeds the UVLO threshold, the user can select GPIO2 to perform one of the other nine available functions.
D2	SCL	I^2C clock pin. This pin is the input of the serial bus clock signal.
D3	SDA	I^2C data pin. This pin is the input and output of the serial bus data signal.
D4	GPIO5	GPIO5 is pre-configured as an nIRQ (Negative Interrupt Request) output pin with an open drain configuration, which requires the use of an external pull-up resistor. Once the AVIN voltage exceeds the UVLO threshold, the user can select GPIO5 to perform one of the other nine available functions.
D5	FB_B3	Buck3 feedback sense for output regulation. It is used to detect output voltage status for OVP, UVP, and Power Good of Buck3. Connect it to the Buck3 output capacitor.
D6	AVIN	Input voltage pin of internal analog circuitry. Connecting the ceramic capacitor (C = 2.2μF/0402) as close as possible from the AVIN pin to the AGND pin is necessary. It is also used to detect input voltage status for VIN OV and UV.
E1	FB_B4	Buck4 feedback sense for output regulation. It is used to detect output voltage status for OVP, UVP, and Power Good of Buck4. Connect it to the Buck4 output capacitor.
E2	GPIO8	By default, GPIO8 is configured as a Sleep Mode 2 input pin with an open drain configuration, which requires the use of an external pull-up resistor. Once the AVIN voltage exceeds the UVLO threshold, the user can select GPIO8 to perform one of the other nine available functions.
E3	GPIO1	GPIO1 is an output pin dedicated to the nRESET signal. Following the power-up sequence of Buck1, the state of nRESET provides an indication of the PMIC's status: nRESET = H indicates PMIC is in a Power-Good (PG) state, whereas nRESET = L indicates a Power Bad (PBAD) status.
E4, F3, F4	PGND34	Power Stage Power Ground for Buck3 and Buck4. This is the ground return path for the low-side power MOSFETs and drivers of Buck3 and Buck4. To minimize the parasitic impedance and thermal resistance, it is essential to directly solder this ground to a large PCB Power Ground (PGND) plane and to incorporate thermal vias beneath the PGND pin.

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Pin No.	Pin Name	Pin Function
E5	GPIO4	GPIO4 is initially set as an EXT_EN1_O output pin with an open drain configuration, which requires the use of an external pull-up resistor. Once the AVIN voltage exceeds the UVLO threshold, the user can select GPIO4 to perform one of the other nine available functions.
E6	VIN_B3	Buck3 input voltage pin. It is internally connected to the source terminal of the Buck3 high-side MOSFET. It is necessary to connect a ceramic capacitor (C = 10μF/0603) as close as possible from the VIN_B3 pin to the PGND34 pin.
F1	VIN_B4	Buck4 input voltage pin. It is internally connected to the source terminal of the Buck4 high-side MOSFET. It is necessary to connect a ceramic capacitor (C = 10μF/0603) as close as possible from the VIN_B4 pin to the PGND34 pin.
F2	SW_B4	Switch node of Buck4. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to the output inductor and keep the sensitive trace and signals away.
F5, F6	SW_B3	Switch node of Buck3. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to the output inductor and keep the sensitive trace and signals away.

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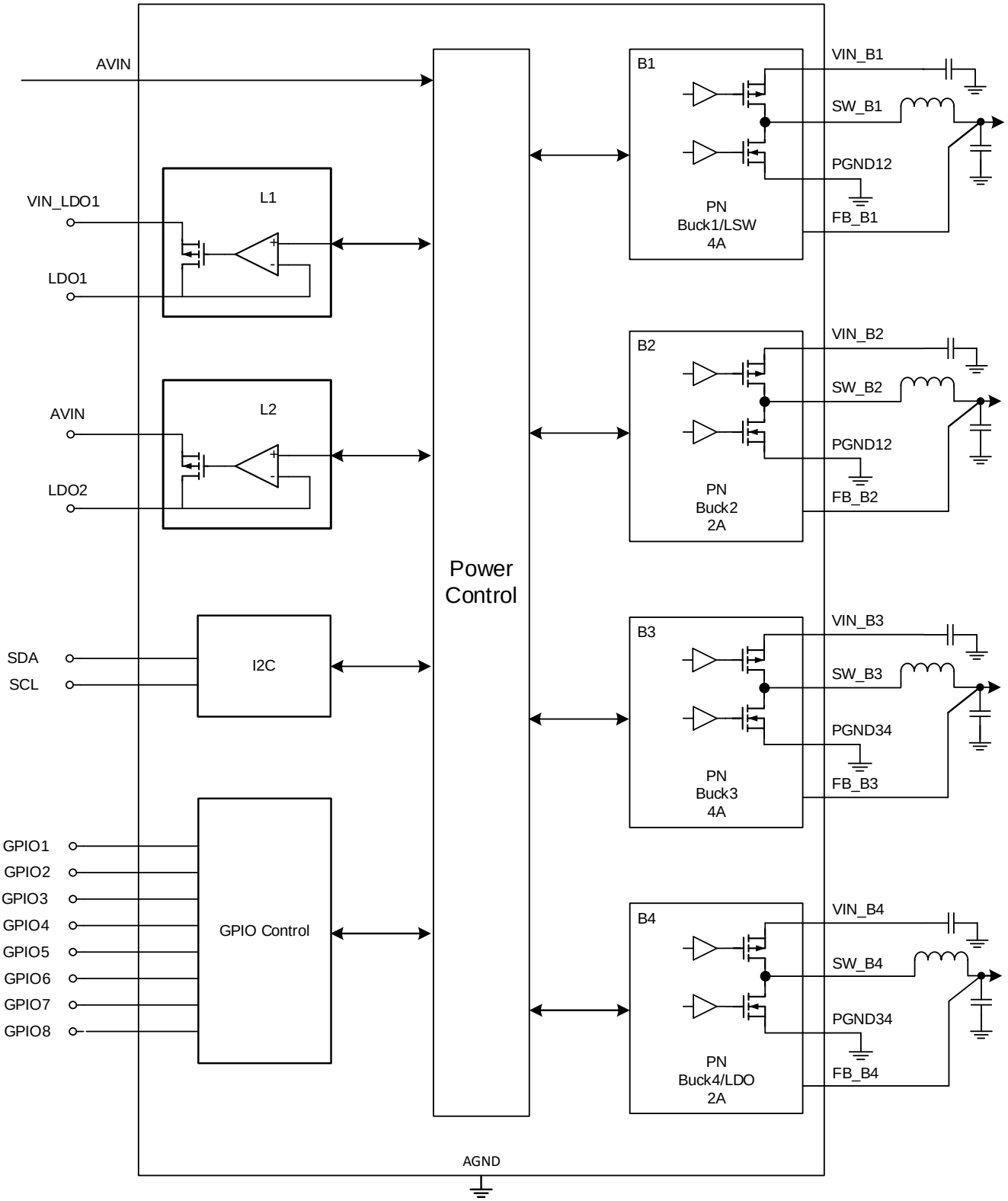
9 Functional Block Diagram



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10 Absolute Maximum Ratings

(Note 3)

- Supply Input Voltage, VIN ---------- –0.3V to 6V
- VIN_B1, VIN_B2, VIN_B3, VIN_B4, AVIN, VIN_LDO1 ---------- –0.3V to 6V
- SWx to PGNDx (DC) ---------- –0.3V to 6V
- SWx to PGNDx (<100ns) ---------- –0.3V to 6.5V
- SWx to PGNDx (<10ns) ---------- –2.5V to 9.0V
- PGNDx to AGNDx ---------- –0.3V to 0.3V
- Other Pins to AGNDx ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-36B 2.66x2.70 (BSC) ---------- 3.5W
- Package Thermal Resistance (Note 4)

  WL-CSP-36B 2.66x2.70 (BSC), θ_{JA} ---------- 28.56°C/W
- Lead Temperature (Soldering, 10 sec) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)

  HBM (Human Body Model) ---------- ±2kV

  CDM (Charge Device Model) ---------- ±500V

Note 3. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 4. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-9 thermal measurement standard.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 6)

- Supply Input Voltage ---------- 2.7V to 3.7V
- Other Pins ---------- 0V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 6. The device is not guaranteed to function outside its operating conditions.

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12 Electrical Characteristics

(VIN_B1 = VIN_B2 = VIN_B3 = VIN_B4 = AVIN = VIN_LDO1 = 3.3V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input Voltage Range						
VIN_B1 to PGND12 VIN_B2 to PGND12 VIN_B3 to PGND34 VIN_B4 to PGND34	V_{VIN_Bx}	Input voltage range	2.7	--	3.7	V
VIN_LDO1 to AGND	V_{VIN_LDO1}	LDO mode	1.62	--	5.5	V
	$V_{VIN_LDO1_NLSW}$	NLSW mode	0.4	--	3.6	
	$V_{VIN_LDO1_PLSW}$	PLSW mode	1.62	--	AVIN	
AVIN UVLO	$V_{AVIN_UV_F_TH}$	Falling threshold	2.4	2.5	2.6	V
	$V_{AVIN_UVLO_HYS}$	Hysteresis	--	100	--	mV
AVIN OV	$V_{AVIN_OV_R_TH}$	Rising threshold	3.8	3.9	4	V
	$V_{AVIN_OV_HYS}$	Hysteresis	--	300	--	mV
AVIN POK OV	$V_{AVIN_POK_R_TH}$	REG_0x10_bit 7 = 0b, rising threshold	3.38	3.5	3.62	V
		REG_0x10_bit 7 = 1b, rising threshold	3.66	3.8	3.93	V
	$V_{AVIN_POK_HYS}$	Hysteresis	100	200	300	mV
	$t_{AVIN_POK_R_DEG}$	Deglitch time	--	10	--	μs
Operating Supply Current						
AVIN Supply Current	I_{AVIN_Q}	All rails are off	--	30	--	μA
VIN_LDO1	$I_{VIN_LDO1_Q}$	Normal mode	--	31	--	μA
	$I_{VIN_LDO1_LPM_Q}$	Low power mode, LPM	--	15	--	
VIN_Bx	$I_{VIN_Bx_Q}$	Normal mode	--	25	35	μA
	$I_{VIN_Bx_LPM_Q}$	Low power mode, LPM	--	15	25	
System Monitor/Warning						
SYSMON Rising Threshold	$V_{SYSMON_R_TH}$	25mV Step	2.725	--	3.1	V
SYSMON Accuracy			–3.5	--	3.5	%
SYSWARN Rising Threshold	$V_{SYSWARN_R_TH}$	25mV Step	2.755	--	3.15	V
SYSWARN Accuracy			–3.5	--	3.5	%

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Deglitch Time						
AVIN UV	$t_{AVIN_UV_R_EXIT}$		--	20	--	μs
AVIN OV	$t_{AVIN_OV_R_TH}$		--	10	--	μs
Others						
Over-Temperature Protection	$T_{Critical_SD}$	Temperature for critical shutdown	--	150	--	°C
	$T_{Recovery_HYS}$	Hysteresis for thermal recovery	--	25	--	
	$T_{Interrupt_TH}$	Interrupt flag threshold	--	110	--	
OV/UV Retry Time	$t_{Recovery_Dwell_Time}$	VIN = 3.3V, power rails OV or UV	--	200	--	ms
Bx Startup Delay		Bx_ON_DLY_Bits = 000b	--	0	--	ms
		Bx_ON_DLY_Bits = 001b	--	0.25	--	
		Bx_ON_DLY_Bits = 010b	--	0.5	--	
		Bx_ON_DLY_Bits = 011b	--	0.75	--	
		Bx_ON_DLY_Bits = 100b	--	1	--	
		Bx_ON_DLY_Bits = 101b	--	2	--	
		Bx_ON_DLY_Bits = 110b	--	4	--	
		Bx_ON_DLY_Bits = 111b	--	8	--	
Bx Turn Off Delay		Bx_OFF_DLY_Bits = 000b	--	0	--	ms
		Bx_OFF_DLY_Bits = 001b	--	0.25	--	
		Bx_OFF_DLY_Bits = 010b	--	0.5	--	
		Bx_OFF_DLY_Bits = 011b	--	0.75	--	
		Bx_OFF_DLY_Bits = 100b	--	1	--	
		Bx_OFF_DLY_Bits = 101b	--	2	--	
		Bx_OFF_DLY_Bits = 110b	--	4	--	
		Bx_OFF_DLY_Bits = 111b	--	8	--	
EXT_EN Delay		EXT_EN1_DLY_Bits = 0000b	--	0	--	ms
		EXT_EN1_DLY_Bits = 0001b	--	0.25	--	
		EXT_EN1_DLY_Bits = 0010b	--	0.5	--	
		EXT_EN1_DLY_Bits = 0011b	--	0.75	--	
		EXT_EN1_DLY_Bits = 0100b	--	1	--	
		EXT_EN1_DLY_Bits = 0101b	--	1.25	--	
		EXT_EN1_DLY_Bits = 0110b	--	1.5	--	
		EXT_EN1_DLY_Bits = 0111b	--	1.75	--	
		EXT_EN1_DLY_Bits = 1000b	--	2	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
		EXT_EN1_DLY_Bits = 1001b	--	2.25	--	
		EXT_EN1_DLY_Bits = 1010b	--	2.5	--	
		EXT_EN1_DLY_Bits = 1011b	--	2.75	--	
		EXT_EN1_DLY_Bits = 1100b	--	3	--	
		EXT_EN1_DLY_Bits = 1101b	--	3.25	--	
		EXT_EN1_DLY_Bits = 1110b	--	3.5	--	
		EXT_EN1_DLY_Bits = 1111b	--	3.75	--	
nRESET		POR_DLY_TIME_Bits = 000b	--	0.5	--	ms
		POR_DLY_TIME_Bits = 001b	--	1	--	
		POR_DLY_TIME_Bits = 010b	--	2	--	
		POR_DLY_TIME_Bits = 011b	--	4	--	
		POR_DLY_TIME_Bits = 100b	--	8	--	
		POR_DLY_TIME_Bits = 101b	--	16	--	
		POR_DLY_TIME_Bits = 110b	--	32	--	
		POR_DLY_TIME_Bits = 111b	--	64	--	
Buck1 Converter						
Output Voltage Range	V_{B1_VOUT}	B1 (Buck1) VID Range	1.7	--	2.9	V
	$V_{B1_Per_Step}$	B1 programmable step	--	20	--	mV
Standby Current	$I_{Standby_B1}$	Enable, not switching	--	25	35	µA
		Enable, not switching, LPM	--	15	25	
Output Voltage Accuracy	V_{B1_Error}	GPIO2 = Hi-Z or Low	2.475	2.5	2.525	V
Line Regulation		VIN = 2.7V to 3.7V	--	0.5	--	%/V
Load Regulation		I_{OUT} = 0 to Max Rating	--	0.5	--	%/A
Transient Load Regulation	$V_{B1_TLR_Error}$	VIN_B1 = 3.3V, FB1 = 2.5V, L = 0.47µH, C_{OUT} = 22µF x 2. 1. Load = 1A to 2A @ 0.2A/µs 2. Load = 50mA to 1A @ 0.2A/µs	–75 (–3%)	--	100 (4%)	mV
PG Threshold (Low Level)	$V_{B1_PGL_R_0b}$	VOUT_B1 rises from 0V to PG rising (EFUSE_UVSEL = 0b, default)	90	93	96	%
	$V_{B1_PGL_R_1b}$	VOUT_B1 rises from 0V to PG rising (EFUSE_UVSEL = 1b)	82	85	88	
	$V_{B1_PGL_HYS}$	VOUT_B1 falls from VID to PG falling	--	3	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PG Threshold (High Level)	$V_{B1_PGH_F}$	VOUT_B1 rises from VID to PG falling	107	110	113	%
	$V_{B1_PGH_HYS}$	VOUT_B1 falls from VID to PG rising	--	3	--	%
Switching Frequency	f_{SW_B1}	REG_0x1B[3:1] = 101b	1.8	2	2.2	MHz
Minimum Off-Time	$t_{B1_OFF_MIN}$		--	120	160	ns
Soft-Start Time	$t_{B1_Soft_Start}$	REG_0x19[7:6] = 00b. The time for VOUT to rise from 10% to 90% of 2.5V.	--	50	--	µs
		REG_0x19[7:6] = 01b (Default). The time for VOUT to rise from 10% to 90% of 2.5V.	--	100	--	
		REG_0x19[7:6] = 10b. The time for VOUT to rise from 10% to 90% of 2.5V.	--	200	--	
		REG_0x19[7:6] = 11b. The time for VOUT to rise from 10% to 90% of 2.5V.	--	300	--	
Current Limit	I_{B1_CL}	Valley Current, REG_0x1B[7:6] = 00b	3.5	4	--	A
		Valley Current, REG_0x1B[7:6] = 01b	4.5	5	--	
		Valley Current, REG_0x1B[7:6] = 10b	5.5	6	--	
		Valley Current, REG_0x1B[7:6] = 11b	6.5	7	--	
PMOS On-Resistance	$R_{DS(ON)_B1_P}$	PVIN = 3.3V	--	60	--	mΩ
NMOS On-Resistance	$R_{DS(ON)_B1_N}$	PVIN = 3.3V	--	35	--	mΩ
Output Discharge Resistance	R_{DISCH_B1}		--	4.4	--	Ω
Efficiency	Eff_{B1}	PVIN = 3.3V, FB_B1 = 2.5V, I_{OUT} = 10mA	85	--	--	%
		PVIN = 3.3V, FB_B1 = 2.5V, I_{OUT} = 1A	90	--	--	
Buck1 Bypass Mode						
Input Voltage Range	$V_{VIIN_B1_BYP}$	GPIO2 = H	2.7	3.3	3.7	V
PMOS On-Resistance	$R_{DS(ON)_B1_BYP_P}$	I_{SW} = –1A, VIN_B1 = 3.3V	--	60	--	mΩ

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal PMOS Shutdown Current	$I_{B1_BYP_OC_OFF}$	REG_0x1B[7:6] = any, all registers code (00~11) are the same as OC value	4.5	5	--	A
Internal PMOS Shutdown Current Off-Time	$t_{B1_BYP_OC_OFF}$		--	14	--	ms
Internal PMOS Soft-Start Time	$t_{B1_BYP_SStart}$	PVIN = 3.3V	--	250	--	μs
OV Threshold	$V_{B1_BYP_OV_TH}$		--	3.8	--	V
OV Deglitch Time	$t_{B1_BYP_OV_DEG}$		--	20	--	μs
Buck2 Converter						
Output Voltage Range	V_{B2_VOUT}	B2 (Buck2) VID range	0.5	--	1.3	V
	$V_{B2_Per_Step}$	B2 programmable step	--	10	--	mV
Standby Current	$I_{Standby_B2}$	Enable, not switching	--	25	35	μA
		Enable, not switching, LPM	--	15	25	
Output Voltage Accuracy	V_{B2_Error}	GPIO2 = any state	0.901	0.91	0.911	V
Line Regulation		VIN = 2.7V to 3.7V	--	0.5	--	%/V
Load Regulation		I_{OUT} = 0 to max rating	--	0.5	--	%/A
Transient Load Regulation	$V_{B2_TLR_Error}$	VIN_B2 = 3.3V, FB2 = 0.91V, L = 0.47μH, C_{OUT} = 22μF. 1. Load = 1A to 2A @ 0.2A/μs 2. Load = 50mA to 1A @ 0.2A/μs	–27 (–3%)	--	36 (4%)	mV
PG Threshold (Low Level)	$V_{B2_PGL_R_0b}$	VOUT_B2 rises from 0V to PG rising (EFUSE_UVSEL = 0b, Default)	90	93	96	%
	$V_{B2_PGL_R_1b}$	VOUT_B2 rises from 0V to PG rising (EFUSE_UVSEL = 1b)	82	85	88	%
	$V_{B2_PGL_HYS}$	VOUT_B2 falls from VID to PG falling	--	3	--	%
PG Threshold (High Level)	$V_{B2_PGH_F}$	VOUT_B2 rises from VID to PG falling	107	110	113	%
	$V_{B2_PGH_HYS}$	VOUT_B2 falls from VID to PG Rising	--	3	--	%
Switching Frequency	f_{SW_B2}	REG_0x1D[3:1] = 101b	1.8	2	2.2	MHz

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Soft-Start Time	$t_{B2_Soft_Start}$	REG_0x19[5:4] = 00b. The time for VOUT to rise from 10% to 90% of 0.91V.	--	40	--	μs
		REG_0x19[5:4] = 01b (default). The time for VOUT to rise from 10% to 90% of 0.91V.	--	80	--	μs
		REG_0x19[5:4] = 10b. The time for VOUT to rise from 10% to 90% of 0.91V.	--	160	--	μs
		REG_0x19[5:4] = 11b. The time of 10% to 90% of VOUT = 0.91V.	--	240	--	us
Current Limit	I_{B2_CL}	Valley Current, REG_0x1D[7:6] = 00b	1.5	2	--	A
		Valley Current, REG_0x1D[7:6] = 01b	2.5	3	--	A
		Valley Current, REG_0x1D[7:6] = 10b	3.5	4	--	A
		Valley Current, REG_0x1D[7:6] = 11b	4.5	5	--	A
PMOS On-Resistance	$R_{DS(ON)_B2_P}$	PVIN = 3.3V	--	65	--	mΩ
NMOS On-Resistance	$R_{DS(ON)_B2_N}$	PVIN = 3.3V	--	30	--	mΩ
Output Discharge Resistance	R_{DISCH_B2}		--	9.4	--	Ω
Efficiency	Eff_{B2}	PVIN = 3.3V, FB_B1 = 0.91V, I_{OUT} = 10mA	85	--	--	%
		PVIN = 3.3V, FB_B1 = 0.91V, I_{OUT} = 1A	85	--	--	
Buck3 Converter						
Output Voltage Range	V_{B3_VOUT}	B3 (Buck3) VID range	0.5	--	1.3	V
	$V_{B3_Per_Step}$	B3 programmable step	--	10	--	mV
Standby Current	$I_{Standby_B3}$	Enable, not switching	--	25	35	μA
		Enable, not switching, LPM	--	15	25	
Output Voltage Accuracy	V_{B3_Error}	GPIO3 = any state	0.7722	0.78	0.7878	V
Line Regulation		VIN = 2.7V to 3.7V	--	0.5	--	%/V
Load Regulation		I_{OUT} = 0 to max rating	--	0.5	--	%/A

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transient Load Regulation	$V_{B3_TLR_Error}$	VIN_B3 = 3.3V, FB3 = 0.78V, L = 0.47μH, C_{OUT} = 22μF. 1. Load = 2A to 4A @ 0.2A/μs 2. Load = 50mA to 2A @ 0.2A/μs	–27.3 (–3.5%)	--	31.2 (4%)	mV
PG Threshold (Low Level)	$V_{B3_PGL_R_0b}$	VOUT_B3 rises from 0V to PG rising (EFUSE_UVSEL = 0b, Default)	90	93	96	%
	$V_{B3_PGL_R_1b}$	VOUT_B3 rises from 0V to PG rising (EFUSE_UVSEL = 1b)	82	85	88	
	$V_{B3_PGL_HYS}$	VOUT_B3 falls from VID to PG falling	--	3	--	
PG Threshold (High Level)	$V_{B3_PGH_F}$	VOUT_B3 rises from VID to PG falling	107	110	113	%
	$V_{B3_PGH_HYS}$	VOUT_B3 falls from VID to PG rising	--	3	--	
Switching Frequency	f_{SW_B3}	REG_0x1F[3:1] = 101b	1.8	2	2.2	MHz
Soft-Start Time	$t_{B3_Soft_Start}$	REG_0x19[3:2] = 00b. The time for VOUT to rise from 10% to 90% of 0.78V.	--	35	--	μs
		REG_0x19[3:2] = 01b (default) . The time for VOUT to rise from 10% to 90% of 0.78V.	--	70	--	
		REG_0x19[3:2] = 10b. The time for VOUT to rise from 10% to 90% of 0.78V.	--	140	--	
		REG_0x19[3:2] = 11b. The time for VOUT to rise from 10% to 90% of 0.78V.	--	210	--	
Current Limit	I_{B3_CL}	Valley Current, REG_0x1F[7:6] = 00b	3.5	4	--	A
		Valley Current, REG_0x1F[7:6] = 01b	4.5	5	--	
		Valley Current, REG_0x1F[7:6] = 10b	5.5	6	--	
		Valley Current, REG_0x1F[7:6] = 11b	6.5	7	--	
PMOS On-Resistance	$R_{DS(ON)_B3_P}$	PVIN = 3.3V	--	55	--	mΩ
NMOS On-Resistance	$R_{DS(ON)_B3_N}$	PVIN = 3.3V	--	25	--	mΩ

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dynamic Voltage Scaling Rate	$V_{DVID_UP_B3}$	REG_0x1F[5:4] = 00b	--	20	--	mV/μs
		REG_0x1F[5:4] = 01b	--	15	--	
		REG_0x1F[5:4] = 10b	--	10	--	
		REG_0x1F[5:4] = 11b	--	5	--	
Output Discharge Resistance	R_{DISCH_B3}		--	9.4	--	Ω
Efficiency	Eff_{B3}	PVIN = 3.3V, FB_B3 = 0.78V, I_{OUT}= 1mA, LPM	80	--	--	%
		PVIN = 3.3V, FB_B3 = 0.78V, I_{OUT} = 1A	85	--	--	
Buck4 Converter						
Output Voltage Range	V_{B4_VOUT}	B4 (Buck4) VID range	0.9	--	2.0	V
	$V_{B4_Per_Step}$	B4 programmable step	--	10	--	mV
Standby Current	$I_{Standbyt_B4}$	Enable, not switching	--	25	35	μA
		Enable, not switching, LPM	--	15	25	
Output Voltage Accuracy	V_{B4_Error}	GPIO4 = High	1.089	1.1	1.111	V
Output Voltage Accuracy	V_{B4_Error}	GPIO4 = Hi-Z or Low	1.188	1.2	1.212	V
Line Regulation		VIN = 2.7V to 3.7V	--	0.5	--	%/V
Load Regulation		IOUT = 0 to max rating	--	0.5	--	%/A
Transient Load Regulation	$V_{B4_TLR_Error}$	VIN_B4 = 3.3V, FB4 = 1.1V, L = 0.47μH, C_{OUT} = 22μF. 1. Load = 1A to 2A @ 0.2A/μs 2. Load = 50mA to 1A @ 0.2A/μs	–33 (–3%)	--	44 (4%)	mV
		VIN_B4 = 3.3V, FB4 = 1.2V, L = 0.47μH, C_{OUT} = 22μF. 1. Load = 1A to 2A @ 0.2A/μs 2. Load = 50mA to 1A @ 0.2A/μs	–36 (–3%)	--	48 (4%)	
PG Threshold (Low Level)	$V_{B4_PGL_R_0b}$	VOUT_B4 rises from 0V to PG rising (EFUSE_UVSEL = 0b, default)	90	93	96	%
	$V_{B4_PGL_R_1b}$	VOUT_B4 rises from 0V to PG rising (EFUSE_UVSEL = 1b)	82	85	88	
	$V_{B4_PGL_HYS}$	VOUT_B4 falls from VID to PG falling	--	3	--	
PG Threshold (High Level)	$V_{B4_PGH_F}$	VOUT_B4 rises from VID to PG falling	107	110	113	%
	$V_{B4_PGH_HYS}$	VOUT_B4 falls from VID to PG rising	--	3	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency	f_{SW_B4}	REG_0x22[3:1] = 101b	1.8	2	2.2	MHz
Soft-Start Time	$t_{B4_Soft_Start}$	REG_0x19[1:0] = 00b. The time for VOUT to rise from 10% to 90% of 1.1V	--	45	--	µs
		REG_0x19[1:0] = 01b (default). The time for VOUT to rise from 10% to 90% of 1.1V	--	90	--	
		REG_0x19[1:0] = 10b. The time for VOUT to rise from 10% to 90% of 1.1V	--	180	--	
		REG_0x19[1:0] = 11b. The time for VOUT to rise from 10% to 90% of 1.1V	--	270	--	
Current Limit	I_{B4_CL}	Valley Current, REG_0x22[7:6] = 00b	1.5	2	--	A
		Valley Current, REG_0x22[7:6] = 01b	2.5	3	--	
		Valley Current, REG_0x22[7:6] = 10b	3.5	4	--	
		Valley Current, REG_0x22[7:6] = 11b	4.5	5	--	
PMOS On-Resistance	$R_{DS(ON)_B4_P}$	PVIN = 3.3V	--	70	--	mΩ
NMOS On-Resistance	$R_{DS(ON)_B4_N}$	PVIN = 3.3V	--	40	--	mΩ
Output Discharge Resistance	R_{DISCH_B4}		--	9.4	--	Ω
Efficiency	Eff_{B3}	PVIN = 3.3V, FB_B4 = 1.2V, I_{OUT} = 10mA, LPM	85	--	--	%
		PVIN = 3.3V, FB_B4 = 1.2V, I_{OUT} = 1A	85	--	--	
B4_LDO Mode						
Output Voltage Range	$V_{B4_LDO_VOUT}$	GPIO4 = Hi-Z for optional setting	0.9	1.8	2.0	V
Output Voltage Range	$V_{B4_LDO_Per_Step}$	B4_LDO programmable step	--	10	--	mV
Standby Current	$I_{Standby_B4_LDO}$	Enabled, no load, low power mode	--	15	--	µA
		Enabled, no load	--	31	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Accuracy	$V_{B4_LDO_Error}$	AVIN > B4_LDO + 0.4V @ Normal, VNOM = 1.8V (25°C)	-1	--	1	%
		AVIN > B4_LDO + 0.4V@ Normal, VNOM = 1.8V (-40~125°C)	−1.5	--	1.5	
Line Regulation (GBD) (Note 7)		AVIN = 2.7V to 3.3V, B4_LDO Load 5mA @ Normal, VNOM = 1.8V	--	0.5	--	%/V
Load Regulation (GBD)		AVIN > B4_LDO + 0.4V, Load = 1mA to 390mA @ Normal VNOM = 1.8V	--	0.5	--	%/A
Transient Load Regulation (GBD)	$V_{B4_LDO_TLR_Err}$	AVIN > B4_LDO + 0.4V VNOM = 1.8V, C_{OUT} = 2.2µF 1. Load = 5mA to 50mA @ 0.2A/µs 2. Load = 50mA to 100mA @ 0.2A/µs	−3.5	--	+3.5	%
PG Threshold (Low Level)	$V_{B4_LDO_PGL_R_0b}$	VOUT_B4_LDO rises from 0V to PG rising (EFUSE_UVSEL = 0b, default)	90	93	96	%
	$V_{B4_LDO_PGL_R_1b}$	VOUT_B4_LDO rises from 0V to PG rising (EFUSE_UVSEL = 1b)	82	85	88	
	$V_{B4_LDO_PGL_HYS}$	VOUT_B4_LDO falls from VID to PG falling	--	3	--	
PG Threshold (High Level)	$V_{B4_LDO_PGH_F}$	VOUT_B4_LDO rises from VID to PG falling	107	110	113	%
	$V_{B4_LDO_PGH_HYS}$	VOUT_B4_LDO falls from VID to PG rising	--	3	--	
Soft-Start Time	$t_{B4_LDO_Soft_Start}$	B4_LDO = 10% to 90% of VNOM, REG_0x19[0] = 0b	--	140	--	µs
		B4_LDO = 10% to 90% of VNOM, REG_0x19[0] = 1b	--	280	--	
Dropout Voltage	$V_{B4_LDO_DROP}$	AVIN = 2.7V, B4_LDO = 2.6V, Load = 200mA @ Normal	--	--	200	mV
		AVIN = 2.7V, B4_LDO = 2.5V, Load = 400mA @ Normal	--	--	400	
Discharge Resistance	$R_{DISCH_B4_LDO}$		--	9.4	--	Ω
Overcurrent Protection	$I_{B4_LOD_CL}$	AVIN > B4_LDO + 0.4V @ Normal, REG_0x22[6] = 0b	300	400	--	mA
		AVIN > B4_LDO + 0.4V @ Normal, REG_0x22[6] = 1b (default)	400	500	--	
PG/OV Deglitch Time (GBD)	$t_{B4_LDO_PG/OV_DEG}$		--	20	--	µs

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LDO1						
Output Voltage Range	V_{LDO1_VOUT}	LDO1 VID range	1	1.8	2.7	V
Output Voltage Programmable Step	$V_{LDO1_Per_Step}$	LDO1 programmable step	--	50	--	mV
Standby Current	$I_{Standby_LDO1}$	Enabled, no load, low power mode	--	15	--	μA
		Enabled, no load,	--	31	--	
Output Voltage Accuracy	V_{LDO1_Error}	AVIN = VIN_LDO1 > LDO1 + 0.4V @ Normal, VNOM = 2.5V (25°C)	−1	--	1	%
		AVIN = VIN_LDO1 > LDO1 + 0.4V@ Normal, VNOM = 2.5V (-40~125°C)	−1.5	--	1.5	
Line Regulation (GBD)		AVIN = VIN_LDO1 = 2.7V to 3.3V, LDO1 Load 5mA @ Normal, VNOM = 2.5V.	--	0.5	--	%/V
Load Regulation (GBD)		AVIN = VIN_LDO1 > LDO1 + 0.4V, LDO1 Load = 1mA to 390mA @ Normal, VNOM = 2.5V.	--	0.5	--	%/A
Transient Load Regulation (GBD)	$V_{LDO1_TLR_Err}$	AVIN = VIN_LDO1 > LDO1 + 0.4V, VNOM = 2.5V, C_{OUT} = 2.2μF 1. Load= 5mA to 50mA @ 0.2A/μs 2. Load= 50mA to 100mA @ 0.2A/μs	−3.5	--	3.5	%
PG Threshold (Low Level)	$V_{LDO1_PGL_R}$	V_{LDO1} rises from 0V to PG rising	81	84	88	%
	$V_{LDO1_PGL_HYS}$	V_{LDO1} falls from VID to PG falling	--	4	--	
PG Threshold (High Level)	$V_{LDO1_PGH_F}$	V_{LDO1} rises from VID to PG falling	111	114	118	%
	$V_{LDO1_PGH_HYS}$	V_{LDO1} falls from OV to PG rising	--	8	--	%
Soft-Start Time	$t_{LDO1_Soft_Start}$	LDO1 = 10% to 90% of VNOM, REG_0x1A[7] = 0b (Default)	--	60	--	μs
		LDO1 = 10% to 90% of VNOM, REG_0x1A[7] = 1b	--	120	--	
Dropout Voltage	V_{LDO1_DROP}	AVIN = VIN_LDO1 = 2.7V, LDO1 = 2.6V, Load = 200mA @ Normal	--	--	200	mV
		AVIN = VIN_LDO1 = 2.7V, LDO1 = 2.5V, Load = 400mA @ Normal	--	--	400	
Discharge Resistance	R_{DISCH_LDO1}	Discharged path enabled when LDO1 is disabled.	--	20	--	Ω

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Overcurrent Protection	I_{LOD1_CL}	AVIN = VIN_LDO1 > LDO1 + 0.4V @ Normal, EFUSE_LDO1_LIM = 0b	300	400	--	mA
		AVIN = VIN_LDO1 > LDO1 + 0.4V @ Normal, EFUSE_LDO1_LIM = 1b	400	500	--	
LDO1_LSW Mode (Load Switch)						
Operating Voltage Range	$V_{LDO1_SW_VIN}$	NLSW mode, GPIO4 = Hi-z EFUSE_LDO1_LSW_SEL = 0b	0.4	--	AVIN −1	V
		PLSW mode (default), GPIO4 = Hi-z EFUSE_LDO1_LSW_SEL = 1b	--	AVIN	--	
Load Switch On-Resistance	$R_{LDO1_NSW_ON}$	NLSW mode, AVIN = 3.3V, VIN_LDO1 = 0.4V, Load = 100mA	--	50	--	mΩ
	$R_{LDO1_PSW_ON}$	PLSW mode, VIN_LDO1 = 3.3V, Load = 100mA	--	200	--	
Load Switch Standby Current	$I_{Standby_LDO1_SW}$	NLSW mode, enabled, no load, LPM	--	10	--	μA
		NLSW mode, enabled, no load.	--	22	--	
		PLSW mode, enabled, no load	--	12	--	
Soft-Start Time	$t_{LDO1_SW_Soft_Start}$	NLSW mode, VIN_LDO1 = 0.8V, LDO1_LSW = 10% to 90%	--	200	--	μs
		PLSW mode, enable soft-start current limit	--	n/a	--	
Output Current Limit	$I_{LDO1_SW_OC}$	NLSW mode, EFUSE_LDO1_LIM = 0b (default)	0.45	0.6	--	A
		NLSW mode, EFUSE_LDO1_LIM = 1b	0.9	1.2	--	
		PLSW mode, EFUSE_LDO1_LIM = 0b (default)	0.3	0.4	--	
		PLSW mode, EFUSE_LDO1_LIM = 1b	0.4	0.5	--	
OV Protection Threshold	$V_{LDO1_SW_OV}$		--	3.8	--	V
OV Deglitch Time	$t_{LDO1_SW_DEG}$		--	20	--	μs
LDO2						
Output Voltage Range	V_{LDO2_VOUT}	LDO2 VID range, GPIO6 = High	1	1.8	2.7	V
Output Voltage Programmable Step	$V_{LDO2_Per_Step}$	LDO1 programmable step	--	50	--	mV

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Standby Current	$I_{Standby_LDO2}$	Enabled, no load, low power mode	--	15	--	μA
		Enabled, no load	--	31	--	
Output voltage Accuracy	V_{LDO2_Error}	AVIN > LDO2 + 0.4V @ Normal, VNOM = 1.8V (25°C)	–1	--	1	%
		AVIN > LDO2 + 0.4V@ Normal, VNOM = 1.8V (–40 to125°C)	–1.5	--	1.5	
Line Regulation (GBD)		AVIN = 2.7V to 3.3V, LDO2 = 5mA @ Normal, VNOM = 1.8V.	--	0.5	--	%/V
Load Regulation (GBD)		AVIN = LDO2 + 0.4V, LDO2 = 1mA to 390mA @ Normal, VNOM = 1.8V.	--	0.5	--	%/A
Transient Load Regulation (GBD)	$V_{LDO2_TLR_Err}$	AVIN > LDO2 + 0.4V, VNOM = 1.8V, C_{OUT} = 2.2μF 1. Load = 5mA to 50mA @ 0.2A/μs 2. Load = 50mA to 100mA @ 0.2A/μs	–3.5	--	+3.5	%
PG Threshold (Low Level)	$V_{LDO2_PGL_R}$	V_{LDO2} rises from 0V to PG rising	81	84	88	%
	$V_{LDO2_PGL_HYS}$	V_{LDO2} falls from VID to PG falling	--	4	--	
PG Threshold (High Level)	$V_{LDO2_PGH_F}$	V_{LDO2} rises from VID to PG falling	111	114	118	%
	$V_{LDO2_PGH_HYS}$	V_{LDO2} falls from OV to PG rising	--	8	--	
Soft-Start Time	$t_{LDO2_Soft_Start}$	LDO2 = 10% to 90% of VNOM, REG_0x1A[6] = 0b (default)	--	60	--	μs
		LDO2 = 10% to 90% of VNOM, REG_0x1A[6] = 1b	--	120	--	
Dropout Voltage	V_{LDO1_DROP}	AVIN = 2.7V, LDO1 = 2.6V, Load = 200mA @ Normal	--	--	200	mV
		AVIN = 2.7V, LDO1 = 2.5V, Load = 400mA @ Normal	--	--	400	
Discharge Resistance	R_{DISCH_LDO2}		--	20	--	Ω
Overcurrent Protection	I_{LOD2_CL}	AVIN > LDO2 + 0.4V @ Normal, EFUSE_LDO2_LIM = 0b. (default)	300	400	--	mA
		AVIN > LDO2 + 0.4V @ Normal, EFUSE_LDO2_LIM = 1b.	400	500	--	
LDO2_LSW Mode (Load Switch)						
Operating Voltage Range	$V_{LDO2_SW_VIN}$	GPIO6 = Low	--	AVIN	--	V
PMOS On-Resistance	$R_{LDO1_PSW_ON}$		--	200	--	mΩ

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Switch Standby Current	$I_{Standby_LDO2_SW}$	PLSW mode, enabled, no load	--	12	--	μA
Soft-Start Time	$t_{LDO2_SW_Soft_Start}$	PLSW mode, enable soft-start current limit	--	n/a	--	μs
Output Current Limit	$I_{LDO2_SW_OC}$	EFUSE_LDO2_LIM = 0b (default)	0.3	0.4	--	A
		EFUSE_LDO2_LIM = 1b	0.4	0.5	--	
OV Protection Threshold	$V_{LDO2_SW_OV}$		--	3.8	--	V
OV Deglitch Time	$t_{LDO2_SW_DEG}$		--	20	--	μs
Digital I/O						
GPIOs Output Low (Open Drain)	V_{GPIOx_L}		--	--	0.55	V
GPIO1/5/6/7/8 Input High	$V_{GPIO1_5-8_VIN_H}$		1.1	--	--	V
GPIO1/5/6/7/8 Input Low	$V_{GPIO1_508_VIN_L}$		--	--	0.55	V
GPIO2/3/4 Input High	$V_{GPIO2-4_VIN_H}$		2.3	--	--	V
GPIO2/3/4 Input High-Z	$V_{GPIO2-4_VIN_Hi-Z}$		--	1.35	--	V
GPIO2/3/4 Input Low	$V_{GPIO2-4_VIN_L}$		--	--	0.55	V
Input Leakage Current	IIN_{LK}		–3	--	3	μA
Output Leakage Current	$IOUT_{LK}$		–1	--	1	μA
I^2C for Fast Mode						
SDA, SCL Input Voltage High			1.2	--	--	V
SDA, SCL Input Voltage Low			--	--	0.4	V
SCL Clock Rate	f_{SCL}		--	--	400	kHz
Hold Time for a Repeated START Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated.	0.6	--	--	μs
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	μs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	μs
Set Up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	μs

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Data Hold Time	$t_{HD;DAT}$		0	--	0.9	μs
Data Set Up Time	$t_{SU;DAT}$		100	--	--	ns
Set Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time between a STOP and a START Condition	t_{BUF}		1.3	--	--	μs
Rising Time of Both SDA/SCL Signals	t_R		20	--	300	ns
Falling Time of Both SDA/SCL Signals	t_F		20	--	300	ns
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA

Note 7. Guaranteed by design.

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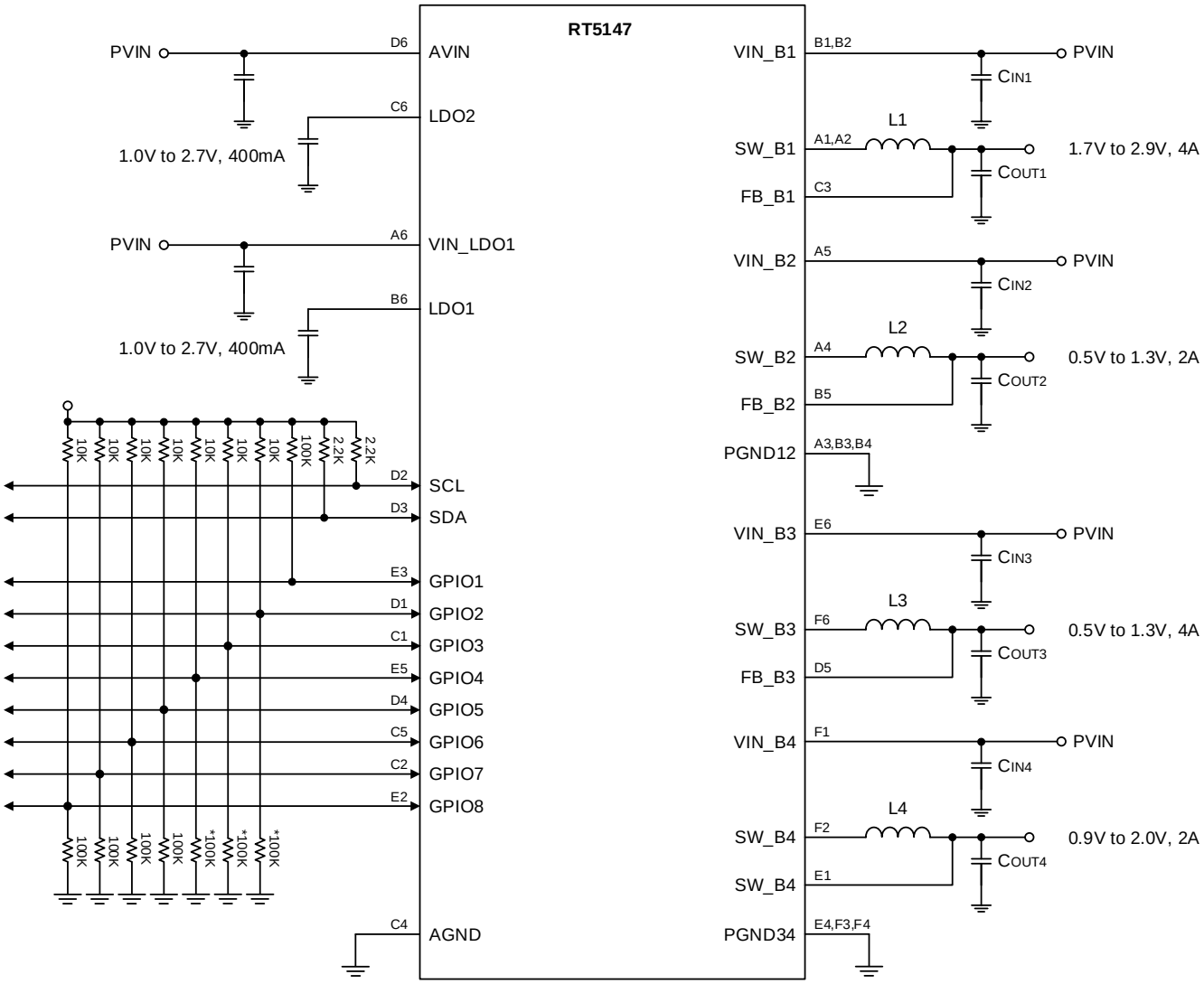
13 Typical Application Circuit



Note 8. If GPIOx is set to High-Z, *100k should be removed.

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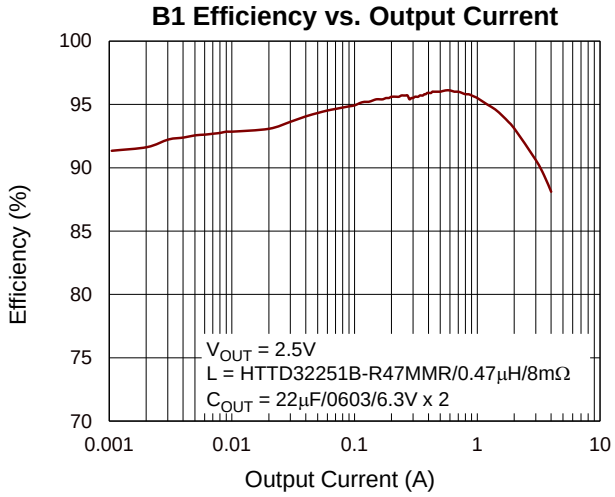
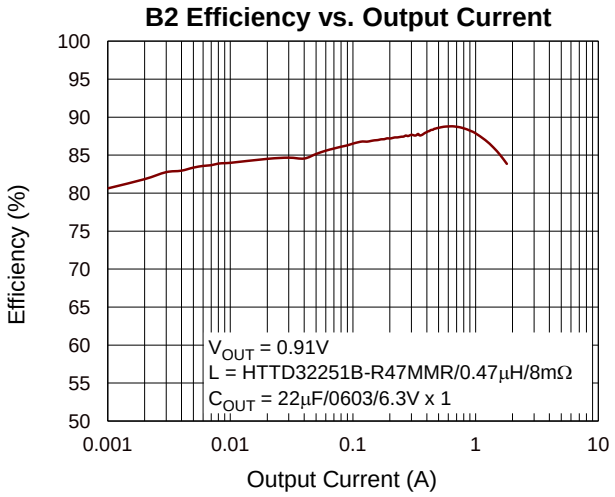
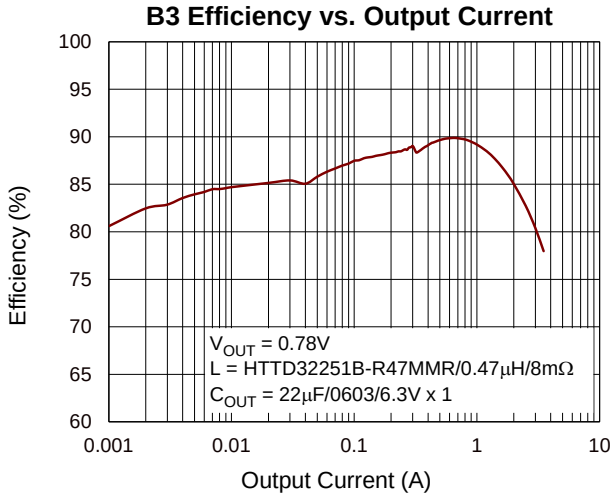
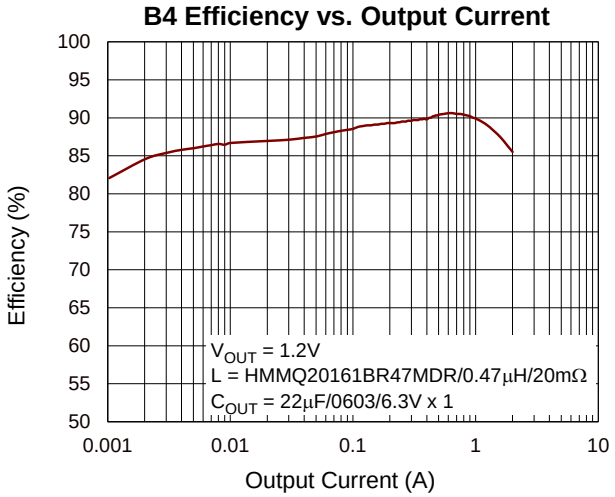
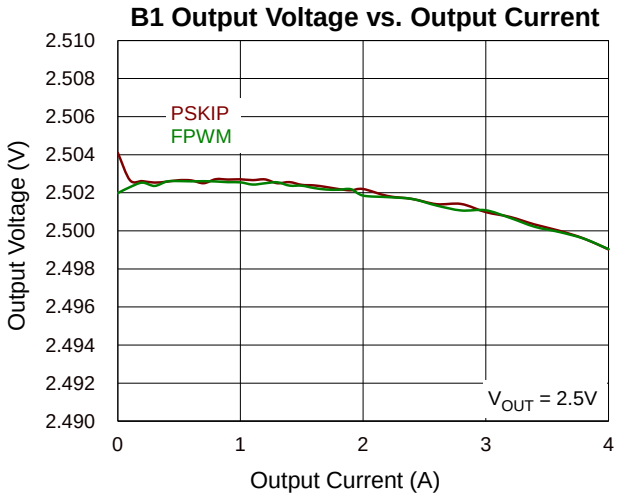
14 Typical Operating Characteristics

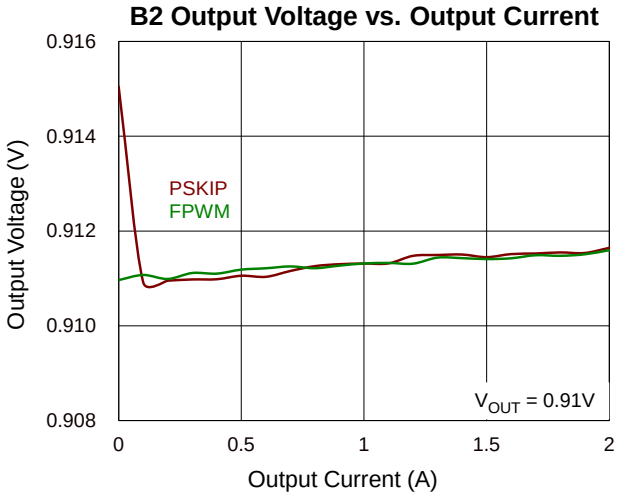












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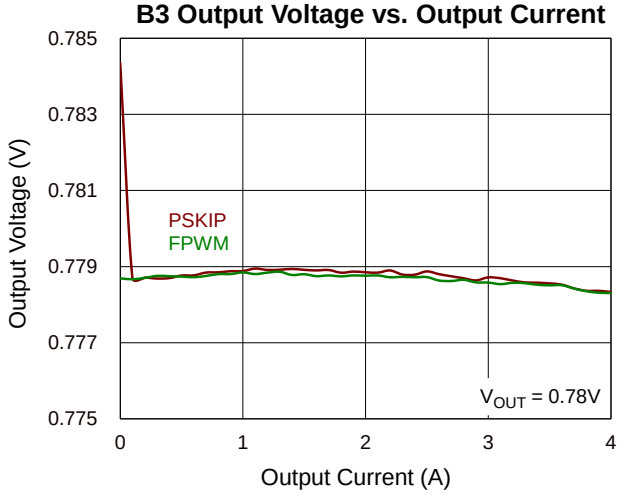
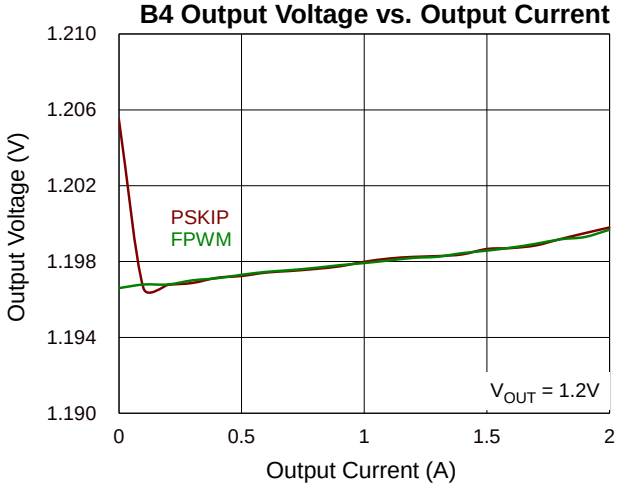
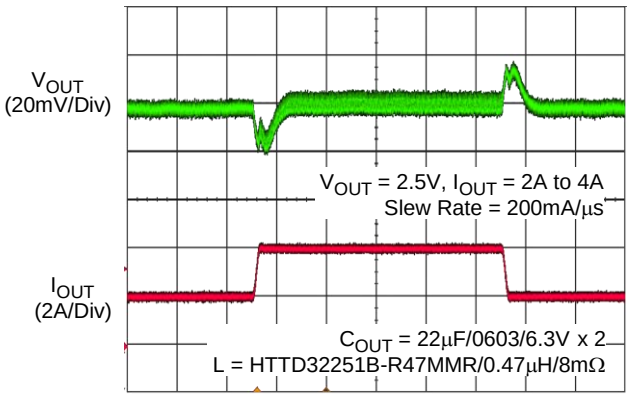
B3 Output Voltage vs. Output Current



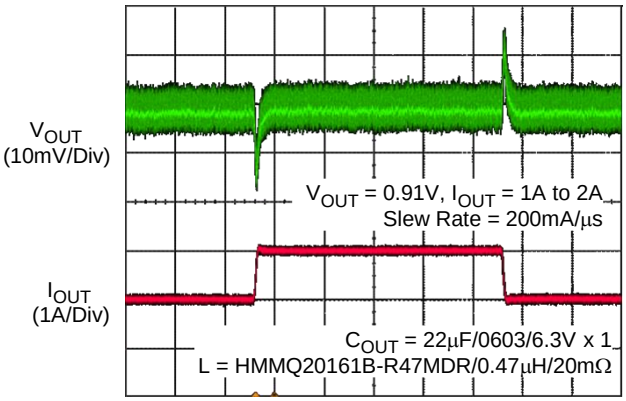
B4 Output Voltage vs. Output Current



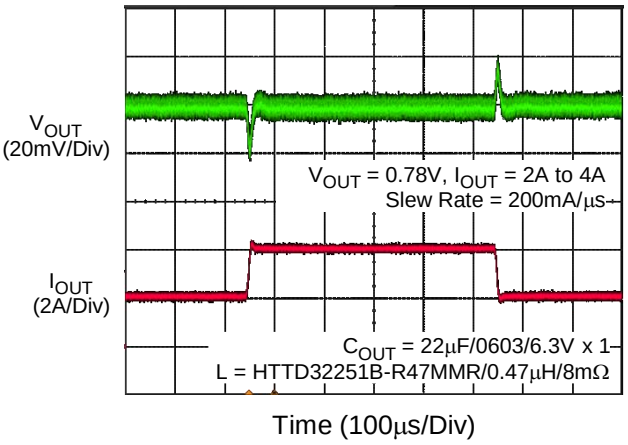
B1 Load Transient Response



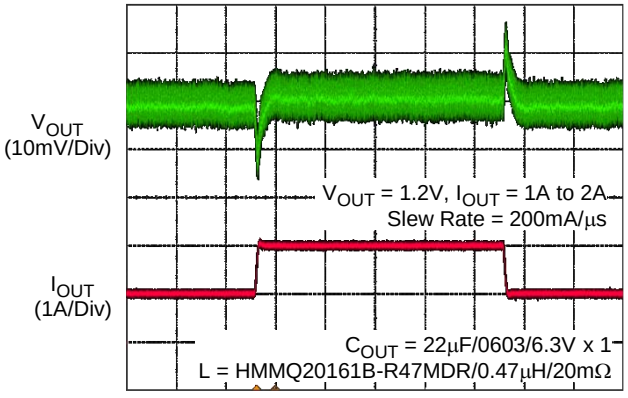
B2 Load Transient Response



B3 Load Transient Response



B4 Load Transient Response



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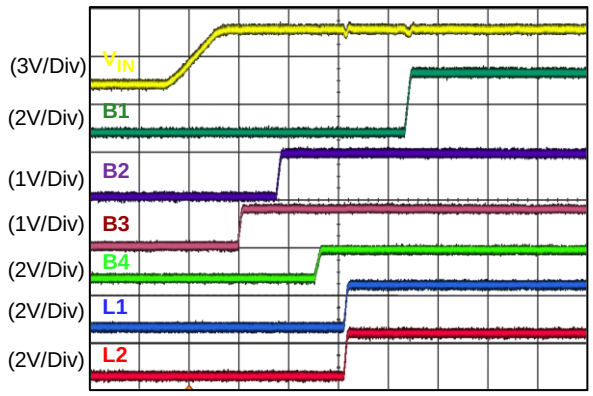
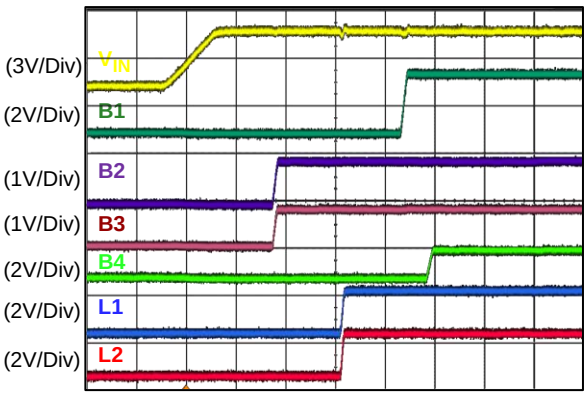
Power Up Sequence for GPIO3 = L



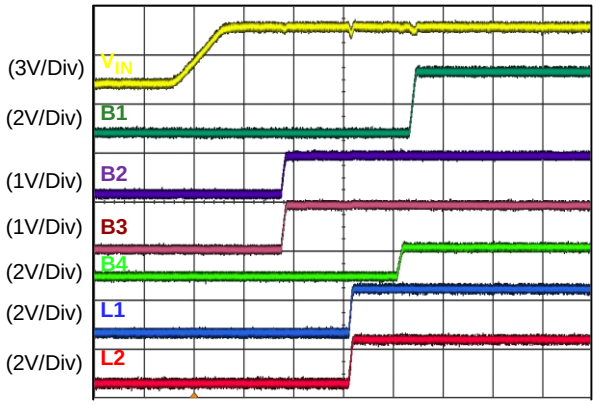
Time (1ms/Div)

Power Up Sequence for GPIO3 = Hiz



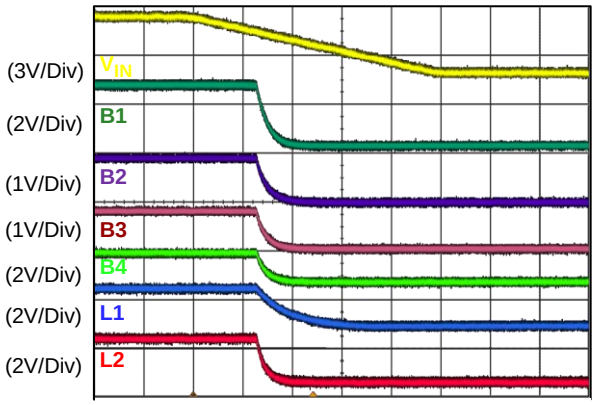
Time (1ms/Div)

Power Up Sequence for GPIO3 = H



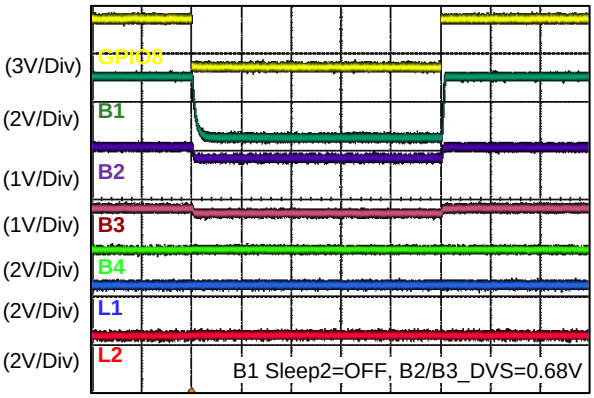
Time (1ms/Div)

Power Off Sequence



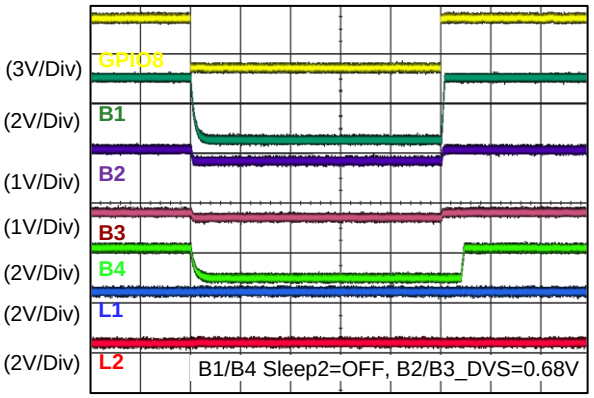
Time (1ms/Div)

PS4.0 Sequence_Case1



Time (2ms/Div)

PS4.0 Sequence_Case2



Time (2ms/Div)

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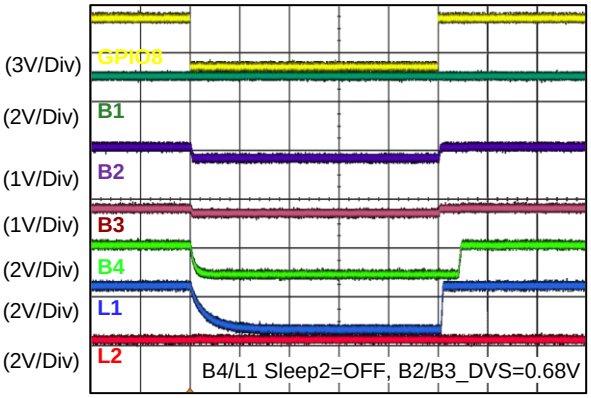
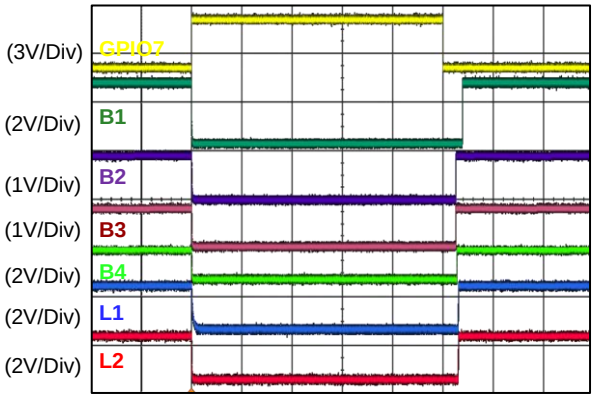
PS4.0 Sequence_Case3



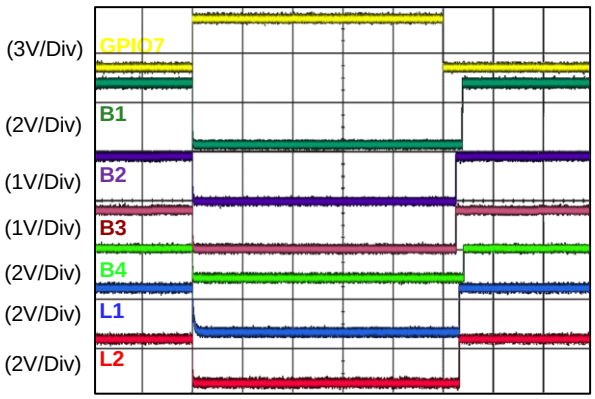
Time (2ms/Div)

PWRDIS Sequence for GPIO3 = L



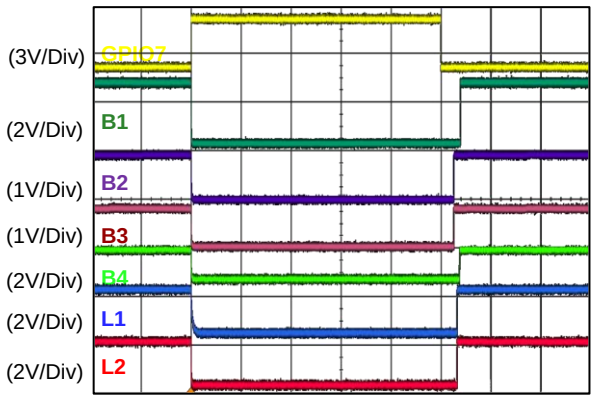
Time (20ms/Div)

PWRDIS Sequence for GPIO3 = Hiz



Time (20ms/Div)

PWRDIS Sequence for GPIO3 = H



Time (20ms/Div)

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15 Operation

The RT5147 provides four high-efficiency synchronous buck converters and two LDO regulators for the power system of an SSD.

15.1 Buck Converter

The RT5147 features four high-efficiency synchronous switching buck converters that deliver programmable output voltages. These converters utilized Advance Constant-On-Time (ACOT®) voltage mode, ensuring low output voltage, quick transient response, and minimal quiescent current. Additionally, these buck converters are equipped with standard protections, including OVP, UVP, and OCP.

15.2 Buck Overcurrent Protection (OCP)

The current limited architecture of all rails is designed to detect valley current. When the low-side MOSFET turns on, the inductor current will be sensed from $R_{DS(ON)}$ of the low-side by the internal ZC/OC circuit. If the voltage on the low-side $R_{DS(ON)}$ exceeds the V_{OC} (overcurrent voltage) which is defined by the register OC_CFG_*, the OC circuit will keep the low-side MOSFET turning on to reduce the inductor current. The low-side will remain on until the inductor current falls below the OC threshold. Once the inductor current is below the OC level, the rail will resume normal operation. See Overcurrent Protection (OCP) for more information.

15.3 Buck Undervoltage Protection (UVP)

The UVP is a level detection feature. If the output voltage falls below either −7% or −15% of the reference voltage (as selected via register settings), undervoltage protection will be triggered and both the high-side and low-side MOSFETs will be turned off immediately. The UVP circuit is disabled during the soft-start period and DVID transitions to prevent false triggering. See Undervoltage Protection (UVP) for more information.

15.4 Buck Overvoltage Protection (OVP)

The OVP is a level detection feature. If the output voltage exceeds +10% of the reference voltage, the overvoltage protection will be triggered and both the high-side and low-side MOSFETs will be turned off immediately. The OVP circuit will be disabled during the soft-start period and DVID transitions. See Overvoltage Protection (OVP) for more information.

15.5 Linear Dropout Regulator (LDO)

The RT5147 features two linear dropout regulators, each with independent current limit, overvoltage, and undervoltage protection circuits to prevent unexpected conditions in applications from damaging the device. When the path current exceeds the current-limit threshold, the current limit circuit adjusts the gate voltage of power stage to limit the output current. If the output voltage drops below −16% of the reference voltage, the LDO will be immediately deactivated by the UVP circuit. Conversely, if the output voltage exceeds +8% of the reference voltage, the OVP circuit will also promptly shut off the LDO.

15.6 Over-Temperature Protection (OTP)

If the device temperature exceeds 150°C, the OTP circuit will shut down all power rails. The PMIC will reboot with the power-up sequence once the device temperature decreases to 125°C. See Over-Temperature Protection (OTP) for more information.

15.7 GPIO1

The GPIO1 is fixed to the nRESET signal. After the power-up sequence, a high nRESET (nRESET = H) indicates that the PMIC is in a Power-Good (PG) state, whereas a low nRESET (nRESET = L) indicates a Power Bad (PBAD) condition.

The n_RESET_MASK_REG register offers a masking feature for various output events, including PBAD, VIN

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overvoltage (VIN_OV), and over-temperature (OT) events. By setting the corresponding bits to ‘1b’ within this register, the nRESET output will not respond to PBAD events for that specific rail. Conversely, any PBAD events on an un-masked rail will cause the nRESET to go low. Additionally, the Power Good delay time from the rising edge of the Buck3 PG flag to the rising edge of the nRESET can be configured in the GPIO1_REG.POR_DELAY_TIME setting.

15.8 GPIO2

GPIO2 is pre-configured to serve as the voltage selection (VSEL) input for buck converters B1 and B2 prior to nRESET being asserted high (nRESET = H). As soon as the AVIN voltage exceeds the Undervoltage-Lockout (UVLO) threshold plus hysteresis (UVLO+HYS), the default VSEL values for B1 and B2 are immediately captured and stored into their respective register values, such as in the B1 Voltage Regulation (VR) structure, B1_SEL, and B2_SEL. For detailed VSEL configurations, refer to Table 1.

Table 1. GPIO2 Function

B1/B2 VSEL			
GPIO2 Status	**High**	**High-Z**	**Low**
B1 Status	B1 = LSW	B1 = Buck/ 2.5V	B1 = Buck/ 2.5V
B2 Status	B2 = 0.91V	B2 = 0.91V	B2 = 1.2V

Following the power-up sequence, when nRESET transitions to a high level (nRESET = H), the function of GPIO2 can be reconfigured to an alternative function by setting the GPIO2_REG.GPIO2_FUNC_SEL register (refer to Table 5 for available functions). The functional architecture of GPIO3, GPIO4, and GPIO6 are the same as the GPIO2. Each of these GPIOs has an internal default function before nRESET = High, and they can be reassigned to different functions after nRESET = High.

To disable the reconfigured function of any of these GPIOs and revert to the internal default function, set the corresponding GPIOx_FUNC_EN bit to '0b' in the GPIOx_FUNC_SEL register. When disabled, GPIO2, GPIO3, GPIO4, and GPIO6 will maintain their default functions as set internally.

15.9 GPIO3

Prior to nRESET being asserted high (nRESET = H), GPIO3 is utilized to control the B3 output, enable Dynamic Voltage Scaling (DVS) for B2 and B3, and set the delay times for B3, B4, LDO1, and LDO2. These configurations are tailored to meet the requirements of different platforms. When the AVIN voltage exceeds the Undervoltage-Lockout (UVLO) threshold plus hysteresis (UVLO+HYS), the RT5147 promptly reads the status of GPIO3 to establish the output levels and sequencing for certain rails.

Moreover, if the PMIC enters Sleep Mode (either Sleep1 or Sleep2) with B2_DVS_EN/B3_DVS_EN set to '1', the output voltage of B2 and B3 will switch to their respective DVS modes. For detailed configurations of B3's voltage scaling, refer to Table 2.

Table 2. GPIO3 Function

B3 VSEL			
GPIO3 Status	**High**	**High-Z**	**Low**
B3 Status	B3_SEL = 0.78V B2/B3_DVS = 0.68V	B3_SEL = 0.78V B2/B3_DVS = 0.68V	B3_SEL = 0.78V B2/B3_DVS = 0.68V
GPIO3 Delay Time for B3/ B4/ L1/ L2	B3 = + 0.75ms B4 = + 3.0ms L1 = + 2.0ms L2 = + 2.0ms	B3 = + 0.75ms B4 = + 3.75ms L1 = + 2.0ms L2 = + 2.0ms	B3 = + 0ms B4 = +1.5ms L1 = + 2.0ms L2 = + 2.0ms

Note 9. The total power-up delay time of the rails will be “Time Slot” + “ON DLY” + GPIO3 Delay Time.

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15.10 GPIO4

Before nRESET is asserted high (nRESET = H), GPIO4 serves the default function of selecting the voltage (VSEL) for B4 and L1 (Linear Regulator 1). When the AVIN voltage exceeds the undervoltage-lockout (UVLO) threshold plus hysteresis (UVLO+HYS), the default VSEL settings for B4 and L1 are captured and stored into their respective register values, such as in the B4/L1 Voltage Regulation (VR) structure, B4/L1_SEL. For detailed VSEL configurations, refer to Table 3.

It is important to note that among the GPIOs, only GPIO2, GPIO3, and GPIO4 are capable of being configured in the High-Z state.

Table 3. GPIO4 Function

B4/L1 VSEL			
GPIO4 Status	**High**	**High-Z**	**Low**
B4 Status	B4 = Buck/ 1.1V	B4 = Buck/ 1.2V	B4 = Buck/ 1.2V
L1 Status	L1 = LDO/ 1.8V	L1 = LDO/ 1.8V	L1 = LDO/ 2.5V

15.11 GPIO6

Prior to nRESET being asserted high (nRESET = H), GPIO6 is pre-configured to select the regulator mode for LDO2. Unlike GPIO2, GPIO3, and GPIO4, which check their voltage levels to determine the rails' mode and voltage once AVIN exceeds the undervoltage lockout (UVLO) threshold plus hysteresis (UVLO+HYS), GPIO6 uniquely checks its voltage level to define LDO2's regulator mode and set its output voltage before LDO2 begins ramping up. For detailed information on LDO2 MODE configurations, refer to Table 4.

Table 4. GPIO6 Function

LDO2 MODE			
GPIO6 Status	**High**	**High-Z**	**Low**
L2 Status	L2 = LDO/ 1.8V	--	L2 = PLSW

15.12 GPIO5/7/8

The default functions of GPIO5, GPIO7, and GPIO8 are determined by the initial values set in the GPIO5_FUNC_SEL, GPIO7_FUNC_SEL, and GPIO8_FUNC_SEL registers, respectively. Based on these settings, GPIO5, GPIO7, and GPIO8 are configured as either input or output signals corresponding to the functions selected, as detailed in Table 5.

After the nRESET signal is asserted high (nRESET = H), the functions of GPIO2, GPIO3, GPIO4, and GPIO6 can be reconfigured. The available functions to which these GPIOs can be adjusted are listed in Table 5.

Table 5. GPIO Function Selection

GPIOx_FUNC_SEL	I/O	FUNC_NAME	Function Description
0x00	O	EXT_EN1_O	EXT_EN1_O (external enable1 signal).
0x01	O	EXT_EN2_O	EXT_EN2_O (external enable2 signal).
0x02	O	nIRQ	Export an internal output signal, nIRQ. nIRQ will response to the un-mask error flags of input or outputs.

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GPIOx_FUNC_SEL	I/O	FUNC_NAME	Function Description
0x03	I	Sleep Mode 1	As the input controlled signal for Sleep1. High = Wake up from Sleep Mode 1 Low = Enter Sleep Mode 1
0x04	I	Sleep Mode 2	As the input controlled signal for Sleep2. High = Wake up from Sleep Mode 2 Low = Enter Sleep Mode 2
0x05	I	B1/B2 EN/DIS	As the enable/disable signal for controlling B1/B2. The priority of this function is lower than Sleep1 and Sleep2. High = Enable B1/B2 Low = Disable B1/B2
0x06	I	PWRDIS	As the Power Disable signal for controlling RT5147 without reload initial efuse codes. High = Shut off all rails of the RT5147 Low = Power up all rails of the RT5147
0x07	I	EXT_EN1_I function. No use for GPIO2/3/4	Input Triggered Signal for EXT_EN1_O. High = EXT_EN1/2_O will go high with the configured delay time. Low = No action.
0x08	I	EXT_EN2_I function. No use for GPIO2/3/4	
0x09	O	SYSMON Output	Only GPIO5 can set the SYSMON output signal. High = VIN > SYSMON Low = VIN < SYSMON

Table 6. GPIO1 - 8 Default Function

GPIOx	GPIO3=H	GPIO3=Hi-Z	GPIO3=L	I/O	Function Description
	GPIOx_FUNC_SEL				
GPIO1	X			O	nRST(nRESET)
GPIO2	0x00			O	EXT_EN1_O
GPIO3	0x00			O	EXT_EN1_O
GPIO4	0x00			O	EXT_EN1_O
GPIO5	0x03	0x02	0x02	I/O	Sleep1 Mode input signal when GPIO3 = High. nIRQ output signal when GPIO3 = Hi-Z or Low.
GPIO6	0x00			O	EXT_EN1_O
GPIO7	0x06			I	PWRDIS
GPIO8	0x04			I	Sleep2 Mode input signal

Note 10. The GPIO5 function can be defined by GPIO3's status.

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16 Application Information

(Note 11)

The RT5147 provides four synchronous buck regulators and two LDOs to satisfy requirements of the entire power system of the client SSD. This device can communicate with processors through the I^{2}C interface for programming the output voltages of the rails, monitoring the status of the rails, or entering sleep mode for power saving. Table 7 lists the information of the power rails provided by the RT5147.

Table 7. Details of Power Rails

Resource Name	Type	Voltage Range	Current Rating
BUCK1	Buck Converter/LSW	1.7V to 2.9V with 20mV/step	4000mA
BUCK2	Buck Converter	0.5V to 1.3V with 10mV/step	2000mA
BUCK3	Buck Converter	0.5V to 1.3V with 10mV/step	4000mA
BUCK4	Buck Converter/LDO	0.9V to 2.0V with 10mV/step	2000mA
LDO1	LDO/PLSW or NLSW	1.0V to 2.7V with 50mV/step	400mA
LDO2	LDO/LSW	1.0V to 2.7V with 50mV/step	400mA

16.1 Bucker Converter

The RT5147 incorporates four high-efficiency, ACOT® based synchronous buck converters that deliver various voltages via the I^{2}C interface. The buck converter features fast transient response with the ACOT® typology.

Each switching regulator is specially designed for very low quiescent current ($< 35\mu A$) and high-efficiency operation across the current rating range. With high switching frequency operation, the external LC filter can be small and keep very low output voltage ripple.

Additional features of these buck converters include soft-start, optional discharge paths, undervoltage protection, overvoltage protection, overcurrent protection and over-temperature protection. The RT5147 will shut off all rails when any output rail triggers under-voltage protection or over-voltage protection. The PMIC will then attempt to restart every 100ms until all the rails power up successfully. The RT5147 provides over-temperature protection when the die temperature exceeds 150°C. The over-temperature protection will also cause all rails to enter discharge mode and remain off. The RT5147 will re-power these rails when the die temperature drops below 125°C.

With the I^{2}C interface, each buck converter can program output voltage, adjust the slew rate of the DVID, change the PWM frequency, and control the on/off state. The PWM controller can switch to forced PWM mode, PSKIP mode, or LPM mode (for even lower quiescent current $< 25\mu A$).

16.2 Inductor Selection

For a given input voltage (V_{IN}), output voltage (V_{OUT}), and operation frequency (f_{SW}), the inductor value (L) determines the inductor ripple current (ΔI_L), as shown in the following equation:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times L \times V_{IN}}$$

Having a lower ripple inductor current not only reduces the power losses on the ESR of the output capacitors but also reduces the output voltage ripple. A reasonable starting point for selecting the ripple current is ΔI_L = 0.3 x I_{MAX} to 0.4 x I_{MAX}. The largest ripple current occurs at the highest VIN. To ensure that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{f_{SW} \times \Delta I_L \times V_{IN(MAX)}}$$

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The current rating of the inductor must be large enough and will not saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

16.3 C_{IN} and C_{SYS} Selection

The input capacitance of every rail, C_{IN}, needs to filter the trapezoidal current at the source of the high-side MOSFET. For preventing a large ripple voltage, a low ESR input capacitor for the maximum current should be used. The relation between C_{IN} ripple voltage and current ripple is shown in Figure 1.

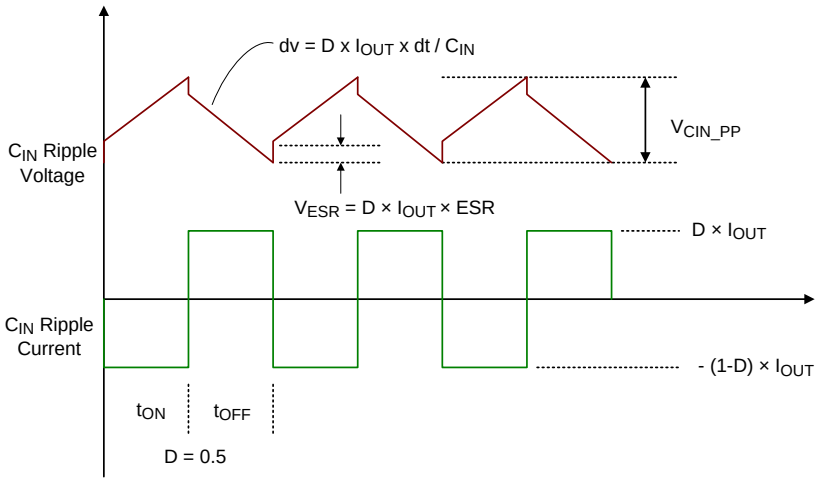

Figure 1. Relationship of C_{IN} Voltage Ripple and Current Ripple (Assuming D = 0.5)

The C_{IN} voltage ripple can be determined by the equations below when a rail works at the f_{SW} of CCM mode.

$$V_{CIN_PP} = D \times I_{OUT(MAX)} \times (ESR + \frac{(1-D)}{C_{IN} \times f_{SW}})$$

where D = V_{OUT}/V_{IN}. If MLCC is used as the input capacitors, the ESR is almost zero, and the minimum input capacitance requirement can be estimated as follows:

$$C_{IN(MIN)} = I_{OUT(MAX)} \times \frac{D \times (1-D)}{V_{CIN_PP(MAX)} \times f_{SW}}$$

Next, it is also necessary to consider the input bulk capacitance, C_{SYS}, to ensure a stable input voltage during large load transients on all rails. Basically, the input host power source cannot provide enough instant input current to respond to a fast and large load current transient of the converters. The insufficient energy during load transient will be provided by the input bulk capacitors until the host power supply meets the input current requirement. Refer to Figure 2 for a better understanding of the above description.

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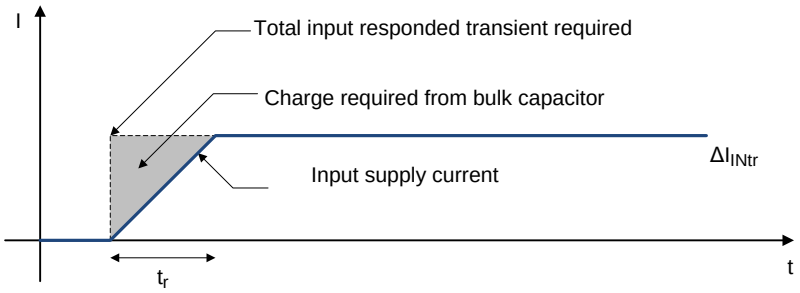

Figure 2. Charge Required from Input Bulk Capacitors during Load Transient

Figure 3 shows the diagram of every power rail of the RT5147 sharing a single bank of input bulk capacitors. The total input transient current required due to load currents of the converters can be calculated using the following equation:

$$\Delta I_{INtr} = \sum_{n=1}^{4} \frac{V_{OUTn} \times \Delta I_{OUTn(MAX)}}{V_{IN} \times \eta_n}$$

where ΔI_{INtr} is the required total input transient current, ΔI_{OUT} is the maximum output transient current, and η is the efficiency of the buck at $I_{OUT(MAX)}$.

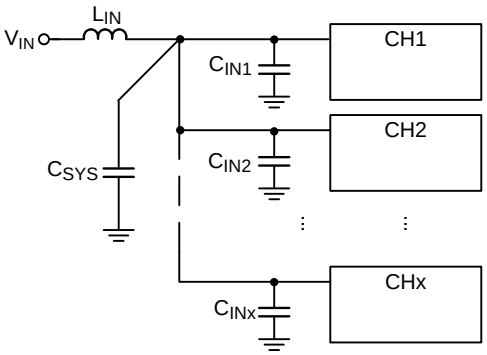

Figure 3. The Location of Input Bulk Capacitors Diagram

When ΔI_{Intr} is confirmed, the input bulk capacitance, C_{SYS}, can be determined using the following equation:

$$C_{SYS(MIN)} \cong \frac{1.21 \times \Delta I_{INtr}^2 \times L_{IN}}{\Delta V_{INPP(MAX)}^2}$$

where $\Delta V_{INPP(MAX)}$ is the maximum allowable dropout voltage and L_{IN} is the input series filter inductance. If L_{IN} is not used, a reasonable parasitic value of 50nH can be assumed for the PCB layout.

16.4 COUT Selection

The output capacitors and the inductor form a low-pass filter in the buck topology. In steady-state conditions, the inductor ripple current flowing into/out of the output capacitors will result in output ripple voltage. The peak-to-peak output ripple voltage (ΔV_{OUTPP}) can be calculated using the following equation:

$$\Delta V_{OUTPP} = \Delta I_L \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right)$$

The output capacitors can be equivalent to a series of ESR, capacitance, and ESL circuit. When a load transient occurs, the output capacitors supply the instant load current before the inductor current catches up with the output current and the controller's response. Therefore, the output voltage undershoot/overshoot can be combined by the ESR voltage, ESL-induced voltage, and the delta voltage caused by the delta electric quantity coming from or charging to the capacitors. The ESR voltage (ΔV_{ESR}) can be calculated using the following equation:

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$$\Delta V_{ESR} = ESR \times \Delta I_{LOAD}$$

Another parameter that can affect the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in $\Delta I_{LOAD}/\Delta t_T$ during transient, where $\Delta I_{LOAD}/\Delta t_T$ is the transient slew rate. The ESL-induced voltage (ΔV_{ESL}) can be calculated using the following equation:

$$\Delta V_{ESR} = ESL \times \frac{\Delta I_{LOAD}}{\Delta t_T}$$

Using a capacitor with low ESL can achieve better transient performance. Generally, using several capacitors connected in parallel can provide better transient performance than using a single capacitor for the same total ESR. Unlike electrolytic capacitors, ceramic capacitors have relatively low ESR and can reduce the voltage deviation during load transients. All the buck converters of the RT5147 can operate stably with MLCC output capacitors.

16.5 Overcurrent Protection (OCP)

The buck converters provide overcurrent protection. The current limit architecture of the buck converter uses the low-side MOSFET turn-on resistance to detect the inductor current. If the low-side sensed voltage exceeds the configuring V_{OC} voltage, the low-side will continue turning on to pull the inductor current down. Once the inductor current across the low-side is lower than V_{OC}, the control loop will switch from the OC loop back to the normal loop. The RT5147 applies 4 overcurrent levels for each buck converter. See Registers Configuration for the OCP values setting on each rail.

For the LDOs, the RT5147 provides overcurrent protection by continuously monitoring the load current. If the sensed current exceeds the current-limit threshold, the OCP will be triggered. Once the OCP is tripped, LDO1 or LDO2 will lock the output current at the overcurrent threshold level until the overcurrent condition is removed or the output voltage triggers the undervoltage protection.

16.6 Undervoltage Protection (UVP)

All the rails of the RT5147 are continuously monitored for undervoltage protection.

The UVP thresholds are as follows:

1. BUCK1 to BUCK4: The output voltage falls below 93% or 85% (configurable via register) of the reference.

2. LDO1 and LDO2: The output voltage falls below 84% of the reference.

If the output voltage falls below the UVP threshold, the RT5147 will shut off all rails immediately, and the nRESET signal will also go low to inform the system.

16.7 Overvoltage Protection (OVP)

All the rails of the RT5147 are continuously monitored for overvoltage protection.

The OVP thresholds are as follows:

1. BUCK1 to BUCK4: The output voltage rises above 110% of the reference.

2. LDO1 and LDO2: The output voltage rises above 114% of the reference.

If the output voltage rises above the OVP threshold, the RT5147 will shut off all rails immediately, and the nRESET signal will also go low to inform the system.

16.8 AVIN Overvoltage Protection (AVIN OVP)

If the AVIN exceeds 3.8V, the AVIN OVP circuit will activate and shut down all power rails , and the nRESET signal will also go low. All the power rails will recover with the power-up sequence when the AVIN drops below 3.5V (3.8V – HYS).

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16.9 AVIN Undervoltage-Lockout (AVIN UVLO)

If the AVIN voltage rises from 0V to above the UVLO falling threshold voltage +100mV but remains below the SYSMON threshold voltage, the PMIC operates in standby mode and all register values are re-loaded from the efuses. The rails remain off in this standby mode. Once AVIN exceeds the SYSMON voltage, the RT5147 will follow the power-up sequence to turn on all rails. After all rails power up successfully, the RT5147 will raise the nRESET signal. If the AVIN voltage falls from above the SYSMON voltage to the UVLO falling threshold voltage, all power rails will stop operation immediately and the digital controller will also shut off. The PMIC stays in off mode at this time.

The PMIC resets all register codes and enters standby mode when the AVIN voltage is higher than the UVLO falling threshold voltage +100mV again. There is a hysteresis voltage of about 100mV between the UVLO rising and falling threshold voltages.

16.10 Over-Temperature Protection (OTP)

If the temperature of the IC exceeds 150°C, the OTP circuit will activate and shut down all power rails, and the nRESET signal will also go low. All the rails recover with the power-up sequence when the die temperature of the PMIC drops to 125°C while keeping VIN > SYSMON.

16.11 Protection Functions

The RT5147 applies several types of protection functions to avoid unexpected events in applications. The details of the protection functions are shown in Table 8. This table shows all events that cause the nRESET = 0, but OCP is not included.

Table 8. Details of the Protection Functions

Fault Event	Shutdown Rail	Fault Response	nRESET Behavior	Register Value
OCL (Buck and LDO)	None	N/A	Keep high	Keep
UVP (Buck and LDO)	Buck B1/2/3/4, LDO1/2	Hiccup every 200ms	Go low	Keep
OVP (Buck and LDO)	Buck B1/2/3/4, LDO1/2	Hiccup every 200ms	Go low	Keep
AVIN OVP	Buck B1/2/3/4, LDO1/2	Non-Latch	Go low	Keep
AVIN UVLO	Buck B1/2/3/4, LDO1/2	No Power	Go low	Reset
OTP	Buck B1/2/3/4, LDO1/2	Non-Latch	Go low	Keep

16.12 Rails Configuration

Any of the rails, Buck1 to Buck4, LDO1 and LDO2, can be changed to another type of regulator via the GPIO2/4/6 setting. Buck1, LDO1 and LDO2 can be configured as the PLSW (PMOS type load switch). When the rails become PLSWs, they retain overvoltage protection and overcurrent protection but no undervoltage protection. Use caution when using the rails as load switches. LDO1 can also become NLSW (NMOS type load switch) for lower input voltages (> VIN – 0.7V) and higher output current applications. Because the maximum voltage of the RT5147, AVIN (range: 2.5V – 3.8V), will be used as the NMOS gate driver voltage, a higher input voltage as the NLSW input source may cause the gate drive to not fully turn on the NMOS.

Buck4 can be configured as an LDO. The LDO has all protections, including overvoltage, undervoltage and overcurrent protections. If the delta voltage between input voltage and output voltage is small, using the Buck4 as the LDO will achieve better efficiency than using it as a Buck4 converter.

Note that if the original rail becomes another type of regulator, their on/off sequence and current rating settings will be different. See Electrical Characteristics for more detailed specifications.

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16.13 I²C Interface

A general-purpose serial interface is provided in the RT5147 to control and monitor the configuration registers, and its I²C slave address is 0x25. This serial interface supports the I²C protocol 2.1 with standard slave mode (100Kbps), fast mode (400Kbps), and high-speed mode (3.4Mbps). Multiple bytes reading or writing over the I²C interface of the RT5147 can also be done in standard slave mode (100Kbps) and fast mode (400Kbps). When performing a multiple byte read or write, the RT5147 will automatically increase to the next address for subsequence bytes (see Figure 4).

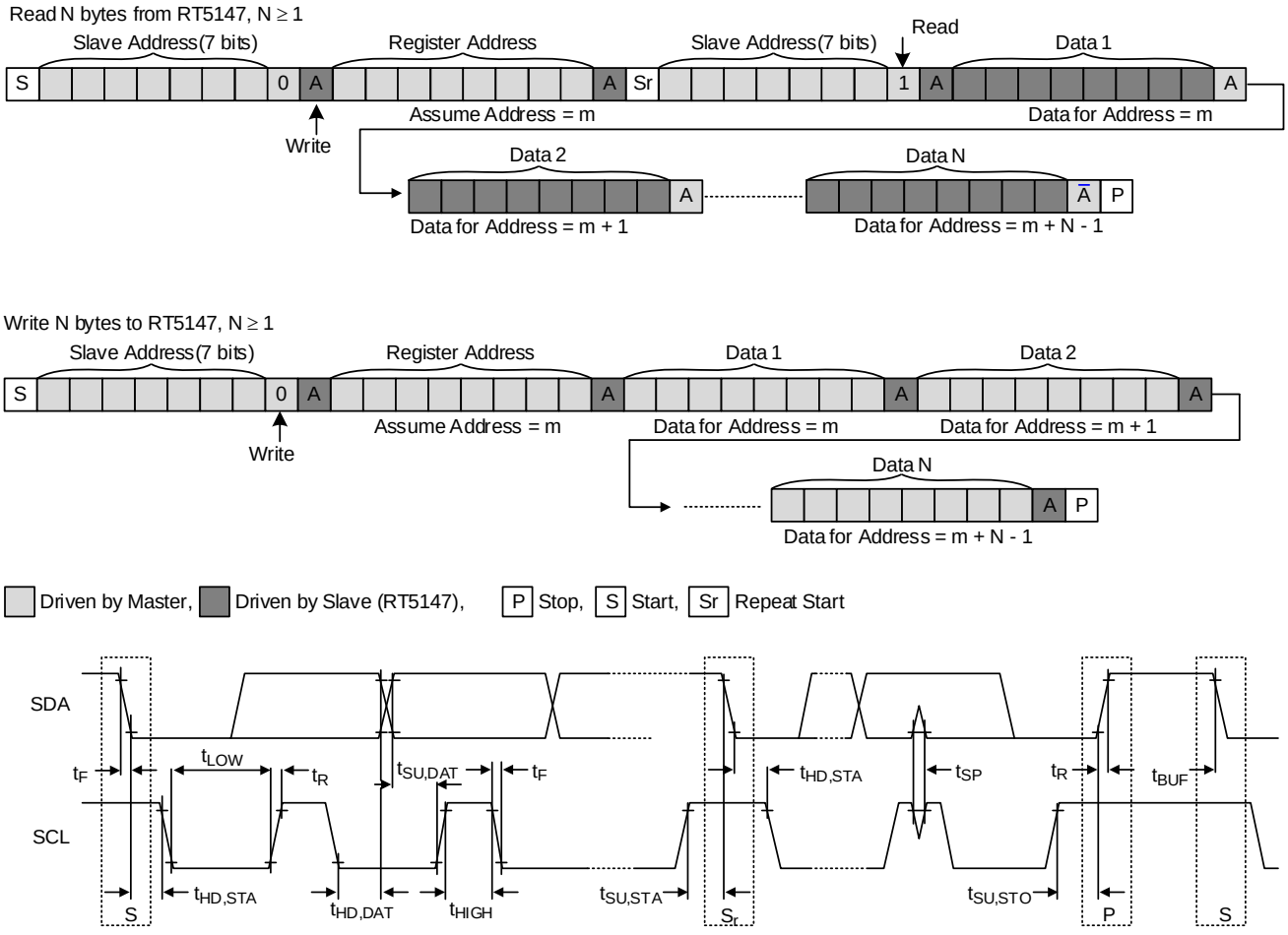

Figure 4. I²C Read/Write Stream and Timing Diagram

Users can modify the output voltage, fault threshold, interrupt masks, and other parameters, via the I²C interface. There are two types of the registers as described below:

Volatile Registers: These include R/W (Read and Write), RO (Read only), R1C (Read 1b to clear bit) and W1C (Write 1b to clear this bit). After AVIN > (UVLO + 100mV) = 2.6V, users can modify the R/W register values to change the register functions. The RO registers are used to provide the rails' status and the RT5147 information, such as various ID numbers. W1C type means that writing a 1b into the bit will clear itself and become 0b. Any changes to these volatile registers are lost when AVIN is below 2.5V. The default values are fixed and cannot be modified.

Non-Volatile Registers: These include R/W and RO. After AVIN > (UVLO + 100mV) = 2.6V, users can modify the R/W register values to change the register functions. The RO registers are used to provide the rails' status and the RT5147 information, such as various ID numbers. Any changes to these non-volatile registers are retained

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even when AVIN is below 2.5V. The default values can be modified at the factory to optimize IC functionality for specific applications. Contact Richtek for custom configurations to meet system requirements.

16.14 State Machine

The RT5147 contains an internal state machine with six states. The definitions of these states described below are related to various signals such as, AVIN, POWER_DIS, Sleep1, Sleep2, and some related register settings. The followings are the classifications about the states.

16.14.1 Off State

If AVIN < “UVLO + HYS” voltage, all the internal circuits of the RT5147 do not work at this state.

16.14.2 Standby State

If AVIN is between “UVLO + HYS” voltage and SYSMON voltage or AVIN is over AVIN_OV voltage, the internal digital controller of the RT5147 starts to work. Once the digital core is active, it will reload register values from the efuses configuration. After completing the reload step, any register function value can still be modified via the I^2C interface.

The only way to reload the register values of the RT5147 from the efuses is by changing the state machine changing from Off State to Standby State. Note that the RT5147 only downloads the specific efuse configurations, which depended on the level status of GPIO2/3/4, into the corresponding register addresses when the state machine is from Off State to Standby State .

16.14.3 Normal State

If AVIN is in the range between SYSMON voltage and VIN OVP voltage and POWER_DIS = L, the rails will follow their GPIO settings and their internal configurations of the time slot functions (X_TIME_SLOT), turn-on delay functions (X_ON_DLY) and the soft-start time functions (X_SST_SEL) to perform the power-up sequence. Once all rails power up successfully, the GPIO1 signal, as the nRESET signal, raises to a high level. When the RT5147 gets nRESET = 1, it will be considered in the Normal State.

In Normal State, a rail can be controlled to turn ON/OFF by configuring the X_EN register function. If the rail powers up by setting X_EN from b0 to b1, it will follow the X_SST_SEL function setting to perform a soft-start immediately, ignoring any configured delay time. Note that if the rails’ X_TIME_SLOT = b00 (disabled setting), the rail will always remain off ignoring any configuring signal.

16.14.4 Sleep1/Sleep2 State

The RT5147 will go to “Sleep State” when one of the following conditions is satisfied:

- A GPIOx set to the SLEEP1 function goes from high voltage to low voltage. The state machine of the RT5147 will go to Sleep State.
- A GPIOx set to the SLEEP2 function goes from high voltage to low voltage. The state machine of the RT5147 will go to Sleep State. Note that the priority of the rail’s off state in the Sleep1 function and Sleep2 function is higher. If one of the rail’s off state in the Sleep1 function or in the Sleep2 function gets real, the rail will be off with the state machine changing to Sleep State.
- Besides the external hardware signal controlling the sleep mode, the RT5147 also applies software control via the I^2C interface to enable sleep mode. If the SLEEP1_EN or SLEEP2_EN function is set to b1, the PMIC will also go to sleep mode.

When the RT5147 changes from normal mode to sleep mode, the rails will follow the SLEEP1/2_REG setting to either remain active or power off.

When Buck2 and Buck3 remain active in sleep mode, both the output voltage of Buck2 and Buck3 have two choices:

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- Buck2/Buck3 will keep their output voltage as B2_VSEL/B3_VSEL configurations when B2/B3_DVS_EN_SLEEPx = 0.
- Buck2/Buck3 will change their output voltage to B2_DVS_SEL/B3_DVS_SEL configurations when B2/B3_DVS_EN_SLEEPx = 1.

For example, if Sleep1 is used to enter sleep mode and B2/B3_DVS_EN_SLEEP1 = 0, B2/B3 will keep their B2/B3_VSEL voltage; if B2/B3_DVS_EN_SLEEP1 = 1, B2/B3 will follow the B2/B3_DVS_SEL to change their output voltages. The above behaviors also apply to the B2/B3_DVS_EN_SLEEP2 bits.

Because the RT5147 only applies one sleep mode, the priority of B2/B3_DVS_EN_SLEEP2 is higher than B2/B3_DVS_EN_SLEEP1 if both Sleep1 and Sleep2 are enabled.

All the alive rails in sleep mode will enter low power mode. When a rail enters low power mode, it will disable some internal circuits to reduce the VIN supply current for power saving.

The RT5147 can easily return to normal state from sleep state by disabling the sleep mode condition. Form sleep state back to normal state, the disabled rails will follow their X_ON_DLY function, X_WAKEUP_DELAY function, and X_SST_SEL function to perform their wake-up sequence.

16.14.5 Thermal Recovery State

When the die temperature of the RT5147 hits a critical over-temperature event (~150°C), all the rails are forced to power off, but the digital controller remains active. The PMIC stays in the Thermal Recovery State. The PMIC will return to normal state when the die temperature is lower than 125°C.

16.14.6 Recovery State

If any rail gets the fault flag of an overvoltage event or undervoltage event, the fault rail will open its high side and low side, and the other rails will discharge power at the same time. After powering off all rails, the RT5147 will try to hiccup every 100ms with the current register settings. Users can read back the fault information via the I^2C interface to understand which rail gets the fault flag.

The RT5147 will continue to retry until all rails are no longer in fault events, and the PMIC will return to normal state. When the RT5147 is in normal mode and the AVIN is below the UVLO falling threshold, the RT5147 will go to OFF State.

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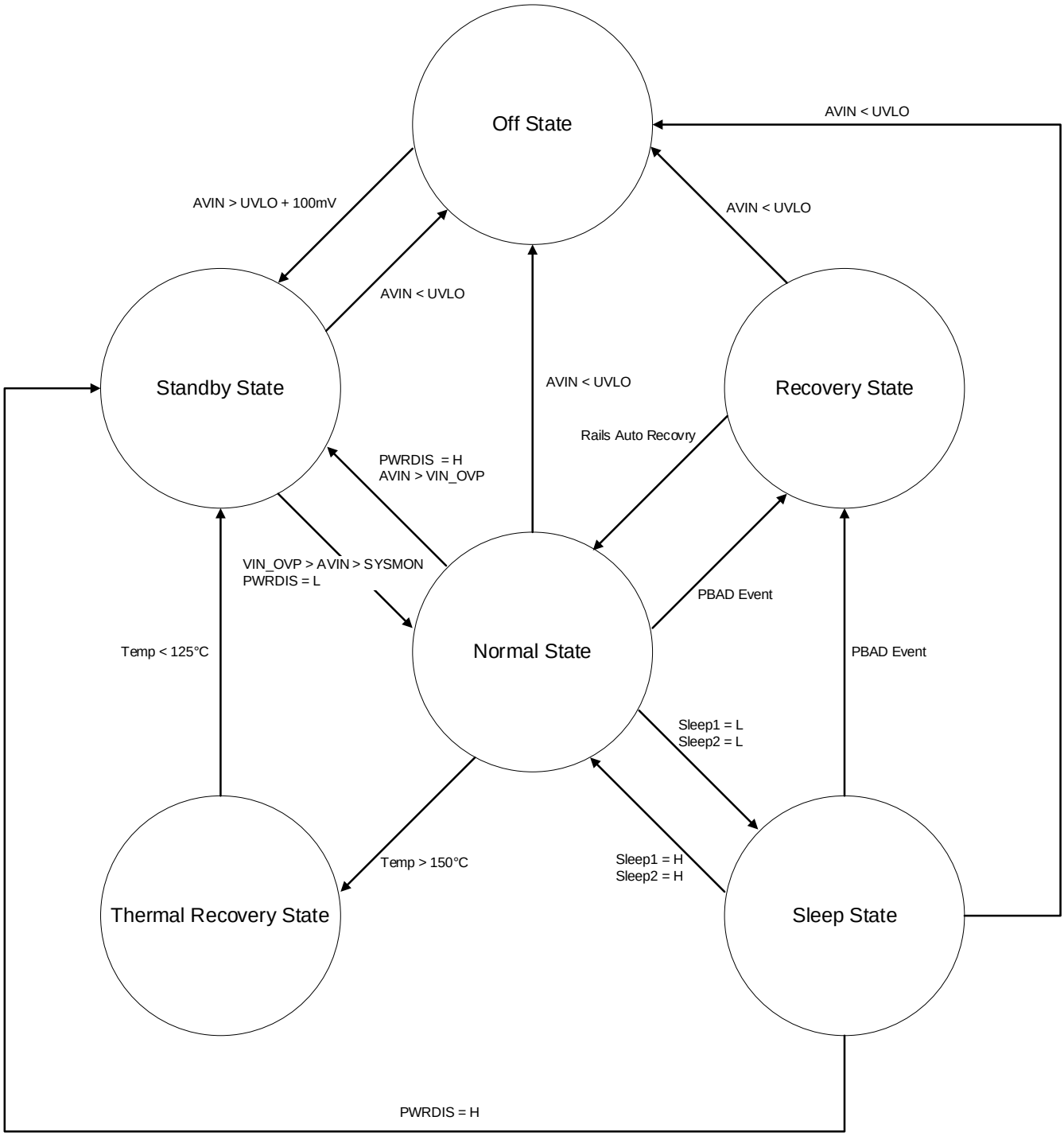

Figure 5. RT5147 State Machine

16.15 Sequence Diagram

The RT5147 starts a power-up sequence when AVIN exceeds the SYSMON threshold voltage, and the device shuts down when VIN falls below the UVLO falling threshold voltage. The RT5147 applies sleep mode to power off some rails, lower both Buck2 and Buck3 output voltage, and turn the alive rail to low power mode for saving power consumption. All the rails will return to normal operation when the RT5147 transitions from sleep state to normal state. The power on/off sequence and sleep-off/wake-up sequence of all rails in the RT5147 are shown in Figure 6, Figure 7, and Figure 8.

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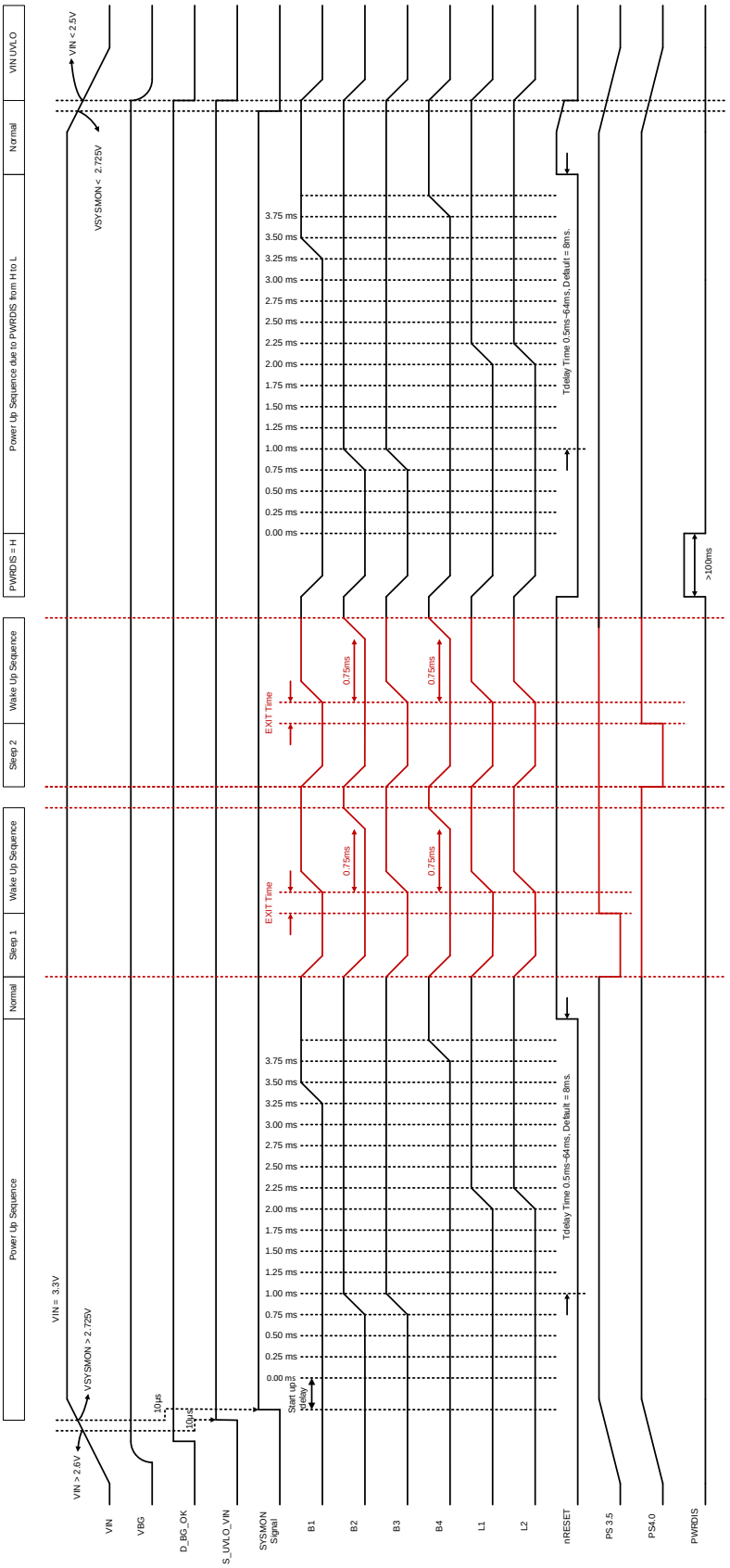

Figure 6. Power-Up/Off Sequence and Sleep Off/Wake-Up Sequence for GPIO3 = Hi-Z.

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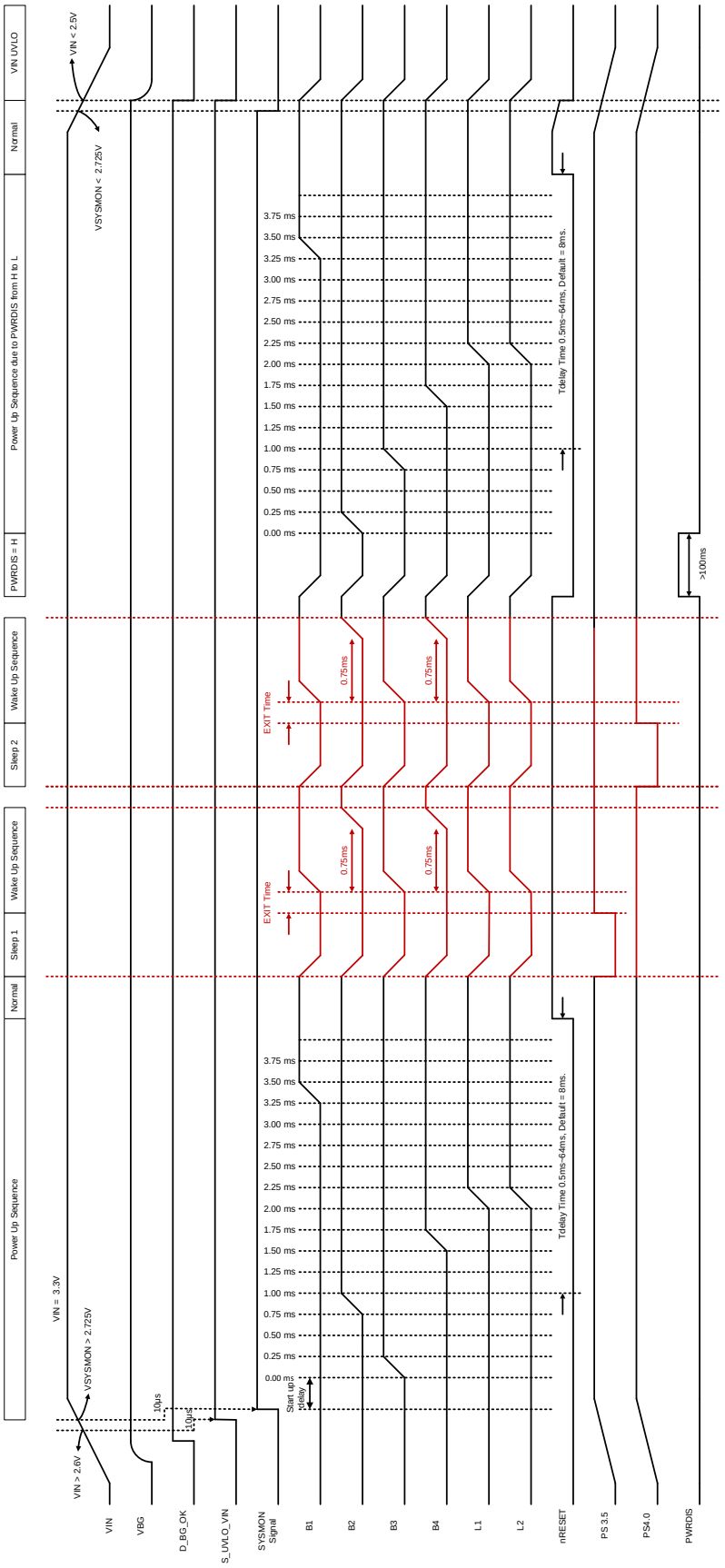

Figure 7. Power-Up/Off Sequence and Sleep Off/Wake-Up Sequence for GPIO3 = L.

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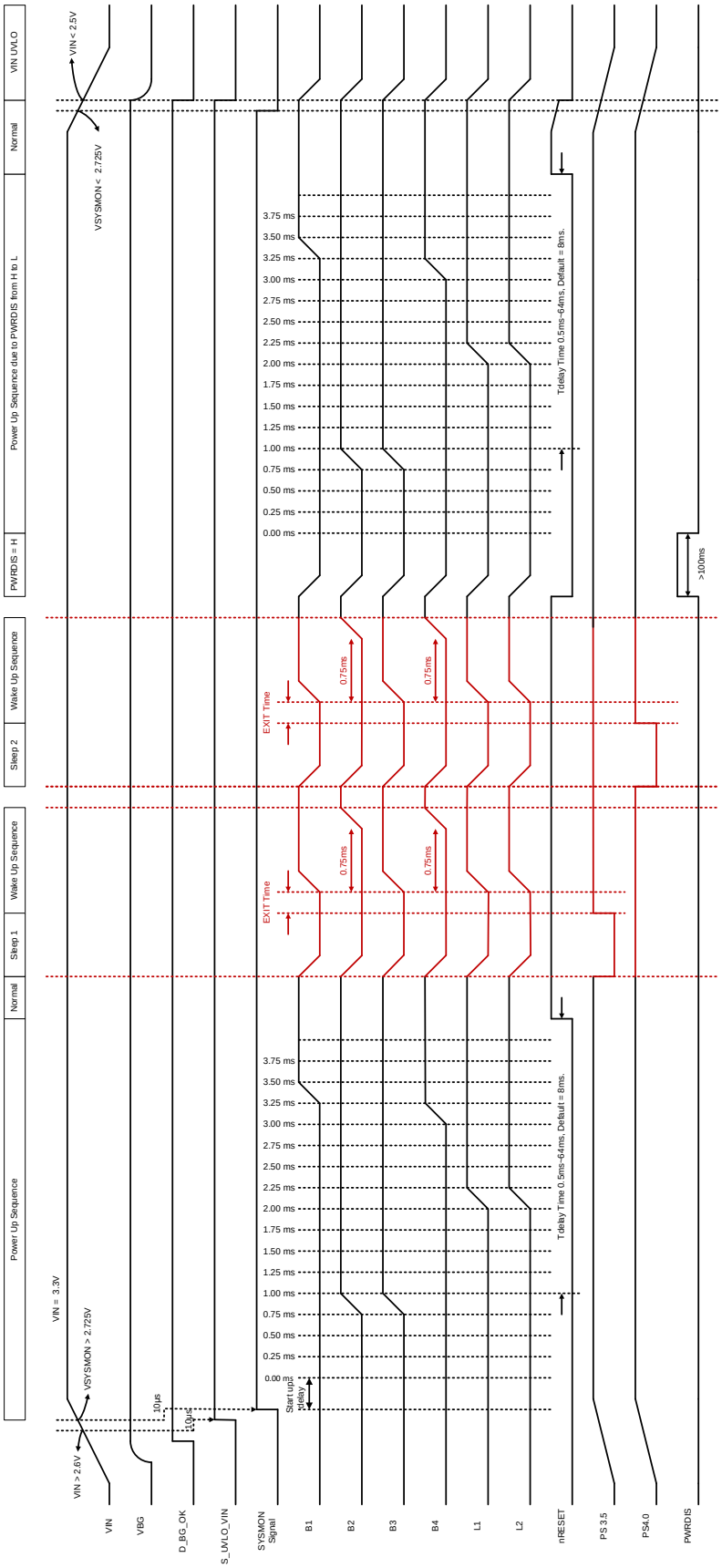

Figure 8. Power-Up/Off Sequence and Sleep Off/Wake-Up Sequence for GPIO3 = H.

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16.16 TIME_SLOT, ON_DLY, WAKE_UP_DLY, and OFF_DLY

The RT5147 embeds four timers to build the power-up sequence, sleep-off sequence, and wake-up sequence for every rail. These four timers are TIME_SLOT, WAKE_UP_DLY, ON_DLY, and OFF_DLY. All their functions are described below:

1. TIME_SLOT timer: This timer is used to design the enable delay time of the buck converter or the LDO with discrete regulated duration during the power-up sequence. The time slot applies the enable delay time from 0ms to 7.5ms with 0.25ms step resolution. The enable delay time = 0ms is counted from AVIN = SYSMON with the deglitched 10us delay and Start-Up Delay". The Start-Up Delay is around 380μs. Note that if set the Time_Slot register of a rail is set to 0x00, the rail will never power up with any sequence. The register of the Time_Slot for enable delay time = 0ms should be 0x01.
2. WAKE_UP_DLY timer: This timer is used to design the enable delay time of a regulator during the wake-up sequence. The options of the WAKE_UP_DLY function are planned as 0μs, 250μs, 500μs, 750μs, 1000μs, 2000μs, 4000μs and 8000μs. The wake-up delay time = 0μs is counted from the rising edge of the Sleep1/2 signal with the additional delay of "EXIT TIME", where the EXIT TIME is less than 1μs. Without wake-up delay time setting to all regulators, they will raise up at the same time during the wake-up sequence.
3. ON_DLY: The ON_DLY timer is used for the additional delay time to a rail's enable signal from 0 to 1 during the power-up sequence and the wake-up sequence. It means that the total delay time of a rail in the power-up sequence is "TIME_SLOT + ON_DLY"; the total delay time of a rail in the wake-up sequence is "WAKE_UP_DLY + ON_DLY".
4. OFF_DLY: The OFF_DLY timer is only used for the delay time to a rail's enable signal from 1 to 0 during sleep-off sequence. All rails without OFF_DLY setting will power off at the same time during the sleep-off sequence.

In addition, the GPIO3 can supply more additional hardware delay time to Buck3, Buck4, LDO1, and LDO2. Thes GPIO3 delay time settings are used to make Buck3, Buck4, LDO1, and LDO2 match at least three different power sequences of different SOCs in one version of the efuse codes. Refer to Table 2 for the hardware delay times of the different GPIO3 statuses.

All the rails in the power-off sequence, when AVIN < UVLO or PWR_DIS = L, always discharge off at the same time. The OFF_DLY will not apply the delay time to the regulator in the power-off sequence. See Table 9 for the functions of the four timers to all the sequences.

Table 9. The Delay Time Contributions of the Timer Register Functions to the Sequences

Sequence	TIME_SLOT	WAKE_UP_DLY	ON_DLY	OFF_DLY
Power up	Yes	--	Yes	--
Sleep off	--	--	--	Yes
Wake up	--	Yes	Yes	--
Power off	--	--	--	--

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16.17 B1/B2_EN

The priority of B1/B2_EN signals, compared with Sleep1 and Sleep2, is the lowest. If B1/B2_EN = H before AVIN > SYSMON, Buck1 and Buck2 will follow the time-slot function and on delay time function to power up. If B1/B2_EN remains L after AVIN > SYSMON, Buck1 and Buck2 will stay off during the power-up sequence. When setting B1/B2_EN to H during normal operation, Buck1 and Buck2 will follow the wake-up delay time and on delay time to power up.

16.18 VOUT_LOW

The RT5147 provides the VOUT_LOW function to prevent erroneous power-up sequence due to the higher residual voltage on the larger output capacitors. Without the VOUT_LOW function, the RT5147 may perform a power-down sequence followed by a power-up sequence in a very short time due to a low short-pulse from AVIN or a high short-pulse from the PMIC_DIS signal. This can result in all outputs still having higher residual voltages during the power-up sequence, as there is not enough time to discharge their output voltages. This behavior will make the system to stop working due to incorrect rail power-up sequences.

The VOUT_LOW function can be enabled by configuring the VOUTLOW_MASK_BIT in the TOP_CTRL_REG to b0. If the VOUT_LOW function is enabled, the RT5147 will not initiate the power-up sequence if any rail is higher than 200mV. This function ensures that the RT5147 provides the correct power-up sequence to the system.

16.19 EXT_ENx_O

The RT5147 provides two additional external enable signals to control external converters for supporting larger current rating or expanding more rails. Any of the GPIO2 to GPIO8 can be configured as the output signal, EXT_EN1_O or EXT_EN2_O. The GPIOx configured as EXT_ENx_O can join the power-up sequence or use manual operation to power up via the I^2C Interface or by receiving an input triggered signal from another GPIOx. The EXT_ENx_O_INPUT_SEL function provides four ways to trigger the EXT_ENx_O pin to issue an enable signal, and the EXT_ENx_O_TIME_SLOT and EXT_ENx_DELAY functions contribute to the delay time to meet the power-up sequence. See the following descriptions for more details about the configuration of EXT_ENx_O:

1. EXT_ENx_O_INPUT_SEL = Rail's POK and its delay time is affected by EXT_ENx_DELAY.

   The EXT_ENx_O will follow the selected rail's power good configured by the EXT_ENx_POK_SEL function to issue the enable signal after a delay time. Note that there is always an offset delay time of about 250μs when the Rail's POK is set as the input triggered signal to EXT_ENx_O.

2. EXT_ENx_O_INPUT_SEL = EXT_ENx_I and its delay time is affected by EXT_ENx_DELAY.

   The EXT_ENx_O will follow an external high-level signal received by the GPIO5/6/7/8, configured by the EXT_ENx_POK_SEL function and EXT_ENx_I_SEL function, to issue its enable signal after a delay time. Make sure that the configurations of EXT_ENx_O and EXT_ENx_I are assigned to different GPIOx.

3. EXT_ENx_O_INPUT_SEL = the command from the I^2C interface and there is no delay time.

   The EXT_ENx_O can be set to follow the command from the I^2C interface. The register address for the command is located in the GPIOx_GENERAL_CTRL function. Write 00b to pull down EXT_ENx_O as a low-level signal and 01b to pull up EXT_ENx_O as a high-level signal.

4. EXT_ENx_O_INPUT_SEL= EXT_ENx_O_Time_Slot and its delay time comes from the time slot setting.

   The EXT_ENx_O will follow the delay time configured by the EXT_ENx_O_Time_Slot function to issue the enable signal during the power-up sequence. Note that there is always an offset delay time of about 400μs when EXT_ENx_O is set to follow its time slot.

EXT_ENx_O will power up as described above. Once the input trigger signal is gone due to unexcepted behavior, the EXT_ENx_O will also follow the input trigger signal to go low. The EXT_ENx_O will go low when the PMIC hits the protection event.

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16.20 SYSMON, SYSWARN, and POK_OV

The SYSMON is the configurable threshold voltage for monitoring AVIN, and the threshold can be configured from 2725mV to 3100mV with a 25mV step resolution. When the AVIN is over the SYSMON Vth, the RT5147 can enable the rail's power-up sequence. Note that the SYSMON can be detected through GPIO5.

The SYSWARN is the warning signal to alert that the AVIN voltage is lower than the SYSWARN monitored voltage. The SYSWARN alarm voltage can be configured from 2775mV to 3150mV with a 25mV step resolution. Similarly, the POK_OV is also a warning signal to alert that the AVIN voltage is higher than the POK_OV monitored voltage. The POK_OV monitored voltage has two selections, 3.5V and 3.8V. The system can monitor AVIN as the input source power good by the two signals, SYSWARN and POK_OV.

The indication bits for SYSMON, SYSWARN, and POK_OV are listed in the TOP_STATUS_REG. These three bits are designed for real-time reaction. Their corresponding bits will show the real status when the AVIN voltage is over their set threshold voltage. This means that if the POK_OV bit in the TOP_STATUS_REG shows b1, the AVIN is over the POK_OV monitored voltage. It should keep the POK_OV bit = b0 to maintain the AVIN within the correct operational range. For SYSMON and SYSWARN indication signals, they will show b0 when the AVIN is lower than their configured monitored voltage. Keep the indication signals of SYSMON and SYSWARN at b1 for normal operation.

16.21 AVIN_OV and AVIN UVLO

Once the AVIN is over the SYSMON voltage, the PMIC starts to work. SYSWARN and POK_OV can be used to monitor the AVIN voltage. If the AVIN is under SYSWARN or over POK_OV, the fault status can be sent by the nIRQ signal to warn the system. When AVIN is lower than SYSWARN (even lower than SYSMON) or higher than POK_OV, the PMIC still works with the warning status. But if the AVIN continues to worsen to be under AVIN UVLO or over AVIN OV, the PMIC will be forced to shut down to protect itself and the backend circuits. Refer to the State Machine section for more details.

16.22 Status and Flag

The monitored AVIN Status, OT, nRESET and nIRQ in the TOP_STATUS_REG and the monitored Outputs' POK Status in the RAIL_STATUS_REG are all real-time-reaction signals. They are designed as level-triggered signals. When the signal is real (equal to 1), the corresponding bit will also show a high level. On the other hand, a bit equal to a low level will indicate that the false status is in the corresponding monitored function.

The status of the Outputs' PBAD flags in the RAIL_FLAGx are used to record that the PBAD events occured once. They are designed as edge-triggered signals. If a fault of a rail happens, the related PBAD bit will record the real status at the same time. Then the corresponding PBAD bit will lock the issued PBAD signal even if the rail's fault is removed. Reading the bit will make the I^2C interface from the "Master Bus" get the real state, but the RT5147 will clear the bit to a false state (equal to b0) if the PBAD event is removed.

TOP_STATUS_REG, RAIL_STATUS_REG and RAIL_FLAG_REG are the fault code systems used to record what happens in the present. When the power system of the SSD application encounters a problem, reading back the register values from the fault code system can help users easily understand what is going on.

16.23 nIRQ (Negative Interrupt Request)

The nIRQ system also belongs to the fault codes system. All the faults that occur under the RT5147 operation will be recorded by the corresponding internal register functions. The nIRQ system can decide which fault to exported to the SSD system.

There are two embedded register functions, nIRQ_CLEAR and nIRQ_MASK, in the nIRQ system. The nIRQ_CLEAR has two functions:

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- The first function is used to record the fault flag from the TOP_STATUS, RAIL_STATUS, and RAIL_FLAGx registers.
- The second function is designed to write a b1 into itself to clear the record of the fault flag from the first function description.

The record function is designed to edge-trigger and lock-out behavior. Once the bit is recorded to b1, the bit will remain locked until it is cleared by writing a b1 to the register (The second function) or if AVIN is under the UVLO voltage.

The nIRQ_MASK function is used to decide that the nIRQ output (active low) will monitor the fault built in the nIRQ_CLEAR. If the fault is recorded but masked by the nIRQ system, the nIRQ output will ignore the record fault. If the fault is recorded and unmasked, the GPIOx as the nIRQ will output a low-level signal (see Figure 9).

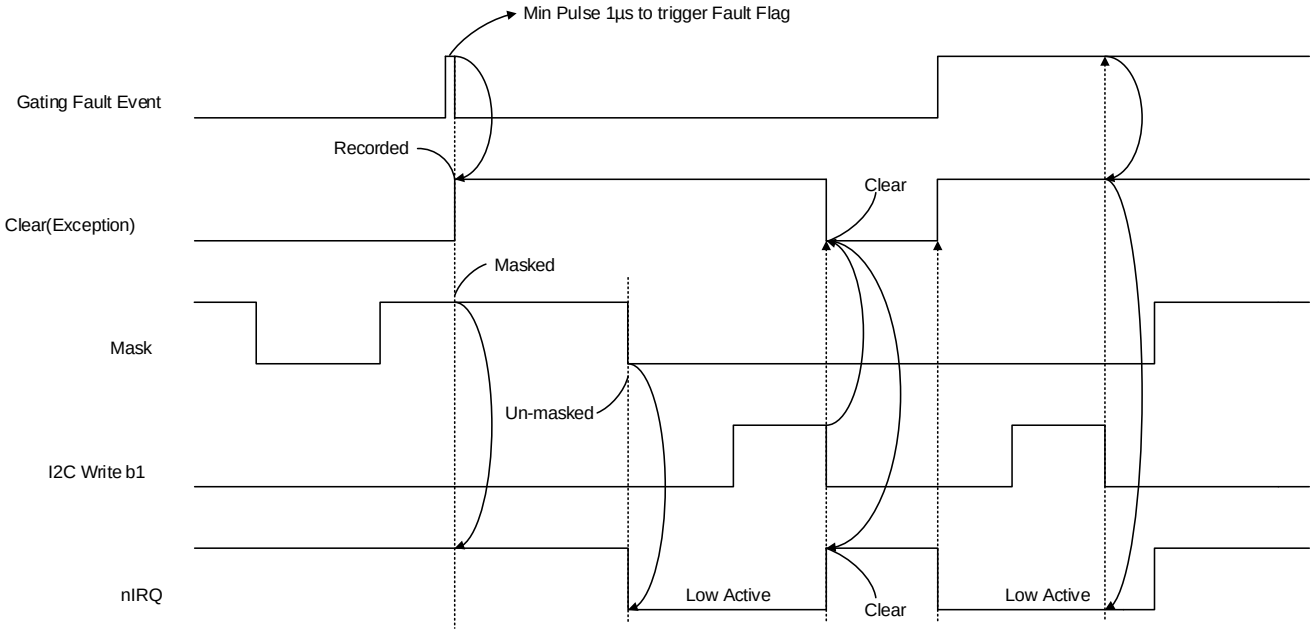

Figure 9. The Relation Chart for nIRQ, Clear and Mask

16.24 Power Disable (PWRDIS)

The PWRDIS is the main on/off signal for the power down/up sequence of the RT5147. However, it will not enable the behavior of the register values re-loaded from the EFUSE when PWRDIS transitions from H to L. The PWRDIS_DELAY_TIME function can delay the PWRDIS signal for the power-off sequence of the RT5147. When PWRDIS = L with AVIN in the normal range, the RT5147 will enable the power-up sequence immediately. The power-off delay time can be set to 0ms, 0.5ms, 1ms, 2ms, 4ms, 8ms, and 16ms. If users want to disable this function, set PWRDIS_DELAY_TIME to 0x7 to make the RT5147 ignore the PWRDIS function.

16.25 B2/B3_DVS_EN_SLEEPx

Buck2 and Buck3 can have another output voltage when the RT5147 enters sleep mode and Buck2 and Buck3 remain alive. The B2/B3 DVS enable signals are controlled by the B2_DVS_EN_SLEEP1, B2_DVS_EN_SLEEP2, B3_DVS_EN_SLEEP1, and B3_DVS_EN_SLEEP2 bits. If the RT5147 enters sleep mode via the SLEEP1 signal, Buck2 and Buck3 will follow B2/B3_DVS_EN_SLEEP1; if the RT5147 enters sleep mode via the SLEEP2 signal, Buck2 and Buck3 will follow B2/B3_DVS_EN_SLEEP2. However, Buck2 and Buck3 will follow B2/B3_DVS_EN_SLEEP2 when the RT5147 enters sleep mode via both SLEEP1 = 0 and SLEEP2 = 0 (low active).

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16.26 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-36B 2.66x2.70 (BSC) package, the thermal resistance, θ_{JA}, is 28.56°C/W on a standard JEDEC 51-9 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)} = (125°C - 25°C) / (28.56°C/W) = 3.5W$ for a WL-CSP-36B 2.66x2.70 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

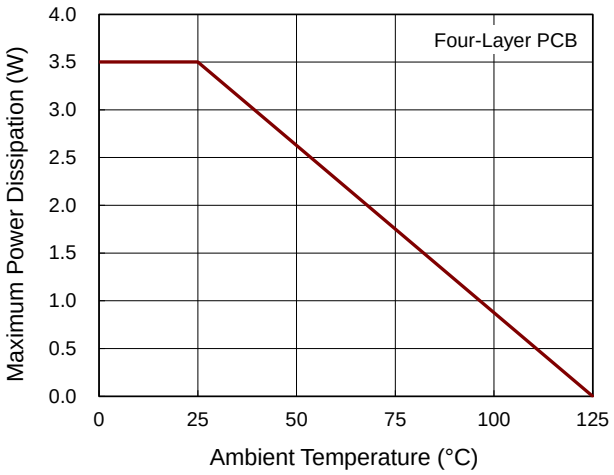

Figure 10. Derating Curve of Maximum Power Dissipation

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16.27 Layout Considerations

Layout is very important in high-frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout.

Power components should be placed on the same side of the board, with power traces routed on the same layer. If it is necessary to route a power trace to another layer, choose a trace in low di/dt paths and use multiple vias for interconnection. When vias are used to connect PCB layers in the high current loop, there should be enough vias to reduce the path impedance as much as possible. The width of the power trace is decided by the maximum current that passes through it. With enough width and vias, the resistance of the entire power trace can be minimized to improve the performance of the converter. Below are some other layout guidelines which should be considered:

- Place the input decoupling capacitors as close as possible to VIN pins (for example, AVIN, VINLDO1, VIN_B1, VIN_B2, VIN_B3, and VIN_B4). The input capacitor can provide instant current to the converter when the high-side MOSFET turns on. It is better to connect the input capacitors to the VIN pins directly with a trace on the same layer. It is preferable to connect the decoupling capacitors directly to the pins without using vias.
- Place the inductors close to the LX pins (for example, SW_B1, SW_B2, SW_B3, and SW_B4), and the power trace between them should be wide and short. Using a wide and short trace to minimize the ESR will gain better efficiency. Additionally, this trace copper area provides a heat sink for the inductor and the internal MOSFETs. Do not make the area of the node small by using narrow traces; keep the area as wide as possible without affecting other paths. However, the largest voltage and current variation also happens on the trace of SW_Bx, it should keep any sensitive trace far away from this node.
- For feedback signals FB_B1, FB_B2, FB_B3, and FB_B4, the sensing point which detects the output voltage must be connected after the output capacitor and keep the trace far away from the switching node or inductor. In addition, the current through the FB_Bx trace should be very small. Place the feedback network as close to the chip as possible.
- Place the output capacitors close to LDO1, LDO2, and the output side of the Bx inductor to minimize trace inductance.
- The GND pins should be connected to a strong ground plane for heat sinking and noise protection.

Table 10. Suggested Inductors for Typical Application Circuit

Component Supplier	Part No.	Inductance (μH)	Dimensions (mm)	Note
Cyntec	HTTD32251B-R47MMR	0.47	3.2 x 2.5 x 1.2	L1, L3
Cyntec	HMMQ20161B-R47MDR	0.47	2 x 1.6 x 1.2	L2, L4

Table 11. Recommended Component Selection for Typical Application Circuit

Component Supplier	Part No.	Capacitance (μF)	Case Size
MURATA	GRM155R60J225ME01	2.2	0402
MURATA	GRM188R60J106ME47	10	0603
MURATA	GRM188R60J226ME15	22	0603

Note 11. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

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17 Functional Register Description

The following Table 12 is a summary of registers. It shows the default register values of the PMIC when the AVIN is over UVLO rising threshold but under VSYSMON. Certain default values of register address are from EFUSE. When AVIN is above UVLO, the status of some registers will be determined by the three states (H, Hi-Z, L) of GPIO#.

Table 12. Register Summary

Address	Register Name	Default Value (Hex.)			Type	EFUSE	Control by GPIO#
		H	Hi-Z	L			
0x00	TOP_STATUS_REG	00	00	00	RO	--	--
0x01	RAIL_FLAG0_REG	00	00	00	R1C	--	--
0x02	RAIL_FLAG1_REG	00	00	00	R1C	--	--
0x03	RAIL_STATUS_REG	00	00	00	RO	--	--
0x04	RAIL_FALG2_REG	00	00	00	R1C	--	--
0x05	GPIO1_REG	04	04	04	RW	Bits[2:0]	--
0x06	GPIO2_REG	00	00	00	RW	Bits[6:3]	--
0x07	GPIO3_REG	00	00	00	RW	Bits[6:3]	--
0x08	GPIO4_REG	00	00	00	RW	Bits[6:3]	--
0x09	GPIO5_REG	18	10	10	RW	Bits[6:3]	GPIO3
0x0A	GPIO6_REG	00	00	00	RW	Bits[6:3]	--
0x0B	GPIO7_REG	30	30	30	RW	Bits[6:3]	--
0x0C	GPIO8_REG	20	20	20	RW	Bits[6:3]	--
0x0D	GPIO3_DELAY_REG0	6C	6F	06	RW	Bits[7:0]	GPIO3
0x0E	GPIO3_DELAY_REG1	88	88	88	RW	Bits[7:0]	GPIO3
0x0F	WARN_VTH_REG0	00	00	00	RW	--	--
0x10	WARN_VTH_REG1	00	00	00	RW	--	--
0x11	nRESET_MASK_REG	00	00	00	RW	--	--
0x12	nIRQ_CLEAR_REG	00	00	00	W1C	--	--
0x13	nIRQ_MASK_REG	FC	FC	FC	RW	--	--
0x14	EXT_EN1_O_TIME_SLOT	07	07	07	RW	Bits[4:0]	--
0x15	EXT_EN2_O_TIME_SLOT	07	07	07	RW	Bits[4:0]	--
0x16	EXT_EN1_I	C0	C0	C0	RW	--	--
0x17	EXT_EN2_I	C0	C0	C0	RW	--	--
0x18	EXT_ENx_O_DELAY	00	00	00	RW	--	--
0x19	SST0_REG	55	55	55	RW	Bits[7:0]	--
0x1A	SST1_REG	00	00	00	RW	Bits[7:6]	--
0x1B	B1_CFG_REG	6A	6A	6A	RW	Bits[3:1]	--
0x1C	B1_SEL_REG	A0	A0	A0	RW	Bits[7:2]	GPIO2
0x1D	B2_CFG_REG	6A	6A	6A	RW	--	--
0x1E	B2_SEL_REG	52	52	8C	RW	Bits[7:1]	GPIO2

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Address	Register Name	Default Value (Hex.)			Type	EFUSE	Control by GPIO#
		H	Hi-Z	L			
0x1F	B2_DVS_SEL_REG	52	52	8C	RW	Bits[7:1]	GPIO2/ GPIO3
0x20	B3_CFG_REG	6A	6A	6A	RW	Bits[3:1]	--
0x21	B3_SEL_REG	38	38	38	RW	Bits[7:1]	GPIO3
0x22	B3_DVS_SEL_REG	38	38	38	RW	Bits[7:1]	GPIO3
0x23	B4_CFG_REG	6A	6A	6A	RW	--	--
0x24	B4_SEL_REG	28	3C	3C	RW	Bits[7:1]	GPIO4
0x25	LDO1_SEL_REG	40	40	78	RW	Bits[7:2]	GPIO4
0x26	LDO2_SEL_REG	40	--	40	RW	Bits[7:2]	GPIO6
0x27	DCDCCTRL0_REG	00	00	00	RW	--	--
0x28	SLEEP_DVS_REG	00	00	00	RW	Bits[7:4]	GPIO2/ GPIO3
0x29	SLEEP1_REG	FC	FC	FC	RW	Bits[7:2]	--
0x2A	SLEEP2_REG	FC	FC	FC	RW	Bits[7:2]	--
0x2B	DCDCCRTL1_REG	00	00	00	RW	--	--
0x2C	DISCHARGE0_REG	FC	FC	FC	RW	--	--
0x2D	DISCHARGE1_REG	15	15	15	RW	--	--
0x2E	DISCHARGE2_REG	D0	D0	D0	RW	--	--
0x2F	DCDCCTRL2_REG	00	00	00	RW	--	--
0x30	B1_TIME0_REG	00	00	00	RW	--	--
0x31	B1_TIME1_REG	0E	0E	0E	RW	Bits[4:0]	--
0x32	B2_TIME0_REG	00	00	00	RW	--	--
0x33	B2_TIME1_REG	04	04	04	RW	Bits[4:0]	--
0x34	B3_TIME0_REG	00	00	00	RW	--	--
0x35	B3_TIME1_REG	01	01	01	RW	Bits[4:0]	--
0x36	B4_TIME0_REG	00	00	00	RW	--	--
0x37	B4_TIME1_REG	61	61	61	RW	Bits[4:0]	--
0x38	MANUFACTURER_ID_REG	21	21	21	RO	--	--
0x39	LDO1_TIME0_REG	00	00	00	RW	--	--
0x3A	LDO1_TIME1_REG	01	01	01	RW	Bits[4:0]	--
0x3B	LDO2_TIME0_REG	00	00	00	RW	--	--
0x3C	LDO2_TIME1_REG	01	01	01	RW	Bits[4:0]	--
0x3D	PWRDIS_REG	07	07	07	RW	Bits[2:0]	--
0x3E	PRODUCT_ID_REG	47	47	47	RO	--	--
0x3F	REVISION_NUMBER_REG	A1	A1	A1	RO	--	--
0x40	TOP_CTRL_REG	70	70	70	RO	Bit[4]	--
0x41	B3_REAL_SEL_REG		--	--	RO	--	--

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17.1 Registers Configuration

See below register tables for the detailed description of their functions. Some of the registers are volatile. Volatile registers are accessible through the I^2C slave bus and are not valid while AVIN is under UVLO. Some of the registers will reload their values from the values fixed by the EFUSE. Table 6 shows which value of the register function can be adjusted by the factory.

Table 13. TOP_STATUS_REG

Address: 0x00
Description: Top status bit indicates VIN and PMIC PG or PBAD.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VSYSMON	VSYSWARN	POK_OV	VIN_OV	OT_WARN	OT_PMIC	nRESET	IRQ
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	VSYSMON	Real Time bit. 1b: VIN ≥ VSYSMON 0b: VIN < VSYSMON If AVIN is above the VSYSMON threshold, REG_0x00[7], VSYSMON, will become 1b with 10μs (typical) deglitch time.
6	VSYSWARN	Real Time bit. 1b: VIN ≥ VSYSWARN 0b: VIN < VSYSWARN If AVIN is above the VSYSWARN threshold, REG_0x00[6], VSYSWARN, will become 1b with 10μs (typical) deglitch time.
5	POK_OV	Real Time bit. 1b: VIN ≥ POK_OV 0b: VIN < POK_OV If AVIN is above the POK_OV threshold, REG_0x00[5], POK_OV, will become 1b with 10μs (typical) deglitch time.
4	VIN_OV	Real Time bit. 1b: VIN ≥ VIN_OV 0b: VIN < VIN_OV If AVIN is above the VIN_OV threshold, REG_0x00[4], VIN_OV, will become 1b with 10μs (typical) deglitch time.
3	OT_WARN	Real Time bit. 1b: PMIC temperature ≥ OT_WARN 0b: PMIC temperature < OT_WARN If the PMIC temperature is above OT_WARN threshold, REG_0x00[3], OT_WARN, will become 1b.
2	OT_PMIC	Real Time bit. 1b: PMIC temperature ≥ OT_PMIC 0b: PMIC temperature < OT_PMIC If the PMIC temperature is above OT_PMIC threshold, REG_0x00[2], OT_PMIC, will become 1b.
1	nRESET	Real Time bit. 1b: Indicates PMIC Power Good (PG) after power-up sequence 0b: Indicates PMIC Power Bad (PBAD)
0	IRQ	Real Time bit. 1b: Indicates triggered fault 0b: Indicates non-fault

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Table 14. RAIL_FLAG0_REG

Address: 0x01
Description: This register bit records the UVP event when it is triggered.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_UV	B2_UV	B3_UV	B4_UV	LDO1_UV	LDO2_UV	Reserved	
Read/Write	R1C	R1C	R1C	R1C	R1C	R1C	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_UV	Rails' flag bit. 1b: Indicates UV on B1 once 0b: Normal Reading this bit will reset this bit to 0b.
6	B2_UV	Rails' flag bit. 1b: Indicates UV on B2 once 0b: Normal Reading this bit will reset this bit to 0b.
5	B3_UV	Rails' flag bit. 1b: Indicates UV on B3 once 0b: Normal Reading this bit will reset this bit to 0b.
4	B4_UV	Rails' flag bit. 1b: Indicates UV on B4 once 0b: Normal Reading this bit will reset this bit to 0b.
3	LDO1_UV	Rails' flag bit. 1b: Indicates UV on LDO1 once 0b: Normal Reading this bit will reset this bit to 0b.
2	LDO2_UV	Rails' flag bit. 1b: Indicates UV on LDO2 once 0b: Normal Reading this bit will reset this bit to 0b.

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Table 15. RAIL_FLAG1_REG

Address: 0x02
Description: This register bit records the OVP event when it is triggered.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_OV	B2_OV	B3_OV	B4_OV	LDO1_OV	LDO2_OV	Reserved	
Read/Write	R1C	R1C	R1C	R1C	R1C	R1C	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_OV	Rails' flag bit. 1b: Indicates OV on B1 once 0b: Normal Reading this bit will reset this bit to 0b.
6	B2_OV	Rails' flag bit. 1b: Indicates OV on B2 once 0b: Normal Reading this bit will reset this bit to 0b.
5	B3_OV	Rails' flag bit. 1b: Indicates OV on B3 once 0b: Normal Reading this bit will reset this bit to 0b.
4	B4_OV	Rails' flag bit. 1b: Indicates OV on B4 once 0b: Normal Reading this bit will reset this bit to 0b.
3	LDO1_OV	Rails' flag bit. 1b: Indicates OV on LDO1 once 0b: Normal Reading this bit will reset this bit to 0b.
2	LDO2_OV	Rails' flag bit. 1b: Indicates OV on LDO2 once 0b: Normal Reading this bit will reset this bit to 0b.

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Table 16. RAIL_STATUS_REG

Address: 0x03
Description: The rail's status bit indicates the output POK.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_POK	B2_POK	B3_POK	B4_POK	LDO1_POK	LDO2_POK	Reserved	
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_POK	Real time for rail's flag bit. 1b: Indicates POK on B1 0b: No POK on B1
6	B2_POK	Real time for rail's flag bit. 1b: Indicates POK on B2 0b: No POK on B2
5	B3_POK	Real time for rail's flag bit. 1b: Indicates POK on B3 0b: No POK on B3
4	B4_POK	Real time for rail's flag bit. 1b: Indicates POK on B4 0b: No POK on B4
3	LDO1_POK	Real time for rail's flag bit. 1b: Indicates POK on LDO1 0b: No POK on LDO1
2	LDO2_POK	Real time for rail's flag bit. 1b: Indicates POK on LDO2 0b: No POK on LDO2

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Table 17. RAIL_FLAG2_REG

Address: 0x04
Description: This register bit records the ILIM event when it is triggered.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_ILIM	B2_ILIM	B3_ILIM	B4_ILIM	LDO1_ILIM	LDO2_ILIM	Reserved	
Read/Write	R1C	R1C	R1C	R1C	R1C	R1C	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_ILIM	Rails' flag bit. Indicates ILIM on B1 once. 1b: Indicates ILIM on B1 once 0b: Normal Reading this bit will reset this bit to 0b.
6	B2_ILIM	Rails' flag bit. Indicates ILIM on B2 once. 1b: Indicates ILIM on B2 once 0b: Normal Reading this bit will reset this bit to 0b.
5	B3_ILIM	Rails' flag bit. Indicates ILIM on B3 once. 1b: Indicates ILIM on B3 once 0b: Normal Reading this bit will reset this bit to 0b.
4	B4_ILIM	Rails' flag bit. Indicates ILIM on B4 once. 1b: Indicates ILIM on B4 once 0b: Normal Reading this bit will reset this bit to 0b.
3	LDO1_ILIM	Rails' flag bit. Indicates ILIM on LDO1 once. 1b: Indicates ILIM on LDO1 once 0b: Normal Reading this bit will reset this bit to 0b.
2	LDO2_ILIM	Rails' flag bit. Indicates ILIM on LDO2 once. 1b: Indicates ILIM on LDO2 once 0b: Normal Reading this bit will reset this bit to 0b.

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Table 18. GPIO1(nRESET)_REG

Address: 0x05 **Description:** GPIO1 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved					nRST_DELAY_TIME		
Read/Write	RO	RO	RO	RO	RO	RW	RW	RW
Default Value	0	0	0	0	0	1	0	0

Bits	Name	Description
2:0	nRST _DELAY_TIME	The timing from the POK signal of the B3 rail in the power-up sequence to the nRESET signal. 000b = Delay 0.5ms. 001b = Delay 1ms. 010b = Delay 2ms. 011b = Delay 4ms. 100b = Delay 8ms. 101b = Delay 16ms. 110b = Delay 32ms. 111b = Delay 64ms.

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Table 19. GPIO2_REG

Address: 0x06 **Description:** GPIO2 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO2_FUNC_EN	GPIO2_FUNC_SEL				Reserved	GPIO2_GENERAL_CTRL	
Read/Write	RW	RW	RW	RW	RW	RO	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GPIO2_FUNC_EN	GPIO2 has an initial function before nRESET=1. This bit can disable the function of “GPIO2_FUNC_SEL” after nRESET=1. 0b: Disable 1b: Enable
6:3	GPIO2_FUNC_SEL	0000b = EXT_EN1_O output 0001b = EXT_EN2_O output 0010b = nIRQ (output) 0011b = SLEEP1 (input, low active) 0100b = SLEEP2 (input, low active) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ not used for GPIO2/3/4 1000b = EXT_EN2_I (input)/ not used for GPIO2/3/4
1:0	GPIO2_GENERAL_CTRL	If the function selection is as “EXT_EN1/2_O”, these bits can control the voltage level of the EXT_EN1/2_O as the general purpose input/output. If GPIO2/3/4/6 is set to EXT_EN1/2_O, the EXT_EN1/2_O function only can be enabled after nRESET = 1. (Note 12) 00b = Low level 01b = High level

Note 12. GPIO2/3/4/6 is used to control the VSELx of the rails of the RT5147 before nRESET = 1. Send out the EXT_EN1/2_O signal manually after nRESET = 1 if GPIO2/3/4/6 is set as the EXT_EN1/2_O function. If GPIO5/7/8 is used as EXT_EN1/2_O, the EXT_EN1/2_O can join the power-up sequence.

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Table 20. GPIO3_REG

Address: 0x07 **Description:** GPIO3 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO3_FUNC_EN	GPIO3_FUNC_SEL				Reserved	GPIO3_GENERAL_CTRL	
Read/Write	RW	RW	RW	RW	RW	RO	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GPIO3_FUNC_EN	GPIO3 has an initial function before nRESET=1. This bit can disable the function of “GPIO3_FUNC_SEL” after nRESET=1. 0b: Disable 1b: Enable
6:3	GPIO3_FUNC_SEL	0000b = EXT_EN1_O output 0001b = EXT_EN2_O output 0010b = nIRQ (output) 0011b = SLEEP1 (input, low active) 0100b = SLEEP2 (input, low active) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ not used for GPIO2/3/4 1000b = EXT_EN2_I (input)/ not used for GPIO2/3/4
1:0	GPIO3_GENERAL_CTRL	If the function selection is as “EXT_EN1/2_O”, these bits can control the voltage level of the EXT_EN1/2_O as the general purpose input/output. If the GPIO2/3/4/6 is set to EXT_EN1/2_O, the EXT_EN1/2_O function can only be enabled after nRESET = 1. 00b = Low level 01b = High level

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Table 21. GPIO4_REG

Address: 0x08 **Description:** GPIO4 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO4_FUNC_EN	GPIO4_FUNC_SEL				Reserved	GPIO4_GENERAL_CTRL	
Read/Write	RW	RW	RW	RW	RW	RO	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GPIO4_FUNC_EN	GPIO4 has an initial function before nRESET=1. This bit can disable the function of “GPIO4_FUNC_SEL” after nRESET=1. 0b: Disable 1b: Enable
6:3	GPIO4_FUNC_SEL	0000b = EXT_EN1_O output 0001b = EXT_EN2_O output 0010b = nIRQ (output) 0011b = SLEEP1 (input, low active) 0100b = SLEEP2 (input, low active) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ not used for GPIO2/3/4 1000b = EXT_EN2_I (input)/ not used for GPIO2/3/4
1:0	GPIO4_GENERAL_CTRL	If the function selection is as “EXT_EN1/2_O”, these bits can control the voltage level of the EXT_EN1/2_O as the general purpose input/output. If the GPIO2/3/4/6 is set to EXT_EN1/2_O, the EXT_EN1/2_O function can only be enabled after nRESET = 1. 00b = Low level 01b = High level

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Table 22. GPIO5_REG

Address: 0x09
Description: The function of GPIO5 can be selected by GPIO3 status (H, Hi-Z, L).

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		Reserved	GPIO5_FUNC_SEL				Reserved	GPIO5_GENERAL_CTRL	
Read/Write		RO	RW	RW	RW	RW	RO	RW	RW
Default Value	H	0	0	0	1	1	0	0	0
	Hi-Z	0	0	0	1	0	0	0	0
	L	0	0	0	1	0	0	0	0

Bits	Name	Description
6:3	GPIO5_FUNC_SEL	0000b = EXT_EN1_O output 0001b = EXT_EN2_O output 0010b = nIRQ (output) 0011b = SLEEP1 (input, low active) 0100b = SLEEP2 (input, low active) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ not used for GPIO2/3/4 1000b = EXT_EN2_I (input)/ not used for GPIO2/3/4 1001b = SYSMON
1:0	GPIO5_GENERAL_CTRL	If the function selection is as “EXT_EN1/2_O”, these bits can control the voltage level of the EXT_EN1/2_O as the general purpose input/output after nRESET = 1. If GPIO5/7/8 is set to EXT_EN1/2_O, the EXT_EN1/2_O function can be enabled by other signals before nRESET = 1. (Refer to Table 35 and Table 36.) 00b = Low level 01b = High level

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Table 23. GPIO6_REG

Address: 0x0A **Description:** GPIO6 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO6_FUNC_EN	GPIO6_FUNC_SEL				Reserved	GPIO6_GENERAL_CTRL	
Read/Write	RW	RW	RW	RW	RW	RO	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GPIO6_FUNC_EN	GPIO6 has an initial function before nRESET=1. This bit can disable the function of “GPIO6_FUNC_SEL” after nRESET=1. 0b: Disable 1b: Enable
6:3	GPIO6_FUNC_SEL	0000b = EXT_EN1_O output 0001b = EXT_EN2_O output 0010b = nIRQ (output) 0011b = SLEEP1 (input, low active) 0100b = SLEEP2 (input, low active) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ not used for GPIO2/3/4 1000b = EXT_EN2_I (input)/ not used for GPIO2/3/4
1:0	GPIO6_GENERAL_CTRL	If the function selection is as “EXT_EN1/2_O”, these bits can control the voltage level of the EXT_EN1/2_O as the general purpose input/output. If the GPIO2/3/4/6 is set to EXT_EN1/2_O, the EXT_EN1/2_O function can only be enabled after nRESET = 1. 00b = Low level 01b = High level

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Table 24. GPIO7_REG

Address: 0x0B **Description:** GPIO7 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	GPIO7_FUNC_SEL				Reserved	GPIO7_GENERAL_CTRL	
Read/Write	RO	RW	RW	RW	RW	RO	RW	RW
Default Value	0	0	1	1	0	0	0	0

Bits	Name	Description
6:3	GPIO7_FUNC_SEL	0000b = EXT_EN1_O output 0001b = EXT_EN2_O output 0010b = nIRQ (output) 0011b = SLEEP1 (input, low active) 0100b = SLEEP2 (input, low active) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ not used for GPIO2/3/4 1000b = EXT_EN2_I (input)/ not used for GPIO2/3/4
1:0	GPIO7_GENERAL_CTRL	If the function selection is as “EXT_EN1/2_O”, these bits can control the voltage level of the EXT_EN1/2_O as the general purpose input/output after nRESET = 1. If the GPIO5/7/8 is set to EXT_EN1/2_O, the EXT_EN1/2_O function can be enabled by other signals before nRESET = 1. (Refer to Table 35 and Table 36.) 00b = Low level 01b = High level

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Table 25. GPIO8_REG

Address: 0x0C **Description:** GPIO8 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	GPIO8_FUNC_SEL				Reserved	GPIO8_GENERAL_CTRL	
Read/Write	RO	RW	RW	RW	RW	RO	RW	RW
Default Value	0	0	1	0	0	0	0	0

Bits	Name	Description
6:3	GPIO8_FUNC_SEL	0000b = EXT_EN1_O output 0001b = EXT_EN2_O output 0010b = nIRQ (output) 0011b = SLEEP1 (input, low active) 0100b = SLEEP2 (input, low active) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ not used for GPIO2/3/4 1000b = EXT_EN2_I (input)/ not used for GPIO2/3/4
1:0	GPIO8_GENERAL_CTRL	If the function selection is as “EXT_EN1/2_O”, these bits can control the voltage level of the EXT_EN1/2_O as the general purpose input/output after nRESET = 1. If the GPIO5/7/8 is set to EXT_EN1/2_O, the EXT_EN1/2_O function can be enabled by other signals before nRESET = 1. (Refer to Table 35 and Table 36.) 00b = Low level 01b = High level

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Table 26. GPIO3_DELAY0_REG

Address: 0x0D **Description:** B3 and B4 delay time selection during the power-up sequence by GPIO3 status (H, Hi-Z, L).									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B3_DELAY_SEL			B4_DELAY_SEL				
Read/Write		RW	RW	RW	RW	RW	RW	RW	RW
Default Value	H	0	1	1	0	1	1	0	0
	Hi-Z	0	1	1	0	1	1	1	1
	L	0	0	0	0	0	1	1	0

Bits	Name	Description
7:5	B3_DELAY_SEL	Offset = 0ms Step = 0.25ms Delay time = DEC(0x0D[7:5]) x 0.25ms
4:0	B4_DELAY_SEL	Offset = 0ms Step = 0.25ms Delay time = DEC(0x0D[4:0]) x 0.25ms

Table 27. GPIO3_DELAY1_REG

Address: 0x0E **Description:** LDO1 and LDO2 delay time selection during the power-up sequence by GPIO3 status (H, Hi-Z, L).									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		LDO1_DELAY_SEL				LDO2_DELAY_SEL			
Read/Write		RW	RW	RW	RW	RW	RW	RW	RW
Default Value	H	1	0	0	0	1	0	0	0
	Hi-Z	1	0	0	0	1	0	0	0
	L	1	0	0	0	1	0	0	0

Bits	Name	Description
7:4	LDO1_DELAY_SEL	Offset = 0ms Step = 0.25ms Delay time = DEC(0x0E[7:4]) x 0.25ms
3:0	LDO2_DELAY_SEL	Offset = 0ms Step = 0.25ms Delay time = DEC(0x0E[3:0]) x 0.25ms

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Table 28. WARN0_REG

Address: 0x0F **Description:** SYSWARN and SYSMON Vth configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SYSWARN_SEL				SYSMON_SEL			
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	SYSWARN_SEL	Vth of the SYSWARN selection: Offset = 2775mV Step = 25mV Max = 3150mV SYSWARN threshold = 2775mV + DEC(0x0F[7:4]) x 25mV
3:0	SYSMON_SEL	Vth of the SYSMON selection Offset = 2725mV Step = 25mV Max = 3100mV SYSMON threshold = 2725mV + DEC(0x0F[3:0]) x 25mV

Table 29. WARN1_REG

Address: 0x10 **Description:** POK_OV Vth configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	POK_OV_SEL	Reserved						
Read/Write	RW	RO	RO	RO	RO	RO	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	POK_OV_SEL	Vth of POK_OV warning signal selection: 0b = 3.5V 1b = 3.8V

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Table 30. nRESET_MASK_REG

Address: 0x11 **Description:** Mask the protection function will make nRESET signal active.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_PBAD_RESET_MASK	B2_PBAD_RESET_MASK	B3_PBAD_RESET_MASK	B4_PBAD_RESET_MASK	L1_PABD_RESET_MASK	L2_PBAD_RESET_MASK	VIN_OV_RESET_MASK	OT_RESET_MASK
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	B1_PBAD_RESET_MASK	Mask the analog circuit protection behavior, but still implement the digital fault flags. 0b = Nothing 1b = Mask the analog protection behavior
6	B2_PBAD_RESET_MASK	
5	B3_PBAD_RESET_MASK	
4	B4_PBAD_RESET_MASK	
3	L1_PBAD_RESET_MASK	
2	L2_PBAD_RESET_MASK	
1	VIN_OV_RESET_MASK	
0	OT_RESET_MASK	

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Table 31. nIRQ_CLEAR_REG

Address: 0x12 **Description:** Indicate the interrupt flag and this bit can be cleared by writing 1b to it.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_UNDER_SYSMON_CLR	VIN_UNDER_SYSWARN_CLR	VIN_OVER_POK_OV_CLR	VIN_OV_CLR	OT_WARN_CLR	OUTPUT_OVUV_CLR	Reserved	
Read/Write	W1C	W1C	W1C	W1C	W1C	W1C	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	VIN_UNDER_SYSMON_CLR	0b: Nothing 1b: Indicates the interrupt flag of the event Write 1b to clear the exception bit, if the event does not exist.
6	VIN_UNDER_SYSWARN_CLR	
5	VIN_OVER_POK_OV_CLR	
4	VIN_OV_CLR	
3	OT_WARN_CLR	
2	OUTPUT_OVUV_CLR	

Table 32. nIRQ_MASK_REG

Address: 0x13 **Description:** Mask the interrupt flag (nIRQ) of the event but the flag of the exception bit will still work.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_UNDER_SYSMON_MASK	VIN_UNDER_SYSWARN_MASK	VIN_OVER_POK_OV_MASK	VIN_OV_MASK	OT_WARN_MASK	OUTPUT_OVUV_MASK	Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	RO	RO
Default Value	1	1	1	1	1	1	0	0

Bits	**Name**	**Description**
7	VIN_UNDER_SYSMON_MASK	Only mask the interrupt flag (nIRQ) of the event but the flag of the exception bit will still work well. 0b: Does not mask the interrupt flag of the event 1b: Mask the interrupt flag of the event
6	VIN_UNDER_SYSWARN_MASK	
5	VIN_OVER_POK_OV_MASK	
4	VIN_OV_MASK	
3	OT_WARN_MASK	
2	OUTPUT_OVUV_MASK	

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Table 33. EXT_EN1_O_TIME_SLOT_REG

Address: 0x14
Description: Configure the time slot of the external enable1 output (EXT_EN1_O) during the power-up sequence. The EXT_EN1_O will issue from low to high automatically at the setting time slot.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved			EXT_EN1_O_TIME_SLOT				
Read/Write	RO	RO	RO	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	1	1	1

Bits	Name	Description
4:0	EXT_EN1_O_TIME_SLOT	EXT_EN1_O power-up sequence without external controlled signal when VIN is from 0V to above SYSMON. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 34. EXT_EN2_O_TIME_SLOT_REG

Address: 0x15
Description: Configure the time slot of the external enable2 output (EXT_EN2_O) during the power-up sequence. The EXT_EN2_O will issue from low to high automatically at the setting time slot.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved			EXT_EN2_O_TIME_SLOT				
Read/Write	RO	RO	RO	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	1	1	1

Bits	Name	Description
4:0	EXT_EN2_O_TIME_SLOT	EXT_EN1_O power-up sequence without external controlled signal when VIN is from 0V to above SYSMON. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

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Table 35. EXT_EN1_I

Address: 0x16
Description: Configure the input signals to trigger EXT_EN1_O.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EXT_EN1_O_INPUT_SEL		EXT_EN1_O_POK_SEL			EXT_EN1_I_SEL		Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	RO
Default Value	1	1	0	0	0	0	0	0

Bits	Name	Description
7:6	EXT_EN1_O_INPUT_SEL	EXT_EN1_O follows below selected signal and issue the high level voltage signal with a delay time. 00b = Rails' POK 01b = EXT_EN1_I 10b = I^2C Interface. (as general purpose IO) 11b = EXT_EN1_O_TIME_SLOT
5:3	EXT_EN1_POK_SEL	If bits [7:6] = 00b, EXT_EN1_O will go high after the POK signal of the rail below with a delay time. 000b = B1 001b = B2 010b = B3 011b = B4 100b = L1 101b = L2 110b = nRESET 111b = VSYSMON
2:1	EXT_EN1_I_SEL	If bit[7:6] = 01b, EXT_EN1_O will go high after the GPIOx (as EXT_EN1_I) below going high with a delay time. 00b = GPIO5 01b = GPIO6 10b = GPIO7 11b = GPIO8

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Table 36. EXT_EN2_I

Address: 0x17
Description: Configure the input signals to trigger EXT_EN2_O.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EXT_EN2_O_INPUT_SEL		EXT_EN2_O_POK_SEL			EXT_EN2_I_SEL		Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	RO
Default Value	1	1	0	0	0	0	0	0

Bits	Name	Description
7:6	EXT_EN2_O_INPUT_SEL	EXT_EN2_O follows the selected signal below and issue the high level voltage signal with a delay time. 00b = Rails' POK 01b = EXT_EN2_I 10b = I^2C Interface. (as general purpose IO) 11b = EXT_EN2_O_TIME_SLOT
5:3	EXT_EN2_POK_SEL	If bits [7:6] = 00b, EXT_EN2_O will go high after the POK signal of the rail below with a delay time. 000b = B1 001b = B2 010b = B3 011b = B4 100b = L1 101b = L2 110b = nRESET 111b = VSYSMON
2:1	EXT_EN2_I_SEL	If bit[7:6] = 01b, EXT_EN2_O will go high after the GPIOx (as EXT_EN2_I) below going high with a delay time. 00b = GPIO5 01b = GPIO6 10b = GPIO7 11b = GPIO8

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Table 37. EXT_ENx_O_DELAY

Address: 0x18
Description: The delay time setting for EXT_EN1_O and EXT_EN2_O.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EXT_EN1_O_DELAY				EXT_EN2_O_DELAY			
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	EXT_EN1_O_DELAY	If the following signal is Rail's POK or EXT_EN1/2_I, EXT_EN1/2_O will issue from low to high with below delay time. Offset = 0ms Step = 0.25ms EXT_EN1_O Delay time = DEC(0x18[7:4]) x 0.25ms EXT_EN2_O Delay time = DEC(0x18[3:0]) x 0.25ms
3:0	EXT_EN2_O_DELAY	

Table 38. SST0_REG

Address: 0x19
Description: Rails' soft-start time configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_SST_SEL		B2_SST_SEL		B3_SST_SEL		B4_SST_SEL	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	1	0	1	0	1	0	1

Bits	Name	Description
7:6	B1_SST_SEL	Soft-start time for B1 00b = 125μs, 01b = 250μs, 10b = 500μs, 11b = 750μs
5:4	B2_SST_SEL	Soft-start time for B2 00b = 125μs, 01b = 250μs, 10b = 500μs, 11b = 750μs
3:2	B3_SST_SEL	Soft-start time for B3 00b = 125μs, 01b = 250μs, 10b = 500μs, 11b = 750μs
1:0	B4_SST_SEL	Soft-start time for B4_BUCK Mode 00b = 125μs, 01b = 250μs, 10b = 500μs, 11b = 750μs Soft-start time for B4_LDO Mode 00b = 250μs, 01b = 500μs, 10b = Reserved, 11b = Reserved.

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Table 39. SST1_REG

Address: 0x1A **Description:** Rails' soft-start time configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDO1_SST_SEL	LDO2_SST_SEL	Reserved					
Read/Write	RW	RW	RO	RO	RO	RO	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	LDO1_SST_SEL	Soft-start time for LDO1/2 mode 0b = 250μs 1b = 500μs
6	LDO2_SST_SEL	

Table 40. B1_CFG_REG

Address: 0x1B **Description:** Configure OC level, DVID slew rate, and Fsw of B1.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_ILMAX		B1_TSTEP		B1_FREQ			Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	RO
Default Value	0	1	1	0	1	0	1	0

Bits	Name	Description
7:6	B1_ILMAX	OCL 00b = 4A 01b = 5A (default) 10b = 6A 11b = 7A
5:4	B1_TSTEP	DVID Slew Rate 00b = DVID up:20mV/μs, DVID down:5mV/μs 01b = DVID up:15mV/μs, DVID down:5mV/μs 10b = DVID up:10mV/μs, DVID down:5mV/μs (default) 11b = DVID up:5mV/μs, DVID down:5mV/μs
3:1	B1_FREQ	Fsw 000b to 011b = 1MHz 100b = 1.5MHz 101b = 2MHz (default) 110b = 2.5MHz 111b = 3MHz

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Table 41. B1_SEL_REG

Address: 0x1C **Description:** B1 VID selection by GPIO2 status (H, Hi-Z, L).									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B1_SEL						Reserved	
Read/Write		RW	RW	RW	RW	RW	RW	RO	RO
Default Value	H	1	0	1	0	0	0	0	0
	Hi-Z	1	0	1	0	0	0	0	0
	L	1	0	1	0	0	0	0	0

Bits	Name	Description
7:2	B1_SEL	B1 VOUT supply voltage: 000000b: 1.7V 000001b: 1.72V 000010b: 1.74V … 101000b: 2.5V … 111100b: 2.9V 111100b ~111111b: 2.9V

Table 42. B2_CFG_REG

Address: 0x1D **Description:** Configure OC level, DVID slew rate, and Fsw of B2.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_ILMAX		B2_TSTEP		B2_FREQ			Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	RO
Default Value	0	1	1	0	1	0	1	0

Bits	Name	Description
7:6	B2_ILMAX	OCL 00b = 2A 01b = 3A (default) 10b = 4A 11b = 5A
5:4	B2_TSTEP	DVID Slew Rate 00b = DVID up:20mV/μs, DVID down:5mV/μs 01b = DVID up:15mV/μs, DVID down:5mV/μs 10b = DVID up:10mV/μs, DVID down:5mV/μs (default) 11b = DVID up:5mV/μs, DVID down:5mV/μs
3:1	B2_FREQ	Fsw 000b to 011b = 1MHz 100b = 1.5MHz 101b = 2MHz (default) 110b = 2.5MHz 111b = 3MHz

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Table 43. B2_SEL_REG

Address: 0x1E **Description:** B2 VID selection by GPIO2 status (H, Hi-Z, L).									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B2_SEL							Reserved
Read/Write		RW	RW	RW	RW	RW	RW	RW	RO
Default Value	**H**	0	1	0	1	0	0	1	0
	Hi-z	0	1	0	1	0	0	1	0
	L	1	0	0	0	1	1	0	0

Bits	**Name**	**Description**
7:1	B2_SEL	B2 VOUT supply voltage at sleep mode: 0000000b: 0.5V 0000001b: 0.51V 0000010b: 0.52V … 0101001b: 0.91V … 1000110b: 1.2V … 1010000b: 1.3V 1010000b ~1111111b: 1.3V

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Table 44. B2_DVS_SEL_REG

Address: 0x1F **Description:** B2 DVID target when PMIC enters sleep mode.									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B2_DVS_SEL							Reserved
Read/Write		RW	RW	RW	RW	RW	RW	RW	RO
Default Value	**H**	0	1	0	1	0	0	1	0
	Hi-z	0	1	0	1	0	0	1	0
	L	1	0	0	0	1	1	0	0

Bits	**Name**	**Description**
7:1	B2_DVS_SEL	When VIN > 2.6V for the first time and B2_DVS_EN_SLEEP2 = 0b (default), the default value of B2_DVS_SEL is equal to B2_SEL, depending on the status of GPIO2. When VIN > 2.6V for the first time and B2_DVS_EN_SLEEP2 = 1b, the default value of B2_DVS_SEL is equal to B3_DVS_SEL, depending on the status of GPIO3. 0000000b: 0.5V 0000001b: 0.51V 0000010b: 0.52V … 0101001b: 0.91V … 1000110b: 1.2V … 1010000b: 1.3V 1010000b ~1111111b: 1.3V

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Table 45. B3_CFG_REG

Address: 0x20 **Description:** Configure OC level, DVID slew rate, and Fsw of B3.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B3_ILMAX		B3_TSTEP		B3_FREQ			Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	RO
Default Value	0	1	1	0	1	0	1	0

Bits	Name	Description
7:6	B3_ILMAX	OCL 00b = 4A 01b = 5A (default) 10b = 6A 11b = 7A
5:4	B3_TSTEP	DVID Slew Rate 00b = DVID up:20mV/μs, DVID down:5mV/μs 01b = DVID up:15mV/μs, DVID down:5mV/μs 10b = DVID up:10mV/μs, DVID down:5mV/μs (default) 11b = DVID up:5mV/μs, DVID down:5mV/μs
3:1	B3_FREQ	Fsw 000b to 011b = 1MHz 100b = 1.5MHz 101b = 2MHz (default) 110b = 2.5MHz 111b = 3MHz

Table 46. B3_SEL_REG

Address: 0x21 **Description:** B3 VID selection by GPIO3 status (H, Hi-Z, L).									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B3_SEL							Reserved
Read/Write		RW	RW	RW	RW	RW	RW	RW	RO
Default Value	H	0	0	1	1	1	0	0	0
	Hi-Z	0	0	1	1	1	0	0	0
	L	0	0	1	1	1	0	0	0

Bits	Name	Description
7:1	B3_SEL	B3 VOUT supply voltage: 0000000b: 0.5V 0000001b: 0.51V 0000010b: 0.52V … 0011100b: 0.78V … 1010000b: 1.3V 1010000b ~1111111b: 1.3V

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Table 47. B3_DVS_SEL_REG

Address:0x22
Description: B3 DVID target when PMIC enters sleep mode.

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B3_DVS_SEL							Reserved
Read/Write		RW	RW	RW	RW	RW	RW	RW	RO
Default Value	H	0	0	1	1	1	0	0	0
	Hi-Z	0	0	1	1	1	0	0	0
	L	0	0	1	1	1	0	0	0

Bits	Name	Description
7:1	B3_DVS_SEL	When VIN > 2.6V for the first time and B3_DVS_EN_SLEEP2 = 0b (default), the default value of B3_DVS_SEL is equal to B3_SEL, depending on the status of GPIO3.When VIN > 2.6V for the first time and B3_DVS_EN_SLEEP2 = 1b, the default value of B3_DVS_SEL is reloaded from the corresponding eFuse memory, depending on the status of GPIO3. 0000000b: 0.5V 0000001b: 0.51V 0000010b: 0.52V … 0011100b: 0.78V … 1010000b: 1.3V 1010000b ~1111111b: 1.3V

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Table 48. B4_CFG_REG

Address: 0x23
Description: Configure OC level, DVID slew rate, and Fsw of B4.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B4_ILMAX		B4_TSTEP		B4_FREQ			Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	RO
Default Value	0	1	1	0	1	0	1	0

Bits	Name	Description
7:6	B4_ILMAX	OCL for B4_BUCK Mode 00b = 2A 01b = 3A (default) 10b = 4A 11b = 5A OCL for B4_LDO Mode 00b = 400mA 01b = 500mA (default) 10b = Reserved 11b = Reserved
5:4	B4_TSTEP	DVID Slew Rate 00b = DVID up:20mV/μs, DVID down:5mV/μs 01b = DVID up:15mV/μs, DVID down:5mV/μs 10b = DVID up:10mV/μs, DVID down:5mV/μs (default) 11b = DVID up:5mV/μs, DVID down:5mV/μs
3:1	B4_FREQ	Fsw 000b to 011b = 1MHz 100b = 1.5MHz 101b = 2MHz (default) 110b = 2.5MHz 111b = 3MHz

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Table 49. B4_SEL_REG

Address: 0x24
Description: B4 VID selection by GPIO4 status (H, Hi-Z, L).

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B4_SEL							Reserved
Read/Write		RW	RW	RW	RW	RW	RW	RW	RO
Default Value	H	0	0	1	0	1	0	0	0
	Hi-Z	0	0	1	1	1	1	0	0
	L	0	0	1	1	1	1	0	0

Bits	Name	Description
7:1	B4_SEL	B4 VOUT supply voltage: 0000000b: 0.9V 0000001b: 0.91V 0000010b: 0.92V … 0010100b: 1.1V … 0011110b: 1.2V … 1101110b: 2.0V 1101110b ~1111111b: 2.0V

Table 50. LDO1_SEL_REG

Address: 0x25
Description: LDO1 VID selection by GPIO4 status (H, Hi-Z, L).

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		LDO1_SEL						Reserved	
Read/Write		RW	RW	RW	RW	RW	RW	RO	RO
Defaul t Value	H	0	1	0	0	0	0	0	0
	Hi-Z	0	1	0	0	0	0	0	0
	L	0	1	1	1	1	0	0	0

Bits	Name	Description
7:2	LDO1_SEL	LDO1 VOUT supply voltage: 000000b: 1.0V 000001b: 1.05V … 010000b: 1.8V … 011110b: 2.5V … 100010b:2.7V 100010b ~111111b: 2.7V

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Table 51. LDO2_SEL_REG

Address: 0x26 **Description:** LDO2 VID selection by GPIO6 status (H, L).									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		LDO2_SEL						Reserved	
Read/Write		RW	RW	RW	RW	RW	RW	RO	RO
Default Value	**H**	0	1	0	0	0	0	0	0
	L	0	1	0	0	0	0	0	0

Bits	Name	Description
7:2	LDO2_SEL	GPIO6 = H, LDO2 VOUT supply voltage: 000000b: 1.0V 000001b: 1.05V 000010b: 1.10V … 010000b: 1.8V … 100010b:2.7V 100010b ~111111b: 2.7V GPIO6 = L LDO2 will be configured as load switch.

Table 52. DCDCCTRL0_REG

Address: 0x27 **Description:** Rails' enable signal control.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_EN	B2_EN	B3_EN	B4_EN	LDO1_EN	LDO2_EN	Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_EN	0b = Low level ENABLE signal 1b = High level ENABLE signal For nRESET = 0, if the "Time_Slot_X" function of the corresponding regulator did not set to "Disable", the regulator's ENABLE signal will be high and the regulator will follow its time slot setting to power up. For nRESET = 1, if set ENABLE from low level to high level manually, the regulator will ramp up immediately.
6	B2_EN	
5	B3_EN	
4	B4_EN	
3	LDO1_EN	
2	LDO1_EN	

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Table 53. SLEEP_DVS_REG

Address: 0x28 **Description:** Buck2, Buck3 DVS_EN signal control for SLEEP1 and SLEEP2.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_SLEEP1_DVS_EN	B3_SLEEP1_DVS_EN	B2_SLEEP2_DVS_EN	B3_SLEEP2_DVS_EN	Reserved			
Read/Write	RW	RW	RW	RW	RO	RO	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B2_SLEEP1_DVS_EN	0b: When PMIC enters sleep mode via SLEEP1 signal, B2 VOUT follows B2_SEL target. 1b: When PMIC enters sleep mode via SLEEP1 signal, B2 VOUT follows B2_DVS_SEL target.
6	B3_SLEEP1_DVS_EN	0b: When PMIC enters sleep mode via SLEEP1 signal, B3 VOUT follows B3_SEL target. 1b: When PMIC enters sleep mode via SLEEP1 signal, B3 VOUT follows B3_DVS_SEL target.
5	B2_SLEEP2_DVS_EN	0b: When PMIC enters sleep mode via SLEEP2 signal, B2 VOUT follows B2_SEL target. 1b: When PMIC enters sleep mode via SLEEP2 signal, B2 VOUT follows B2_DVS_SEL target.
4	B3_SLEEP2_DVS_EN	0b: When PMIC enters sleep mode via SLEEP2 signal, B3 VOUT follows B3_SEL_REG target. 1b: When PMIC enters sleep mode via SLEEP2 signal, B2 VOUT follows B3_DVS_SEL target.

Note 13. If the PMIC enters sleep mode with both SLEEP1 and SLEEP2 set to 0 (active low), the PMIC will listen to the B2_SLEEP2_DVS_EN and B3_SLEEP2_DVS_EN signals.

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Table 54. SLEEP1_REG

Address: 0x29
Description: Configure the rail to be off or enter low power mode (LPM) in SLEEP1 mode.

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B1_ALIVE_SLEEP1	B2_ALIVE_SLEEP1	B3_ALIVE_SLEEP1	B4_ALIVE_SLEEP1	LDO1_ALIVE_SLEEP1	LDO2_ALIVE_SLEEP1	Reserved	SLEEP1_ENABLE
Read/Write		RW	RW	RW	RW	RW	RW	RO	RW
Default Value	H	1	1	1	1	1	1	0	0
	Hi-Z	1	1	1	1	1	1	0	0
	L	1	1	1	1	1	1	0	0

Bits	Name	Description
7	B1_ALIVE_SLEEP1	0b = When PMIC is at sleep mode via SLEEP1 signal, B1 turns off. 1b = When PMIC is at sleep mode via SLEEP1 signal, B1 remains active and enters LPM.
6	B2_ALIVE_SLEEP1	0b = When PMIC is at sleep mode via SLEEP1 signal, B2 turns off. 1b = When PMIC is at sleep mode via SLEEP1 signal, B2 remains active and enters LPM.
5	B3_ALIVE_SLEEP1	0b = When PMIC is at sleep mode via SLEEP1 signal, B3 turns off. 1b = When PMIC is at sleep mode via SLEEP1 signal, B3 remains active and enters LPM.
4	B4_ALIVE_SLEEP1	0b = When PMIC is at sleep mode via SLEEP1 signal, B4 turns off. 1b = When PMIC is at sleep mode via SLEEP1 signal, B4 remains active and enters LPM.
3	LDO1_ALIVE_SLEEP1	0b = When PMIC is at sleep mode via SLEEP1 signal, L1 turns off. 1b = When PMIC is at sleep mode via SLEEP1 signal, L1 remains active and enters LPM.
2	LDO2_ALIVE_SLEEP1	0b = When PMIC is at sleep mode via SLEEP1 signal, L2 turns off. 1b = When PMIC is at sleep mode via SLEEP1 signal, L2 remains active and enters LPM.
1	Reserved	Reserved bit.
0	SLEEP1_ENABLE	Support the I^2C commands to let PMIC enter sleep mode. 0b = PMIC is in normal mode, if SLEEP2_ENABLE is also 0b. 1b = PMIC is in sleep mode Via SLEEP1 signal, if SLEEP2_ENABLE keeps 0b all rails follow the settings in this register function to ramp down or to enter LPM. If both SLEEP1_ENABLE = 1b and SLEEP2_ENABLE2 = 1b, the priority of the rail's **OFF STATE** in the SLEEP1_REG or SLEEP2_REG is higher than the rail's LPM STATE. The rail will only keep alive and enter LPM with both alive settings in the SLEEP1_REG and SLEEP2_REG.

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Table 55. SLEEP2_REG

Address: 0x2A
Description: Configure the rail to be off or enter low power mode (LPM) in SLEEP2 (PS4) mode.

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B1_ALIVE_SLEEP2	B2_ALIVE_SLEEP2	B3_ALIVE_SLEEP2	B4_ALIVE_SLEEP2	LDO1_ALIVE_SLEEP2	LDO2_ALIVE_SLEEP2	Reserved	SLEEP2_ENABLE
Read/Write		RW	RW	RW	RW	RW	RW	RO	RW
Default Value	H	1	1	1	1	1	1	0	0
	Hi-Z	1	1	1	1	1	1	0	0
	L	1	1	1	1	1	1	0	0

Bits	Name	Description
7	B1_ALIVE_SLEEP2	0b = When PMIC is at sleep mode via SLEEP2 signal, B1 turns off. 1b = When PMIC is at sleep mode via SLEEP2 signal, B1 remains active and enters LPM.
6	B2_ALIVE_SLEEP2	0b = When PMIC is at sleep mode via SLEEP2 signal, B2 turns off. 1b = When PMIC is at sleep mode via SLEEP2 signal, B2 remains active and enters LPM.
5	B3_ALIVE_SLEEP2	0b = When PMIC is at sleep mode via SLEEP2 signal, B3 turns off. 1b = When PMIC is at sleep mode via SLEEP2 signal, B3 remains active and enters LPM.
4	B4_ALIVE_SLEEP2	0b = When PMIC is at sleep mode via SLEEP2 signal, B4 turns off. 1b = When PMIC is at sleep mode via SLEEP2 signal, B4 remains active and enters LPM.
3	LDO1_ALIVE_SLEEP2	0b = When PMIC is at sleep mode via SLEEP2 signal, L1 turns off. 1b = When PMIC is at sleep mode via SLEEP2 signal, L1 remains active and enters LPM.
2	LDO2_ALIVE_SLEEP2	0b = When PMIC is at sleep mode via SLEEP2 signal, L2 turns off. 1b = When PMIC is at sleep mode via SLEEP2 signal, L2 remains active and enters LPM.
1	Reserved	Reserved bit.
0	SLEEP2_ENABLE	Support the I^2C commands to let PMIC enter sleep mode. 0b = PMIC is in normal mode, if SLEEP1_ENABLE is also 0b. 1b = PMIC is in sleep mode Via SLEEP2 signal, if SLEEP1_ENABLE keeps 0b, all rails follow the settings in this register function to ramp down or to enter LPM. If both SLEEP1_ENABLE = 1b and SLEEP2_ENABLE2 = 1b, the priority of the rail's **OFF STATE** in the SLEEP1_REG or SLEEP2_REG is higher than the rail's LPM STATE. The rail will only keep alive and enter LPM with both alive settings in the SLEEP1_REG and SLEEP2_REG.

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Table 56. DCDCCTRL1_REG

Address: 0x2B **Description:** Configure the rail to enter Forced PWM Mode (FPWM) at normal operation.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_FPWM	B2_FPWM	B3_FPWM	B4_FPWM	Reserved			
Read/Write	RW	RW	RW	RW	RO	RO	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_FPWM	0b = PSKIP mode 1b = Forced PWM mode
6	B2_FPWM	0b = PSKIP mode 1b = Forced PWM mode
5	B3_FPWM	0b = PSKIP mode 1b = Forced PWM mode
4	B4_FPWM	0b = PSKIP mode 1b = Forced PWM mode

Table 57. DISCHARGE0_REG

Address: 0x2C **Description:** Enable or disable the rail's output discharged path.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_DISCH_EN	B2_DISCH_EN	B3_DISCH_EN	B4_DISCH_EN	L1_DISCH_EN	L2_DISCH_EN	Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	RO	RO
Default Value	1	1	1	1	1	1	0	0

Bits	Name	Description
7	B1_DISCH_EN	0b = Disable discharged resistor path 1b = Enable discharged resistor path The discharged resistor path will be connected from VOUT to ground with the rail's ENABLE = low level, if the setting of the rail's discharged resistor path enable signal is 1b.
6	B2_DISCH_EN	
5	B3_DISCH_EN	
4	B4_DISCH_EN	
3	LDO1_DISCH_EN	
2	LDO2_DISCH_EN	

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Table 58. DISCHARGE1_REG

Address: 0x2D **Description:** Enable or disable the rail's output discharge path								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_DISCH_SEL		B2_DISCH_SEL		B3_DISCH_SEL		B4_DISCH_SEL	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	1	0	1	0	1

Bits	Name	Description
7:6	B1_DISCH_SEL	B1 output discharge resistor path selection 00b: 4.4Ω, 01b: 9.4Ω, 10b: 18.8Ω, 11b: 37.6Ω
5:4	B2_DISCH_SEL	B2 output discharge resistor path selection 00b: 9.4Ω, 01b: 9.4Ω, 10b: 18.8Ω, 11b: 37.6Ω
3:2	B3_DISCH_SEL	B3 output discharge resistor path selection 00b: 9.4Ω, 01b: 9.4Ω, 10b: 18.8Ω, 11b: 37.6Ω
1:0	B4_DISCH_SEL	B4 output discharge resistor path selection 00b: 4.4Ω, 01b: 9.4Ω, 10b: 18.8Ω, 11b: 37.6Ω

Table 59. DISCHARGE2_REG

Address: 0x2E **Description:** Enable or disable the rail's output discharge path								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDO1_DISCH_SEL		LDO2_DISCH_SEL		Reserved			
Read/Write	RW	RW	RW	RW	RO	RO	RO	RO
Default Value	1	1	0	1	0	0	0	0

Bits	Name	Description
7:6	LDO1_DISCH_SEL	LDO1 output discharge resistor path selection 00b: 20Ω, 01b: 20Ω, 10b: 40Ω, 11b: 80Ω
5:4	LDO2_DISCH_SEL	LDO2 output discharge resistor path selection 00b: 20Ω, 01b: 20Ω, 10b: 40Ω, 11b: 80Ω

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Table 60. DCDCCTRL2_REG

Address: 0x2F
Description: Configure the rail to enter PSKIP mode or LPM mode during normal operation. All regulators will be forced to enter LPM when PMIC is in sleep mode.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_LPM	B2_LPM	B3_LPM	B4_LPM	LDO1_LPM	LDO2_LPM	Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	RO	RO
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_LPM	0b = PSKIP mode 1b = Low Power Mode (LPM mode)
6	B2_LPM	0b = PSKIP mode 1b = LPM mode
5	B3_LPM	0b = PSKIP mode 1b = LPM mode
4	B4_LPM	0b = PSKIP mode 1b = LPM mode
3	LDO1_LPM	0b = PSKIP mode 1b = LPM mode
2	LDO2_LPM	0b = PSKIP mode 1b = LPM mode

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Table 61. B1_TIME0_REG

Address: 0x30
Description: Configure the turn-on delay time and sleep-off delay time of B1 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		B1_ON_DLY			B1_SLEEP_OFF_DLY		
Read/Write	RO	RO	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	B1_ON_DLY	B1 turn-on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B1 will turn on with the setting delay time when PMIC is in the power-up sequence and wake-up sequence.
2:0	B1_SLEEP_OFF_DLY	B1 turn-off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B1 will turn off with the setting delay time when PMIC is in the sleep-off sequence.

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Table 62. B1_TIME1_REG

Address: 0x31
Description: Configure the wake-up delay time and the time slot of B1 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_WAKEUP_DELAY			B1_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	1	1	1	0

Bits	Name	Description
7:5	B1_WAKEUP_DELAY	B1 wake-up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms B1 will turn on with the wake-up delay time when PMIC wakes up from the sleep mode.
4:0	B1_TIME_SLOT	B1 time slot setting for power-up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

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Table 63. B2_TIME0_REG

Address: 0x32
Description: Configure the turn-on delay time and sleep-off delay time of B2 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		B2_ON_DLY			B2_SLEEP_OFF_DLY		
Read/Write	RO	RO	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	B2_ON_DLY	B2 turn-on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B2 will turn on with the setting delay time when PMIC is in the power-up sequence and wake-up sequence.
2:0	B2_SLEEP_OFF_DLY	B2 turn-off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B2 will turn off with the setting delay time when PMIC is in the sleep-off sequence.

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Table 64. B2_TIME1_REG

Address: 0x33
Description: Configure the wake-up delay time and the time slot of B2 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_WAKEUP_DELAY			B2_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	1	0	0

Bits	Name	Description
7:5	B2_WAKEUP_DELAY	B2 wake-up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms B2 will turn on with the wake-up delay time when PMIC wakes up from the sleep mode.
4:0	B2_TIME_SLOT	B2 time slot setting for power-up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

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Table 65. B3_TIME0_REG

Address: 0x34
Description: Configure the turn-on delay time and sleep-off delay time of B3 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		B3_ON_DLY			B3_SLEEP_OFF_DLY		
Read/Write	RO	RO	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	B3_ON_DLY	B3 turns on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B3 will turn on with the setting delay time when PMIC is in the power-up sequence and wake-up sequence.
2:0	B3_SLEEP_OFF_DLY	B3 turns off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B3 will turn off with the setting delay time when PMIC is in the sleep-off sequence.

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Table 66. B3_TIME1_REG

Address: 0x35
Description: Configure the wake-up delay time and the time slot of B3 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B3_WAKEUP_DELAY			B3_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	1

Bits	Name	Description
7:5	B3_WAKEUP_DELAY	B3 wake-up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms B3 will turn on with the wake-up delay time when PMIC wakes up from the sleep mode.
4:0	B3_TIME_SLOT	B3 time slot setting for power-up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

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Table 67. B4_TIME0_REG

Address: 0x36
Description: Configure the turn-on delay time and sleep-off delay time of B4 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		B4_ON_DLY			B4_SLEEP_OFF_DLY		
Read/Write	RO	RO	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	B4_ON_DLY	B4 turn-on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B4 will turn on with the setting delay time when PMIC is in the power-up sequence and wake-up sequence.
2:0	B4_SLEEP_OFF_DLY	B4 turn-off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B4 will turn off with the setting delay time when PMIC is in the sleep-off sequence.

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Table 68. B4_TIME_REG1

Address: 0x37 **Description:** Configure the wake-up delay time and the time slot of B4 rail.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B4_WAKEUP_DELAY			B4_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	1	1	0	0	0	0	1

Bits	Name	Description
7:5	B4_WAKEUP_DELAY	B4 wake-up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms B4 will turn on with the wake-up delay time when PMIC wakes up from the sleep mode.
4:0	B4_TIME_SLOT	B4 time slot setting for power-up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 69. MANUFACTURE_ID_REG

Address: 0x38 **Description:** Show the Manufacturer ID.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MANUFACTURER_ID				EFUSE_VERSION_NUM			
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default Value	0	0	1	0	0	0	0	1

Bits	Name	Description
7:4	MANUFACTURER_ID	Manufacturer ID number = 0x02 (Fixed Code).
3:0	EFUSE_VERSION_NUM	EFUSE revision number. [3:0] = EFUSE code version number (EFUSE number)

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Table 70. LDO1_TIME0_REG

Address: 0x39
Description: Configure the turn-on delay time and sleep-off delay time of LDO1 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		LDO1_ON_DLY			LDO1_SLEEP_OFF_DLY		
Read/Write	RO	RO	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	LDO1_ON_DLY	LDO1 turn-on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms LDO1 will turn on with the setting delay time when PMIC is in the power-up sequence and wake-up sequence.
2:0	LDO1_SLEEP_OFF_DLY	LDO1 turn-off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms LDO1 will turn off with the setting delay time when PMIC is in the sleep-off sequence.

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Table 71. LDO1_TIME1_REG

Address: 0x3A
Description: Configure the wake-up delay time and the time slot of LDO1 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDO1_WAKEUP_DELAY			LDO1_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	1

Bits	Name	Description
7:5	LDO1_WAKEUP_DELAY	LDO1 wake-up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms LDO1 will turn on with the wake-up delay time when PMIC wakes up from the sleep mode.
4:0	LDO1_TIME_SLOT	LDO1 time slot setting for power-up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

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Table 72. LDO2_TIME0_REG

Address: 0x3B
Description: Configure the turn-on delay time and sleep-off delay time of LDO2 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		LDO2_ON_DLY			LDO2_SLEEP_OFF_DLY		
Read/Write	RO	RO	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	LDO2_ON_DLY	LDO2 turn-on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms LDO2 will turn on with the setting delay time when PMIC is in the power-up sequence and wake-up sequence.
2:0	LDO2_SLEEP_OFF_DLY	LDO2 turn-off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms LDO2 will turn off with the setting delay time when PMIC is in the sleep-off sequence.

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Table 73. LDO2_TIME1_REG

Address: 0x3C
Description: Configure the wake-up delay time and the time slot of LDO2 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDO2_WAKEUP_DELAY			LDO2_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	1

Bits	Name	Description
7:5	LDO2_WAKEUP_DELAY	LDO2 wake-up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms LDO2 will turn on with the wake-up delay time when PMIC wakes up from the sleep mode.
4:0	LDO2_TIME_SLOT	LDO2 time slot setting for power-up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

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Table 74. PWRDIS_REG

Address: 0x3D **Description:** Configure the delay time of the PWRDIS signal.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved					PWRDIS_DELAY_TIME		
Read/Write	RO	RO	RO	RO	RO	RW	RW	RW
Default Value	0	0	0	0	0	1	1	1

Bits	Name	Description
2:0	PWRDIS_DELAY_TIME	PMIC will enter power-off sequence with the delay time after the low-level detected PWRDIS signal. 000b = 0ms 001b = 0.5ms 010b = 1.0ms 011b = 2.0ms 100b = 4.0ms 101b = 8.0ms 110b = 16ms 111b = disable PWRDIS function

Table 75. PRODUCT_ID_REG

Address: 0x3E **Description:** Show the PRODUCT_ID.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRODUCT_ID							
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default Value	0	1	0	0	0	1	1	1

Bits	Name	Description
7:0	PRODUCT_ID	Product ID number.

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Table 76. REVISION_NUMBER_REG

Address: 0x3F **Description:** Show the REVISION_NUMBER.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ALL LAYER NUMBER				METAL NUMBER			
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default Value	1	0	1	0	0	0	0	1

Bits	Name	Description
7:4	ALL LAYER NUMBER	Record the all layer change times. 0xA = 1 time 0xB = 2 times 0xC = 3 times … 0xF = 6 times After 7 times, it will reset back to 0xA.
3:0	METAL NUMBER	Record the metal change times for all layer change. 0x1 = 1 time 0x2 = 2 times 0x3 = 3 times …. 0xF = 15 times After 16 times, it will reset back to 0x0.

Table 77. TOP_CTRL_REG

Address: 0x40 **Description:** TOP circuit: PUSHPULL_EN, SYSMON_EN, SYSWARN_EN and VOUTLOW_MASK setting. (Read/write available only when the PMIC enters hidden mode)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reversed			VOUTLOW_MASK	Reserved			
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default Value	0	1	1	1	--	--	--	--

Bits	Name	Description
4	VOUTLOW_MASK	0b = Disable 1b = Enable It will not check low VOUT, if VOUTLOW_MASK = 1b.

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Table 78. B3_REAL_VID_REG

Address: 0x41
Description: This register will show Buck3 real VID selection, which is used to define Buck3 VOUT = B3_SEL or B3_DVS_SEL.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B3_REAL_VID							Reserved
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default Value	--	--	--	--	--	--	--	--

Bits	Name	Description
7:1	B3_REAL_VID	Read back to confirm B3 VID value: 0000000b = 0.5V 0000001b = 0.51V 0000010b = 0.52V 0000011b = 0.53V … … 1001111b = 1.29V 1010001b ~ 1111111b = 1.30V

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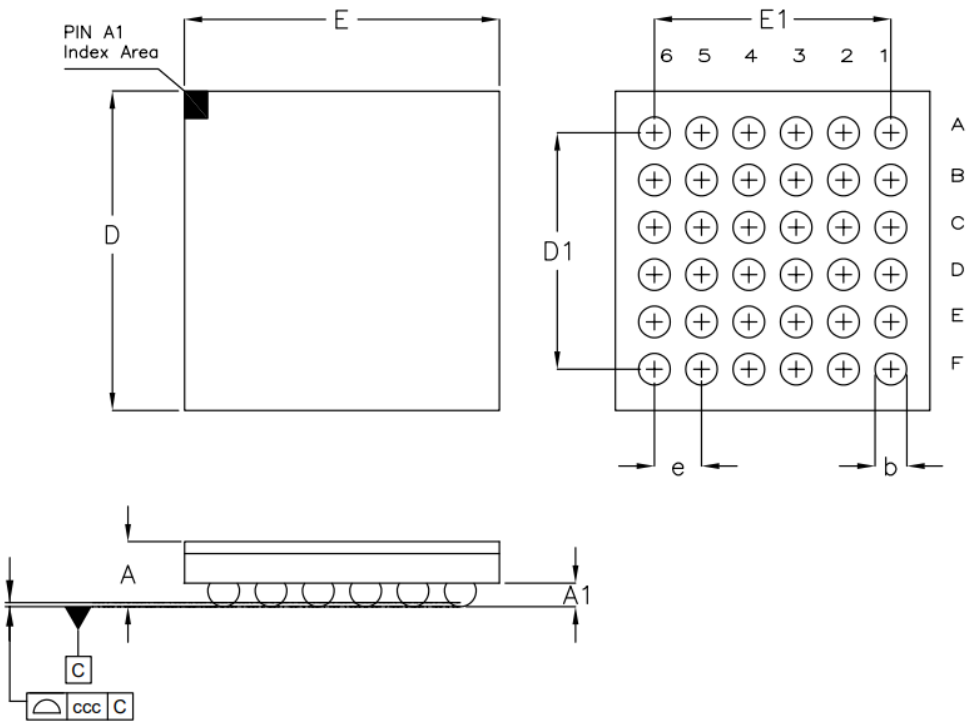
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.660	2.740	0.105	0.108
D1	2.000		0.079	
E	2.620	2.700	0.103	0.106
E1	2.000		0.079	
e	0.400		0.016	
ccc	0.020		0.001	

36B WL-CSP 2.66x2.70 Package (BSC)

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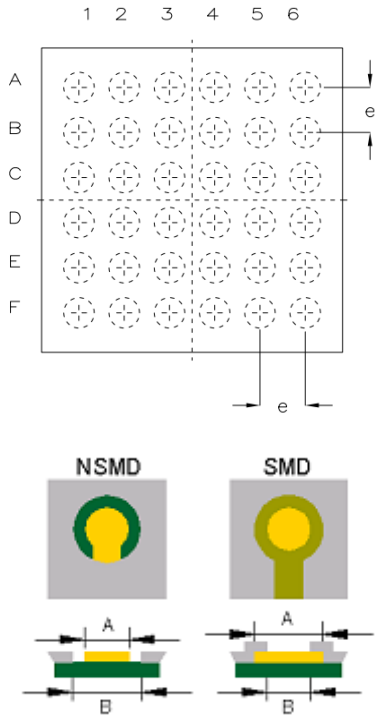
19 Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.66x2.70-36(BSC)	36	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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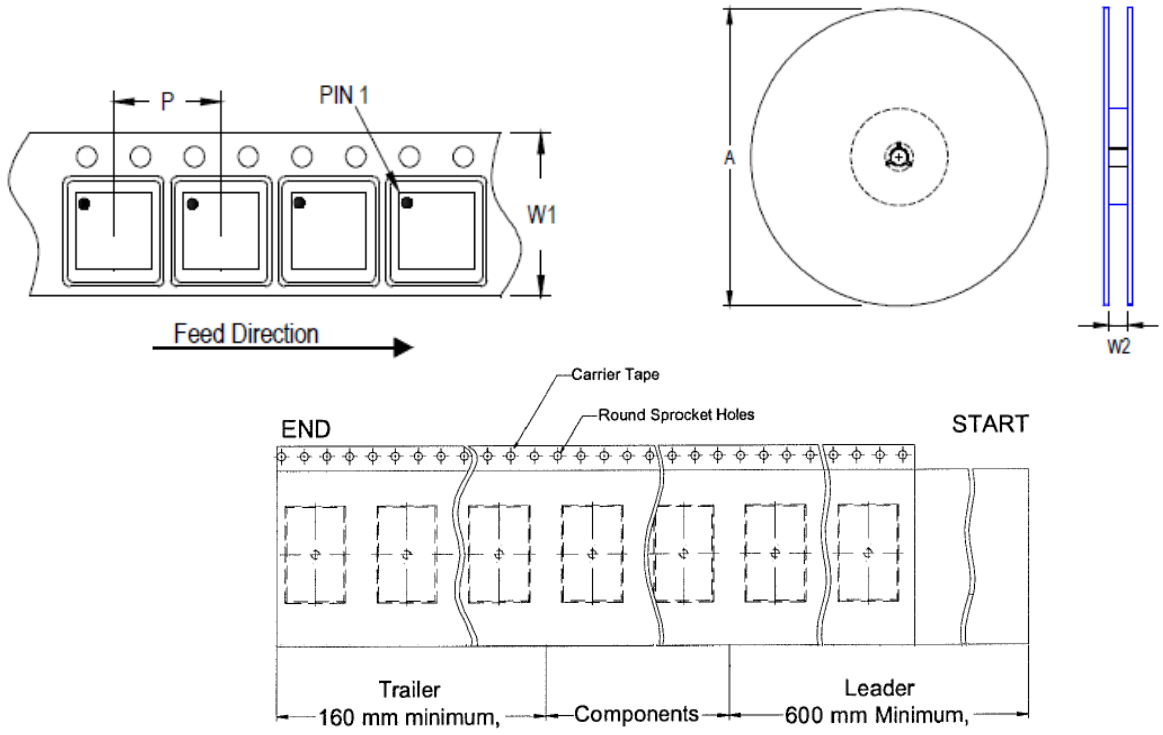
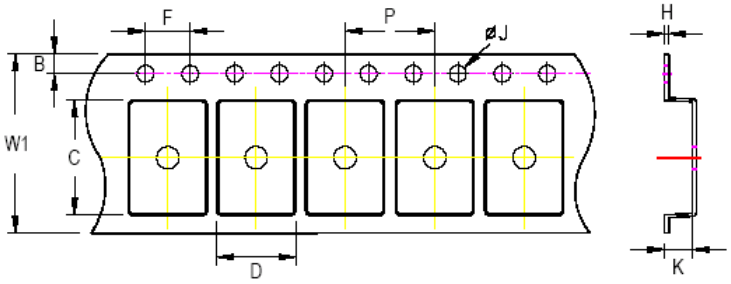
20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
WL-CSP 2.66x2.70	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.7mm	0.8mm	0.6mm

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20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	Reel 7”	4	12 inner boxes per outer box
2	Packing by Anti-Static Bag	5	Outer box **Carton A**
3	3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 2.66x2.70	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

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20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2024/8/8	Final	
01	2025/2/21	Modify	*Ordering Information on page 1* *Operation on page 30* *Application Information on page 42, 43, 44, 45* *Functional Register Description on page 87* *Packing Information on page 106*

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