Smart Power-Management Integrated Circuit for Camera Module Application

General Description

The RT5112A device is a smart power management IC which includes two low-quiescent-current HCOT Buck converters and four high PSRR low dropout regulators (LDO). One can control the channel power sequence, output voltage level and DVS slew rate by setting registers via I^2C interface. The output voltage OVP/UVP, OCP and OTP protection are built in the RT5112A. The RT5112A is available in a WL-CSP-25B 2.2x2.3 (BSC) package.

Applications

- Camera Module
- Optical Module
- SSD

Ordering Information

RT5112A□

Package Type
WSC : WL-CSP-25B 2.2x2.3 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

System Control

- **Hardware Enable Pin**
- **I^2C Controlled Interface**
- **Programmable Channel Power Sequence**
- **IRQ Output for Indication**
- **Over-Voltage Protection**
- **Under-Voltage Protection**
- **Over-Current Protection**
- **Over-Temperature Protection**
- **Available in a WL-CSP-25B 2.2x2.3 (BSC) Package**

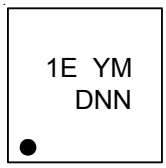
Two High Efficiency Buck Converters

- **Wide 2.5V to 5.5V Operating Input Range**
- **Programmable Output Voltage from 0.6V to 3.3V by 12.5mV/Step**
- **Maximum Continuous Load Current : 1.2A**
- **HCOT Control Operation**
- **Low Quiescent Current**

Four Low Dropout Regulators

- **Wide 1.9V to 5.5V Operating Input Range**
- **Programmable Output Voltage from 0.6V to 3.775V by 25mV/Step**
- **High PSRR : 70dB @ 1kHz, 40dB @ 100kHz with LDO1/LDO2**
- **High PSRR : 50dB @ 1kHz, 40dB @ 10kHz with LDO3/LDO4**
- **300mA Low Dropout Voltage Regulators**
- **Low Quiescent Current**

Marking Information

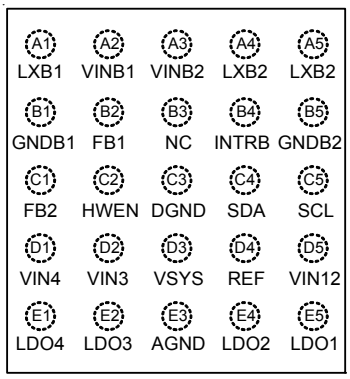


1E : Product Code

YMDNN : Date Code

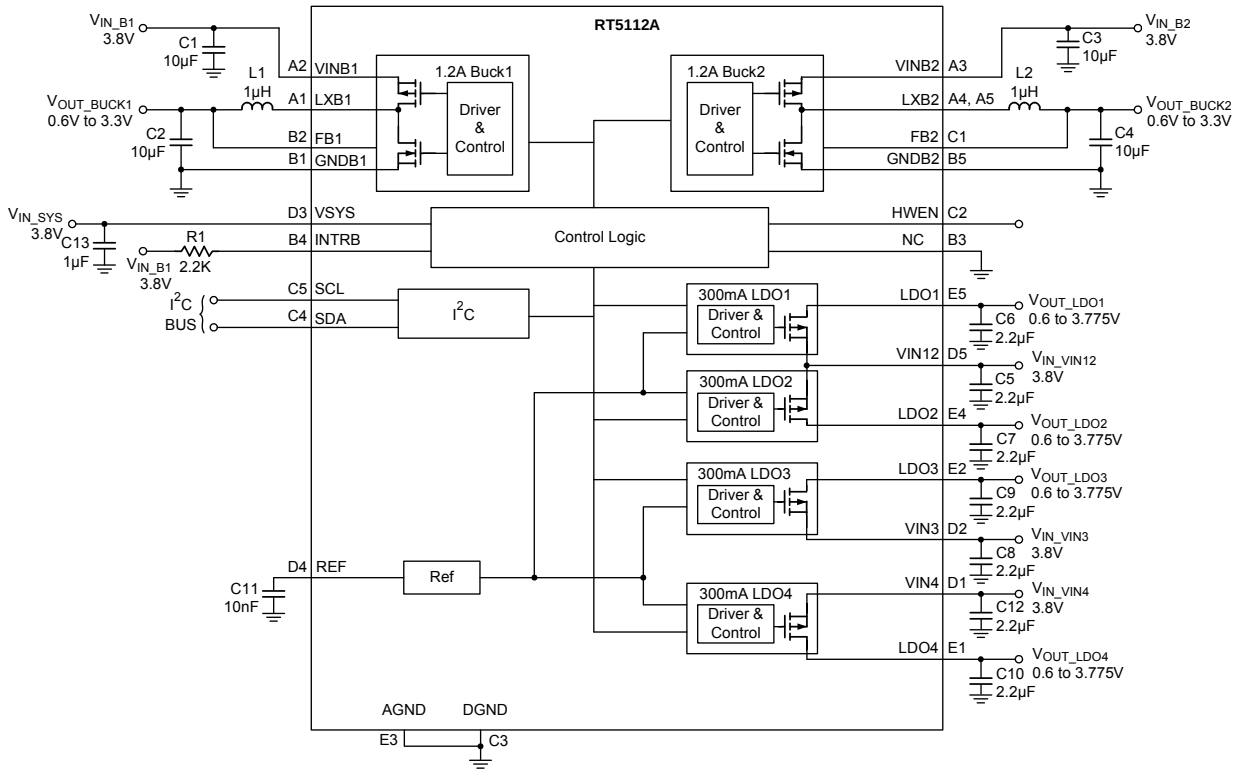
Pin Configuration

(TOP VIEW)



WL-CSP-25B 2.2 x 2.3 (BSC)

Typical Application Circuit



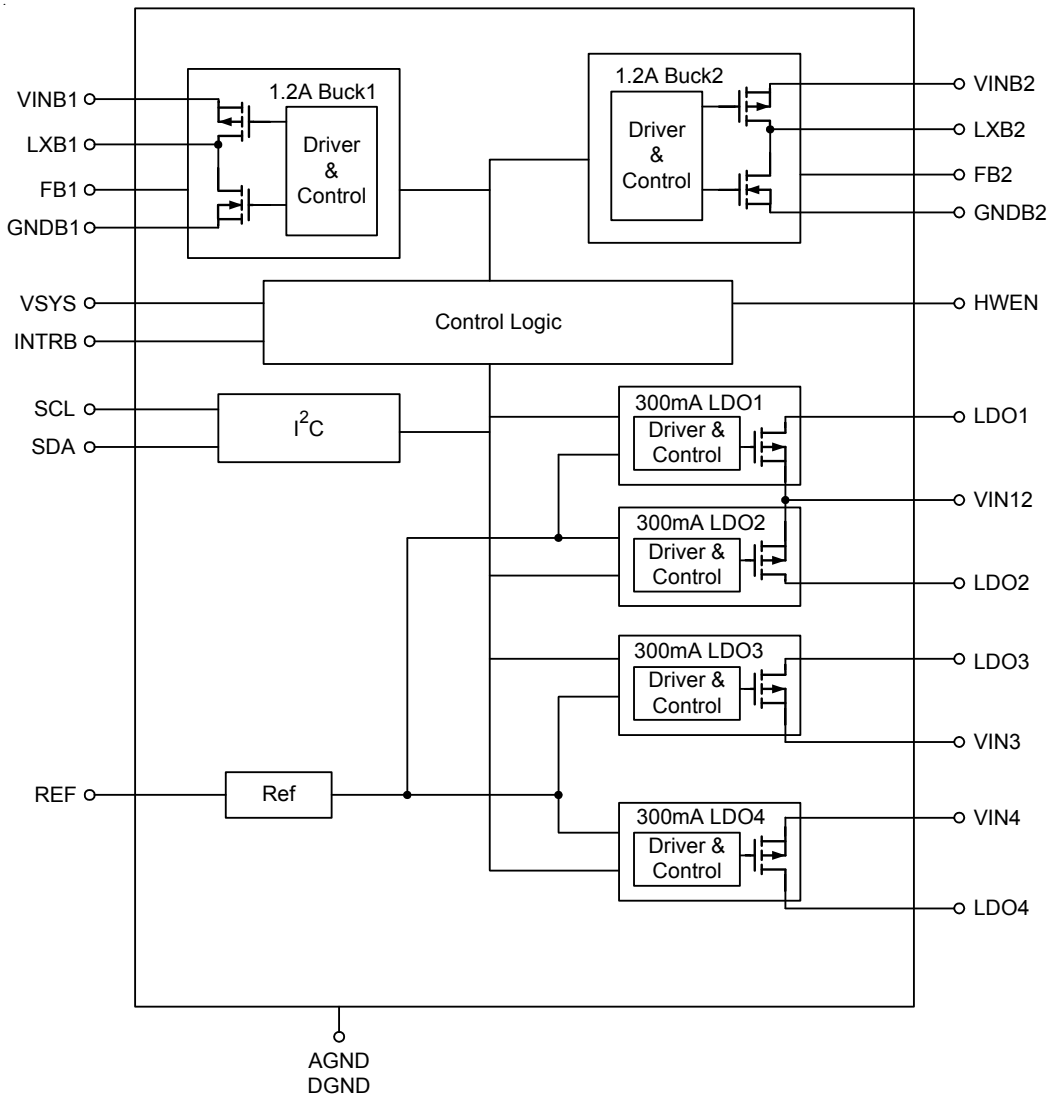
Component List of Evaluation Board

Reference	Qty	Part Number	Description	Package	Manufacturer
C1, C2, C3, C4	1	JMK105CBJ106MV-F	10µF/X5R/6.3V	0402	TAIYO YUDEN
C5, C8, C12	1	JMK105BJ225KV-F	2.2µF/X5R/6.3V	0402	TAIYO YUDEN
C6, C7, C9, C10	1	GRM033R60J225ME47D	2.2µF/X5R/6.3V	0201	MURATA
C11	1	LMK105BJ103KV-F	10nF/X5R/6.3V	0402	TAIYO YUDEN
C13	1	LMK063BBJ105MPLF	1µF/X5R/10V	0201	TAIYO YUDEN
L1, L2	1	MEKK2016T1R0M	1µH/3.1A/50mΩ	2016	TAIYO YUDEN

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	LXB1	Buck1 switch output. Connect with a wide PCB trace.
A2	VINB1	Supply voltage input of Buck1. The IC operates from a 2.5V to 5.5V input rail. Requires a 10μF ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.
A3	VINB2	Supply voltage input of Buck2. The IC operates from a 2.5V to 5.5V input rail. Requires a 10μF ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.
A4, A5	LXB2	Buck2 switch output. Connect with a wide PCB trace.
B1	GNDB1	Buck1 power ground.
B2	FB1	Feedback of Buck1. Directly connect the Buck1's output to this pin.
B3	NC	This pin should connect to ground.
B4	INTRB	Interrupt output. Open drain output. When interrupt happens, interrupt pin is pulled down.
B5	GNDB2	Buck2 power ground.
C1	FB2	Feedback of Buck2. Directly connect the Buck2's output to this pin.
C2	HWEN	Chip enable control input.
C3	DGND	Digital ground.
C4	SDA	I^2C data pin.
C5	SCL	I^2C clock signal input.
D1	VIN4	LDO4 power supply input. Requires a 2.2μF ceramic capacitor to decouple the input rail.
D2	VIN3	LDO3 power supply input. Requires a 2.2μF ceramic capacitor to decouple the input rail.
D3	VSYS	System analog power supply. Requires a 1uF ceramic capacitor to decouple the input rail. It also connected to V_{INB} externally.
D4	REF	Internal reference output, require a 10nF decouple capacitor.
D5	VIN12	LDO1 and 2 power supply input. Requires a 2.2μF ceramic capacitor to decouple the input rail.
E1	LDO4	LDO4 output. Requires a 2.2μF ceramic decouple capacitor.
E2	LDO3	LDO3 output. Requires a 2.2μF ceramic decouple capacitor.
E3	AGND	Analog ground.
E4	LDO2	LDO2 output. Requires a 2.2μF ceramic decouple capacitor.
E5	LDO1	LDO1 output. Requires a 2.2μF ceramic decouple capacitor.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VSYS, VINB1, VINB2, VIN12, VIN3, VIN4, LDO1, LDO2, LDO3, LDO4, FB1, FB2, REF, SCL, SDA, HWEN, INTRB ---------- –0.3V to 6.5V
- LXB1, LXB2 (< 20ns) ---------- –2V to 9V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-25B 2.2x2.3 (BSC) ---------- 3.05W
- Package Thermal Resistance (Note 2)
  WL-CSP-25B 2.2x2.3 (BSC), θ_{JA} ---------- 32.7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage V_{IN_B1}, V_{IN_B2}, V_{SYS} ---------- 2.5V to 5.5V
- Supply Voltage V_{IN_VIN12}, V_{IN_VIN3}, V_{IN_VIN4} ---------- 1.9V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System Parameter						
Quiescent Current	I_{QTATOL}	HWEN = H, V_{IN_SYS} = V_{IN_B1} = V_{IN_B2} = V_{IN_VIN12} = V_{IN_VIN3} = V_{IN_VIN4} = 3.8V, LDO/Buck1/Buck2 on, no load, automode –40°C to 85°C	--	107	138	µA
	I_{QLDO}	HWEN = H, V_{IN_SYS} = V_{IN_VIN12} = V_{IN_VIN3} = V_{IN_VIN4} = 3.8V, LDO on, no load, automode	--	95	118	
	I_{QBASE}	HWEN = H, V_{IN_SYS} = V_{IN_B1} = V_{IN_B2} = V_{IN_VIN12} = V_{IN_VIN3} = V_{IN_VIN4} = 3.8V, all power regulators are off	--	7	10	
	I_{QBUCK1}	HWEN = H, V_{IN_SYS} = V_{IN_B1} = 3.8V, Buck1 on, no load, automode	--	13	20	
	I_{QBUCK2}	HWEN = H, V_{IN_SYS} = V_{IN_B2} = 3.8V, Buck2 on, no load, automode	--	13	20	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Leakage Current	I_{LEAK}	Leak current, HWEN = H, V_{IN_SYS} = V_{IN_B1} = V_{IN_B2} = V_{IN_VIN12} = V_{IN_VIN3} = V_{IN_VIN4} = 2.5V to 5.5V, –40°C to 85°C	--	--	1.5	μA
V_{SYS} Under-Voltage Lockout Threshold Rising	UVLO		--	2.35	2.45	V
Hysteresis Voltage of UVLO	UVLO_H		--	100	--	mV
HWEN Control						
HWEN Low Level Input Voltage	V_{IL}		--	--	0.4	V
HWEN High Level Input Voltage	V_{IH}		1.2	--	--	V
HWEN Pull Down Resistor	R_{EN}		--	1	-	MΩ
Step Down Converter Buck1 (V_{IN_B1} = 3.8V, C1 = C2 = 10μF, L1 = 1μH)						
Input Voltage Range	V_{IN_B1}		2.5	--	5.5	V
Output Voltage Range	V_{OUT_BUCK1}		0.6	--	3.3	V
Output Voltage Step			--	12.5	--	mV
Output Voltage Accuracy	$V_{OUT\_ACCBUCK1}$	All output range of V_{OUT_BUCK1}, I_{OUT} = $I_{OUT(MAX)}$	–2	--	2	%
Switching Frequency	f_{SW_BUCK1}	V_{OUT_BUCK1} = 1.1V, operating under CCM	2	2.5	3	MHz
P-Channel MOSFET On Resistance	$R_{ON\_HG\_BUCK1}$	From VINB1 pin to LXB1 pin	--	150	200	mΩ
N-Channel MOSFET On Resistance	$R_{ON\_LG\_BUCK1}$	From LXB1 pin to GNDB1 pin	--	70	140	mΩ
Maximum Duty Cycle	D_{MAX_BUCK1}		--	--	100	%
Output Discharge Resistor	R_{DIS_BUCK1}		80	100	140	Ω
Over-Voltage Rising Threshold Detection	$OVP_{\_R\_BUCK1}$		--	V_{OUT_BUCK1} x 120%	--	V
Over-Voltage Falling Threshold Detection	$OVP_{\_F\_BUCK1}$		--	V_{OUT_BUCK1} x 109%	--	V
Under-Voltage Rising Threshold Detection	$UVP_{\_R\_BUCK1}$		--	V_{OUT_BUCK1} x 92%	--	V
Under-Voltage Falling Threshold Detection	$UVP_{\_F\_BUCK1}$		--	V_{OUT_BUCK1} x 80%	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FB1 Leakage Current	I_{FB1_LK}	Buck1 disable, 0x0B[7] = 0 (Buck1 discharge disable), V_{IN_B1} = 5.5V, V_{LXB1} = 5.5V, V_{FB1} = 5.5V	0	50	100	nA
Switch Leakage Current	I_{LXB1_LK}	Buck1 disable, 0x0B[7] = 0 (Buck1 discharge disable), V_{IN_B1} = 5.5V, V_{LXB1} = 0 or 5.5V	0	--	1	μA
UG Peak Current Limit	$I_{CL\_peak\_B1}$	2.5V ≤ V_{IN_B1} ≤ 5.5V	1.5	2	2.5	A
LG Valley Current Limit	$I_{CL\_valley\_B1}$	V_{IN_B1} = 3.6V	1	1.5	2	A
LG Negative Current Limit	$I_{NCL\_NEG\_B1}$	V_{IN_B1} = 3.6V, CCM	0.5	--	3	A
Minimum On Time	$t_{MIN\_ON\_B1}$	V_{IN_B1} = 3.6V, V_{OUT_BUCK1} = 1.8V	167	200	250	ns
Minimum Off Time	$t_{MIN\_OFF\_B1}$	V_{IN_B1} = V_{OUT_BUCK1} = 3.3V	20	40	60	ns
Step Down Converter Buck2 (V_{IN_B2} = 3.8V, C3 = C4 = 10μF, L2 = 1μH)						
Input Voltage Range	V_{IN_B2}		2.5	--	5.5	V
Output Voltage Range	V_{OUT_BUCK2}		0.6	--	3.3	V
Output Voltage Step			--	12.5	--	mV
Output Voltage Accuracy	$V_{OUT\_ACCBUCK2}$	All output range of V_{OUT_BUCK2}, I_{OUT} = $I_{OUT(MAX)}$	–2	--	2	%
Switching Frequency	f_{SW_BUCK2}	V_{OUT_BUCK2} = 2.85V, operating under CCM	2	2.5	3	MHz
P-Channel MOSFET On Resistance	$R_{ON\_HG\_BUCK2}$	From VINB2 pin to LXB2 pin	--	95	120	mΩ
N-Channel MOSFET On Resistance	$R_{ON\_LG\_BUCK2}$	From LXB2 pin to GNDB2 pin	--	100	130	mΩ
Maximum Duty Cycle	D_{MAX_BUCK2}		--	--	100	%
Output Discharge Resistor	R_{DIS_BUCK2}		80	100	120	Ω
Over-Voltage Rising Threshold Detection	$OVP_{\_R\_BUCK2}$		--	V_{OUT_BUCK2} x 120%	--	V
Over-Voltage Falling Threshold Detection	$OVP_{\_F\_BUCK2}$		--	V_{OUT_BUCK2} x 109%	--	V
Under-Voltage Rising Threshold Detection	$UVP_{\_R\_BUCK2}$		--	V_{OUT_BUCK2} x 92%	--	V
Under-Voltage Falling Threshold Detection	$UVP_{\_F\_BUCK2}$		--	V_{OUT_BUCK2} x 80%	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FB2 Leakage Current	I_{FB2_LK}	Buck2 disable, 0x0B[2] = 0 (Buck2 discharge disable), V_{IN_B2} = 5.5V, V_{LXB2} = 5.5V, V_{FB2} = 5.5V	0	50	100	nA
Switch Leakage Current	I_{LXB2_LK}	Buck2 disable, 0x0B[2] = 0 (Buck 2discharge disable), V_{IN_B2} = 5.5V, V_{LXB2} = 0 or 5.5V	0	--	1	μA
UG Peak Current Limit	$I_{CL\_peak\_B2}$	2.5V ≤ V_{IN_B2} ≤ 5.5V	1.5	2	2.5	A
LG Valley Current Limit	$I_{CL\_valley\_B2}$	V_{IN_B2} = 3.6V	1	1.5	2	A
LG Negative Current Limit	$I_{NCL\_NEG\_B2}$	V_{IN_B2} = 3.6V, CCM	0.5	--	3	A
Minimum On Time	$t_{MIN\_ON\_B2}$	V_{IN_B2} = 3.6V, V_{OUT_BUCK2} = 1.8V	167	200	250	ns
Minimum Off Time	$t_{MIN\_OFF\_B2}$	V_{IN_B2} = V_{OUT_BUCK2} = 3.3V	20	40	60	ns
Low Dropout Voltage Regulator LDO1 and LDO2 (V_{IN_VIN12} = V_{OUT_LDO1}/V_{OUT_LDO2} + 1V, V_{HWEN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 2.2μF, C_{OUT} = 2.2μF)						
Input Voltage Range	V_{IN_VIN12}		1.9	--	5.5	V
Output Voltage Range	V_{OUT_LDO1}/ V_{OUT_LDO2}		0.6	2.8	3.775	V
Output Voltage Step			--	25	--	mV
Maximum Output Current	I_{OUT_LDO1}/ I_{OUT_LDO2}		300	--	--	mA
Soft-Start Time	t_{SS_LDO1}/ t_{SS_LDO2}	Time from V_{OUT_LDO1}/ V_{OUT_LDO2} start rising to 90% nominal value, V_{OUT_LDO1}/ V_{OUT_LDO2} = 2.8V, no load	--	--	150	μs
DC Output Voltage Accuracy	$V_{OUT\_ACCLDO1}$/ $V_{OUT\_ACCLDO2}$	All output range of V_{OUT_LDO1}/ V_{OUT_LDO2}, I_{OUT} = $I_{OUT(MAX)}$	–2	--	2	%
Load Regulation	$V_{LOAD\_REG\_LDO1}$/ $V_{LOAD\_REG\_LDO2}$	I_{OUT} = 0 to $I_{OUT(MAX)}$	–0.5	--	0.5	%
Line Regulation	$V_{LINE\_REG\_LDO1}$/ $V_{LINE\_REG\_LDO2}$	I_{OUT} = 50mA to 300mA, V_{IN_VIN12} = 3.0V to 4.4V, V_O = 2.8V	–0.5	--	0.5	%
Dropout Voltage	$V_{DROPLDO1}$/ $V_{DROPLDO2}$	I_{OUT} = 300mA, V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V (Note 5)	--	--	250	mV
Output Discharge Resistor	R_{DIS_LDO1}/ R_{DIS_LDO2}		--	10	--	Ω
Over-Voltage Rising Threshold Detection	$OVP_{\_R\_LDO1}$/ $OVP_{\_R\_LDO2}$		--	V_{OUT_LDO1}/ V_{OUT_LDO2} x 120%	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Voltage Falling Threshold Detection	$OVP_{\_F\_LDO1}$/ $OVP_{\_F\_LDO2}$		--	V_{OUT_LDO1}/ V_{OUT_LDO2} x 110%	--	V
Under-Voltage Rising Threshold Detection	$UVP_{\_R\_LDO1}$/ $UVP_{\_R\_LDO2}$		--	V_{OUT_LDO1}/ V_{OUT_LDO2} x 90%	--	V
Under-Voltage Falling Threshold Detection	$UVP_{\_F\_LDO1}$/ $UVP_{\_F\_LDO2}$		--	V_{OUT_LDO1}/ V_{OUT_LDO2} x 80%	--	V
Quiescent Current	I_{Q_LDO1}/I_{Q_LDO2}	HWEN = 1.2V, I_{OUT} = 0mA	--	22	27	μA
		HWEN = 0.3V (disable)	--	0.1	1	
Short Circuit Current Limit	I_{sc_LDO1}/ I_{sc_LDO2}		360	--	--	mA
Current Limit	I_{Limt_LDO1}/ I_{Limt_LDO2}	0x01[3:2] = 11 (LDO1 current limit = 360mA), 0x02[3:2] = 11 (LDO2 current limit = 360mA)	360	415	470	mA
Short Protection On Timer	$t_{scp\_ON\_LDO1}$/ $t_{scp\_ON\_LDO2}$		--	2	--	ms
Short Protection Off Timer	$t_{scp\_OFF\_LDO1}$/ $t_{scp\_OFF\_LDO2}$		--	40	--	ms
Low Dropout Voltage Regulator LDO3 and LDO4 (V_{IN_VIN3}/V_{IN_VIN4} = V_{OUT_LDO3}/V_{OUT_LDO4} + 1V, V_{HWEN} = 1.2V, I_{OUT} = 1mA, C_{IN}= 2.2μF, C_{OUT} = 2.2μF)						
Input Voltage Range	V_{IN_VIN3}/ V_{IN_VIN4}		1.9	--	5.5	V
Output Voltage Range	V_{OUT_LDO3}/ V_{OUT_LDO4}		0.6	1.8	3.775	V
Output Voltage Step			--	25	--	mV
Maximum Output Current	I_{OUT_LDO3}/ I_{OUT_LDO4}		300	--	--	mA
Soft-Start Time	t_{SS_LDO3}/ t_{SS_LDO4}	Time from V_{OUT_LDO3} / V_{OUT_LDO4} start rising to 90% nominal value, V_{OUT_LDO3} / V_{OUT_LDO4} = 1.8V, no load	--	--	150	μs
DC Output Voltage Accuracy	$V_{OUT\_ACCLDO3}$/ $V_{OUT\_ACCLDO4}$	All output range of V_{OUT_LDO3} / V_{OUT_LDO4}, I_{OUT} = $I_{OUT(MAX)}$	–2	--	2	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Regulation	$V_{LOAD\_REG\_LDO3}$/ $V_{LOAD\_REG\_LDO4}$	I_{OUT} = 0 to $I_{OUT(MAX)}$	–0.5	--	0.5	%
Line Regulation	$V_{LINE\_REG\_LDO3}$/ $V_{LINE\_REG\_LDO4}$	I_{OUT} = 50mA/300mA, V_{IN_VIN3} / V_{IN_VIN4} = 3.0 to 4.4V, V_O = 1.8V	–0.5	--	0.5	%
Dropout Voltage	$V_{DROPLDO3}$/ $V_{DROPLDO4}$	I_{OUT} = 300mA, V_{OUT_LDO3} / V_{OUT_LDO4} = 1.8V (Note 5)	--	--	150	mV
Output Discharge Resistor	R_{DIS_LDO3}/ R_{DIS_LDO4}		--	10	--	Ω
Over-Voltage Rising Threshold Detection	$OVP_{\_R\_LDO3}$/ $OVP_{\_R\_LDO4}$		--	V_{OUT_LDO3}/ V_{OUT_LDO4} x 120%	--	V
Over-Voltage Falling Threshold Detection	$OVP_{\_F\_LDO3}$/ $OVP_{\_F\_LDO4}$		--	V_{OUT_LDO3}/ V_{OUT_LDO4} x 110%	--	V
Under-Voltage Rising Threshold Detection	$UVP_{\_R\_LDO3}$/ $UVP_{\_R\_LDO4}$		--	V_{OUT_LDO3}/ V_{OUT_LDO4} x 90%	--	V
Under-Voltage Falling Threshold Detection	$UVP_{\_F\_LDO3}$/ $UVP_{\_F\_LDO4}$		--	V_{OUT_LDO3}/ V_{OUT_LDO4} x 80%	--	V
Quiescent Current	I_{Q_LDO3}/I_{Q_LDO4}	HWEN = 1.2V, I_{OUT} = 0mA	--	22	27	μA
		HWEN = 0.3V (disable)	--	0.1	1	
Short Circuit Current Limit	I_{sc_LDO3}/ I_{sc_LDO4}		360	--	--	mA
Current Limit	I_{Limt_LDO3}/ I_{Limt_LDO4}	0x03[3:2] = 11 (LDO3 current limit = 360mA), 0x04[3:2] = 11 (LDO4 current limit = 360mA)	360	415	470	mA
Short Protection On Timer	$t_{scp\_ON\_LDO3}$/ $t_{scp\_ON\_LDO4}$		--	2	--	ms
Short Protection Off Timer	$t_{scp\_OFF\_LDO3}$/ $t_{scp\_OFF\_LDO4}$		--	40	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C Characteristics						
SCL, SDA Low Input Voltage	$V_I{}^2C_{IL}$		--	--	0.4	V
SCL, SDA High Input Voltage	$V_I{}^2C_{IH}$		1.2	--	--	V
SCL, SDA Low Output Voltage	$V_I{}^2C_{OL}$		--	--	0.4	V
I²C CLK Frequency	f_{SCL}		1	--	--	MHz
I²C Work Voltage	$V_I{}^2C_{int}$		--	1.8	--	V
Input Current Each IO Pin	$I_{IN\_I}{}^2C$		−10	--	10	μA
Data Hold Time	$t_{DH\_I}{}^2C$		30	--	--	ns
Data Set-Up Time	$t_{DS\_I}{}^2C$		70	--	--	ns

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

System Characteristics

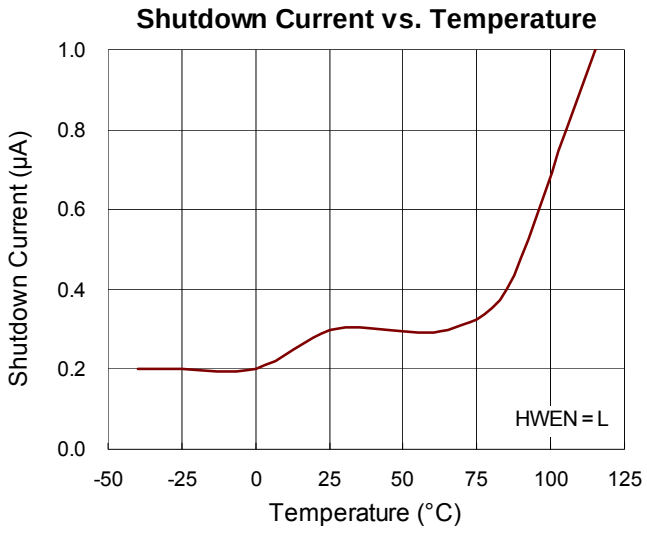
The following system specifications are guaranteed by designed and are not performed in production testing.
(T_A = 25°C, unless otherwise specified.)

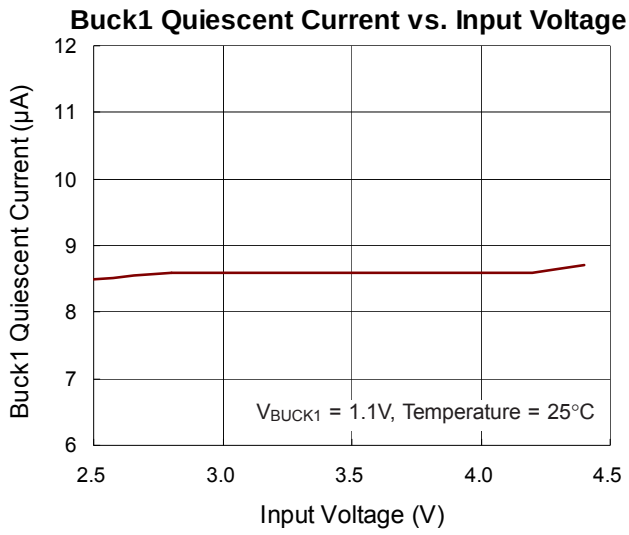
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System Parameter						
Over-Temperature Warning	OTW		115	125	135	°C
Over-Temperature Warning Hysteresis	OTW_H		--	20	--	°C
Over-Temperature Protection	OTP		130	140	150	°C
Over-Temperature Protection Hysteresis	OTP_H	0x0A[4:3] = 01	--	20	--	°C
HWEN Control						
HWEN Turn On Delay	t_{HWEN_ON}	HWEN = H to I²C operation available	--	50	--	μs
HWEN Turn Off Delay	t_{HWEN_OFF}	HWEN = L to I²C operation stop	--	50	--	μs

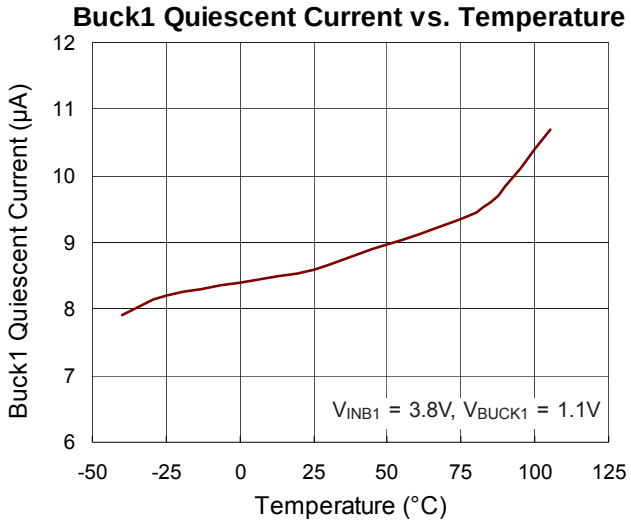
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Step Down Converter Buck1 (V_{IN_B1} = 3.8V, C1 = C2 = 10μF, L1 = 1μH)						
Maximum Output Current	I_{OUT_BUCK1}		1.2	--	--	A
Load Regulation	$V_{LOAD\_REG\_BUCK1}$	CCM, V_{OUT_BUCK1} = 1.1V	--	--	1.5	%
Line Regulation	$V_{LINE\_REG\_BUCK1}$	CCM, I_{OUT} = 50/300/1200mA, V_{OUT_BUCK1} = 1.1V, V_{IN_B1} = 3.0V to 4.4V	--	--	1.5	%
Output Ripple	V_{RIPPLE_BUCK1}	CCM, V_{OUT_BUCK1} = 1.1V, V_{IN_B1} < 4.35V	--	--	10	mV
		PFM, V_{OUT_BUCK1} = 1.1V, V_{IN_B1} < 4.35V	--	30	40	
Soft-Start Time	t_{SS_BUCK1}	0x09[7:6] = 10, time from V_{OUT_BUCK1} = 0V rising to 90% nominal value, V_{OUT_BUCK1} = 1.1V, no load	--	235	--	μs
Load Transient	VTRAN_BUCK1	VOUT_BUCK1 = 1.1V, 20 to 80% IOUT(MAX), 1? s, recovery time < 10? s	--	--	70	μς
Efficiency	Eff_BUCK1	VOUT_BUCK1 = 1.1V, IOUT = 200mA to 600mA	85	--	--	%
Step Down Converter Buck2 (V_{IN_B2} = 3.8V, C3 = C4 = 10μF, L2 = 1μH)						
Maximum Output Current	I_{OUT_BUCK2}		1.2	--	--	A
Load Regulation	$V_{LOAD\_REG\_BUCK2}$	CCM, V_{OUT_BUCK2} = 2.85V	--	--	1.5	%
Line Regulation	$V_{LINE\_REG\_BUCK2}$	CCM, I_{OUT} = 50/300/1200mA, V_{OUT_BUCK2} = 2.85V, V_{IN_B2} = 3.0V to 4.4V	--	--	1.5	%
Output Ripple	V_{RIPPLE_BUCK2}	CCM, V_{OUT_BUCK2} = 2.85 V, V_{IN_B2} < 4.35V	--	--	20	mV
		PFM, V_{OUT_BUCK2} = 2.85V, V_{IN_B2} < 4.35V	--	40	50	
Soft-Start Time	t_{SS_BUCK2}	0x09[7:6] = 10, time from V_{OUT_BUCK2} = 0V rising to 90% nominal value, V_{OUT_BUCK2} = 2.85V, no load	--	607	--	μs
Load Transient	V_{TRAN_BUCK2}	V_{OUT_BUCK2} = 2.85V, 20 to 80% $I_{OUT(MAX)}$, 1μs, recovery time < 10μs	--	--	80	mV
Efficiency	$Eff_{\_BUCK2}$	V_{OUT_BUCK2} = 2.85V, I_{OUT} = 200mA to 600mA	93	--	--	%

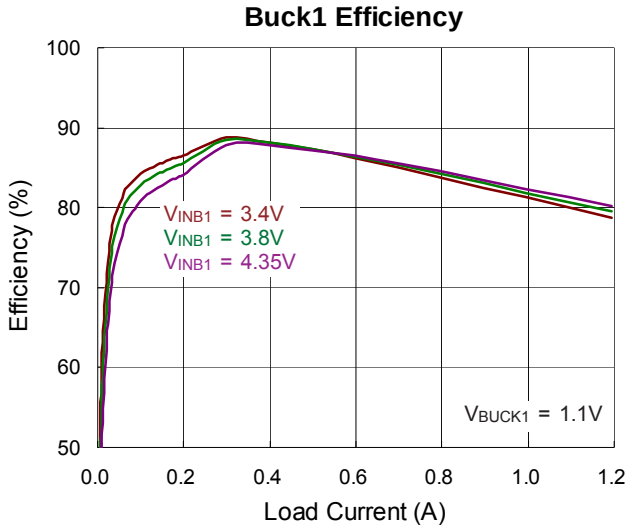
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low Dropout Voltage Regulator LDO1 and LDO2 (V_{IN_VIN12} = V_{OUT_LDO1}/V_{OUT_LDO2} + 1V, V_{HWEN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 2.2μF, C_{OUT} = 2.2μF)						
Output Ripple Voltage	V_{RIPPLE_LDO1}/ V_{RIPPLE_LDO2}	I_{OUT} = 0 to $I_{OUT(MAX)}$, V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V	--	--	10	mV
Load Transient	V_{TRAN_LDO1}/ V_{TRAN_LDO2}	I_{OUT} = 1mA to 150mA, 150mA/μs, V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V	--	--	50	mV
Power Supply Rejection Ratio	$PSRR_{\_LDO1}$/ $PSRR_{\_LDO2}$	V_{IN_VIN12} = 3.4V, f = 1kHz, I_{OUT} = 100mA, V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V	70	--	--	dB
		V_{IN_VIN12} = 3.4V, f = 100kHz, I_{OUT} = 100mA, V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V	40	--	--	
Output Noise Voltage	e_{N_LDO1}/ e_{N_LDO2}	100Hz to 100kHz, I_{OUT} = 100mA, V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V	--	50	--	μV
Low Dropout Voltage Regulator LDO3 and LDO4 (V_{IN_VIN3}/V_{IN_VIN4} = V_{OUT_LDO3}/V_{OUT_LDO4} + 1V, V_{HWEN} = 1.2V, I_{OUT} = 1mA, C_{IN}= 2.2μF, C_{OUT} = 2.2μF)						
Output Ripple Voltage	V_{RIPPLE_LDO3}/ V_{RIPPLE_LDO4}	I_{OUT} = 0 to $I_{OUT(MAX)}$, V_{OUT_LDO3} / V_{OUT_LDO4} = 1.8V	--	--	10	mV
Load Transient	V_{TRAN_LDO3}/ V_{TRAN_LDO4}	I_{OUT} = 1mA to 150mA, 150mA/μs	--	--	50	mV
Power Supply Rejection Ratio	$PSRR_{\_LDO3}$/ $PSRR_{\_LDO4}$	V_{IN_VIN3} / V_{IN_VIN4} = 1.95V, f = 1kHz, I_{OUT} = 100mA, V_{OUT_LDO3}/V_{OUT_LDO4} = 1.8V	50	--	--	dB
		V_{IN_VIN3} / V_{IN_VIN4} = 1.95V, f = 10kHz, I_{OUT} = 100mA, V_{OUT_LDO3}/V_{OUT_LDO4} = 1.8V	40	--	--	
Output Noise Voltage	eN_LDO3/ eN_LDO4	100Hz to 100kHz, I_{OUT} = 100mA, V_{OUT_LDO3}/V_{OUT_LDO4} = 2.8V/1.8V	--	50	--	μV

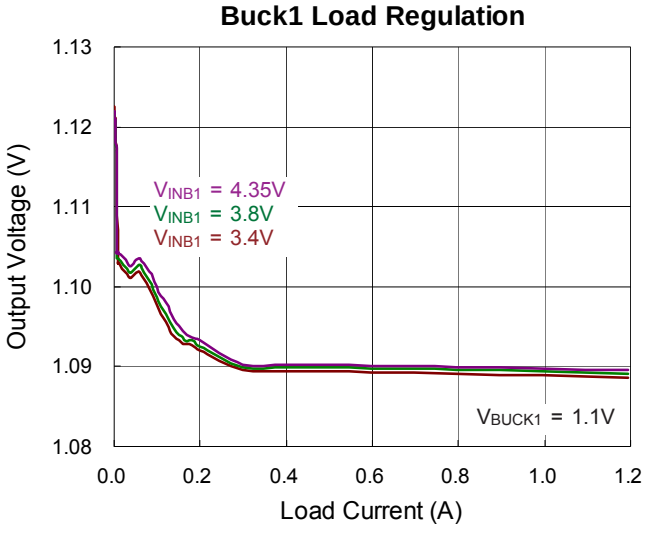
Typical Operating Characteristics

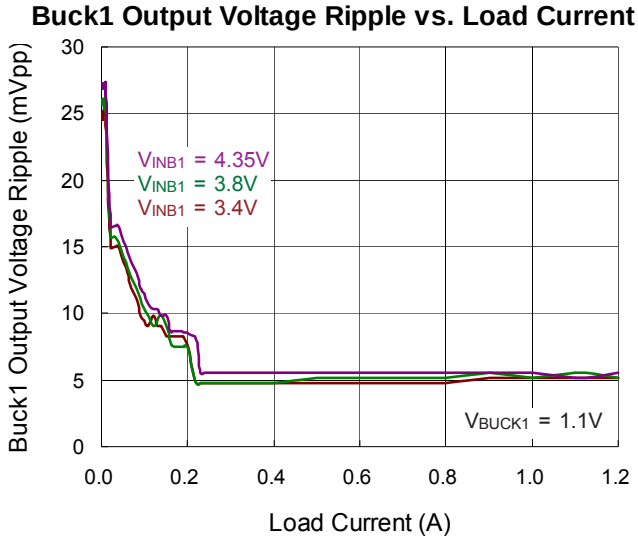




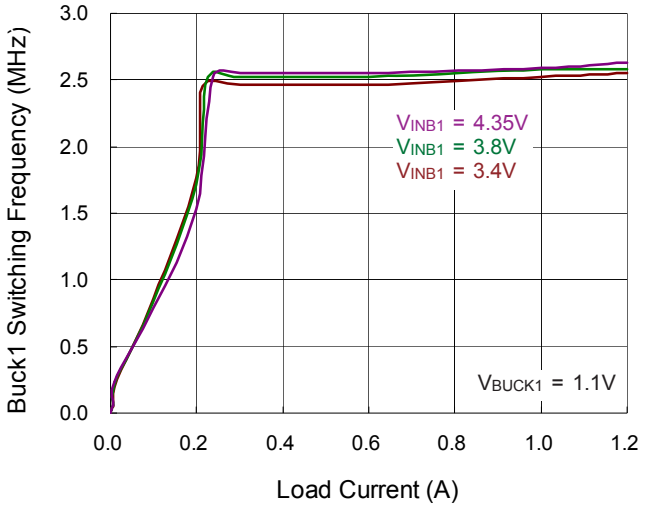




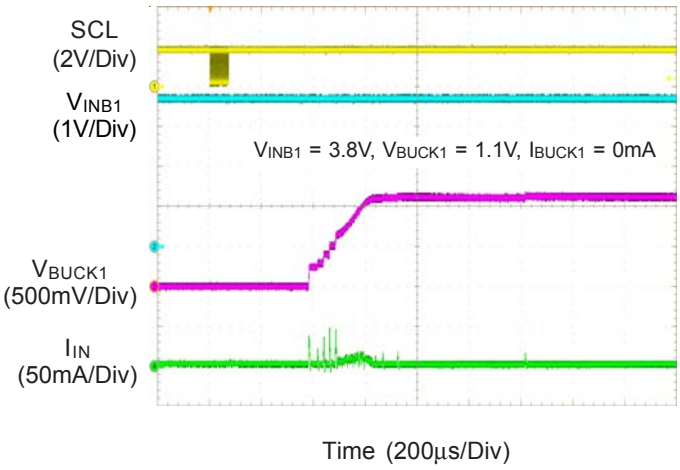




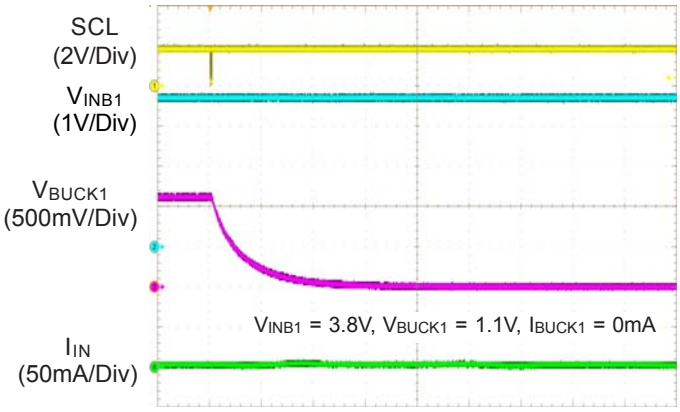
Buck1 Switching Frequency vs. Load Current



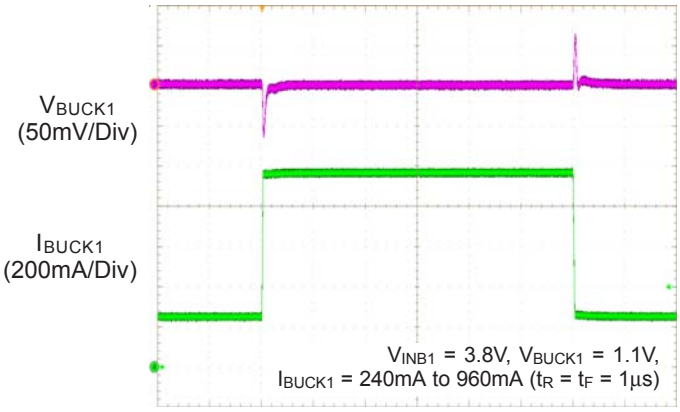
Buck1 Power On



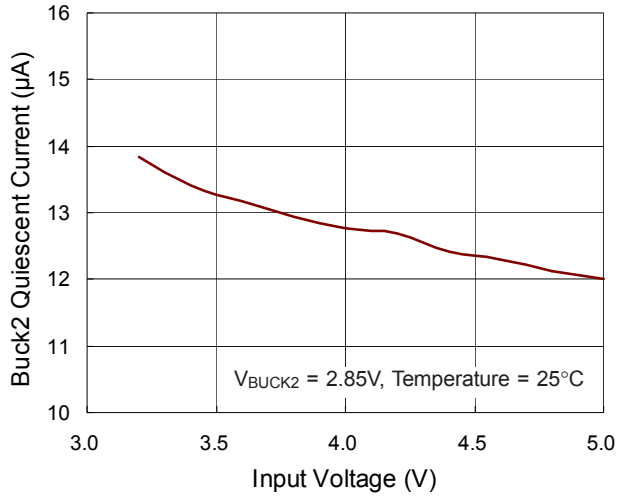
Buck1 Power Off



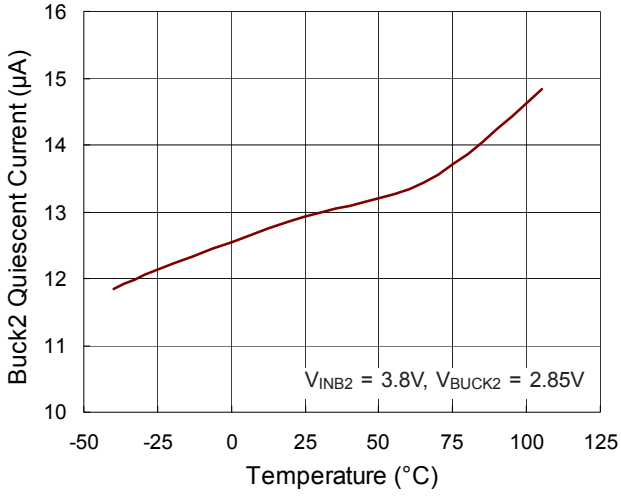
Buck1 Load Transient



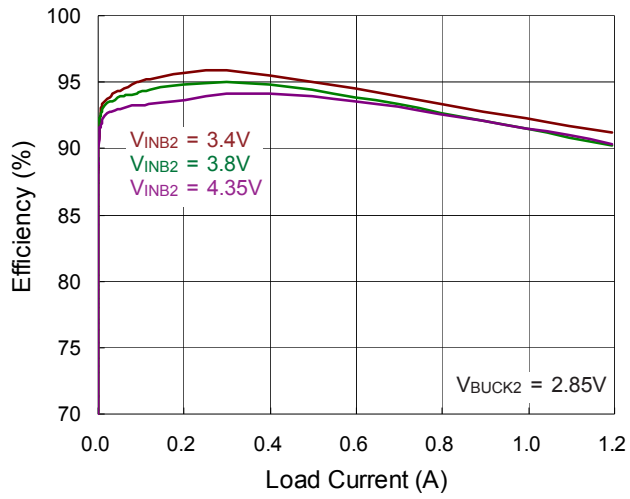
Buck2 Quiescent Current vs. Input Voltage



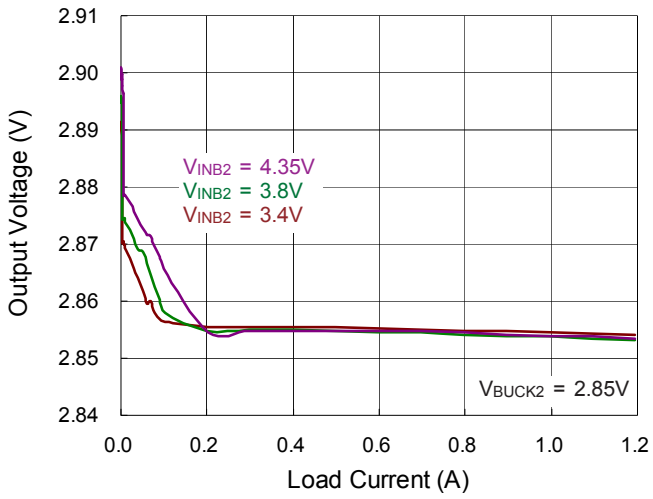
Buck2 Quiescent Current vs. Temperature



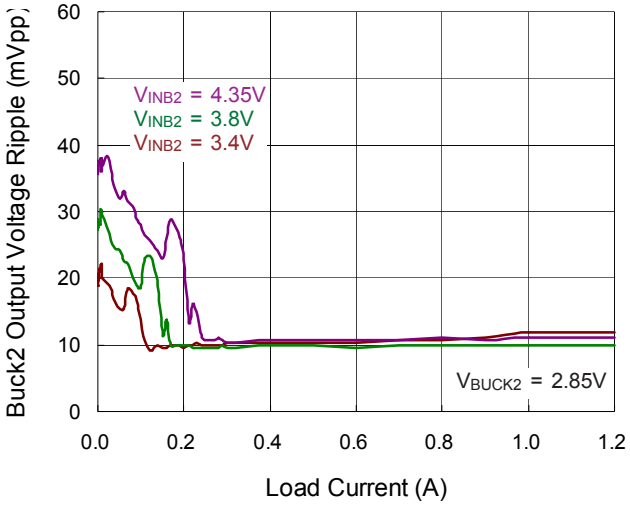
Buck2 Efficiency



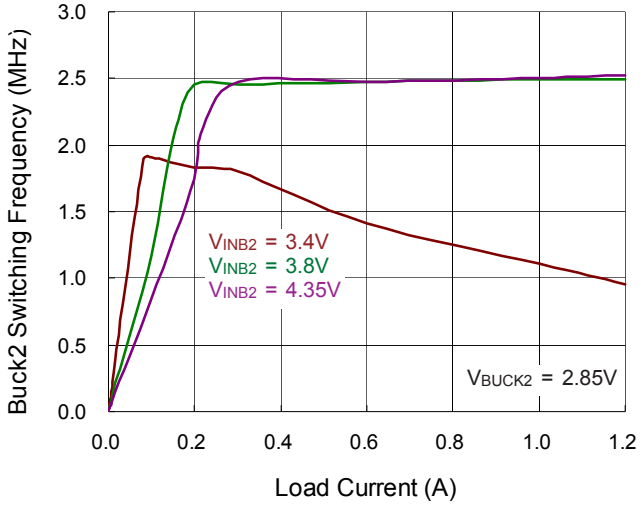
Buck2 Load Regulation



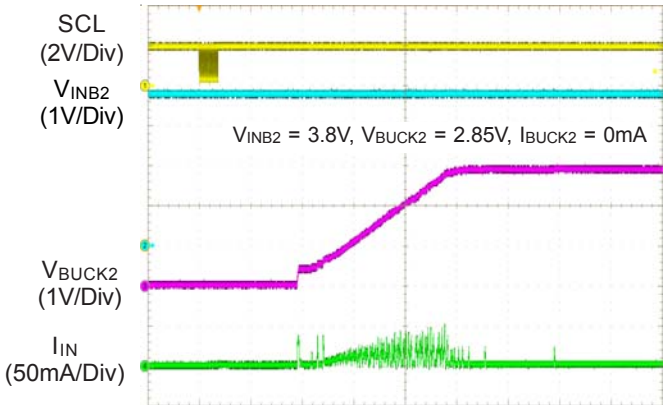
Buck2 Output Voltage Ripple vs. Load Current



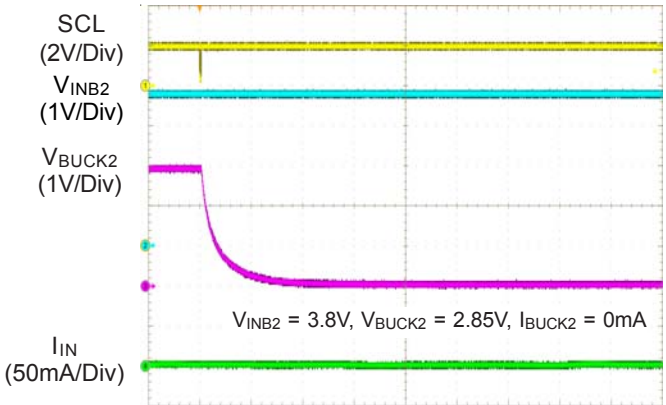
Buck2 Switching Frequency vs. Load Current



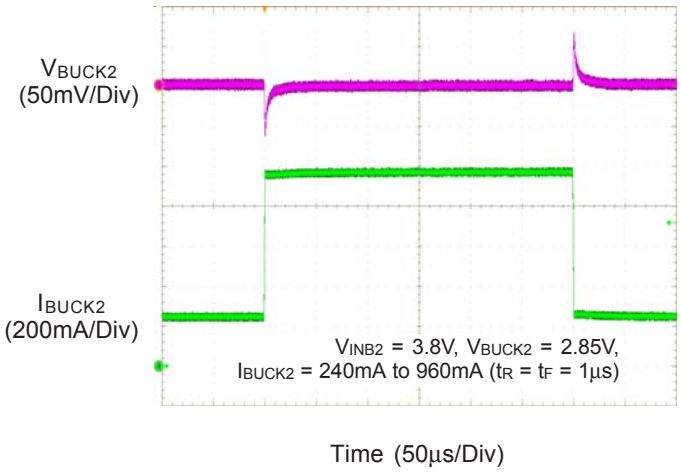
Buck2 Power On



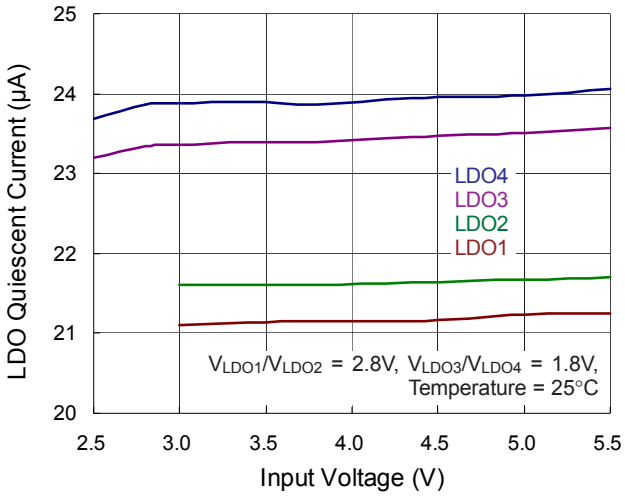
Buck2 Power Off



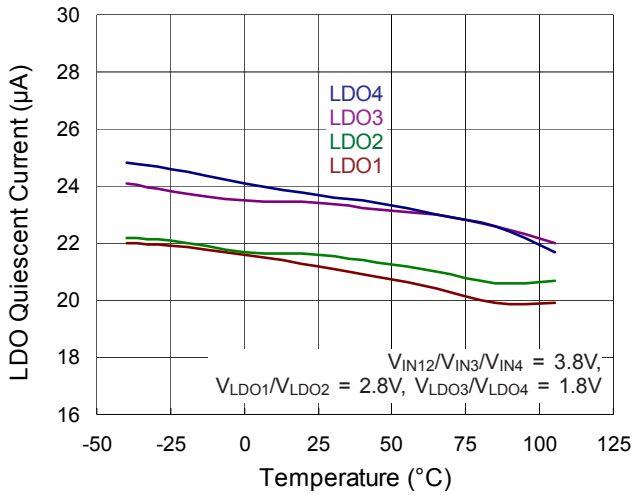
Buck2 Load Transient



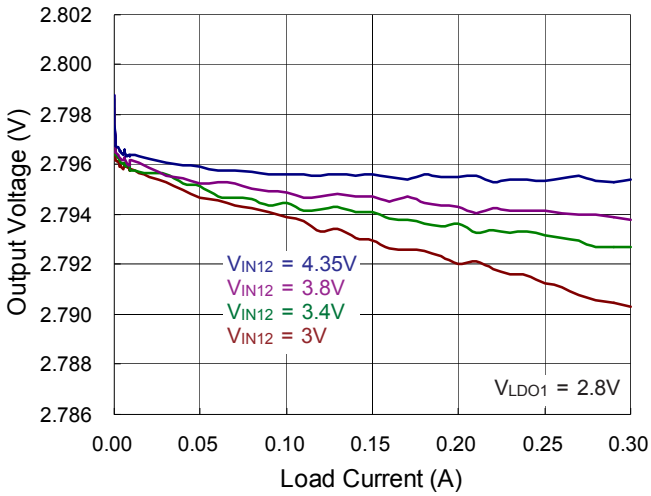
LDO Quiescent Current vs. Input Voltage



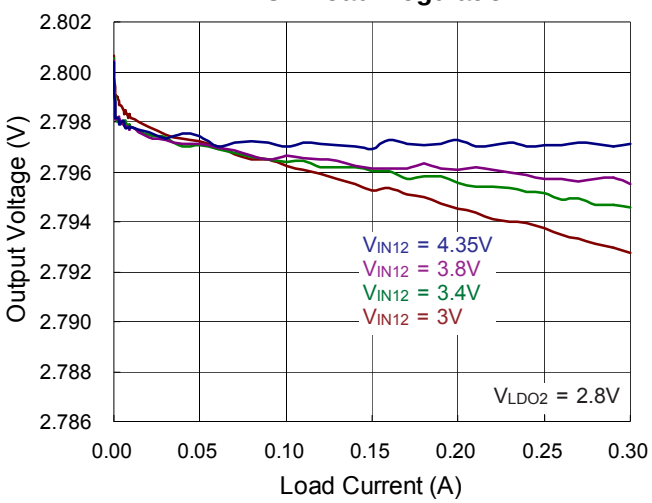
LDO Quiescent Current vs. Temperature



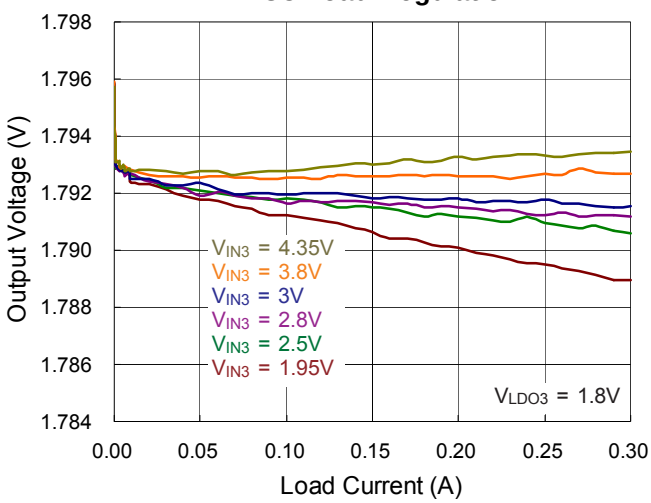
LDO1 Load Regulation



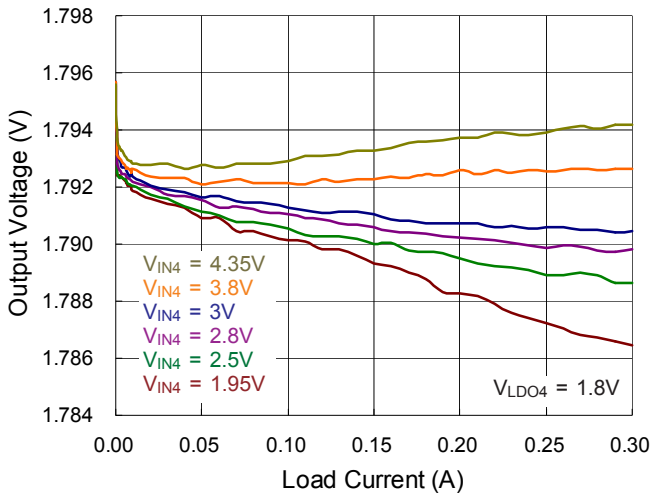
LDO2 Load Regulation



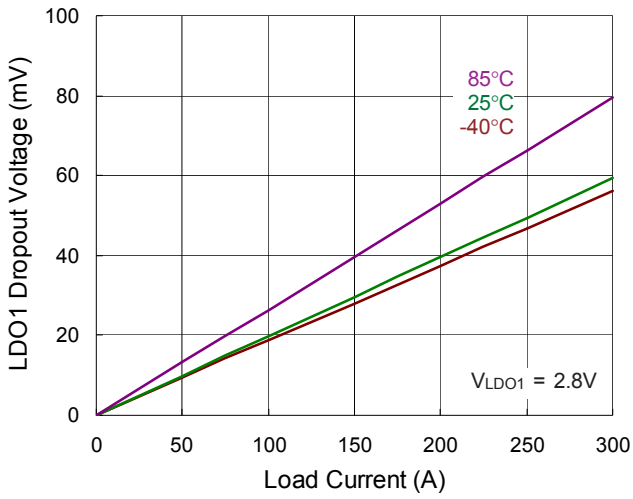
LDO3 Load Regulation



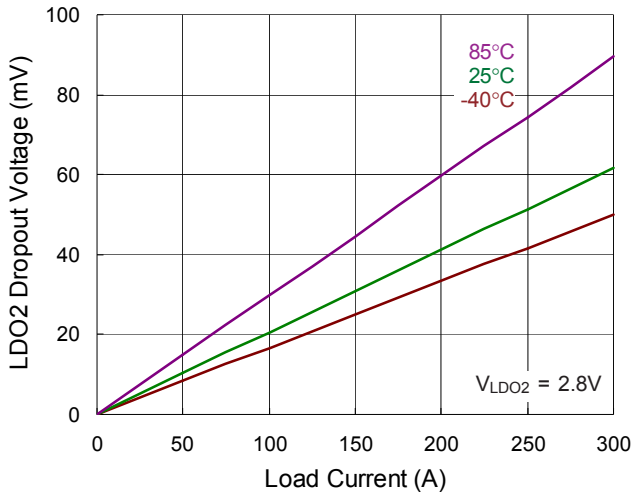
LDO4 Load Regulation



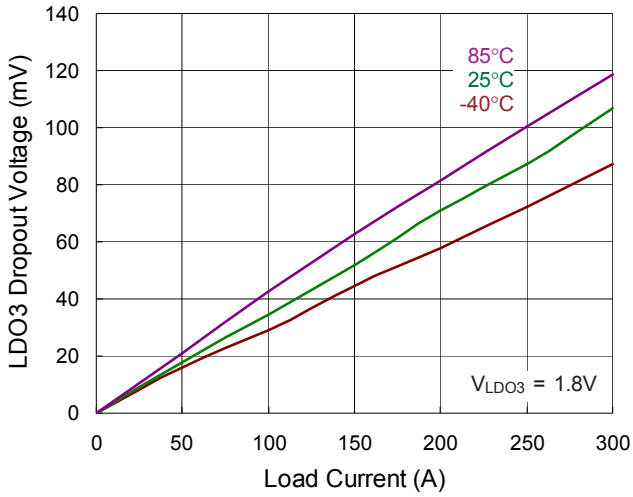
LDO1 Dropout Voltage vs. Load Current



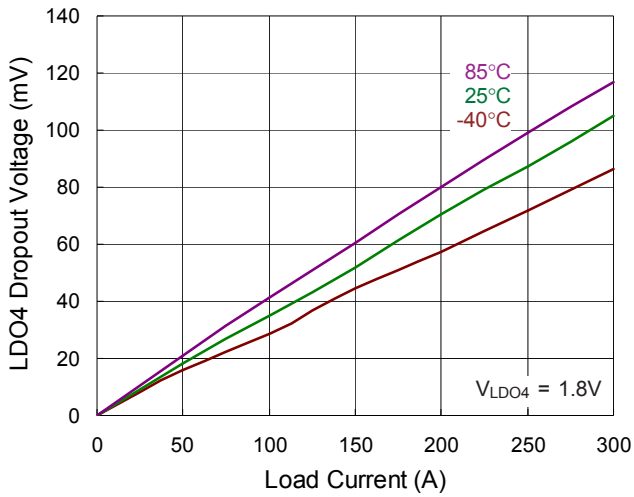
LDO2 Dropout Voltage vs. Load Current



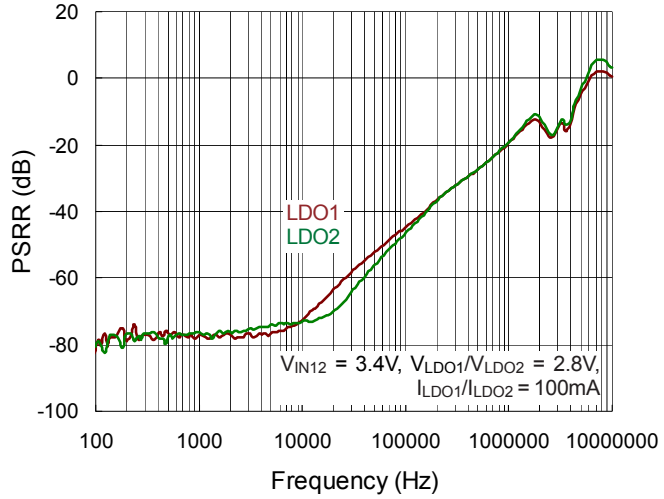
LDO3 Dropout Voltage vs. Load Current



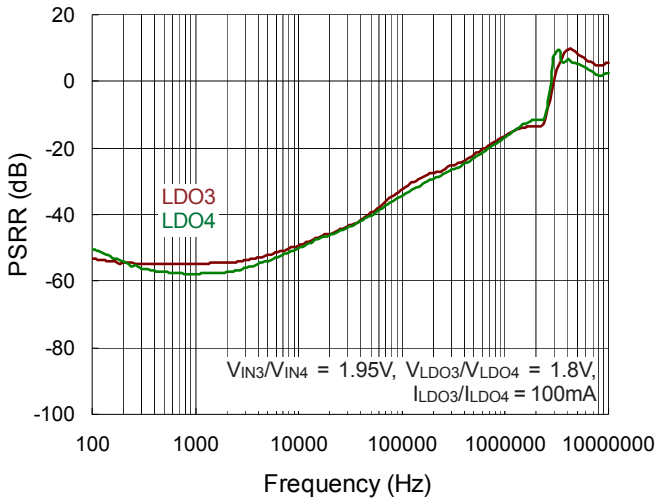
LDO4 Dropout Voltage vs. Load Current



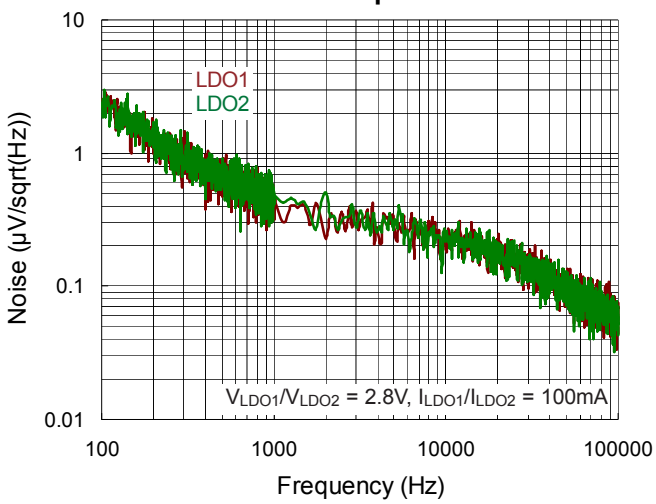
LDO1/2 PSRR



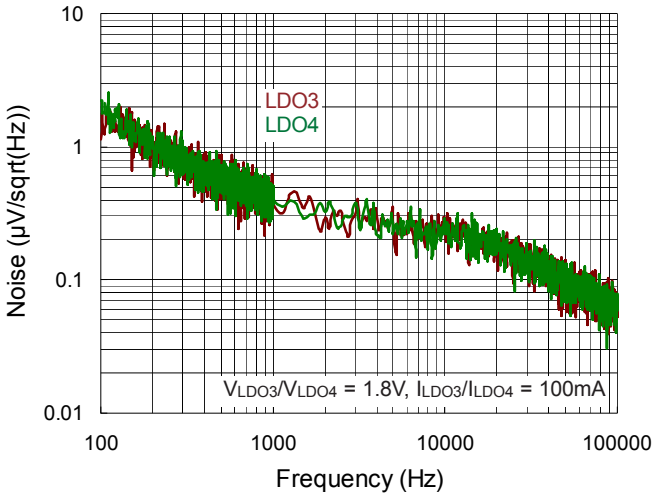
LDO3/4 PSRR



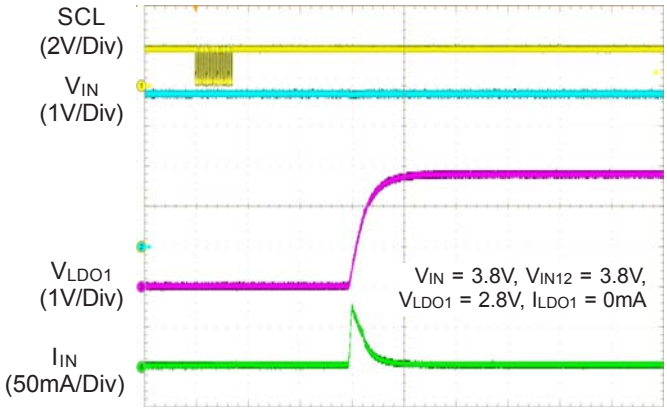
LDO1/2 Output Noise



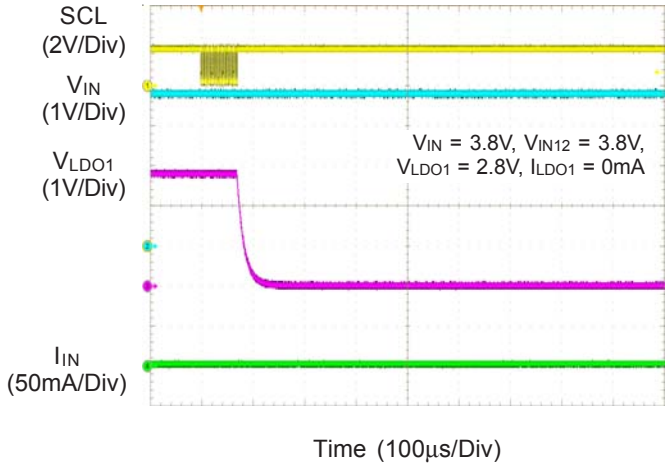
LDO3/4 Output Noise



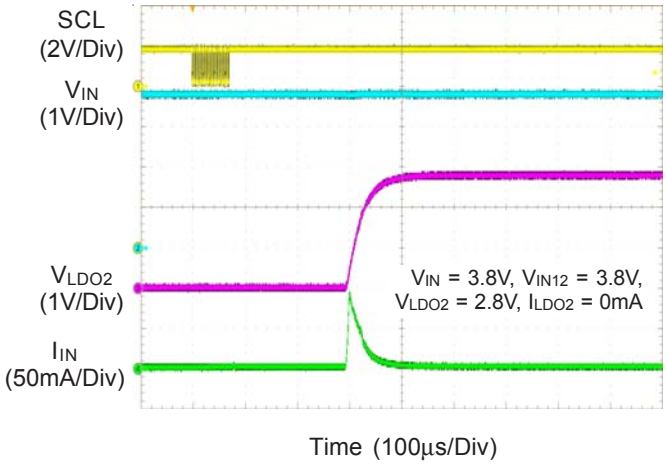
LDO1 Power On



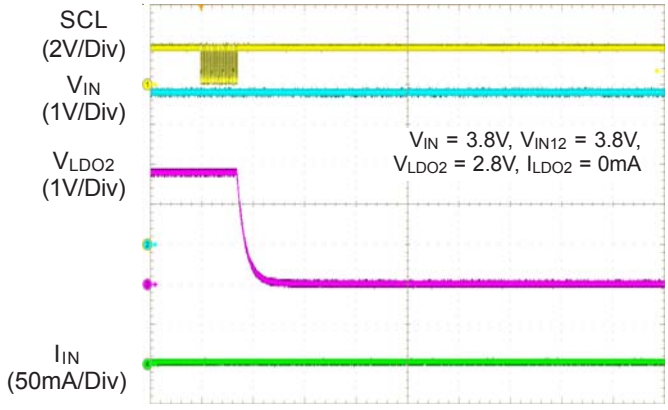
LDO1 Power Off



LDO2 Power On

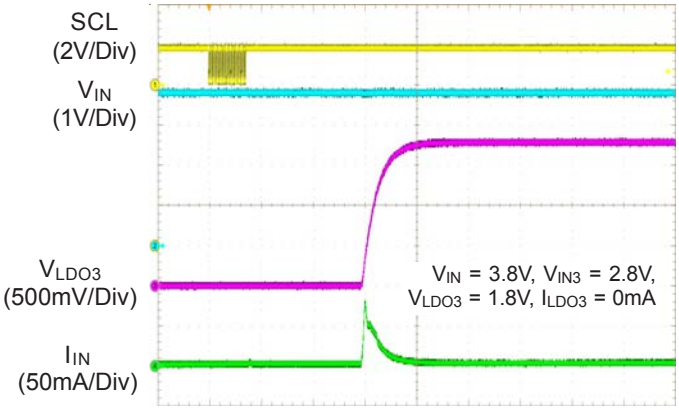


LDO2 Power Off



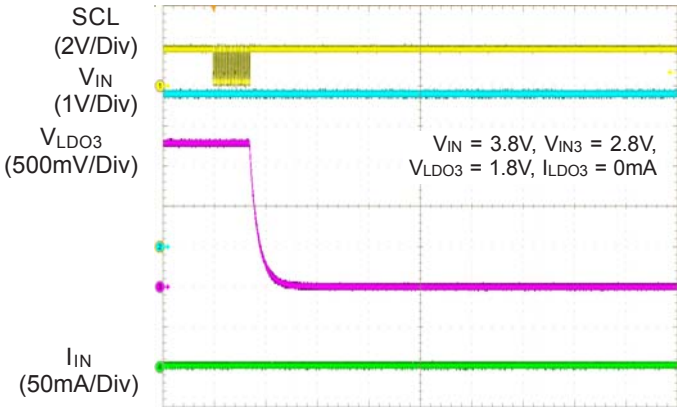
Time (100μs/Div)

LDO3 Power On



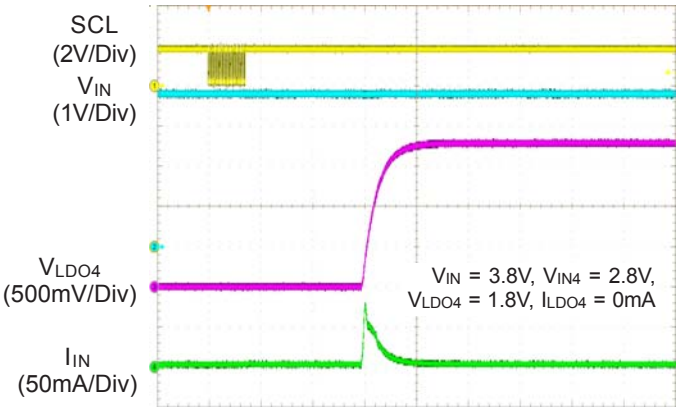
Time (100μs/Div)

LDO3 Power Off



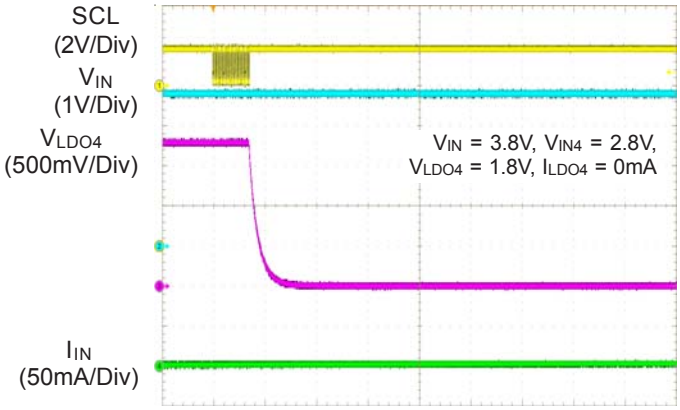
Time (100μs/Div)

LDO4 Power On



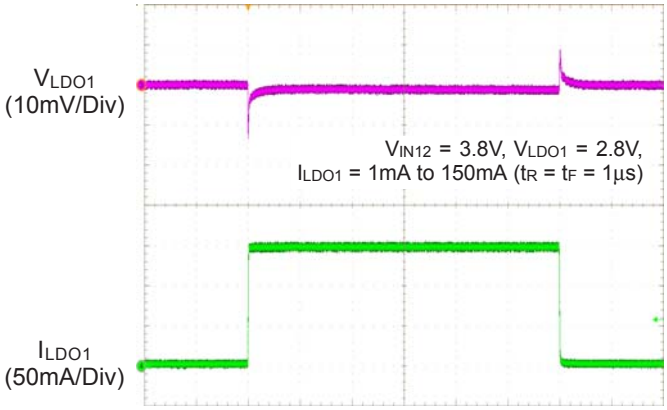
Time (100μs/Div)

LDO4 Power Off



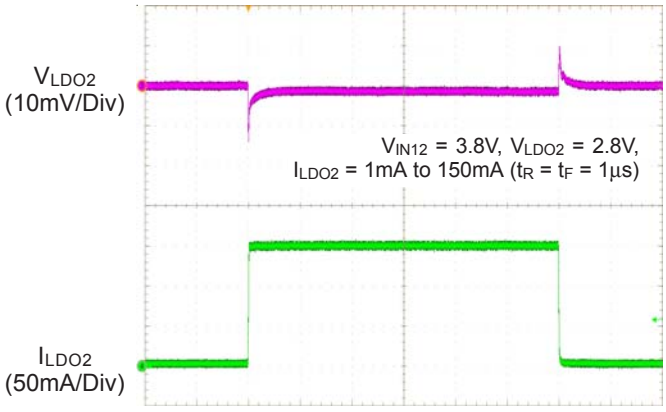
Time (100μs/Div)

LDO1 Load Transient

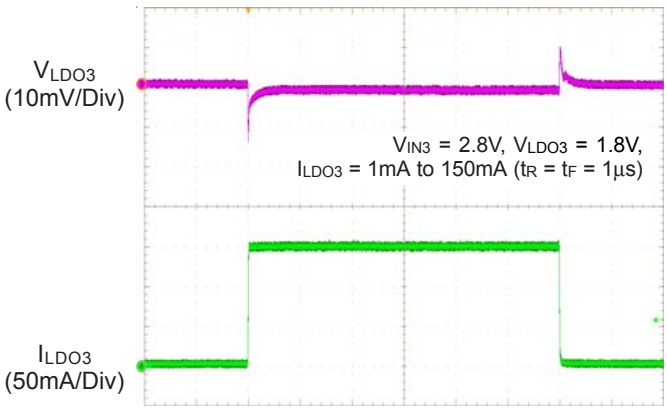


Time (5μs/Div)

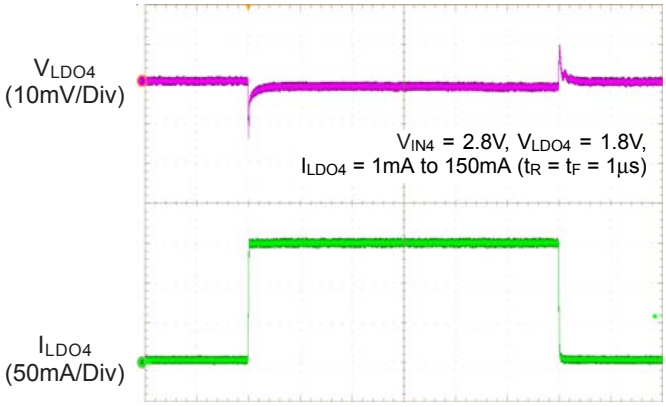
LDO2 Load Transient



LDO3 Load Transient



LDO4 Load Transient



Application Information

The RT5112A is a smart power-management integrated circuit (PMIC), which includes two Buck converters and four LDOs.

System Under-Voltage Protection and Over-Voltage Protection

The device does not operate with V_{SYS} voltages below the Under-Voltage Lock Out (UVLO) level. There is a typical 100mV hysteresis implemented to avoid unstable on/ off behavior. The RT5112A is initialized in its default state after V_{SYS} voltage recovers from UVLO. When V_{SYS} voltage reaches the Over Voltage Protection level, the RT5112A will disable Buck converter immediately to protect next stage circuit input. The V_{SYS} UV and OV status bits and interrupt bits will be set, and INTRB pin will be pulled low with corresponding to protection detected.

Thermal Protection

The RT5112A features over-temperature warning (OTW) and over-temperature protection (OTP). The OTW status bit and interrupt bit are set and INTRB pin will be pulled low when the junction temperature is higher than typical 125°C. If the junction temperature further exceeds typical 160°C, OTP will be triggered to shut down the device.

When the RT5112A recovers from OTP, it can re-start in three configurations with register 0x0A[4:3] bits.

- 0x0A[4:3] = 00, the RT5112A is manual re-start with default register values.
- 0x0A[4:3] = 01, the RT5112A is auto recovery with last register values before OTP.
- 0x0A[4:3] = 10, the RT5112A is latched off. Re-set V_{IN} or HWEN to re-start the RT5112A with default register values.

Enable and Disable Control

The HWEN pin controls the RT5112A start up without enabling channels. If HWEN pin is at low state, the RT5112A is in power down mode and I^2C will return NACK to any request. Only when HWEN pin is at high state, all channels are controllable via I^2C with corresponding ENABLE command. There is a built-in resistor on HWEN pin to keep at low state if the pin is left unconnected.

The below tables provide channels state with combinations of different ENABLE pins and register EN bits.

- **Sequence Control Setting**
  The RT5112A sequence on/off control setting can be programmed via I^2C with dedicated registers as below.

Table 1. Buck and LDOs Control

HWEN pin	SEQ bits	EN bits	SEQ_CTRL bits Dependent	On / Off
Low	000	0	No	Off
Low	000	1	No	Off
Low	≠000	0	No	Off
Low	≠000	1	No	Off
High	000	0	No	Off
High	000	1	No	On
High	≠000	0	Yes	On
High	≠000	1	CTRL	On / Off

Note : CTRL indicates several operating conditions as below.

(1) SEQ_CTRL[1:0] = 00, set SEQ bits ≠ 000 and EN bit = 1, channel is turned off after 7 sequence slot count regardless EN bit.

(2) SEQ_CTRL[1:0] = 01, set SEQ bits000 and EN bit = 1, channel is turned on depends on EN bit.

- **Sequence (7 slots)**

  Registers 0x00[6:4]/ 0x06[6:4] are used to control Buck1/Buck2 sequence on/off slot.

  Registers 0x01[6:4], 0x02[6:4], 0x03[6:4] and 0x04[6:4] are used to control LDOs sequence on/off slots.

- **Slot Interval Time**

  Register 0x09[7:6] is used to control interval time between each slot.

- **Soft Start Time**

  Register 0x09[7:6] is used to control Bucks sequence on soft start time.

  Register 0x11[1:0] is used to control LDOs sequence on soft start time.

- **Sequence Control**

  Register 0x09[5:4] = 00 is used to enable sequence off with sequence setting ≠ 000.

  Register 0x09[5:4] = 01 is used to enable sequence on with sequence setting000.

  Note :

  (1) Any changes in Sequence (7 slots), slot interval time and soft-start time during sequence on or off procedure is not valid and will not modify the RT5112A setting.

  (2) Channel setting (output voltage, current limit...etc.) is fixed during on or off sequence.

  (3) Register 0x09[5:4] = 11 will turn off all channels immediately.

  (4) HWEN = 0 will turn off all channels and the RT5112A enters into power down mode.

- **Normal Control Setting**

  When register bits 0x09[5:4] = 10, the Bucks and LDOs on/off control depends on channel Enable bit.

  - Registers 0x00[7]/0x06[7] are used to control Bucks on/off.
  - Register 0x01[7], 0x02[7], 0x03[7] and 0x04[7] are used to control LDOs on/off.

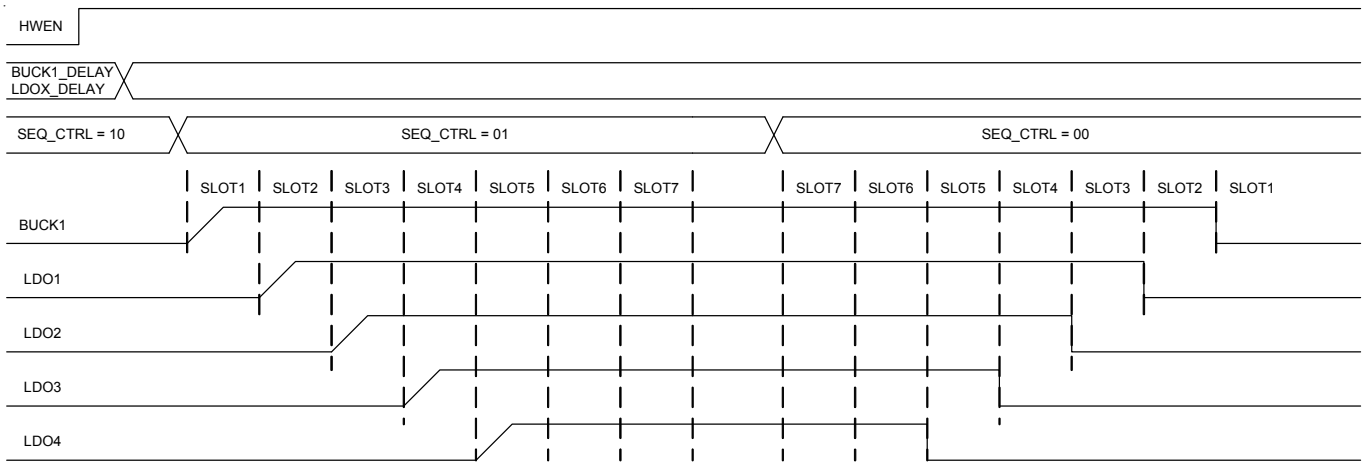


Figure 1.

Example for sequence on/off with BUCK1 assign to SLOT1, LDO1 assign to SLOT2, LDO2 assign to SLOT3, LDO3 assign to SLOT4 and LDO4 assign to SLOT5.

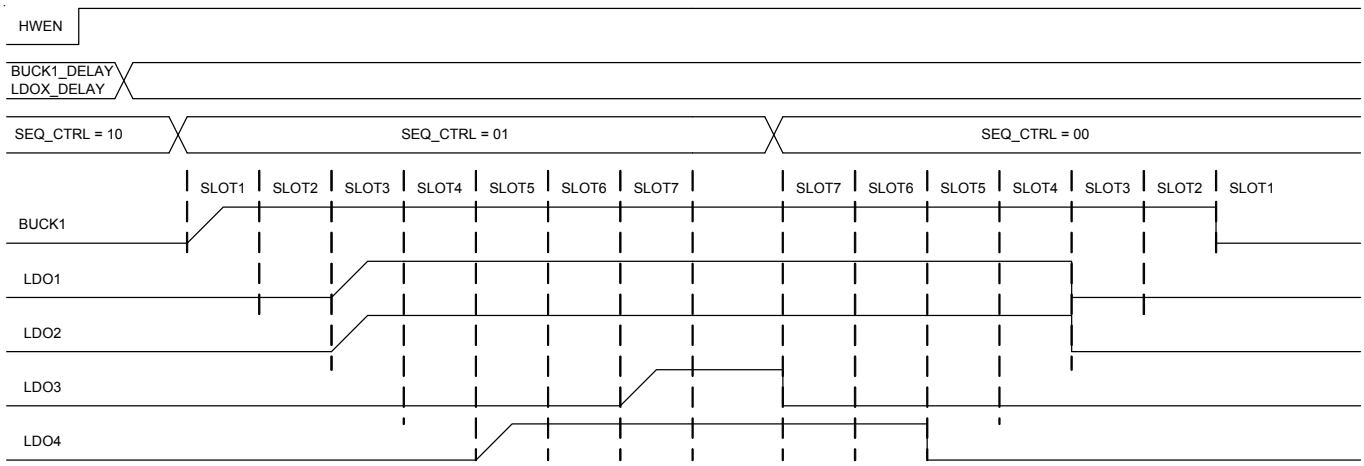


Figure 2.

Example for sequence on/off with BUCK1 assign to SLOT1, LDO1 assign to SLOT3, LDO2 assign to SLOT3, LDO3 assign to SLOT7 and LDO4 assign to SLOT5.

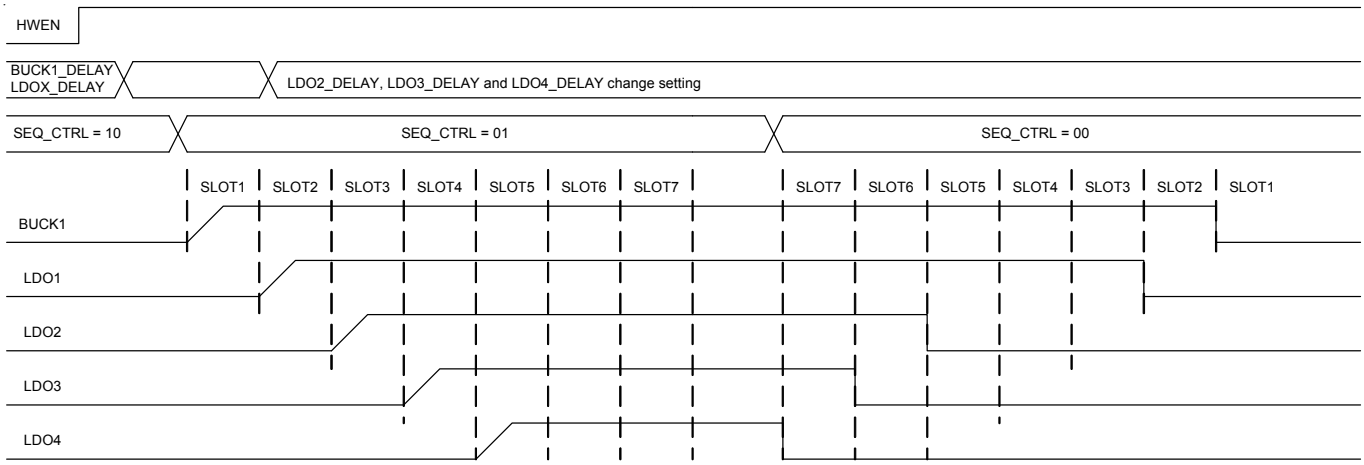


Figure 3.

Example for sequence slot change when on procedure. LDO2 assign from SLOT3 to SLOT5, LDO3 assign from SLOT4 to SLOT6 and LDO4 assign from SLOT5 to SLOT7. There is no influence with on procedure and new setting will executed after on sequence finish.

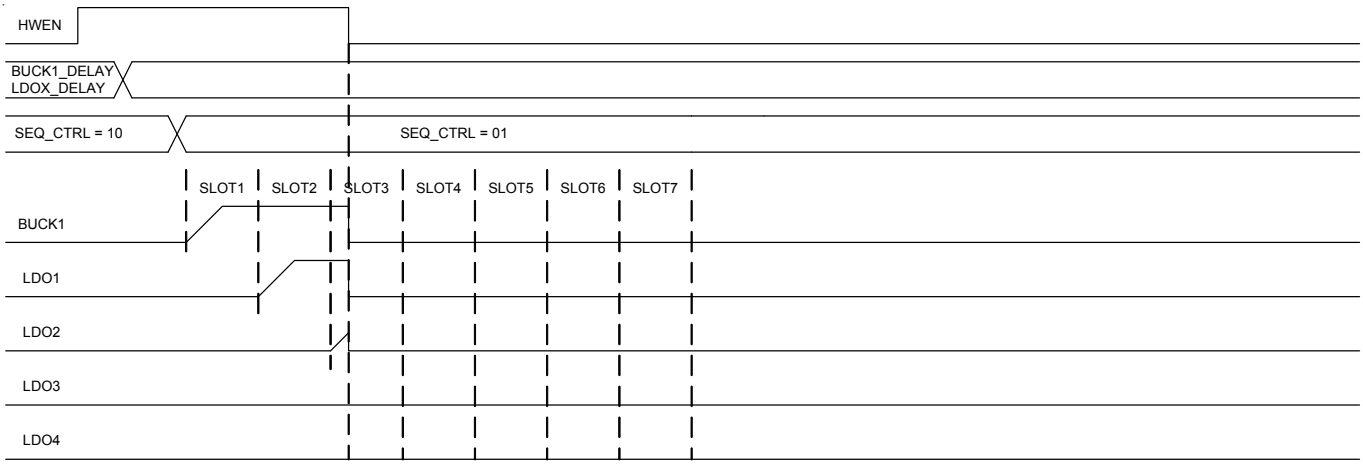


Figure 4.

Example for sequence on is interrupted by HWEN signal low. The RT5112A turns off all channels immediately.

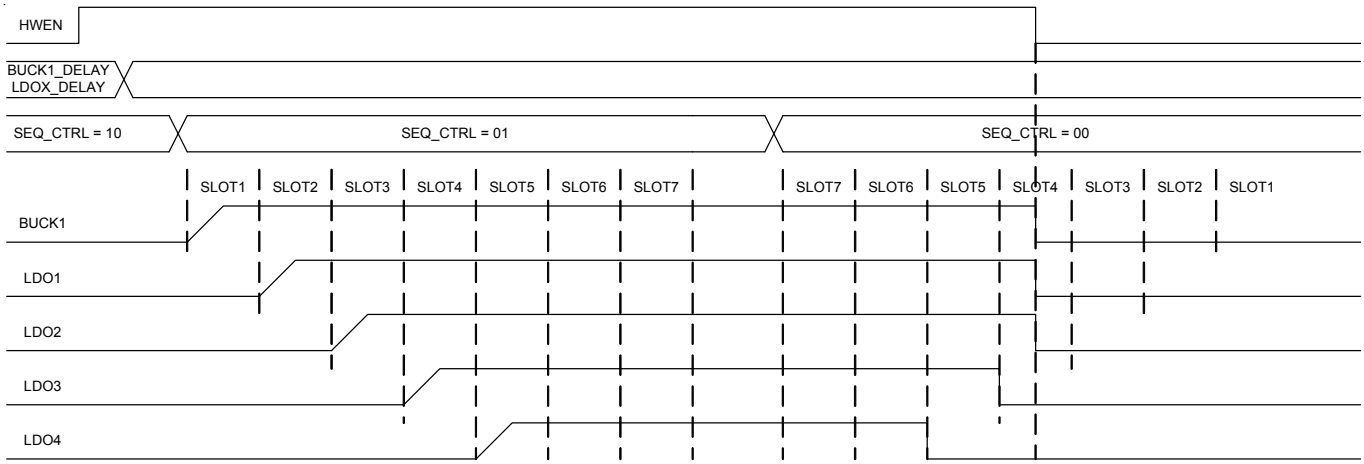


Figure 5.

Example for sequence off is interrupted by HWEN signal low. The RT5112A turns off all channels immediately.

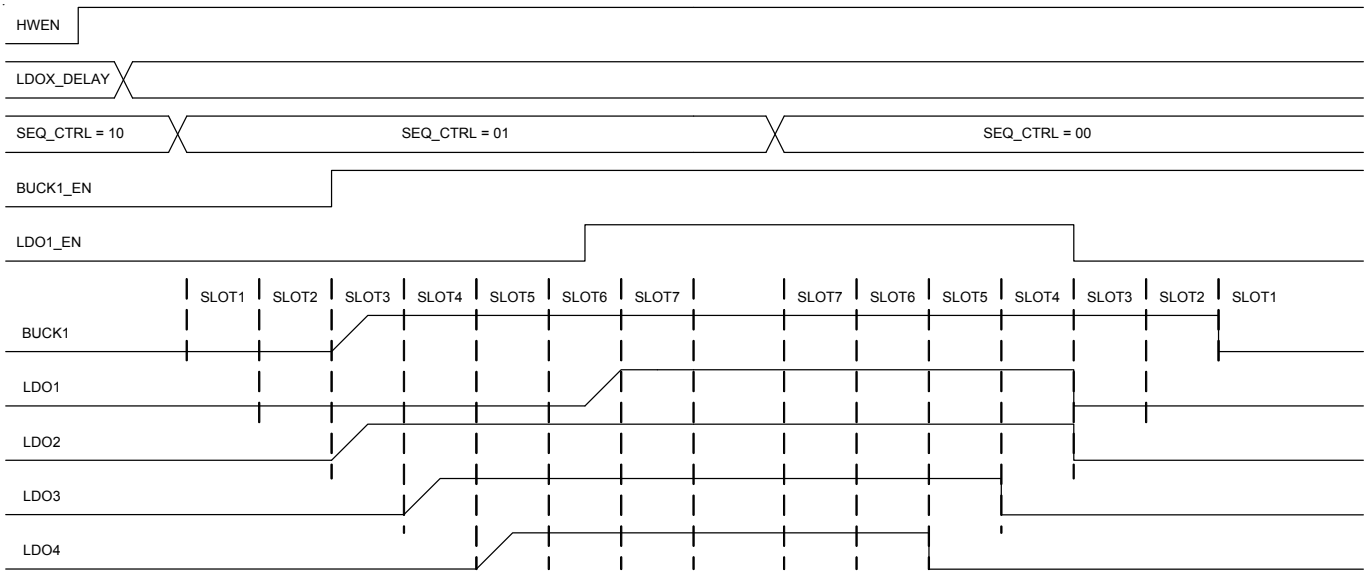


Figure 6.

Example for sequence control SEQ_CTRL change from 01 to 00. LDO2, LDO3, LDO4 are sequence off and LDO1 is turned off by itself enable bit. BUCK1 is turned off after 7 sequence slot count even itself enable bit is at high state.

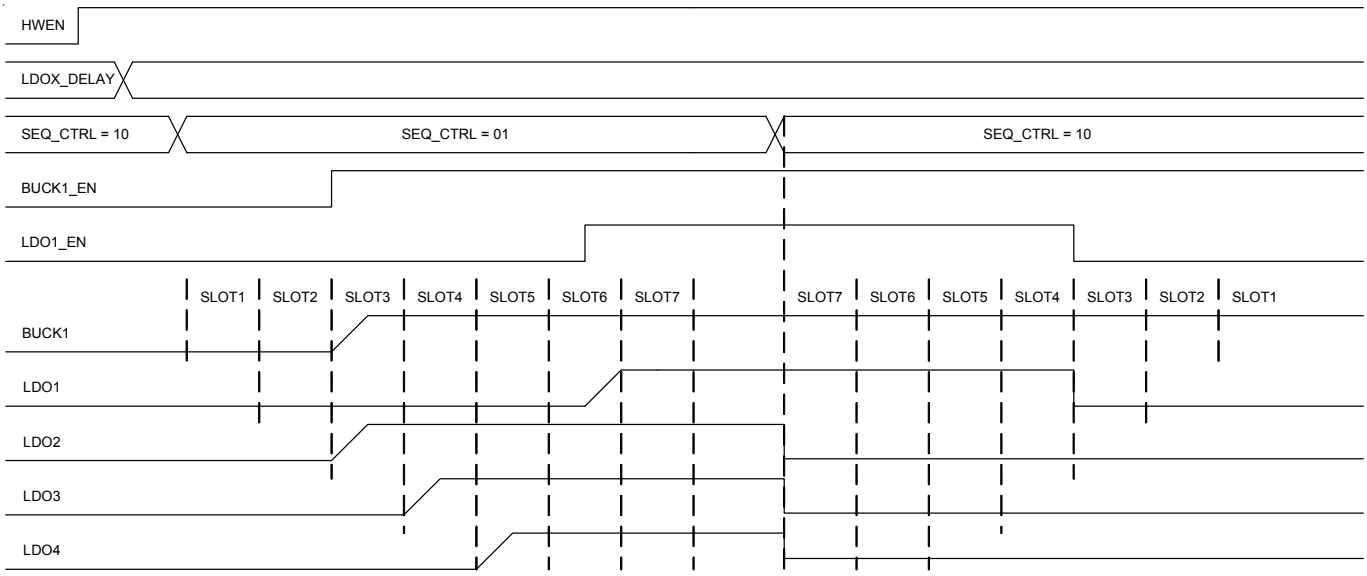


Figure 7.

Example for sequence control SEQ_CTRL change from 01 to 10. LDO2, LDO3, LDO4 are turned off and state of BUCK1, LDO1 depends on itself enable bit.

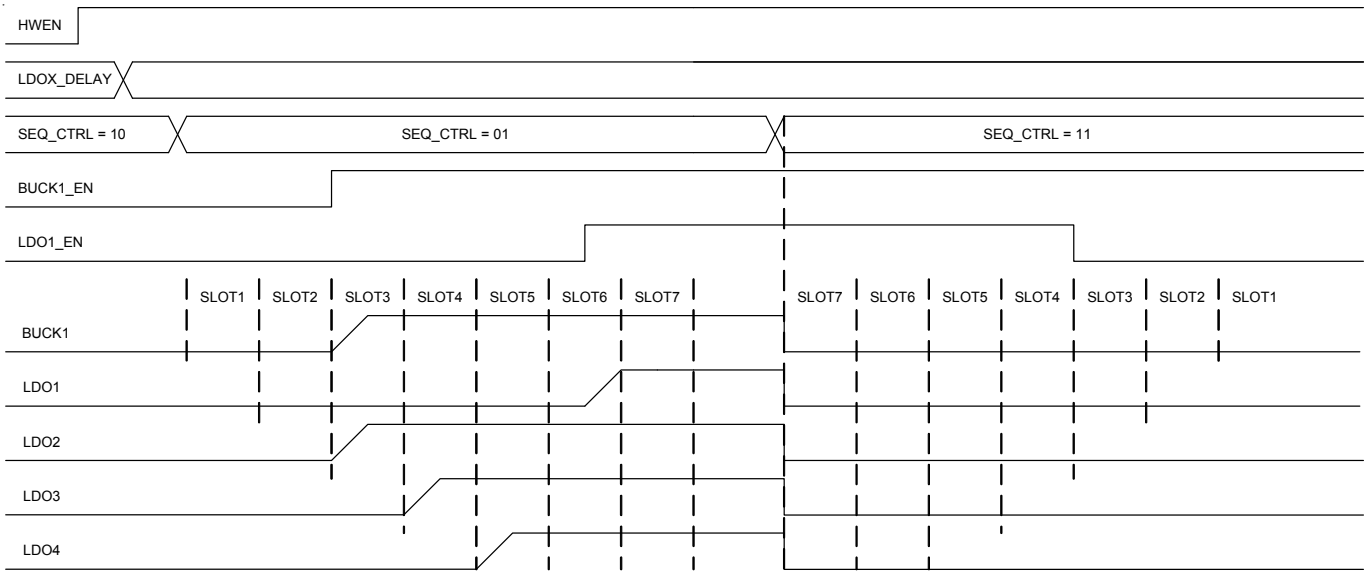


Figure 8.

Example for sequence control SEQ_CTRL change from 01 to 11. All channels are turned off immediately.

Output Voltage Setting

The RT5112A output voltage can be programmed via I^2C with dedicated registers.

- **Bucks**

  Registers 0x0C[7:0]/0x12[7:0] are used to control Bucks output voltage.

  Register 0x14[7:6] is used to control Bucks voltage scaling slew rate.

- **LDOs**

  Registers 0x0D[7:1], 0x0E[7:1], 0x0F[7:1], 0x10[7:1] are used to control LDO1, LDO2, LDO3 and LDO4 output voltage.

  Register 0x14[5:4] is used to control LDOs voltage scaling slew rate.

Operating Mode

The RT5112A provides different operating modes for Bucks and LDOs for flexible application. Registers 0x00[1:0], 0x01[1:0], 0x02[1:0], 0x03[1:0], 0x04[1:0] and 0x06[1:0] are used to control the operating mode.

- **Bucks**
  - **Auto PFM (Pulse Frequency Modulation) Mode**

    In order to save power and improve efficiency at low loads, the Buck operates in PFM mode as the inductor drops into DCM (Discontinuous Current Mode). The switching frequency is proportional to loading to reach output voltage regulation. When load increases and inductor current becomes continuous again, the Buck automatically goes back to PWM fixed frequency mode. Additionally, the RT5112A will enters DSLP (Deep Sleep) to reach input low quiescent current at no load.

  - **FPWM (Forced Pulse Width Modulation) Mode**

    The switching frequency is forced into PWM mode 2.5MHz (typ.) operation. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM.

  - **Normal Mode**

    The operation is same as Auto PFM mode. The only one difference is that there is no DSLP in this mode.

- **Ultra-Sonic Mode**

  To avoid acoustic noise problem when operation, the switching frequency is designed to be always higher than 20kHz even there is no load at output.

- **LDOs**
  - **Auto Mode**

    This mode is for general use.

  - **EN Forced Mode**

    When EN Forced Mode is selected, the RT5112A can provide higher PSRR (Power Supply Rejection Ratio) to mitigate interference from input voltage. However, it brings out higher quiescent current to get the function.

  - **Bypass Mode**

    LDO internal power MOSFET is fully turned on. Input voltage will pass through it to the output terminal directly.

Channel Protection Features

The RT5112A equips Over-Current Protection, Under-Voltage Protection and Over-Voltage Protection to prevent the device from damages causing by abnormal operation or fault conditions. (over-load, short-circuit, soldering issue...etc.)

- **Over-Current Protection (OCP)**
  - **Behavior after OCP**

    Register 0x37[7:6] is used to select the operation after over-current failure detected.

  - **OCP Mechanism**
    - **Bucks**

      When the inductor current reaches the high-side MOSFET peak current limit threshold, the high-side MOSFET will be turned-off. The low-side MOSFET turns on to discharge the inductor current until the inductor current trips below the low-side MOSFET valley current limit threshold. After high-side MOSFET peak current limit triggered, the maximum inductor current is decided by the inductor current rising rate and the response delay time of the internal network.

    - **LDOs**

      When the loading reaches the current limit threshold, the current sent to the output will kept at current limit level.

- **Under-Voltage Protection (UVP)**
  - **Behavior after UVP**

    Register 0x0A[7:6] is used to select the operation after under voltage failure detected.

- **Ovrt-Voltage Protection (OVP)**
  - **Behavior after OVP**

    Register 0x0A[2:1] is used to select the operation after over voltage failure detected.

Table 2. Protection

Channel	Type	Threshold (typ.)	Deglitch Time (typ.)	Protection	Reset and Threshold (typ.)
System	UVLO	V_{SYS} < 2.35V $V_{SYS} \leq$ 2.25V (after IC Operation)	525µs	IC Shutdown	$V_{SYS} \geq$ 2.35V
	OVP	$V_{SYS} \geq$ 5.9V	200µs	Buck Disable	$V_{SYS} \leq$ 5.6V
	OTW	Temperature ≥ 125°C	50µs	Report only	Temperature ≤ 105°C
	OTP	Temperature ≥ 140°C	50µs	IC Shutdown	Selection by 0x0A[4:3] 00 : Manual recovery after TSD with reset register 01 : Auto recovery after TSD with no reset register 10 : Latch off after TSD with reset register
BUCKs	UVP	$V_{BUCK} \leq V_{BUCK\_SET}$ x 80%	50µs	Selection by 0x0A[7] 0 : Hiccup mode 1 : Latch-off mode	$V_{BUCK} \geq V_{BUCK\_SET}$ x 92%
	OVP	$V_{BUCK} \geq V_{BUCK\_SET}$ x 120%	50µs	Selection by 0x0A[2] 0 : Discharge mode 1 : Latch-off mode	$V_{BUCK} \leq V_{BUCK\_SET}$ x 109%
	OCP	$I_{LXBUCK\_peak} \geq$ 2A $I_{LXBUCK\_valley} \geq$ 1.5A (peak - 0.5A)	8µs	Selection by 0x037[7] 0 : Hiccup mode 1 : Latch-off mode	I_{LXBUCK_peak} < 2A I_{LXBUCK_valley} < 1.5A (peak - 0.5A)
LDOs	UVP	$V_{LDO} \leq V_{LDO}$ x 80%	50µs	Selection by 0x0A[6] 0 : Hiccup mode 1 : Latch-off mode	$V_{LDO} \geq V_{LDO}$ x 90%
	OVP	$V_{LDO} \geq V_{LDO}$ x 120%	50µs	Selection by 0x0A[1] 0 : Discharge mode 1 : NA	$V_{LDO} \leq V_{LDO}$ x 110%
	OCP	I_{LDO} > 415mA	8µs	Selection by 0x037[6] 0 : Hiccup mode 1 : Latch-off mode	$I_{LDO} \leq$ 415mA

Interrupt

- **Fault Event and Status**

  The RT5112A interrupt controller continuously monitors the device operation. Once the fault is ever detected, the fault event bit will be set to 1 and the open drain interrupt indicate pin INTRB will be driven to ground level. Meanwhile, the fault status bit will also be set to 1 to show the present fault. When the host reads the fault event bit and set interrupt clear bit 0x14[0] = 1, the INTRB pin will be released to high impedance. The fault status bit goes back to 0 only till the fault condition is cleared.

Table 3. Interrupt

Fault Event	Fault Status	Description
BUCK_UV_EVT 0x15[7]	BUCK_UV_STAT 0x2B[7]	BUCK output under-voltage
LDO1_UV_EVT 0x15[6]	LDO1_UV_STAT 0x2B[6]	LDO1 output under-voltage
LDO2_UV_EVT 0x15[5]	LDO2_UV_STAT 0x2B[5]	LDO2 output under-voltage
LDO3_UV_EVT 0x15[4]	LDO3_UV_STAT 0x2B[4]	LDO3 output under-voltage
LDO4_UV_EVT 0x15[3]	LDO4_UV_STAT 0x2B[3]	LDO4 output under-voltage
BUCK2_UV_EVT 0x15[1]	BUCK2_UV_STAR 0x2B[1]	BUCK2 output under-voltage
BUCK_OV_EVT 0x16[7]	BUCK_OV_STAT 0x2C[7]	BUCK output over-voltage
LDO1_OV_EVT 0x16[6]	LDO1_OV_STAT 0x2C[6]	LDO1 output over-voltage
LDO2_OV_EVT 0x16[5]	LDO2_OV_STAT 0x2C[5]	LDO2 output over-voltage
LDO3_OV_EVT 0x16[4]	LDO3_OV_STAT 0x2C[4]	LDO3 output over-voltage
LDO4_OV_EVT 0x16[3]	LDO4_OV_STAT 0x2C[3]	LDO4 output over-voltage
BUCK2_OV_EVT 0x16[1]	BUCK2_OV_STAT 0x2C[1]	BUCK2 output over-voltage
BUCK_OCP_EVT 0x17[7]	BUCK_OCP_STAT 0x2D[7]	BUCK over-current
LDO1_OCP_EVT 0x17[6]	LDO1_OCP_STAT 0x2D[6]	LDO1 over-current
LDO2_OCP_EVT 0x17[5]	LDO2_OCP_STAT 0x2D[5]	LDO2 over-current
LDO3_OCP_EVT 0x17[4]	LDO3_OCP_STAT 0x2D[4]	LDO3 over-current
LDO4_OCP_EVT 0x17[3]	LDO4_OCP_STAT 0x2D[3]	LDO4 over-current
BUCK2_OCP_EVT 0x17[1]	BUCK2_OCP_STAT 0x2D[1]	BUCK2 over-current
TWARN_EVT 0x19[7]	TWARN_STAT 0x2F[7]	Thermal warning
TSD_EVT 0x19[6]	TSD_STAT 0x2F[6]	Thermal shutdown
VSYSUV_EVT 0x19[5]	VSYSUV_STAT 0x2F[5]	System under-voltage
VSYSOV_EVT 0x19[4]	VSYSOV_STAT 0x2B[4]	System over-voltage

- **Fault Event Mask**

  The host can set the fault event mask bits to hide the fault events. When the mask bit is set to 1, the corresponding fault is hidden and the interrupt indicate pin INTRB will keep high impedance without being pulled to ground level. The host requires to read the fault event bits to clear its value to 0, otherwise the interrupt indicate pin INTRB will be driven to low level again when mask bits being set to 1. The mask bits will be reset to default value with conditions : HWEN voltage goes to low level or IC power shutdown.

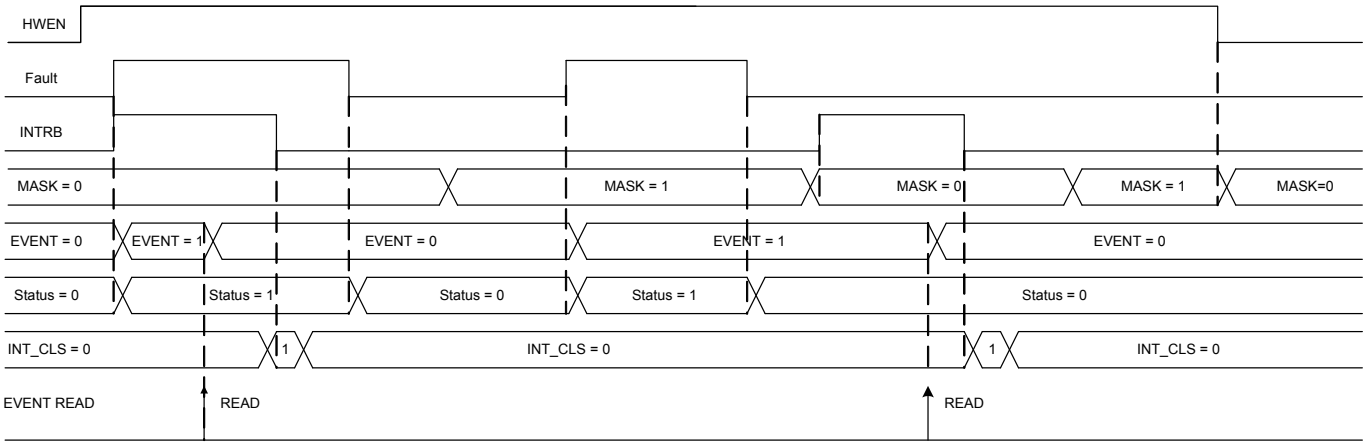


Figure 9.

Component Selection

- **Inductor Selection**

  The recommended nominal inductance 1μH for Buck converter. The inductor saturation current must be chosen carefully considering the current limit level. It is suggested to select an inductor with the low DCR to provide good performance and efficiency for application.

- **Input and Output Capacitor Selection**

  It is recommended at least a 10μF (6.3V) input capacitor for Buck, a 10μF (6.3V) output capacitor for Buck. The ripple voltage is an important index for choosing output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The output ripple can be calculated as below.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT1} + \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where $\Delta V_{ESR} = I_{COUT\_RMS} \times R_{COUT\_ESR}$

- **LDOs**

  Like any low dropout regulator, the external capacitors of the RT5112A must be carefully selected for regulator stability and performance. Using a capacitor of at least 2.2μF (X5R or X7R) is suitable.

I²C Interface

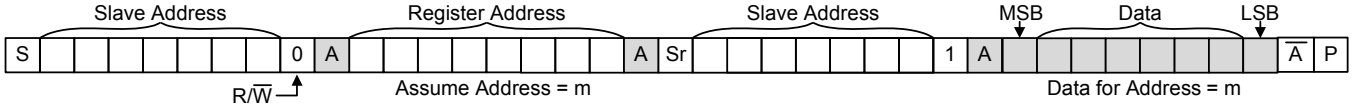
The following table shows the RT5112A unique address as below.

RT5112A I²C Slave Address			
MSB	**LSB**	**R/W bit**	**R/W**
010000	1	1/0	43/42

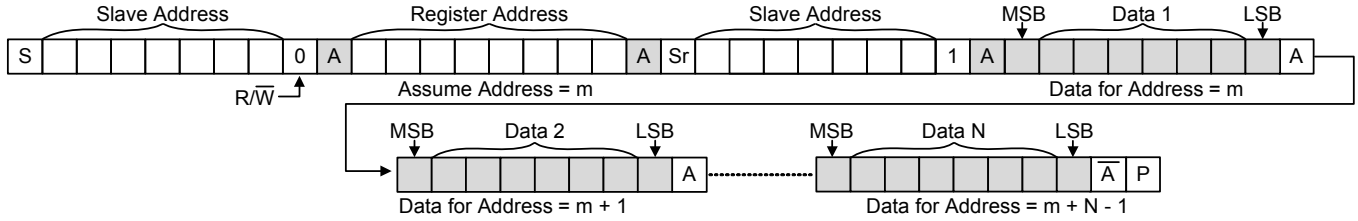
The I²C interface bus must be connect a resistor 2.2kΩ to power node and independent connection to processor, individually. The I²C timing diagrams are listed below.

Read and Write Function

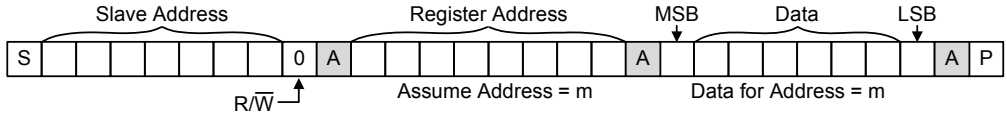
Read single byte of data from Register



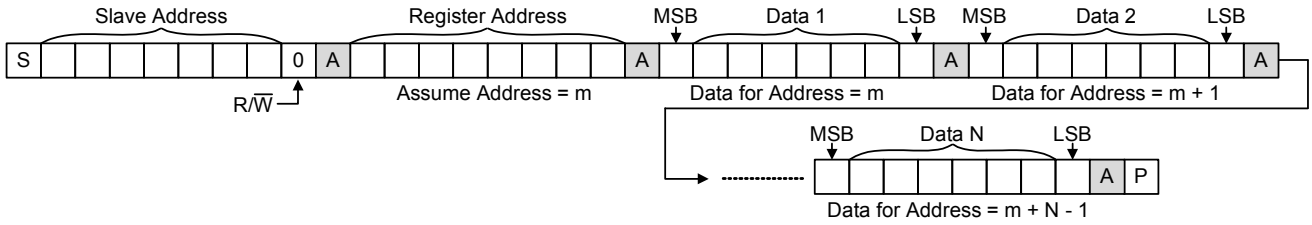
Read N bytes of data from Registers



Write single byte of data to Register

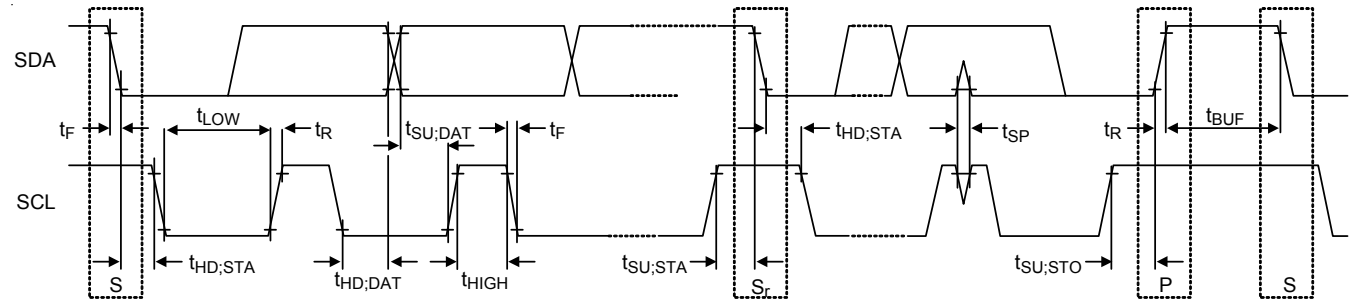


Write N bytes of data to Registers



Driven by Master, Driven by Slave, P Stop, S Start, Sr Repeat Start

I²C Waveform Information



I²C Register Table

R : Read only.

RC : Read then Clear.

RW : Read and Wirte.

WC : Write "1" then clear to "0" after this procedure finish.

Note 6. Below registers setting are only available on the RT5112.

0x05, 0x08, 0x0A[5][0], 0x0B[5][1], 0x11[7:2], 0x13[1:0], 0x14[3:2], 0x15[2][0], 0x16[2], 0x17[2], 0x2B[2][0], 0x2C[2], 0x2D[2], 0x30[2], 0x32[2][0], 0x33[2], 0x34[2], 0x37[5][3:2], 0x3B[2] and 0x43[7:6].

Addr	RegName	Bit	BitName	Default	Type	Description
0x00	Buck_CTRL	7	BUCK_EN	0	RW	Buck enable. This bit is mask if REG0x00[6:4] : BUCK_DELAY ≠ 3'b000 0 : Disable (default) 1 : Enable Note : When Buck's latch-off protection happen, this bit will reset to "0"
		6:4	BUCK_ DELAY	000	RW	Buck power on/off delay time setting: 000 : Controlled by I²C with REG0x00[7] : BUCK_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When Buck's latch-off protection happen, these bits will reset to "000"
		3:2	BUCK_ ILIM	01	RW	Buck current limit set bit. 00 : 1.5A 01 : 2A (default) 10 : 2.5A 11 : 3A
		1:0	BUCK_ MODE	00	RW	Buck operation mode : 00 : Auto PFM mode (default) 01 : Forced PWM mode 10 : Ultra sonic mode 11 : Normal mode

Addr	RegName	Bit	BitName	Default	Type	Description
0x01	LDO1_CTRL	7	LDO1_EN	0	RW	LDO1 enable. This bit is mask if REG0x01[6:4] : LDO1_DELAY ≠ 3'b000 0 : Disable (default) 1 : Enable Note : When LDO1's latch-off protection happen, this bit will reset to "0"
		6:4	LDO1_ DELAY	000	RW	LDO1 power on/off delay time setting: 000 : Controlled by I^2C with REG0x01[7] : LDO1_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When LDO1's latch-off protection happen, these bits will reset to "000"
		3:2	LDO1_ILIM	11	RW	LDO1 current limit set bit. 00 : 150mA 01 : 250mA 10 : 300mA 11 : 360mA (default)
		1:0	LDO1_ MODE	00	RW	LDO1 operation mode : 00 : Auto mode (default) 01 : EN forced mode. (High PSRR mode). 10 : Bypass mode. LDO1 internal power MOSFET turns on fully. 11 : Bypass mode. LDO1 internal power MOSFET turns on fully.

Addr	RegName	Bit	BitName	Default	Type	Description
0x02	LDO2_CTRL	7	LDO2_EN	0	RW	LDO2 enable. This bit is mask if REG0x02[6:4] : LDO2_DELAY ≠ 3'b000 0 : Disable (default) 1 : Enable Note : When LDO2's latch-off protection happen, this bit will reset to "0"
		6:4	LDO2_ DELAY	000	RW	LDO2 power on/off delay time setting : 000 : Controlled by I^2C with REG0x02[7] : LDO2_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When LDO2's latch-off protection happen, these bits will reset to "000"
		3:2	LDO2_ ILIM	11	RW	LDO2 current limit set bit. 00 : 150mA 01 : 250mA 10 : 300mA 11 : 360mA (default)
		1:0	LDO2_ MODE	00	RW	LDO2 operation mode : 00 : Auto mode (default) 01 : EN forced mode. (High PSRR mode). 10 : Bypass mode. LDO2 internal power MOSFET turns on fully. 11 : Bypass mode. LDO2 internal power MOSFET turns on fully.

Addr	RegName	Bit	BitName	Default	Type	Description
0x03	LDO3_CTRL	7	LDO3_EN	0	RW	LDO3 enable. This bit is mask if REG0x03[6:4] : LDO3_DELAY ≠ 3'b000 0 : Disable (default) 1 : Enable Note : When LDO3's latch-off protection happen, this bit will reset to "0"
		6:4	LDO3_ DELAY	000	RW	LDO3 power on/off delay time setting : 000 : Controlled by I^2C with REG0x03[7] : LDO3_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When LDO3's latch-off protection happen, these bits will reset to "000"
		3:2	LDO3_ ILIM	11	RW	LDO3 Current limit set bit. 00 : 150mA 01 : 250mA 10 : 300mA 11 : 360mA (default)
		1:0	LDO3_ MODE	00	RW	LDO3 operation mode : 00 : Auto mode (default) 01 : EN forced mode. (High PSRR mode). 10 : Bypass mode. LDO3 internal power MOSFET turns on fully. 11 : Bypass mode. LDO3 internal power MOSFET turns on fully.

Addr	RegName	Bit	BitName	Default	Type	Description
0x04	LDO4_CTRL	7	LDO4_EN	0	RW	LDO4 enable. This bit is mask if REG0x04[6:4] : LDO4_DELAY ≠ 3'b000 0 : Disable (default) 1 : Enable Note : When LDO4's latch-off protection happen, this bit will reset to "0"
		6:4	LDO4_DELAY	000	RW	LDO4 power on/off delay time setting : 000 : Controlled by I^2C with REG0x04[7] : LDO4_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When LDO4's latch-off protection happen, these bits will reset to "000"
		3:2	LDO4_ILIM	11	RW	LDO4 current limit set bit. 00 : 150mA 01 : 250mA 10 : 300mA 11 : 360mA (default)
		1:0	LDO4_MODE	00	RW	LDO4 operation mode : 00 : Auto mode (default) 01 : EN forced mode. (High PSRR mode). 10 : Bypass mode. LDO4 internal power MOSFET turns on fully. 11 : Bypass mode. LDO4 internal power MOSFET turns on fully.

Addr	RegName	Bit	BitName	Default	Type	Description
0x05	BOOST_CTRL	7	LCH_ON	0	RW	Boost linear charge current : 0 : 400mA (default) 1 : 800mA
		6	NFC_EN	1	RW	Boost NFC enable. 0x39[2] must set 0 when bit NFC_EN = 1. 0 : Disable 1 : Enable (default)
		5:4	BOOST_SS	00	RW	Voltage scaling slew rate for Boost. 00 : 14mV/μs (default) 01 : 10mV/μs 10 : 6mV/μs 11 : 4mV/μs
		3:2	BOOST_ILIM	01	RW	Boost current limit set bit. 00 : 2A 01 : 2.5A (default) 10 : 3A 11 : 3.5A
		1:0	BOOST_MODE	00	RW	Boost operation mode: 00 : Auto PFM mode (default) 01 : Forced PWM mode 10 : Ultra sonic mode 11 : Normal mode

Addr	RegName	Bit	BitName	Default	Type	Description
0x06	Buck2_CTRL	7	BUCK2_EN	0	RW	BUCK2 enable. This bit is mask if REG0x06[6:4] : BUCK2_DELAY ≠ 3'b000 0 : Disable (default) 1 : Enable Note : When Buck2's latch-off protection happen, this bit will reset to "0"
		6:4	BUCK2_DELAY	000	RW	BUCK2 power on/off delay time setting : 000 : Controlled by I^2C with REG0x06[7] : BUCK2_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When Buck2's latch-off protection happen, these bits will reset to "000"
		3:2	BUCK2_ILIM	01	RW	BUCK2 current limit set bit. 00 : 1.5A 01 : 2A (default) 10 : 2.5A 11 : 3A
		1:0	BUCK2_MODE	00	RW	BUCK2 operation mode: 00 : Auto mode (default) 01 : Forced PWM mode 10 : Ultra sonic mode 11 : Normal mode

Addr	RegName	Bit	BitName	Default	Type	Description
0x07	Product ID	7:0	PID	11001101	R	Vendor identification

Addr	RegName	Bit	BitName	Default	Type	Description
0x08	BOOST_ ENABLE	7	BOOST_ EN7	0	RW	Enable bit #7 for the Boost. 0 : Disable (default) 1 : Enable
		6	BOOST_ EN6	0	RW	Enable bit #6 for the Boost. 0 : Disable (default) 1 : Enable
		5	BOOST_ EN5	0	RW	Enable bit #5 for the Boost. 0 : Disable (default) 1 : Enable
		4	BOOST_ EN4	0	RW	Enable bit #4 for the Boost. 0 : Disable (default) 1 : Enable
		3	BOOST_ EN3	0	RW	Enable bit #3 for the Boost. 0 : Disable (default) 1 : Enable
		2	BOOST_ EN2	0	RW	Enable bit #2 for the Boost. 0 : Disable (default) 1 : Enable
		1	BOOST_ EN1	0	RW	Enable bit #1 for the Boost. 0 : Disable (default) 1 : Enable
		0	BOOST_ EN0	0	RW	Enable bit #0 for the Boost. 0 : Disable (default) 1 : Enable

Addr	RegName	Bit	BitName	Default	Type	Description
0x09	SEQ_PROG	7:6	SEQ_SPEED[1:0]	10	RW	Set slot period : 00 : 2.73ms 01 : 1.365ms 10 : 0.682ms (default) 11 : 0.341ms (slot period is the base unit of each SLOT, for example SLOT2 = 2*slot period; SLOT3 = 3*slot period) Set soft-start time slew rate (Buck_SR) : 00 : 1mV/μs 01 : 2mV/μs 10 : 4mV/μs (default) 11 : 7mV/μs (Buck's VOUT min. step = 12.5mV, f = 2.5MHz) (Once slot period is chose, corresponding soft start time slew rate is determined.) Note : Buck soft-start time (Buck_tss) 00 : 1ms/V x Vout 01 : 0.5ms/V x Vout 10 : 0.25ms/V x Vout (default) 11 : 0.143ms/V x Vout
		5:4	SEQ_CTRL[1:0]	10	RW	2 bits to control LDOs and Buck's ON/OFF 00 : Power-Down, relative regulators (CHx_DELAY ≠ 3'b000) disable by power off sequence, others turn off by each EN bit 01 : Power-UP,relative regulators (CHx_DELAY ≠ 3'b000) enable by power on sequence, others turn on by each EN bit 10 : All regulators's ON/OFF depend on each EN bit. (default) 11 : All regulators turn off directly.
		3:0	Reserved	0000	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x0A	Latch	7	BUCK_UV_LATCH	0	RW	Buck hiccup or latch off mode selection after V_O UV. 0 : Hiccup mode; (continouously hiccup more than 3 times would enter latch-off mode ,select deglitch time by REG0x38[7:6], hiccup on/off time = 5/8ms) (default) 1 : Latch-off mode
		6	LDO_UV_LATCH	0	RW	LDO hiccup or latch off mode selection after V_O UV. 0 : Hiccup mode; (continouously hiccup more than 3 times would enter latch-off mode ,select deglitch time by REG0x38[3:2], hiccup on/off time = 5/40ms) (default) 1 : Latch-off mode
		5	BOOST_UV_LATCH	0	RW	Boost hiccup or latch off mode selection after V_O UV. 0 : Hiccup mode; (continouously hiccup more than 3 times would enter latch-off mode ,select deglitch time by REG0x37[3:2], hiccup on/off time = 11/100ms) (default) 1 : Latch-off mode
		4:3	TSD[1:0]	01	RW	IC protection after thermal shutdown : 00 : Manual recovery after TSD with reset I^2C register. The power up sequence is initiated with default I^2C register value 01 : Auto recovery after TSD with no reset I^2C register. The power up sequence is initiated with I^2C register value (default) 10 : Latch off after TSD, all Reg reset. Restart by Vin start up or (BSTEN = 0 → 1 to restart Boost) or (HWEN = 0 → 1 to eanble channel), i.e.BSTEN and HWEN need pull low to unlock 11 : No change, follow before setting
		2	BUCK_OV_LATCH	0	RW	Buck discharge or latch off mode selection after V_O OV. 0 : R Discharge (default) 1: Latch-off mode
		1	LDO_OV_LATCH	0	RW	LDO discharge mode selection after V_O OV. 0 : R Discharge; (During DVS period won't sent OV Event to INTRB) (default) 1 : NA
		0	BOOST_OV_LATCH	0	RW	Boost latch off mode selection after V_O OV. 0 : NA (default) 1 : Latch-off mode

Addr	RegName	Bit	BitName	Default	Type	Description
0x0B	DISCHARGE	7	BUCK_DIS	1	RW	Buck active output discharge. 0 : Disable 1 : Enable (default)
		6	LDO_DIS	1	RW	LDO active output discharge. 0 : Disable 1 : Enable (default)
		5	BOOST_DIS	1	RW	Boost active output discharge. 0 : Disable 1 : Enable (default)
		4	Reserved	0	RW	Reserved
		3	Reserved	0	RW	Reserved
		2	BUCK2_DIS	1	RW	Buck2 active output discharge. 0 : Disable 1 : Enable (default)
		1	BCTRL	0	WC	Boost registers keep and reset control. Self reset function: it can recover to 0 when set 1 : 0 : Keep Boost relative Reg value Register0x05[7], 0x05[5:2], 0x08[7:0], 0x0A[5], 0x0A[0], 0x14[3:2], 0x37[5], 0x37[3:2] Boost relative bits. (default) 1 : Boost relative Reg recover to default value. When HWEN OFF and BCTRL = 0 (default), Boost keeps relative Reg. When HWEN ON and BCTRL = 1, Boost recover to default value. BCTRL become 0 automatically, Boost relative Reg is kept. When HWEN ON and BCTRL = 0, Boost relative can be written normally. When write 1 then it will recover to 0.
		0	Reserved	0	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x0C	Buck_Vout	7:0	Buck_Vout [7:0]	00101000	RW	Buck output voltage can be set default voltage from 0.8V to 3.3V with 12.5mV/step. 00000000 : 0.6V 00000001 : 0.6125V … 00101000 : 1.1V (default) … 11010111 : 3.2875V 11011000 : 3.3V … 11111111: 3.3V

Addr	RegName	Bit	BitName	Default	Type	Description
0x0D	LDO1_Vout	7:1	LDO1_ Vout[6:0]	1011000	RW	LDO1 output voltage can be set default voltage from 0.6V to 3.775V with 25mV/step. 0000000 : 0.6V 0000001 : 0.625V … 1011000 : 2.8V (default) … 1111110 : 3.75V 1111111 : 3.775V
		0	Reserved	0	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x0E	LDO2_Vout	7:1	LDO2_ Vout[6:0]	1011000	RW	LDO2 output voltage can be set default voltage from 0.6V to 3.775V with 25mV/step. 0000000 : 0.6V 0000001 : 0.625V … 1011000 : 2.8V (default) … 1111110 : 3.75V 1111111 : 3.775V
		0	Reserved	0	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x0F	LDO3_Vout	7:1	LDO3_ Vout[6:0]	0110000	RW	LDO3 output voltage can be set default voltage from 0.6V to 3.775V with 25mV/step. 0000000 : 0.6V 0000001 : 0.625V … 0110000 : 1.8V (default) … 1111110 : 3.75V 1111111 : 3.775V
		0	Reserved	0	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x10	LDO4_Vout	7:1	LDO4_ Vout[6:0]	0110000	RW	LDO4 output voltage can be set default voltage from 0.6V to 3.775V with 25mV/step. 0000000 : 0.6V 0000001 : 0.625V … 0110000 : 1.8V (default) … 1111110 : 3.75V 1111111 : 3.775V
		0	Reserved	0	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x11	Boost_Vout	7:2	Boost_ Vout[5:0]	010100	RW	Boost output voltage can be set default voltage from 4.5V to 5.5V with 25mV/step. 000000 : 4.5V 000001 : 4.525V … 010100: 5.0V (default) … 100111: 5.475V 101000: 5.5V … 111111: 5.5V
		1:0	LDO_SS	01	RW	Voltage scaling slew rate for LDO. 00 : 100mV/μs 01 : 50mV/μs (default) 10 : 25mV/μs 11 : 12.5mV/μs

Addr	RegName	Bit	BitName	Default	Type	Description
0x12	Buck2_Vout	7:0	Buck2_ Vout[7:0]	10110100	RW	Buck2 output voltage can be set default voltage from 0.6V to 3.3V with 12.5mV/step. 00000000 : 0.6V 00000001 : 0.6125V … 10110100 : 2.85V (default) … 11010111 : 3.2875V 11011000 : 3.3V … 11111111: 3.3V

Addr	RegName	Bit	BitName	Default	Type	Description
0x13	LX_SR	7:6	Buck_SR [1:0]	01	RW	Buck SW on/off speed set. Decrease SW speed can help the EMI performance. 00 : Slower 01 : Slow (default) 10 : Normal 11 : Fast
		5:4	Buck2_SR [1:0]	01	RW	Buck2 SW on/off speed set. Decrease SW speed can help the EMI performance. 00 : Slower 01 : Slow (default) 10 : Normal 11 : Fast
		3	Reserved	0	RW	Reserved
		2	Reserved	0	RW	Reserved
		1:0	Boost_SR [1:0]	10	RW	Boost SW on/off speed set. Decrease SW speed can help the EMI performance. 00 : Fast 01 : Normal 10 : Slow (default) 11 : Slower

Addr	RegName	Bit	BitName	Default	Type	Description
0x14	DVS	7:6	BUCK_ DVS	01	RW	Voltage scaling slew rate for Buck. 00 : 7mV/μs 01 : 4mV/μs (default) 10 : 2mV/μs 11 : 1mV/μs
		5:4	LDO_DVS	01	RW	Voltage scaling slew rate for LDO. 00 : 36mV/μs 01 : 14mV/μs (default) 10 : 8.5mV/μs 11 : 4mV/μs
		3:2	BOOST_ DVS	01	RW	Voltage scaling slew rate for Boost. 00 : 32mV/μs 01 : 15mV/μs (default) 10 : 8mV/μs 11 : 4mV/μs
		1	Reserved	0	RW	Reserved
		0	INT_CLS	0	WC	Interrupt clear pin. 0 : Normal operation (default) 1 : Refresh interrupt bits. (After write “1”, the bit will auto return to “0”.)

Addr	RegName	Bit	BitName	Default	Type	Description
0x15	UV_EVT	7	BUCK_ UV_EVT	0	RC	Buck under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck UV event detected
		6	LDO1_ UV_EVT	0	RC	LDO1 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO1 UV event detected
		5	LDO2_ UV_EVT	0	RC	LDO2 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO2 UV event detected
		4	LDO3_ UV_EVT	0	RC	LDO3 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO3 UV event detected
		3	LDO4_ UV_EVT	0	RC	LDO4 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO4 UV event detected
		2	BOOST_ UV_EVT	0	RC	Boost under-voltage threshold sense acknowledgement.(raising trigger) 0 : No fault or be masked (default) 1 : Boost UV event detected
		1	BUCK2_ UV_EVT	0	RC	Buck2 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck2 UV event detected
		0	BOOST_ FAULT_ EVT	0	RC	Boost SCP (VOUT < 0.7V) or VDS protect (VIN – VOUT > 300mV) or IL > 5A internal Boost FAULT 0 : Not fault or be masked (default) 1 : Boost fault event detected

Addr	RegName	Bit	BitName	Default	Type	Description
0x16	OV_EVT	7	BUCK_ OV_EVT	0	RC	Buck over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck OV event detected
		6	LDO1_ OV_EVT	0	RC	LDO1 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO1 OV event detected
		5	LDO2_ OV_EVT	0	RC	LDO2 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO2 OV event detected
		4	LDO3_ OV_EVT	0	RC	LDO3 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO3 OV event detected
		3	LDO4_ OV_EVT	0	RC	LDO4 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO4 OV event detected
		2	BOOST_ OV_EVT	0	RC	Boost over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Boost OV event detected
		1	BUCK2_ OV_EVT	0	RC	Buck2 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck2 OV event detected
		0	Reserved	0	RC	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x17	OCP_EVT	7	BUCK_ OCP_EVT	0	RC	Buck over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck OCP event detected
		6	LDO1_ OCP_EVT	0	RC	LDO1 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO1 OCP event detected
		5	LDO2_ OCP_EVT	0	RC	LDO2 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO2 OCP event detected
		4	LDO3_ OCP_EVT	0	RC	LDO3 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO3 OCP event detected
		3	LDO4_ OCP_EVT	0	RC	LDO4 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO4 OCP event detected
		2	BOOST_ OCP_EVT	0	RC	Boost over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Boost OCP event detected
		1	BUCK2_ OCP_EVT	0	RC	Buck2 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck2 OCP event detected
		0	Reserved	0	RC	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x19	BASE_EVT	7	TWARN_ EVT	0	RC	Thermal warning sense acknowledgement. (raising/falling trigger) 0 : No fault or be masked (default) 1 : Thermal warning event detected
		6	TSD_EVT	0	RC	Thermal shutdown sense acknowledgement. (raising/falling trigger) 0 : No fault or be masked (default) 1 : Thermal shutdown event detected
		5	VSYSUV_ EVT	0	RC	VSYS under-voltage sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Under-voltage event detected
		4	VSYSOV_ EVT	0	RC	VSYS over-voltage sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Over-voltage event detected
		3:0	Reserved	0000	RC	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x2A	Revision ID	7:0	RID[7:0]	00000011	R	Chip revision 00000000 : 1st Version 00000001 : 2nd Version 00000010 : 3rd Version 00000011 : 4th Version (default) ... 11111111 : 256th Version

Addr	RegName	Bit	BitName	Default	Type	Description
0x2B	UV_STAT	7	BUCK_UV_STAT	0	R	Buck under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		6	LDO1_UV_STAT	0	R	LDO1 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		5	LDO2_UV_STAT	0	R	LDO2 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		4	LDO3_UV_STAT	0	R	LDO3 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		3	LDO4_UV_STAT	0	R	LDO4 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		2	BOOST_UV_STAT	0	R	Boost under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		1	BUCK2_UV_STAT	0	R	Buck2 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		0	BOOST_FAULT_STAT	0	R	Boost SCP (VOUT < 0.7V) or VDS protect (VIN – VOUT > 300mV) or IL > 5A internal boost FAULT status. 0 : No fault occurs (default) 1 : Fault occurs

Addr	RegName	Bit	BitName	Default	Type	Description
0x2C	OV_STAT	7	BUCK_OV_STAT	0	R	Buck over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		6	LDO1_OV_STAT	0	R	LDO1 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		5	LDO2_OV_STAT	0	R	LDO2 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		4	LDO3_OV_STAT	0	R	LDO3 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		3	LDO4_OV_STAT	0	R	LDO4 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		2	BOOST_OV_STAT	0	R	Boost over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		1	BUCK2_OV_STAT	0	R	Buck2 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs
		0	Reserved	0	R	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x2D	OCP_STAT	7	BUCK_OCP_STAT	0	R	Buck over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs
		6	LDO1_OCP_STAT	0	R	LDO1 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs
		5	LDO2_OCP_STAT	0	R	LDO2 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs
		4	LDO3_OCP_STAT	0	R	LDO3 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs
		3	LDO4_OCP_STAT	0	R	LDO4 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs
		2	BOOST_OCP_STAT	0	R	Boost over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs
		1	BUCK2_OCP_STAT	0	R	Buck2 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs
		0	Reserved	0	R	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x2F	BASE_STAT	7	TWARN_STAT	0	R	Thermal warning sense status. 0 : No fault occurs (default) 1 : Fault occurs
		6	TSD_STAT	0	R	Thermal shutdown sense status. 0 : No fault occurs (default) 1 : Fault occurs
		5	VSYSUV_STAT	0	R	VSYS under-voltage sense status. 0 : No fault occurs (default) 1 : Fault occurs
		4	VSYSOV_STAT	0	R	VSYS over-voltage sense status. 0 : No fault occurs (default) 1 : Fault occurs
		3	SEQ_ON	0	R	It indicates status of the internal SEQ_ON signal. 0 : SEQ OFF (default) 1 : SEQ ON
		2:0	Reserved	000	R	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x30	EN_FLG	7	BUCK_EN_FLG	0	R	Indicate Buck final enable status. 0 : Disable (default) 1 : Enable
		6	LDO1_EN_FLG	0	R	Indicate LDO1 final enable status. 0 : Disable (default) 1 : Enable
		5	LDO2_EN_FLG	0	R	Indicate LDO2 final enable status. 0 : Disable (default) 1 : Enable
		4	LDO3_EN_FLG	0	R	Indicate LDO3 final enable status. 0 : Disable (default) 1 : Enable
		3	LDO4_EN_FLG	0	R	Indicate LDO4 final enable status. 0 : Disable (default) 1 : Enable
		2	BOOST_EN_FLG	0	R	Indicate BOOST final enable status. 0 : Disable (default) 1 : Enable
		1	BUCK2_EN_FLG	0	R	Indicate Buck2 final enable status. 0 : Disable (default) 1 : Enable
		0	Reserved	0	R	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x32	UV_MASK	7	BUCK_UV_MASK	0	RW	Buck under-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		6	LDO1_UV_MASK	0	RW	LDO1 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		5	LDO2_UV_MASK	0	RW	LDO2 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		4	LDO3_UV_MASK	0	RW	LDO3 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		3	LDO4_UV_MASK	0	RW	LDO4 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		2	BOOST_UV_MASK	0	RW	Boost under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		1	BUCK2_UV_MASK	0	RW	Buck2 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		0	BOOST_FAULT_MASK	0	RW	Boost SCP (VOUT < 0.7V) or VDS protect (VIN – VOUT > 300mV) or IL > 5A internal boost FAULT mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked

Addr	RegName	Bit	BitName	Default	Type	Description
0x33	OV_MASK	7	BUCK_ OV_MASK	0	RW	Buck over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		6	LDO1_OV _MASK	0	RW	LDO1 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		5	LDO2_OV _MASK	0	RW	LDO2 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		4	LDO3_ OV_MASK	0	RW	LDO3 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		3	LDO4_ OV_MASK	0	RW	LDO4 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		2	BOOST_ OV_MASK	0	RW	Boost over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		1	BUCK2_ OV_MASK	0	RW	Buck2 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		0	Reserved	0	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x34	OCP_MASK	7	BUCK_ OCP_ MASK	0	RW	Buck over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		6	LDO1_ OCP_ MASK	0	RW	LDO1 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		5	LDO2_ OCP_ MASK	0	RW	LDO2 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		4	LDO3_ OCP_ MASK	0	RW	LDO3 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		3	LDO4_ OCP_ MASK	0	RW	LDO4 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		2	BOOST_ OCP_ MASK	0	RW	Boost over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		1	BUCK2_ OCP_ MASK	0	RW	Buck2 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		0	Reserved	0	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x36	BASE_ MASK	7	TWARN_ MASK	0	RW	Thermal warning sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		6	TSD_ MASK	0	RW	Thermal shutdown sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		5	VSYSUV_ MASK	0	RW	VSYS under-voltage sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		4	VSYSOV_ MASK	0	RW	VSYS over-voltage sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		3:0	Reserved	0000	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x37	CHx_PT	7	BUCK_OC _LATCH	0	RW	Buck Hiccup or latch off mode selection after current limit. 0 : Hiccup mode; (Hiccup 3 times will enter latch-off mode. Hiccup on/off time = 4ms / 8ms) (default) 1 : Latch-off mode.
		6	LDO_OC_ LATCH	0	RW	LDO Hiccup or latch off mode selection after current limit. 0 : Hiccup mode; (Hiccup 3 times will enter latch-off mode. Hiccup on/off time = 2ms/40ms) (default) 1 : Latch-off mode.
		5	BOOST_ OC_ LATCH	0	RW	BOOST Hiccup or latch off mode selection after current limit. 0 : Hiccup mode; (Hiccup 3 times will enter latch-off mode, hiccup on/off time = 10ms/100ms) (default) 1 : Latch-off mode.
		4	Reserved	0	RW	Reserved
		3:2	BST_UV_ DT[1:0]	11	RW	Boost UV deglitch time selection : 00 : 10μs 01 : 15μs 10 : 25μs 11: 50μs (default)
		1:0	Reserved	00	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x38	CHx_deglitch time	7:6	Buck_UV_DT[1:0]	11	RW	Buck UV deglitch time selection : 00 : 5μs 01 : 10μs 10 : 15μs 11 : 50μs (default)
		5:4	Buck_OV_DT[1:0]	11	RW	Buck OV deglitch time selection : 00 : 10μs 01 : 15μs 10 : 20μs 11 : 50μs (default)
		3:2	LDO_UV_DT[1:0]	11	RW	LDO UV deglitch time selection : 00 : 10μs 01 : 15μs 10 : 30μs 11 : 50μs (default)
		1:0	LDO_OV_DT[1:0]	11	RW	LDO OV deglitch time selection : 00 : 5μs 01 : 10μs 10 : 25μs 11 : 50μs (default)

Addr	RegName	Bit	BitName	Default	Type	Description
0x39	BASEPT_deglitch time	7:6	VSYSUV_DT[1:0]	11	RW	VSYSUV deglitch time selection : 00 : 70μs 01 : 135μs 10 : 265μs 11 : 525μs (default)
		5:4	VSYSOV_DT[1:0]	10	RW	VSYSOV deglitch time selection: 00 : 20μs 01 : 50μs 10 : 180μs (default) 11 : 360μs
		3	VSYSOV_PT	0	RW	VSYSOV turn off Buck 0 : When Vsys_OV occur will turn off BCK (default) 1 : When Vsys_OV occur will not turn off BCK
		2	BST_NFC_Force	0	RW	NFC load detection. 0x05[6] must set 0 when bit BST_NFC_force = 1. 0 : AUTO NFC (default) 1 : FCCM by load, turn off NFC
		1	Reserved	0	RW	Reserved
		0	Reserved	0	RW	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x3A	SEQ_ON	7:6	SEQ_ON_STAT[1:0]	00	R	It indicates the states of power on sequence 00 : SEQ_ON hasn't started or needless (default) 01 : SEQ_ON is carrying out (During SLOT1 to SLOT8 + 4ms) 10 : There are fail soft-start channels during power on sequence 11 : SEQ_ON has completed
		5:3	SEQ_COUNT[2:0]	000	R	It indicateds the fault SLOT during power on sequence at SEQ_ON_STAT = 2'b10 000 : SLOT1 (default) 001 : SLOT2 010 : SLOT3 011 : SLOT4 100 : SLOT5 101 : SLOT6 110 : SLOT7 111 : SEQ_ON has completed
		2:0	Reserved	000	R	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x3B	SSEND_CHx	7	sSSEND_BCK	0	R	It indicates Buck soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end
		6	sSSEND_LDO1	0	R	It indicates LDO1 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end
		5	sSSEND_LDO2	0	R	It indicates LDO2 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end
		4	sSSEND_LDO3	0	R	It indicates LDO3 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end
		3	sSSEND_LDO4	0	R	It indicates LDO4 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end
		2	sSSEND_BST	0	R	It indicates Boost soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end
		1	sSSEND_BCK2	0	R	It indicates Buck2 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end
		0	Reserved	0	R	Reserved

Addr	RegName	Bit	BitName	Default	Type	Description
0x42	INT_SET	7:6	Reserved	00	RW	Reserved
		5:4	INT_DEG[1:0]	00	RW	Interrupt reflash pulse width timing. 00 : disable (default) 01 : 2μs 10 : 4μs 11 : 8μs
		3:0	SEQ_STAT[2:0]	0000	R	Indicate PMU's State 0000 : IDLE (default) 0001 : ONSEQ (slot1 to slot7 + 4ms, when 4ms clock end will tigger ONSEQ_END) 0010 : ONSEQ_END 0011 : ENSEQ 0100 : OFFSEQ 0101 : OFFSEQ_END (slot7 to slot1, when slot1 sequence end will tigger OFFSEQ_END) 1111 : Else

Addr	RegName	Bit	BitName	Default	Type	Description
0x43	PMU_STAT	7:0	PMU_STAT	00000000	R	BST latch off (BSTEN) 0 : Release (default) 1 : Latch off
						BST latch off (HWEN) 0 : Release (default) 1 : Latch off
						BCK1 latch off 0 : Release (default) 1 : Latch off
						BCK2 latch off 0 : Release (default) 1 : Latch off
						LDO1 latch off 0 : Release (default) 1 : Latch off
						LDO2 latch off 0 : Release (default) 1 : Latch off
						LDO3 latch off 0 : Release (default) 1 : Latch off
						LDO4 latch off 0 : Release (default) 1 : Latch off

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-25B 2.2x2.3 (BSC) package, the thermal resistance, θ_{JA}, is 31.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (32.7°C/W) = 3.05W for a WL-CSP-25B 2.2x2.3 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

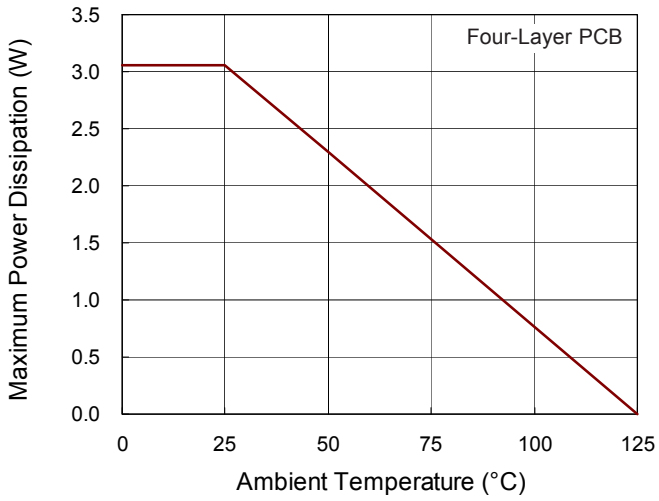


Figure 10. Derating Curve of Maximum Power Dissipation

Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT5112A. Both the high current and the fast switching nodes demand full attention to the PCB layout to keep the robustness of the RT5112A through the PCB layout. Improper layout might lead to the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT5112A, the following PCB layout guidelines must be strictly followed.

- The trace from switching node to inductor should be as short as possible to minimized the switching loop for better EMI.
- Place the input and output capacitors close to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- Connect the AGND, DGND, GNDB1 and GNDB2 to a strong ground plane for maximum thermal dissipation and noise protection.
- Directly connect the Buck output capacitors to the feedback network to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

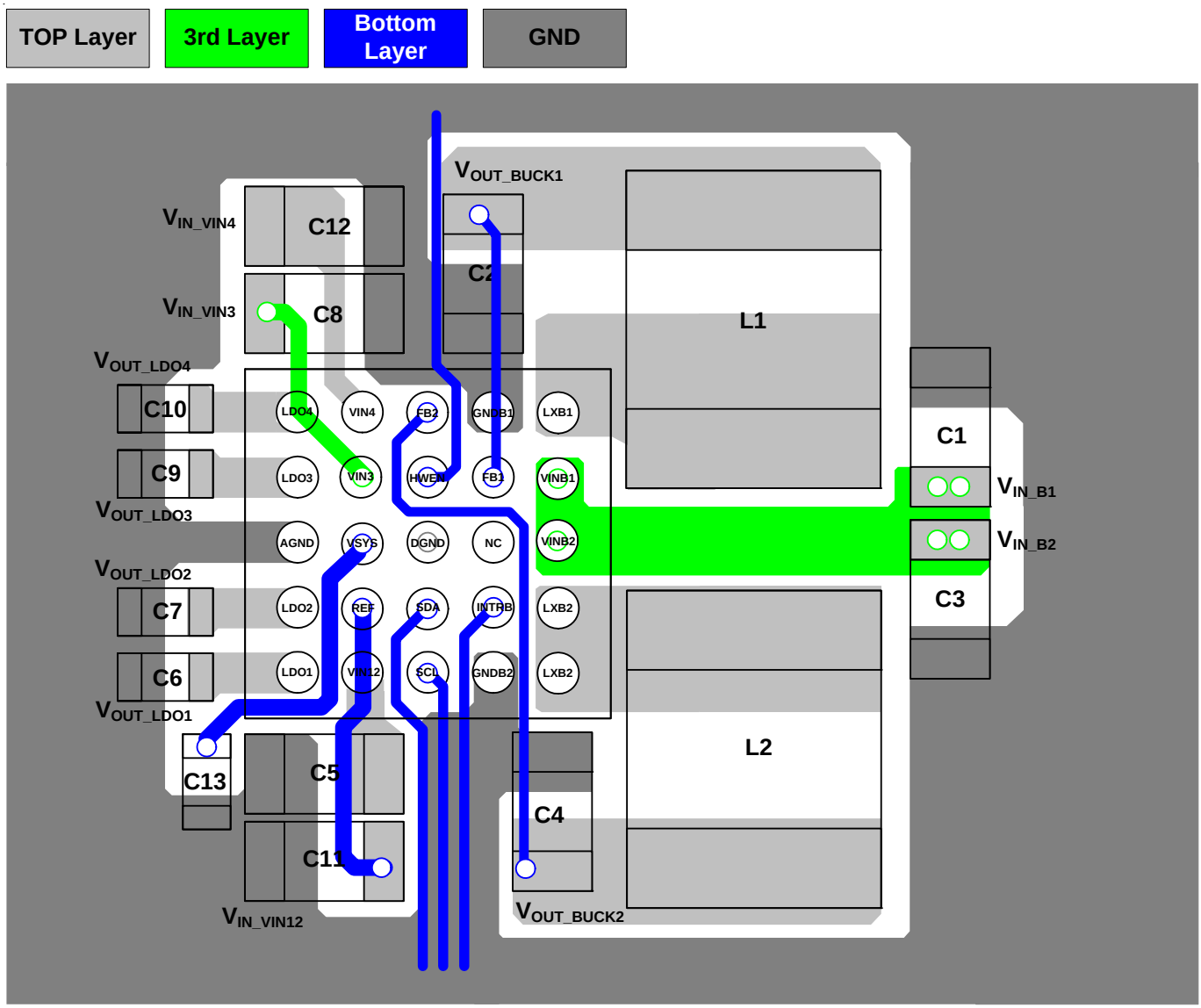
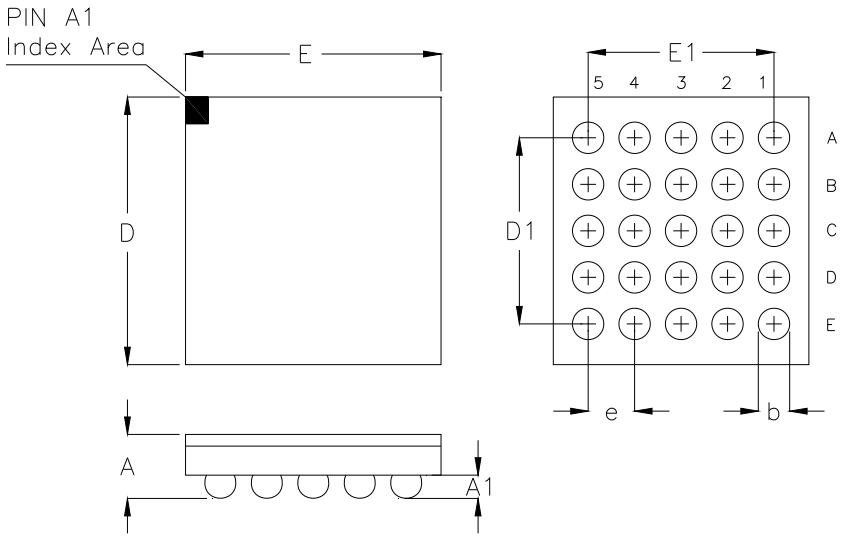


Figure 11. PCB Layout Guide

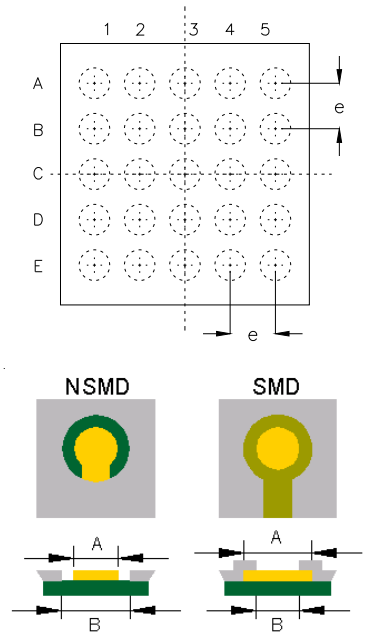
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.260	2.340	0.089	0.092
D1	1.600		0.063	
E	2.160	2.240	0.085	0.088
E1	1.600		0.063	
e	0.400		0.016	

25B WL-CSP 2.2x2.3 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.2x2.3-25(BSC)	25	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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