Wide Input and Ultra-Low Quiescent Current Boost Converter with High Efficiency

General Description

The RT4823N allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The RT4823N is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed to a maximum load current of 1500mA. Quiescent current in shutdown mode is less than 1μA, which maximizes battery life. The regulator transitions smoothly between bypass and normal boost mode. The device can be forced into bypass mode to reduce quiescent current.

The RT4823N is available in the WL-CSP-9B 1.3x1.2 (BSC) package.

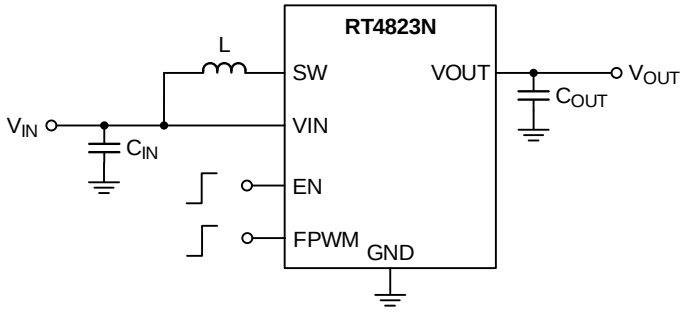
Applications

- NFC Device Power Supply
- USB Charging Ports
- PC Accessory Application (Keyboard, Mouse...etc.)
- TWS (True Wireless Stereo) Hall Sensor
- Gaming Device Sensor

Features

- **Ultra-Low Operating Quiescent Current**
- **Quickly Start-Up Time (< 430μsec)**
- **3 Few External Components: 1μH Inductor, 0402 Case Size Input and 0603 Case Size Output Case Size Capacitors**
- **Input Voltage Range: 1.8V to 5.5V**
- **Support V_{IN} > V_{OUT} Operation**
- **Default Boost Output Voltage Setting: V_{OUT} = 5V**
- **Maximum Continuous Load Current: 1.5A at V_{IN} > 3V Boosting V_{OUT} to 5V**
- **Up to 93% Efficiency**
- **EN(H), FPWM(H): Forced PWM Mode**
- **EN(H): Boost Mode**
- **EN(L): Shutdown Mode**
- **Internal Synchronous Rectifier**
- **Overcurrent Protection**
- **Cycle-by-Cycle Current Limit**
- **Overvoltage Protection**
- **Short-Circuit Protection**
- **Over-Temperature Protection**
- **Small WL-CSP-9B 1.3x1.2 (BSC) Package**

Simplified Application Circuit



Ordering Information

RT4823N □

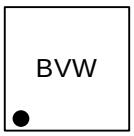
Package Type
WSC: WL-CSP-9B 1.3x1.2 (BSC)

Note:

Richtek products are:

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

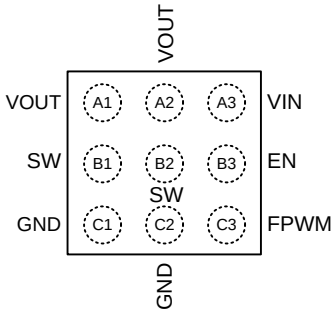
Marking Information



BV: Product Code
W: Date Code

Pin Configuration

(TOP VIEW)

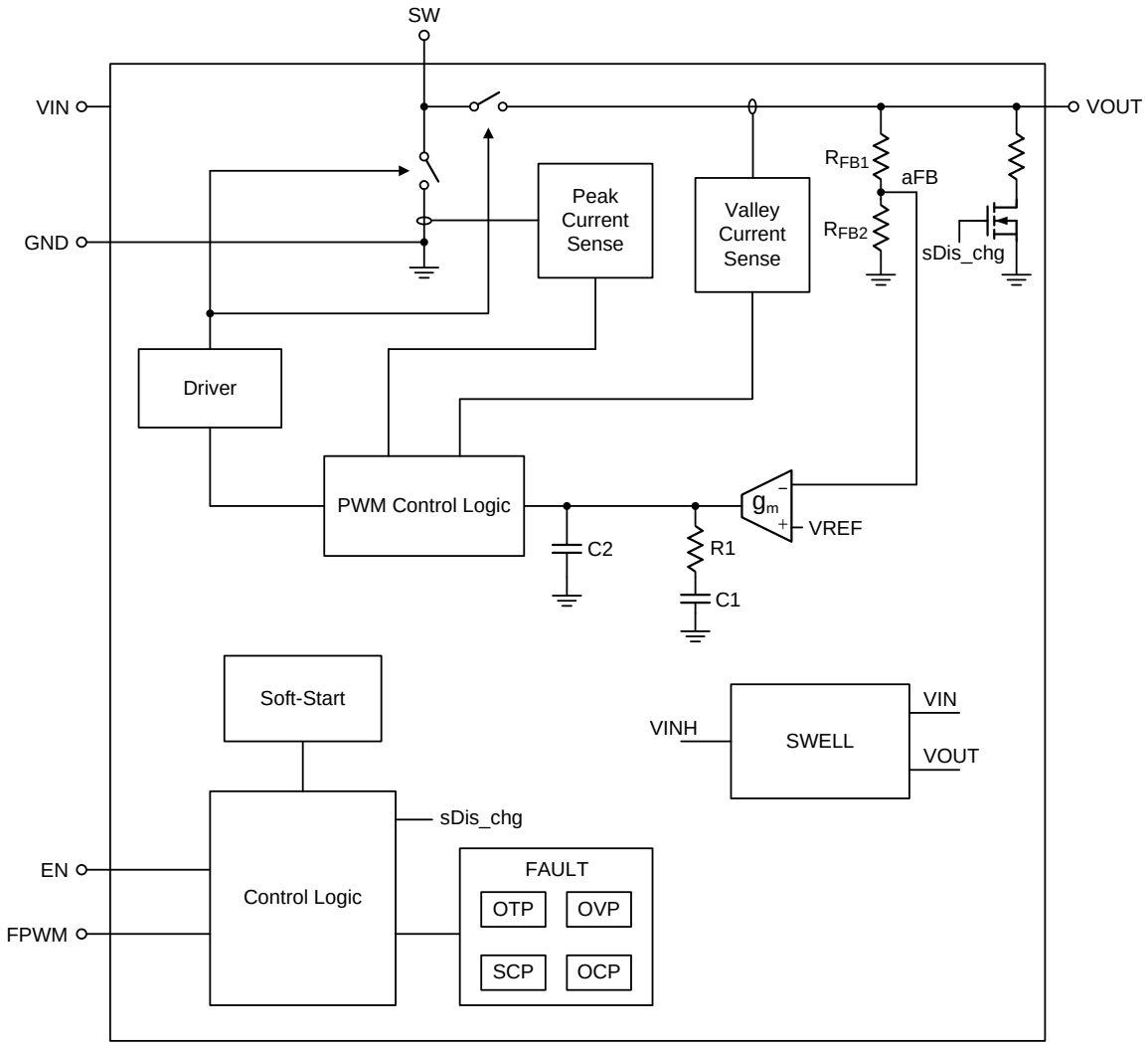


WL-CSP-9B 1.3x1.2 (BSC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, A2	VOUT	Output voltage. Place COUT as close as possible to device.
A3	VIN	Input voltage. This pin has to connect to input power, it is used to supply chip internal power.
B1, B2	SW	Switching node. The power inductor should be connected between SW and power input.
B3	EN	Enable. When this pin is set to HIGH, the circuit is enabled. Do not let this pin floating.
C1, C2	GND	Ground. This is power and signal ground reference for the chip. The COUT bypass capacitor should be returned with the shortest path possible to these pins.
C3	FPWM	Force PWM mode. This pin is used to control converter into force PWM mode. When this pin is set to HIGH, the circuit is into FPWM mode. Do not let this pin floating.

Functional Block Diagram



Operation

The RT4823N combined built-in power transistors, synchronous rectification, and low supply current, it provides a compact solution for system using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed to maximum load current of 1.5A. Quiescent current in Shutdown mode is less than 1μA, which maximizes battery life.

Power-On Reset

If input voltage is lower than POR, the internal digital and analog circuit is disable. If input voltage is higher than POR the Boost converter behavior is shown as below:

1. IC Digital circuit is activated.
2. After turn-on EN pin, internal registers start to load the default value by eFuse.
3. Boost converter is into run free-running mode (detail in free-running mode section).
4. If V_{OUT} > 2.2V (or V_{IN} > 2.2V), Boost converter will into close loop control.

Figure 1and Figure 2 show eFuse download diagram and flow chart. When input voltage is higher than POR and EN go high, eFuse start to load in digital circuit. The deglitch time is 3μs to 15μs (max.), and eFuse download time is 16μs to 24μs (max.). When eFuse data start to download, the RT4823N internal circuit make sure download progress finish unless VIN < POR threshold.

Free-Running Mode

If both voltage of V_{IN} and V_{OUT} are lower than 2.2V, the Boost converter will into free-running mode. In this mode, switching frequency operation is 1.5MHz and duty cycle of Boost converter is 25%. It is translation of power-on stage, and there is implemented current limit function for converter soft-start. The current limit level should be lower than 900mA.

EN and FPWM

In the Table 1 shown, there are three device states in the RT4823N. When EN and FPWM pull low, it is into shutdown mode and quiescent current is less than 1μA. If EN pull high, the RT4823N is into boost mode and it is with low quiescent operation. When the RT4823N is in the boost mode and pull high FPWM, the RT4823N is into FPWM mode. There should be a delay time (< 250μs) from EN pull high to power ready to guarantee normal operation.

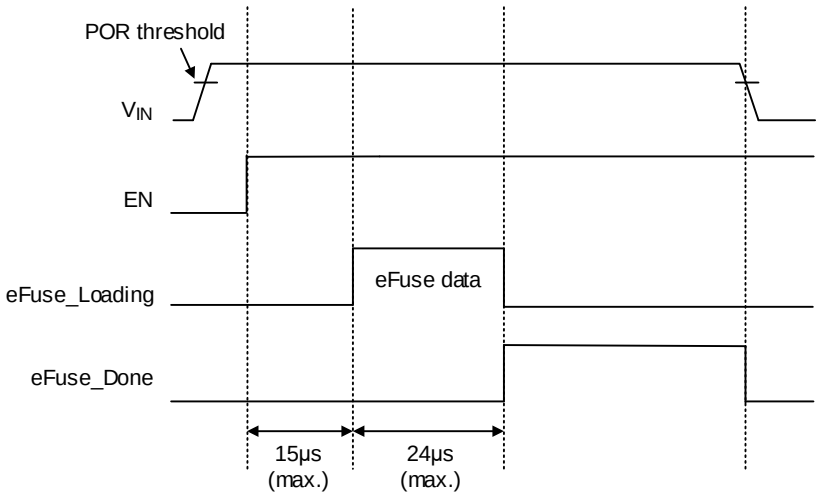


Figure 1. eFuse Download Timing Diagram

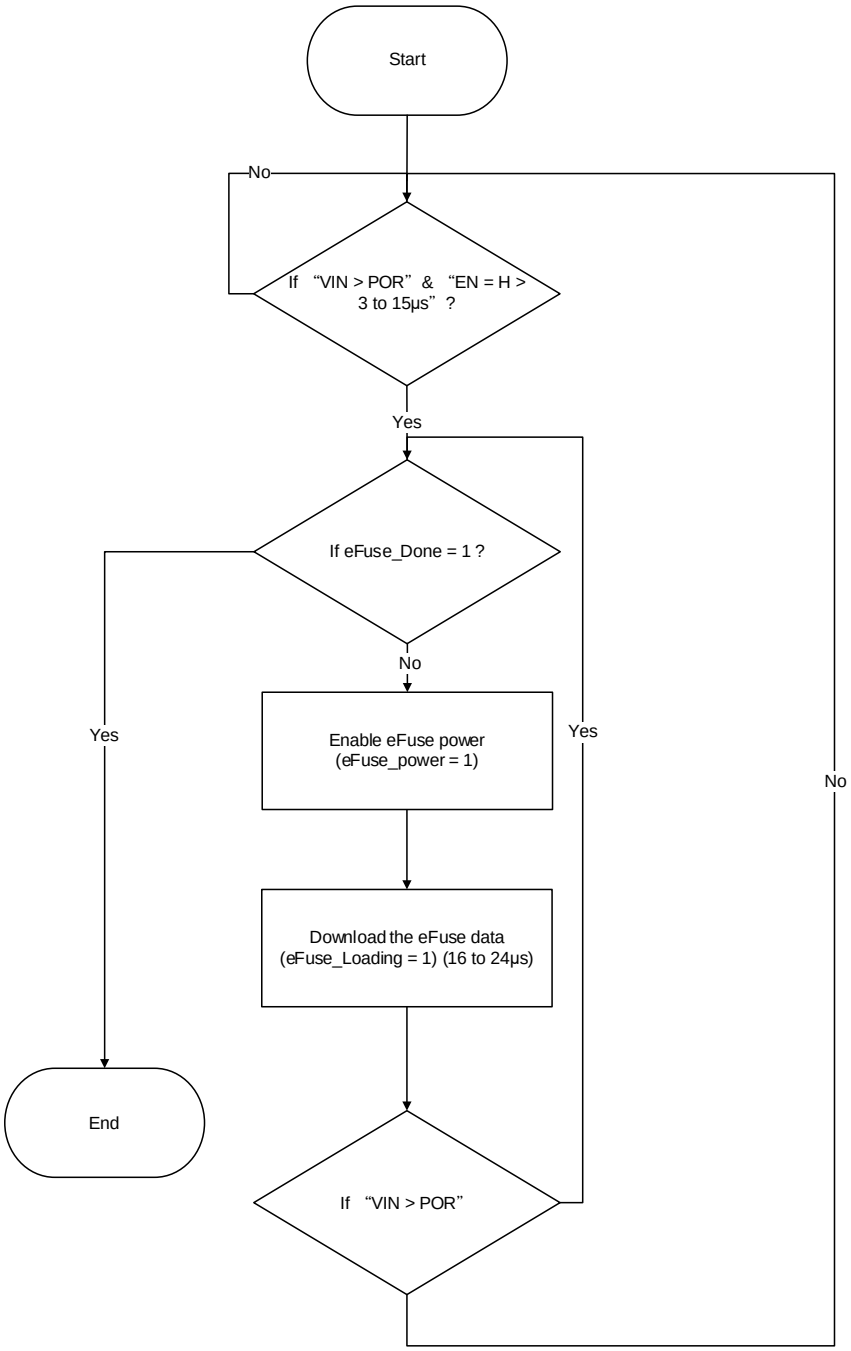


Figure 2. eFuse Download Flow Chart

Table 1. Pin Configuration for Converter

EN Input	FPWM Input	Mode Define	Device State
0	0	Shutdown mode	The device is shutdown. The device shutdown current is approximately about 1μA (max.).
1	0	Boost PFM	The device is active in Boost PFM low quiescent mode. The supply current is approximately about 4μA (typ.).
1	1	Boost PWM	The device is into force PWM mode.

Enable

The boost can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating follow Figure 2 operation diagram. In shutdown mode, the converter stops switching, internal control circuit is turned off. The output voltage is discharging by component consumption (Cap ESR...) that state have not discharge function.

Soft-Start State

During soft-start state, if VOUT reach to 99% V_{OUT_Target}. The RT4823N will into boost operation. When system power-on with heavy loading (higher than pre-charge current), the RT4823N is in pre-charge state until loading release.

Boost/Auto Bypass Mode

EN = H There are two normal operation modes, one is the boost mode, and the other one is auto bypass mode. In the boost mode (V_{IN} – 0.3V < V_{OUT_Target}), the converter boost output voltage to V_{OUT_Target}, it delivers power to loading by internal synchronous switches after the soft-start state. In the auto bypass mode (V_{IN} – 0.3V ≥ V_{OUT_Target}), input voltage will deliver and through to the output terminal loading directly. That can provide max current capacity with the RT4823N. Detail information is shown as below.

Boost Mode (Auto PFM/PWM Control Method)

In order to save power and improve efficiency at low loads, the Boost operate in PFM (Pulse Frequency Modulation) as the inductor drops into DCM (Discontinuous Current Mode). The switching frequency is proportional to loading to reach output voltage regulation. When loading is increase and inductor current is into continuous current mode, the Boost automatically gets in PWM mode.

Table 2. The RT4823N Start-Up Description

Mode	Description	Condition
LIN	Linear startup	V_{IN} - 200mV ≥ V_{OUT}
Soft-Start	Boost soft-start	0.99 x V_{OUT_Target} > V_{OUT} ≥ V_{IN} - 200mV
Boost	Boost mode	V_{OUT_Target} ≥ 0.99 x V_{OUT_Target}
If V_{IN} increase higher than V_{OUT}		
Auto Bypass	Auto bypass mode	V_{IN} ≥ V_{OUT} Control loop auto transfer between auto bypass mode and boost mode.

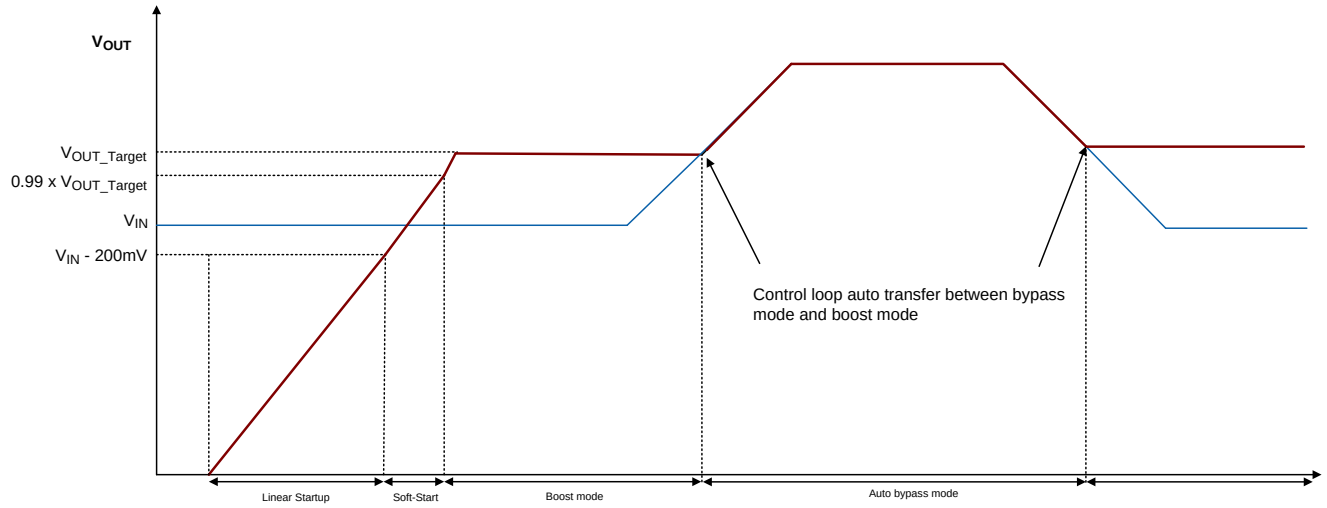


Figure 2. V_{OUT} Mode Transition Diagram with EN L to H and V_{IN} Variation (I_{OUT} = 0A)

Protection

The RT4823N features some protections are listed in below table. It is described the protection behavior.

Protection Type	Fault Event Trigger	Fault Deglitch Time	Protection Method	Fault Protection Latch Time	Reset Method
OCP_IL5A	I_{L_peak} > 5A	No delay	Turn off UG, LG	20ms, Auto-recovery	I_{L_peak} < 5A
OCP	I_{L_peak} > 3.6A	No delay	Stop LG switching	N/A	I_{L_valley} < 3.3A
OVP	V_{OUT} > 6V	100ns	Turn off UG, LG	N/A	V_{OUT} < 6V
SCP	V_{OUT} < 0.7V	No delay	Turn off UG, LG	20ms, Auto-recovery	V_{OUT} > 0.7V
OTP	TEMP > 150°C	170μs	Turn off UG, LG	Turn off UG, LG	TEMP < 130°C
SCP_SS	V_{IN} - V_{OUT} > 0.2V	2ms	UG OCP = 0.3A	N/A	V_{IN} - V_{OUT} < 0.2V

Absolute Maximum Ratings (Note 1)

- VIN, VOUT, SW, EN, FPWM ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
- WL-CSP-9B 1.3x1.2 (BSC) ---------- 1.54W
- Package Thermal Resistance (Note 2)
- WL-CSP-9B 1.3x1.2 (BSC) ---------- 64.9°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage Range (Boost Mode) ---------- 1.8V to 5.5V
- Output Voltage Range ---------- 5V
- Input Capacitor, CIN ---------- 4.7µF
- Output Capacitor, COUT ---------- 3.5µF to 50µF
- Inductance, L ---------- 0.7µH to 2.2µH
- Input Current (Average current into SW) ---------- 1.8A
- Input Current (Peak current into SW) ---------- 4A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.6V, C_{IN} = 4.7µF, C_{OUT} = 10µF, L1 = 1µH. All typical (TYP) limits apply for T_A = 25°C, unless otherwise specified. All minimum (MIN) and maximum (MAX) apply over the full operating ambient temperature range (–40°C ≤ T_A ≤ 85°C).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Operation Range	V_{IN}		1.8	--	5.5	V
Into VIN Operating Quiescent Current	$I_{Q(non-switching)}$	I_{OUT} = 0mA, V_{IN} = 3.6V, EN = FPWM = GND	--	0.1	0.5	µA
Into VOUT Standby Mode Quiescent Current	$I_{Q(non-switching)}$		--	2	3	µA
VIN Quiescent Current (Device Normal Switching)	$I_{Q(switching)}$	V_{IN} = 3.6V, V_{OUT} = 5V, FPWM = EN = GND	--	--	1	µA
		V_{IN} = 3.6V, V_{OUT} = 5V, FPWM = GND, EN = VIN	--	4	6	
		V_{IN} = 3.6V, V_{OUT} = 5V, FPWM = EN = VIN	--	10	--	mA
Power-On Reset	V_{POR}	(Note 5)	1.2	1.5	1.75	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable, FPWM						
Low-Level Input Voltage	V_{IL}		--	--	0.4	V
High-Level Input Voltage	V_{IH}		1.2	--	--	V
Input Leakage Current	I_{lkg}	Input connected to GND or VIN	--	--	0.5	μA
OUTPUT						
Regulated DC Output Voltage	V_{OUT}	1.8V ≤ V_{IN} ≤ 4.8V, I_{OUT} = 0mA, PFM operation	5.04	5.06	5.08	V
		V_{IN} = 3.6V, I_{OUT} = 1A, PWM operation	4.95	5	5.05	V
Output Discharge Resistor	$R_{DISCHARGE}$	V_{IN} = 3.6V, EN = 0V	--	100	--	Ω
Power Switch						
High-Side MOSFET	r_{DS_H}		--	80	--	mΩ
Low-Side MOSFET	r_{DS_L}		--	80	--	mΩ
Minimum On-Time	t_{ON_MIN}	V_{IN} = 1.8V to 4.8V, V_{OUT} = 5V	20	--	60	ns
Maximum Duty Cycle	D_{MAX}	V_{IN} = 1.8V, V_{OUT} = 5V, I_L = 400mA	68.8	--	--	%
Switch Peak Current Limit (V_{IN} or V_{OUT} > 2.2V)	$I_{LIM(Peak)}$	V_{IN} = 3.6V, V_{OUT} = 5V	--	3900	--	mA
Switch Valley Current Limit (V_{IN} or V_{OUT} > 2.2V)	$I_{LIM(Valley)}$	V_{IN} = 3.6V, V_{OUT} = 5V	--	3600	--	mA
Negative OCP	$I_{LIM(Neg)}$		–3000	–2000	–1000	mA
Oscilator						
Oscillator Frequency	f_{OSC}	V_{IN} = 3.6V	3	3.5	4	MHz
		V_{IN} < 2.5V → start to reduce frequency	2	--	--	
Soft-Start						
Start-Up Time	t_{START_BST}	V_{IN} = 3.6V, BP = GND, I_{OUT} = 0mA. Time from active EN to VOUT	130	430	550	μs
Pre-Charge Current Limit	$I_{LIM(Start)}$	V_{IN} = 3.6V, EN = 0 → 1.8V	250	300	350	mA
Protection						
Short-Circuit Protection	V_{SCP}		0.5	0.7	0.9	V
Over-Temperature Protection	T_{OTP}		140	150	160	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Overcurrent Protection	$I_{LIM(5A)}$	V_{IN} = 5V	4	5	5.5	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Efficiency						
Efficiency	Eff	V_{OUT} = 5V, V_{IN} = 3.6V, Load = 10μA	--	72	--	%
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 10mA	--	90	--	
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 600mA	--	93	--	
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 1000mA	--	91	--	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the case top of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Typical Application Circuit

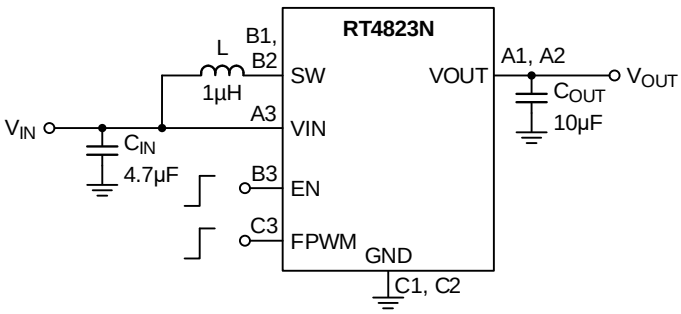
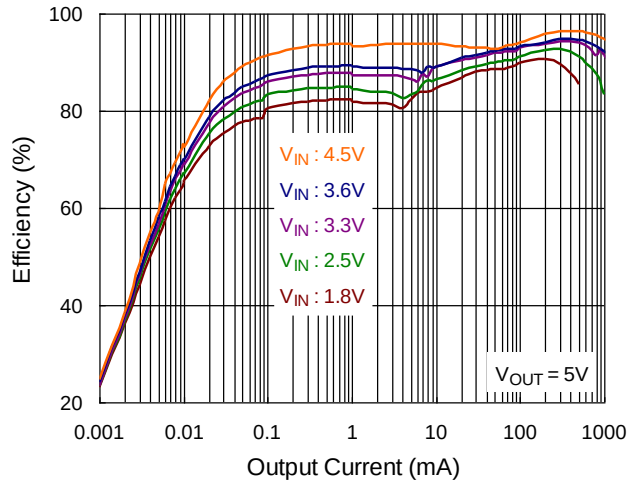


Table 3. Recommended Components Information

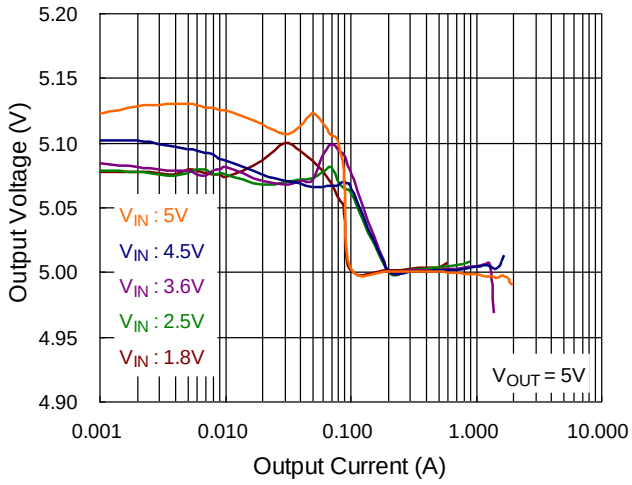
Reference	Part Number	Description	Package	Manufacturer
CIN	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
COUT	GRM188R60J106ME47D	10µF/6.3V/X5R	0603	Murata
L	DFE252012F-1R0M=P2	1.0µH/3.3A	2.5x2.0x1.2mm	Murata

Typical Operating Characteristics

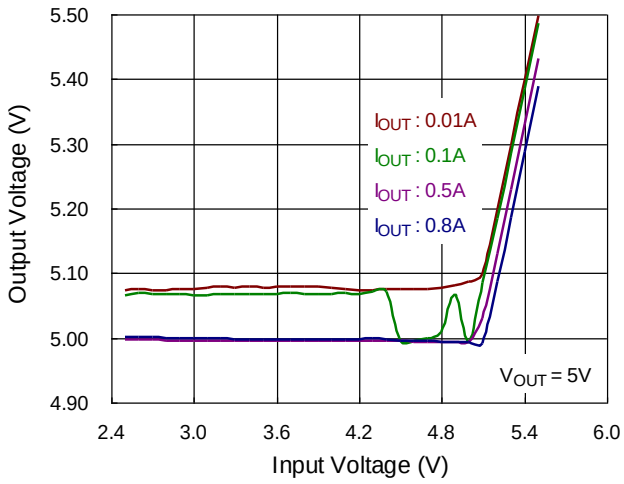
Efficiency vs. Output Current



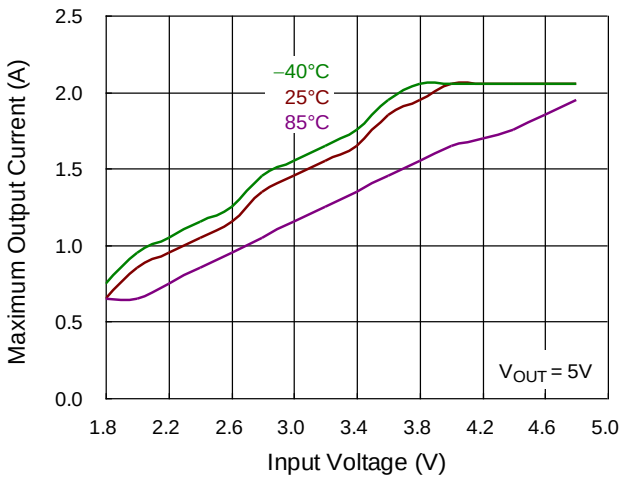
Boost Load Regulation



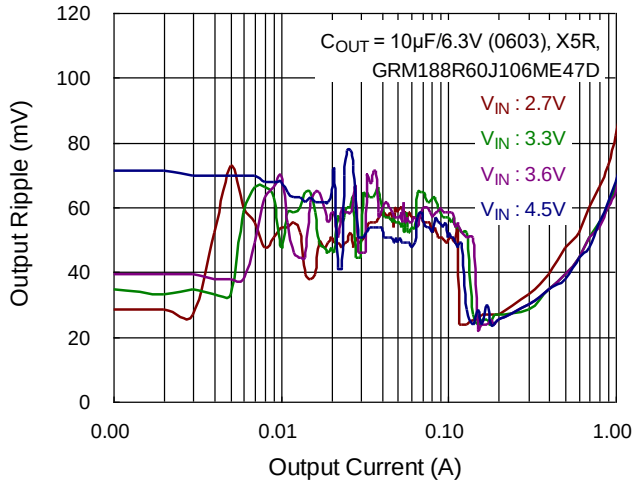
Boost Line Regulation



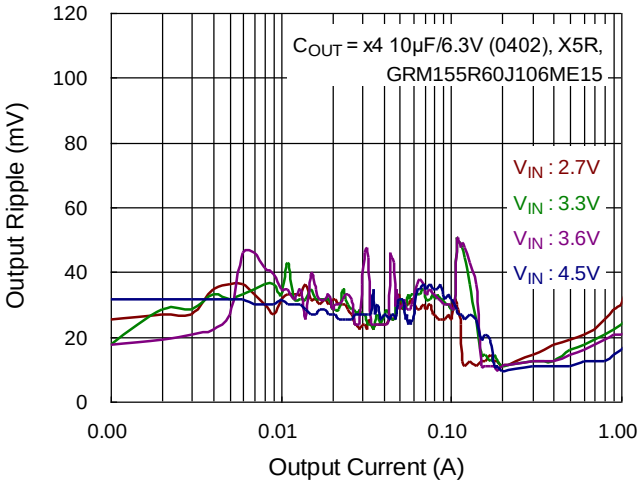
Maximum Output Current vs. Input Voltage



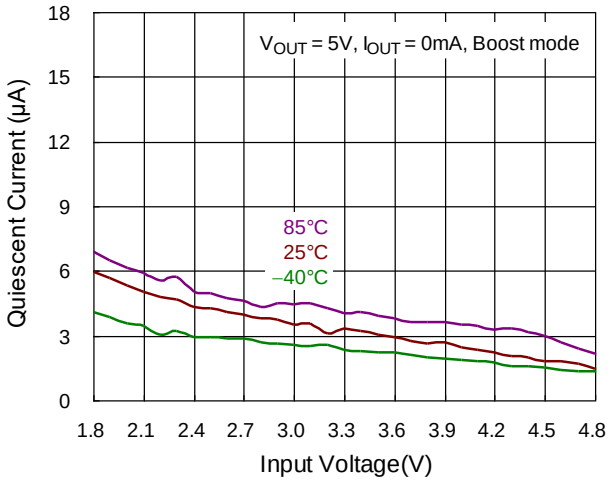
Output Ripple vs. Output Current



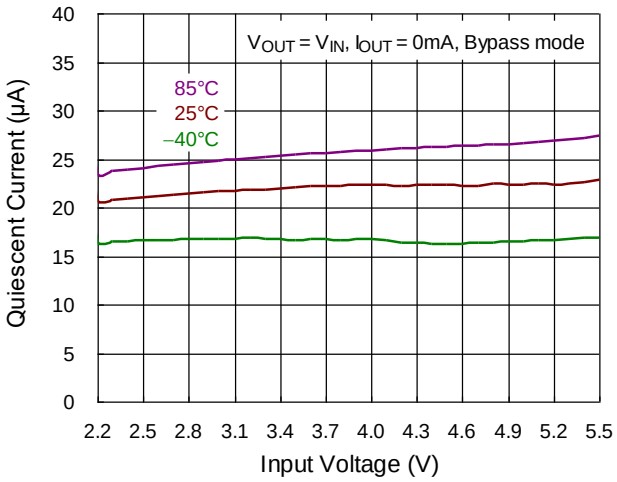
Output Ripple vs. Output Current



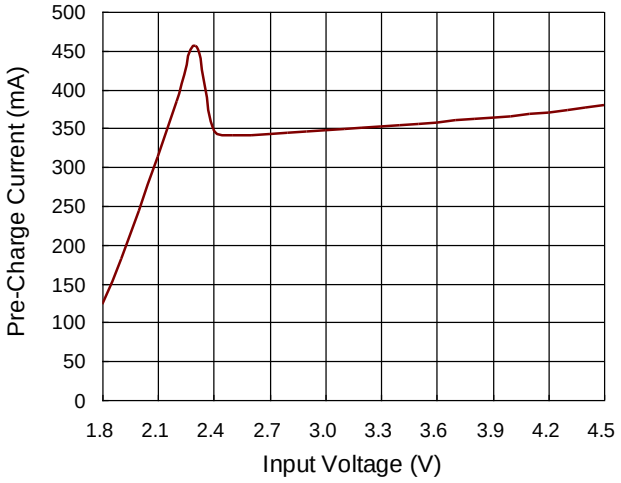
Quiescent Current vs. Input Voltage



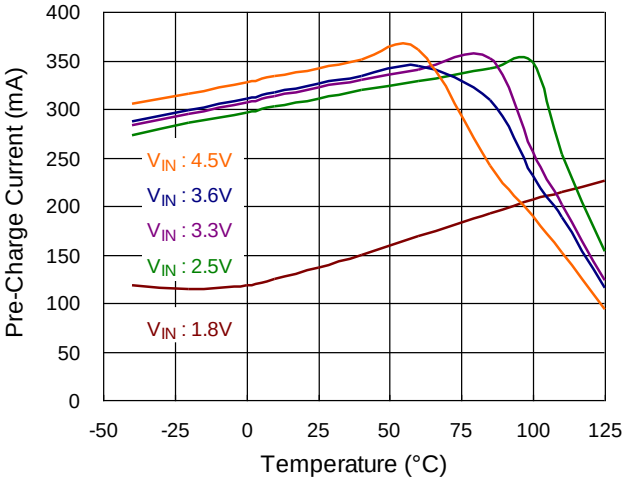
Quiescent Current vs. Input Voltage



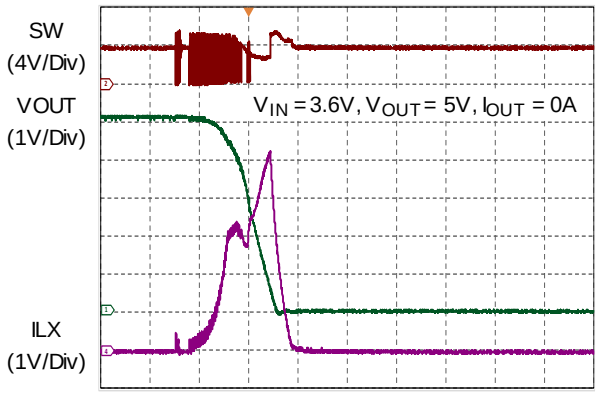
Pre-Charge Current vs. Input Voltage



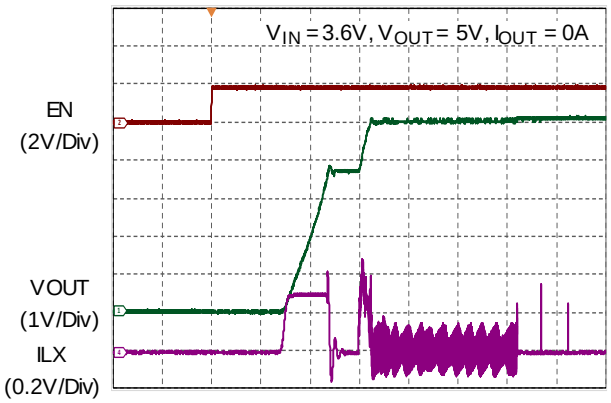
Pre-Charge Current vs. Temperature



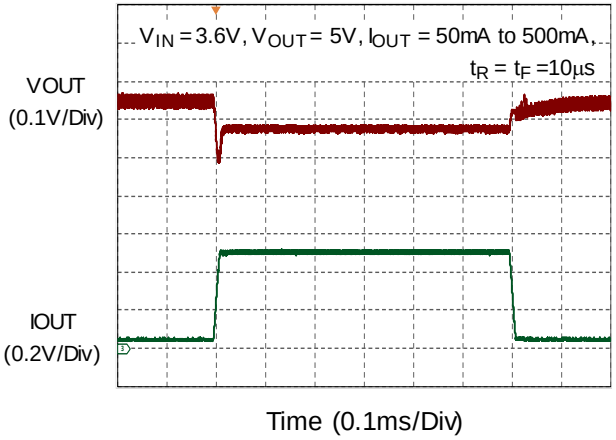
Boost Short Circuit



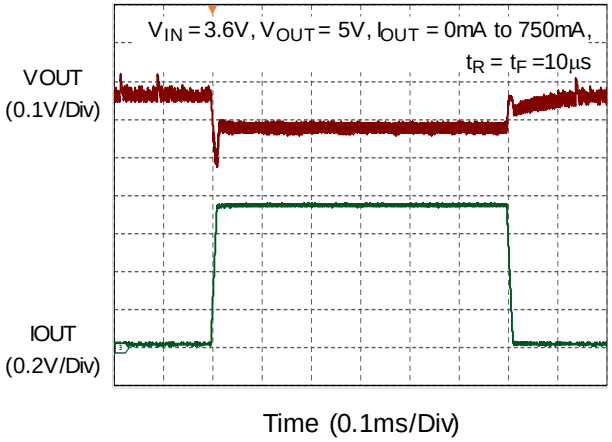
Power-On



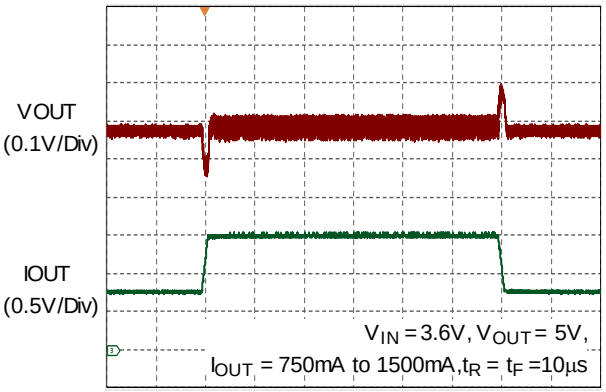
Load Transient



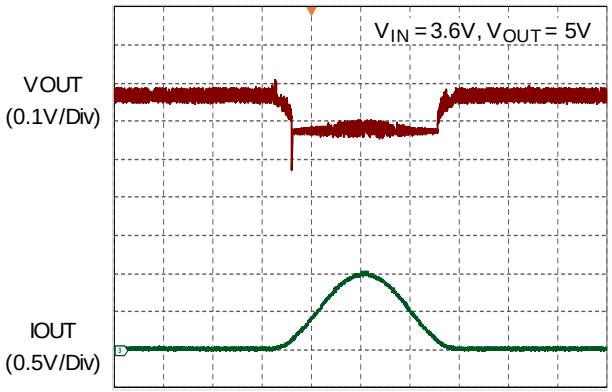
Load Transient



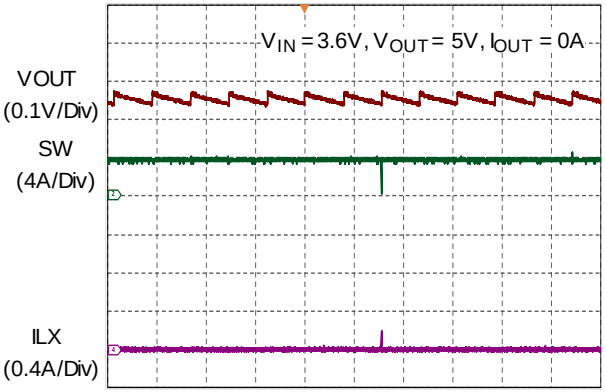
Load Transient



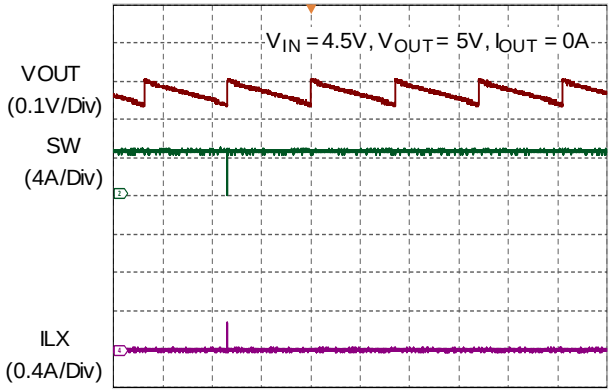
Sine Waveform Stability



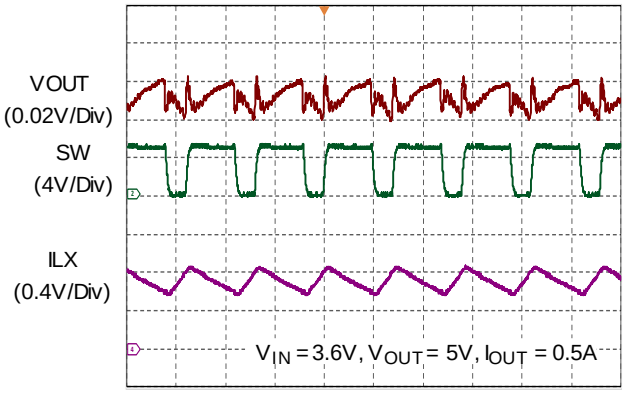
PFM Output Ripple



PFM Output Ripple

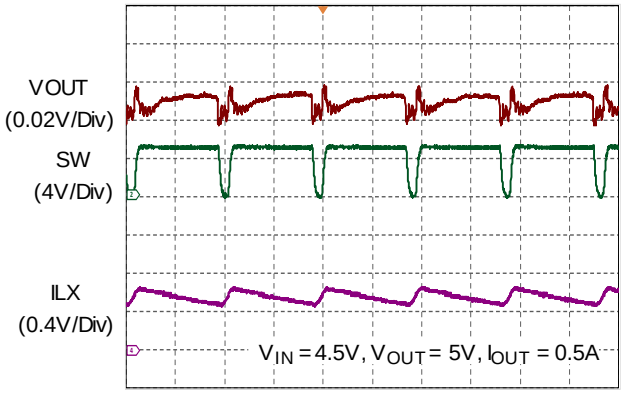


PWM Output Ripple



Time (0.0002ms/Div)

PWM Output Ripple



Time (0.0002ms/Div)

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating with soft-start. Once the EN pin is set at low, the device will be shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

Power Frequency Modulation (PFM)

PFM is used to improve efficiency at light load.

When the output voltage is lower than a set threshold voltage, the converter will operate in PFM.

It raises the output voltage with several pulses until the loop exits PFM.

Thermal Shutdown

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the threshold with a hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over-temperature threshold.

Inductor Selection

The point of inductor selection is the maximum loading of the application. The example is given by below application condition and equations.

Application condition:

V_{IN} = 3V, V_{OUT} = 5V, I_{OUT} = 1.5A, converter efficiency = 81%, Frequency = 3.5MHz, L = 1μH.

Step 1: To calculate input current (I_{IN}).

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times Eff} = 3.086A$$

Step 2: To calculate duty cycle of boost converter.

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 0.4$$

Step 3: To calculate peak current of inductor.

$$I_{L(Peak)} = I_{IN} + 0.5 \times \frac{V_{IN} \times D}{L \times Freq.} = 3.258A$$

The recommended nominal inductance value is 1μH. It is recommended to use inductor with dc saturation current ≥ 3300mA.

Input Capacitor Selection

At least a 4.7μF and the rate voltage is 6.3V for DC bias input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit for SW. And input capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

Output Capacitor Selection

At least 10μF capacitors is recommended to improve V_{OUT} ripple.

Output voltage ripple is inversely proportional to C_{OUT}.

Output capacitor is selected according to output ripple which is calculated as:

$$V_{RIPPLE(P-P)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}}$$

and

$$t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

therefore:

$$C_{OUT} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{V_{RIPPLE(P-P)}}$$

and

$$t_{SW} = \frac{1}{f_{SW}}$$

The maximum V_{RIPPLE} occurs at minimum input voltage and maximum output load.

Output Discharge Function

With the EN pin set to low, the VOUT pin is internally connected to GND by an internal discharge N-MOSFET switch. After the 10ms, IC will be true-shut down.

This feature prevents residual charge voltages on capacitor connected to VOUT pins, which may impact proper power up of the system.

Current Limit

The RT4823N employs a valley-current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current-limit threshold, the off-time is increased until the current is decreased to valley-current threshold. Next on-time begins after current is decreased to valley-current threshold. On-time is decided by (V_{OUT} – V_{IN})/V_{OUT} ratio. The output voltage decreases when further loading current increase. The current limit function is implemented by the scheme, refer to Figure 3.

OCP ($I_{LIM(5A)}$) Shutdown Protection

The RT4823N is implemented OCP shutdown protection. When the converter is operation in boost mode, peak current limit and valley current limit function can not protect IC from short circuit or the huge loading. The RT4823N is implemented truth disconnection function, when peak current is > 5A (Typ.), boost converter will turn off high-side MOSFET (UG) and low-side MOSFET (LG).

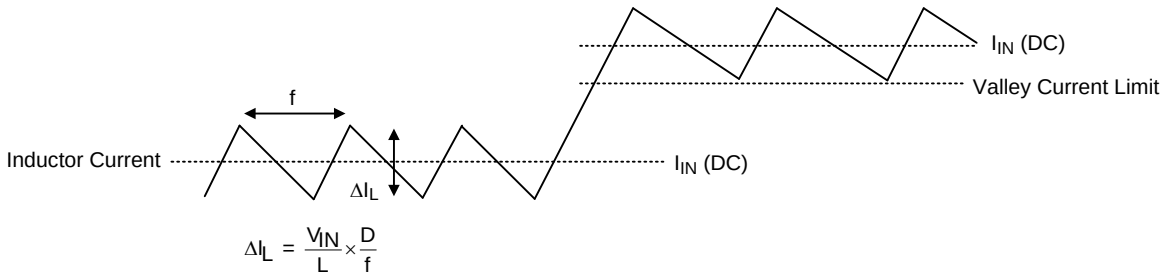


Figure 3. Inductor Currents in Current Limit Operation

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-9B 1.3x1.2 (BSC) package, the thermal resistance, θ_{JA}, is 64.9°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (64.9°C/W) = 1.54W for a WL-CSP-9B 1.3x1.2 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed TJ(MAX) and the thermal resistance, θ_{JA}. The derating curves in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

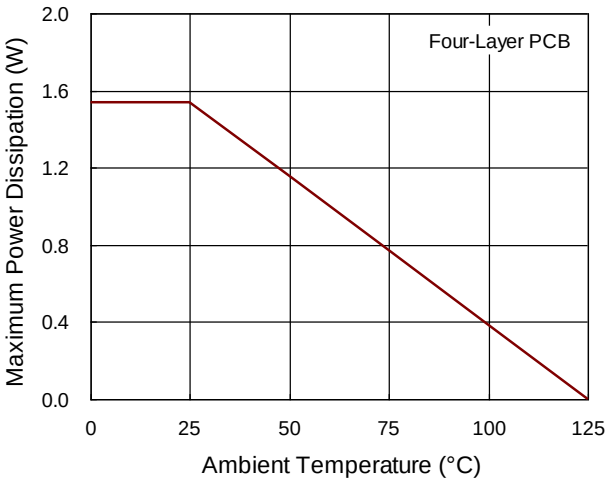


Figure 4. Derating Curve of Maximum Power Dissipation

Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT4823N.

Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the RT4823N through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4823N, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- For thermal consider, it needed to maximize the pure area for power stage area besides the SW.

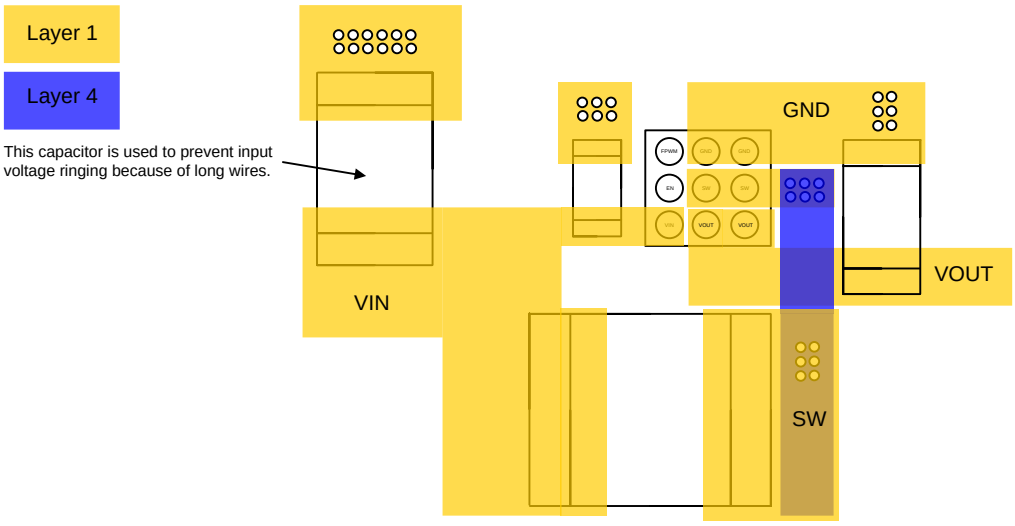
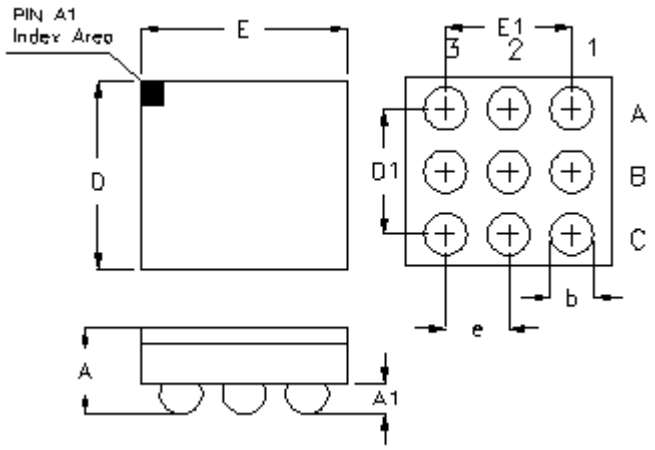


Figure 5. PCB Layout Guide

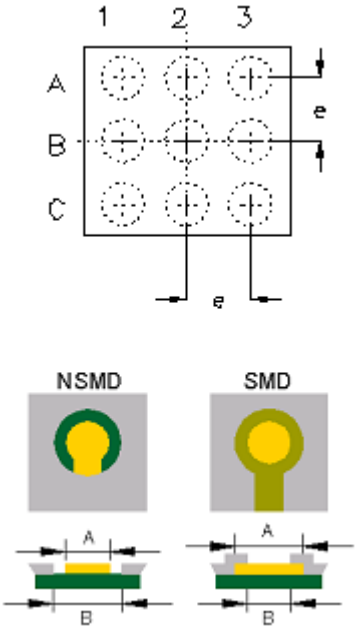
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.160	1.240	0.046	0.049
D1	0.800		0.031	
E	1.260	1.340	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	

9B WL-CSP 1.3x1.2 Package (BSC)

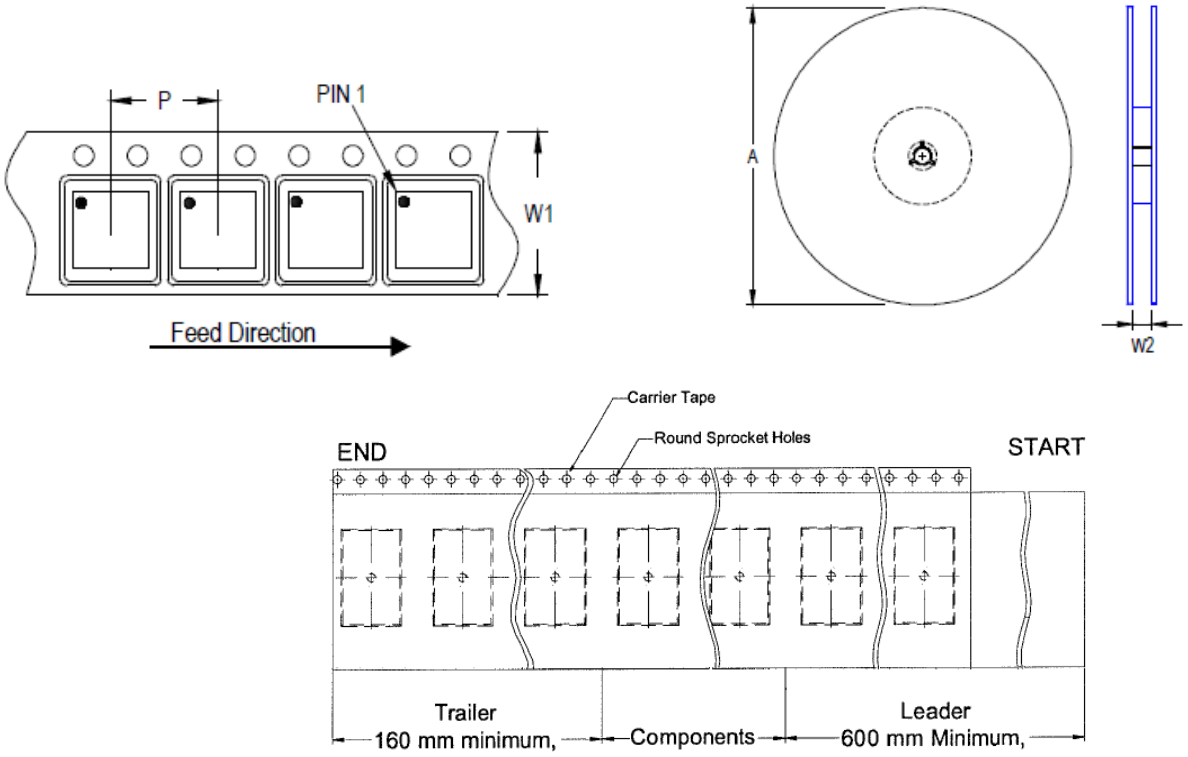
Footprint Information



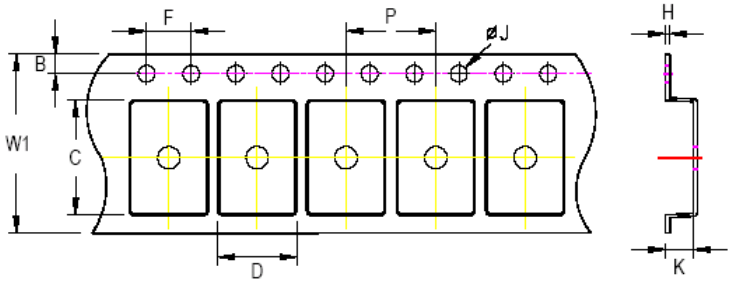
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.3x1.2-9(BSC)	9	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 1.3x1.2	8	4	180	7	3,000	160	600	8.4/9.9



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
WL-CSP 1.3x1.2	7”	3,000	Box A	18.3*18.3*8.0	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	1	3,000	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2023/2/15	Final	Marking Information on P2 Operation on P4, 5