High Efficiency Boost Converter

General Description

The RT4813C allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The RT4813C is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed to a maximum load current of 3.1A. Quiescent current in Shutdown Mode is less than 1μA, which maximizes battery life.

Ordering Information

RT4813C □□

- Package Type
  QUF : UQFN-9L 2x2 (FC) (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▸ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▸ Suitable for use in SnPb or Pb-free soldering processes.

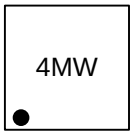
Features

- **CMCOT Topology and Small Output Ripple when VIN Close VOUT Voltage**
- **Operates from a Single Li-ion Cell : 1.8V to 5.5V**
- **Adjustable Output Voltage : 1.8V to 5.5V**
- **PSM Operation**
- **Up to 96% Efficiency**
- **Input Over-Current Limit**
- **Input / Output Over-Voltage Protection**
- **Programmable Average Output Current Limit Range : 3100mA to 550mA**
- **Internal Compensation**
- **Output Discharge**
- **Output Short Protection**
- **True Load Disconnect**

Applications

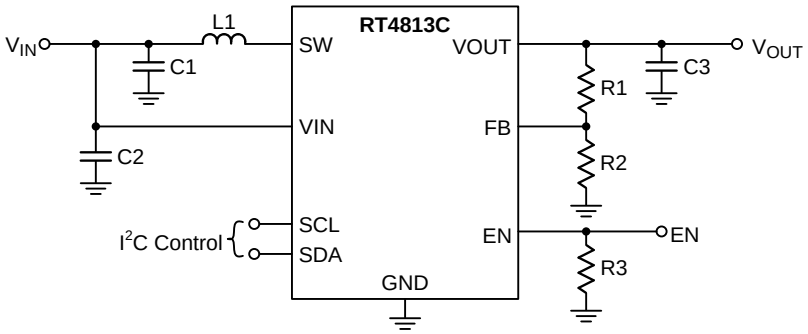
- Single-Cell Li-Ion, LiFePO4 Smart-Phones
- Portable Equipment

Marking Information



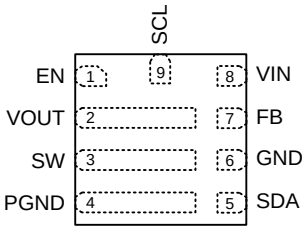
4M : Product Code
W : Date Code

Simplified Application Circuit



Pin Configuration

(TOP VIEW)

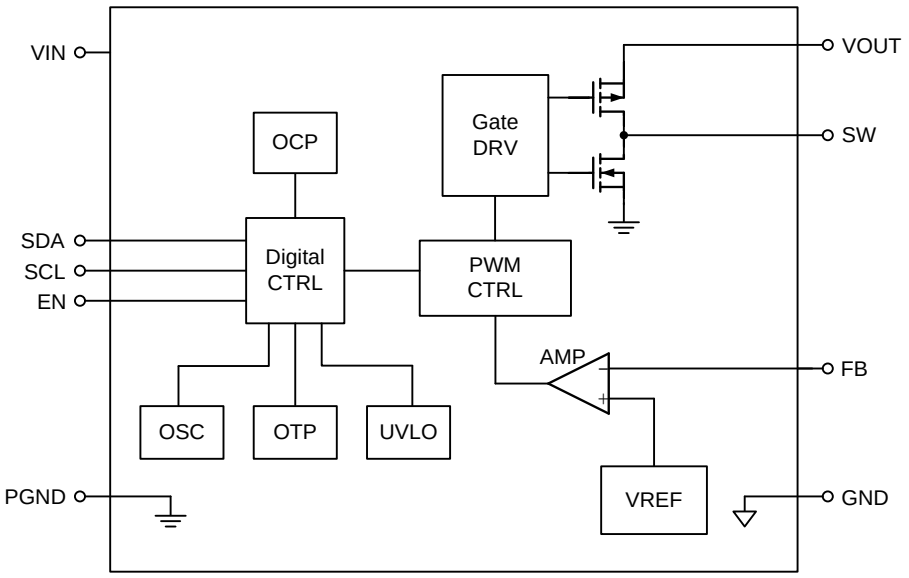


UQFN-9L 2x2 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable input (1 enabled, 0 disabled), must not be left floating.
2	VOUT	Boost converter output.
3	SW	Switching node.
4	PGND	Power ground.
5	SDA	I^2C interface data input.
6	GND	Analog ground.
7	FB	Voltage feedback.
8	VIN	Power input. Input capacitor CIN must be placed as close to IC as possible.
9	SCL	I^2C interface clock input.

Functional Block Diagram



Operation

The RT4813C combined built-in power transistors, synchronous rectification, and low supply current, it provides a compact solution for system using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed to a maximum load current of 3.1A. Quiescent current in Shutdown mode is less than 1μA, which maximizes battery life.

Mode		Depiction	Condition
LIN	LIN 1	Linear startup 1	$V_{IN} > V_{OUT}$
	LIN 2	Linear startup 2	$V_{IN} > V_{OUT}$
Soft-Start		Boost soft-start	$V_{OUT} < V_{OUT(MIN)}$
Boost		Boost mode	$V_{OUT} = V_{OUT(MIN)}$

LIN State

When V_{IN} is rising, it enters the LIN State. There are two parts for the LIN state. It provides maximum current for 1A to charge the C_{OUT} in LIN1, and the other one is for 2A in LIN2. By the way, the EN is pulled high and V_{IN} > UVLO.

As the Figure 1 shown, if the timeout is over the specification, it will enter the Fault mode.

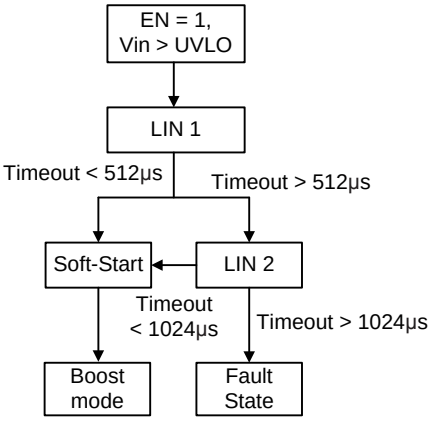


Figure 1. The RT4813C State Chart

Startup and Shutdown State

When V_{IN} is rising and through the LIN state, it will enter the Startup state. If EN is pulled low, any function is turned-off in shutdown mode.

Soft-Start State

It starts to switch in Soft-start state. After the LIN state, output voltage is rising with the internal reference voltage.

Fault State

As the Figure 1 shown, it will enter to the Fault state as below,

- The timeout of LIN2 is over the 1024μs.

It will be the high impedance between the input and output when the fault is triggered. A restart will be start after 20ms.

OCP

The converter senses the current signal when the high-side P-MOSFET turns on. As a result, the OCP is cycle by-cycle current limitation. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit.

OTP

The converter has an over-temperature protection. When the junction temperature is higher than the thermal shutdown rising threshold, the system will be latched and the output voltage will no longer be regulated until the junction temperature drops under the falling threshold.

Absolute Maximum Ratings (Note 1)

- VIN, FB, EN, SW, SDA, SCL to GND ---------- –0.2V to 6V
- VOUT to GND ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  UQFN-9L 2x2 (FC) ---------- 0.89W
- Package Thermal Resistance (Note 2)
  UQFN-9L 2x2 (FC), θ_{JA} ---------- 111.5°C/W
  UQFN-9L 2x2 (FC), θ_{JC} ---------- 19.6 °C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage Range ---------- 1.8V to 5.5V
- Output Voltage Range ---------- 1.8V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Under-Voltage Lockout Rising Threshold	V_{UVLOR}		1.6	1.7	1.8	V
Under-Voltage Lockout Falling Threshold	V_{UVLOF}		1.5	1.6	1.7	V
FB Voltage	V_{FB}	CCM	0.495	0.5	0.505	V
VOUT Voltage (I^2C)	V_{OUT}	CCM	–1	0	1	%
Shutdown Current	I_{SHDN}	EN = 0V,	--	0.1	2	μA
Quiescent Current		Close loop, no load	--	120	--	μA
Pre-Charge Current	I_{Pre}		--	1	--	A
Output Current	$I_{O, 1.2A}$	ILIM_AVG<3:0> : 1011 for I_{OUT} = 1.16A	0.95	--	1.25	A
	$I_{O, 1.5A}$	ILIM_AVG<3:0> : 1001 for I_{OUT} = 1.5A	1.32	--	1.7	
Switching Frequency	f_{SW}	V_{OUT} – V_{IN} > 1V, CCM	--	0.5	--	MHz
Valley Current Limit	I_{OC}		--	6	--	A
High-Side Switch R_{ON}		V_{IN} = 5V	--	43	55	mΩ
Low-Side Switch R_{ON}		V_{IN} = 5V	--	26	35	mΩ
FB Pin Input Leakage	I_{FB}		–1	--	1	μA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Leakage of SW		I_{SW}		--	--	5	μA
Line Regulation		$\Delta V_{OUT, LINE}$	CCM, V_{IN} = 2.7V to 4.5V, V_{OUT} = 5V, I_{OUT} = 500mA	--	0.5	--	%
Load Regulation		$\Delta V_{OUT, LOAD}$	CCM, I_{OUT} < 3.1A, V_{IN} = 3.6V, V_{OUT} = 5V	--	0.5	--	%
Output Over-Voltage Protection		V_{OVP}		--	6	--	V
EN Input Voltage	Low-Level	V_{IL}		--	--	0.4	V
	High-Level	V_{IH}		1.2	--	--	
EN Sink Current				--	0.1	1	μA
Thermal Shutdown		T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	°C
I^2C Characteristics							
SCL, SDA Low Input Voltage		$V_I{}^2C_{IL}$		--	--	0.4	V
SCL, SDA High Input Voltage		$V_I{}^2C_{IH}$		1.2	--	--	V
SCL, SDA Low Output Voltage		$V_I{}^2C_{OL}$		--	--	0.4	V
I^2C Work Voltage		$V_I{}^2C_{int}$		--	1.8	--	V
Input Current Each IO Pin		$I_{IN\_I}{}^2C$		–10	--	10	μA
Data Hold Time		$t_{DH\_I}{}^2C$		30	--	--	ns
Data Set-Up Time		$t_{DS\_I}{}^2C$		70	--	--	ns

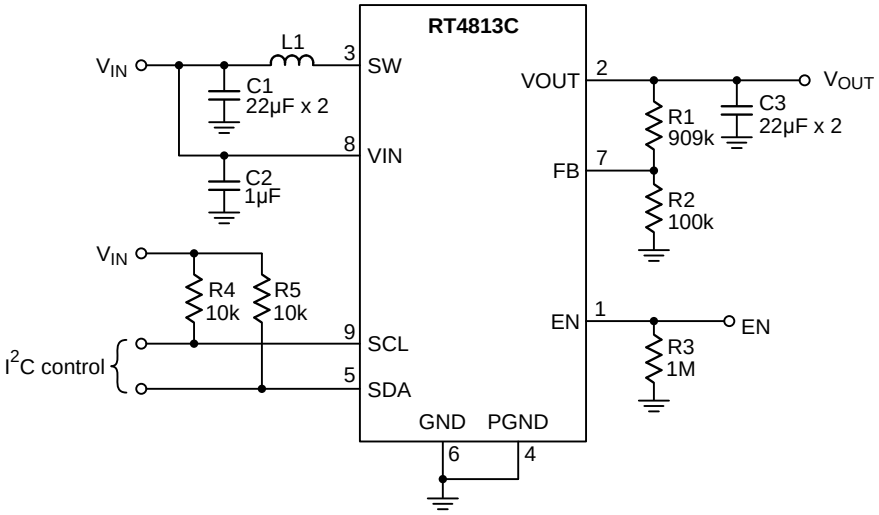
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

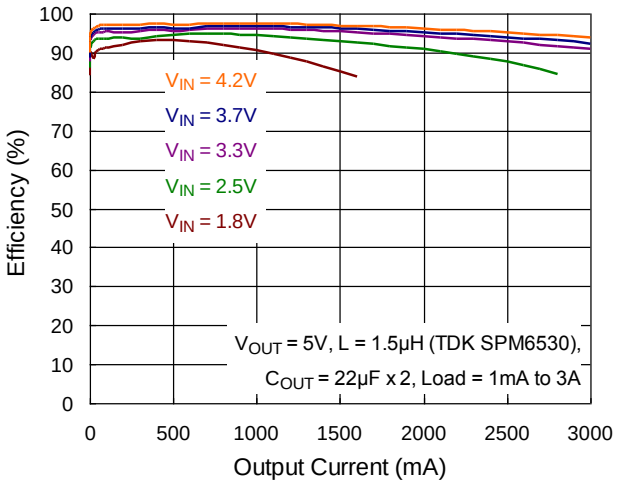
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

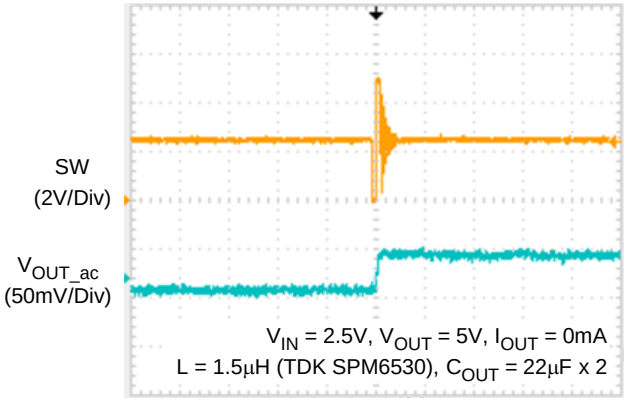


Typical Operating Characteristics

Efficiency vs. Output Curent

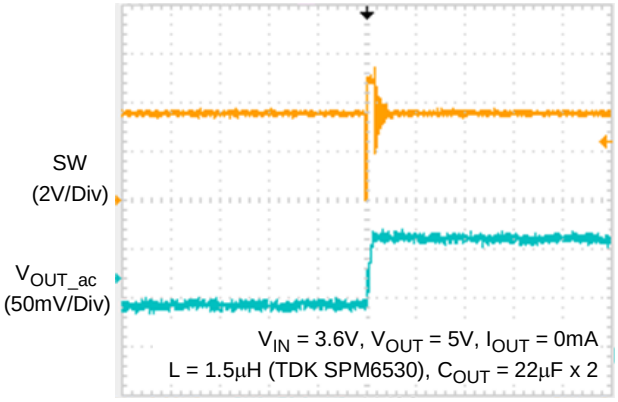


Output Voltage Ripple



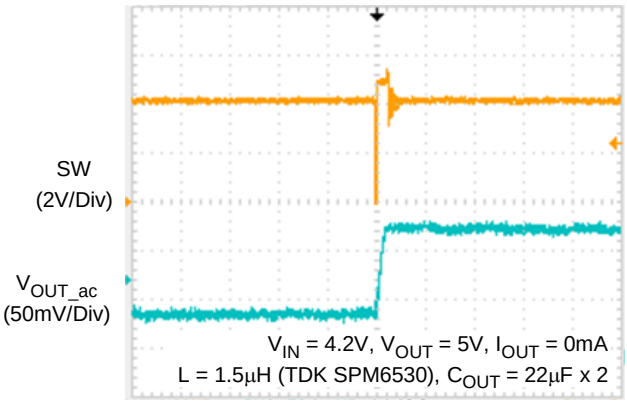
Time (10µs/Div)

Output Voltage Ripple



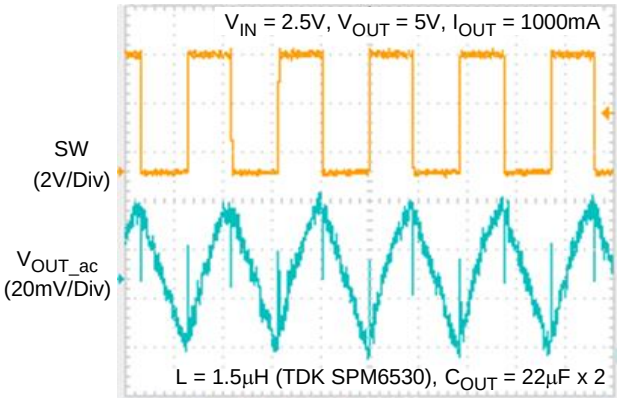
Time (10µs/Div)

Output Voltage Ripple



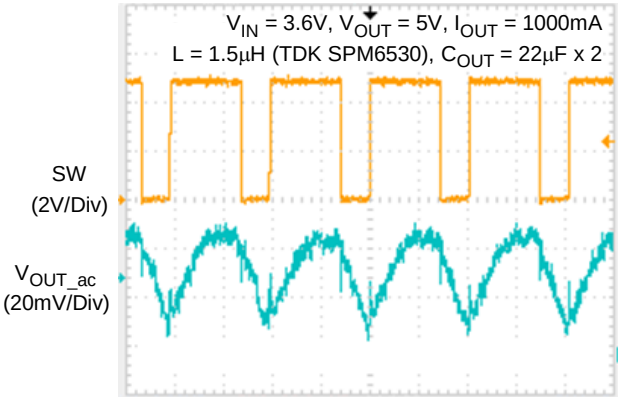
Time (10µs/Div)

Output Voltage Ripple



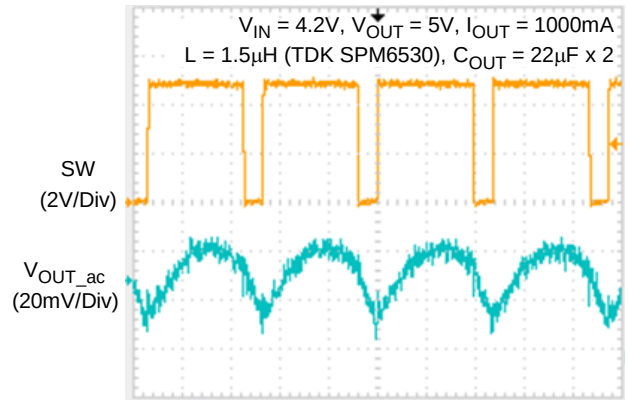
Time (1µs/Div)

Output Voltage Ripple

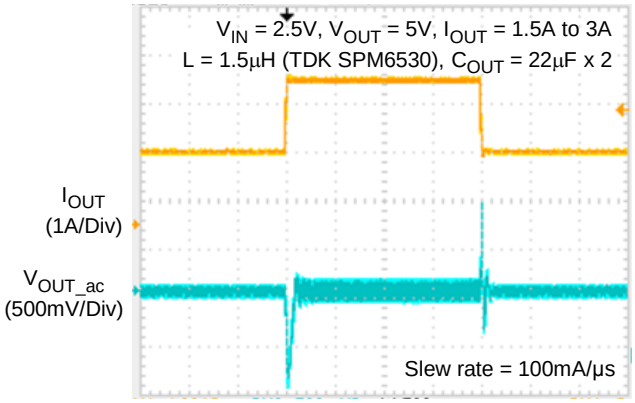


Time (1µs/Div)

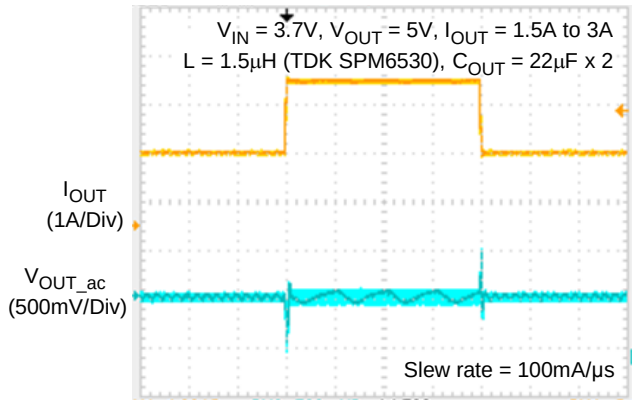
Output Voltage Ripple



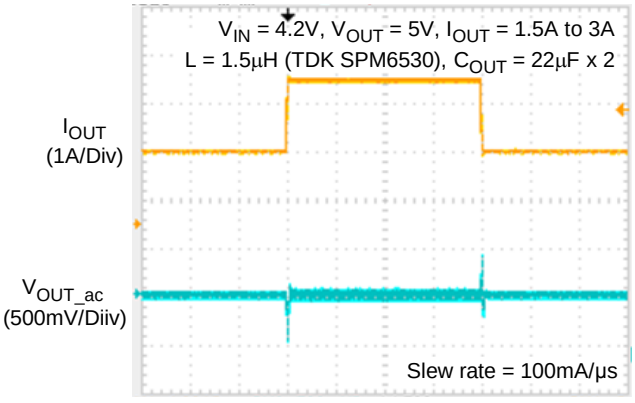
Load Transient Response



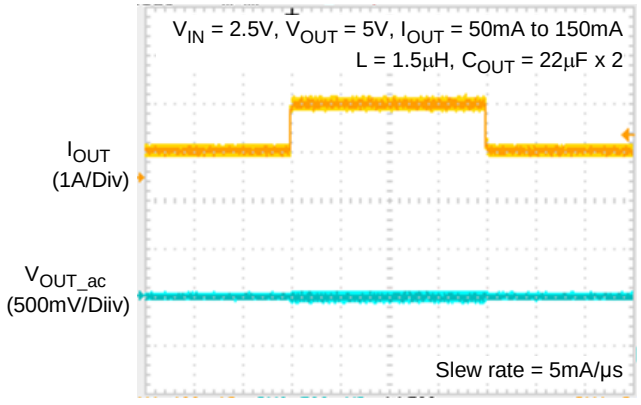
Load Transient Response



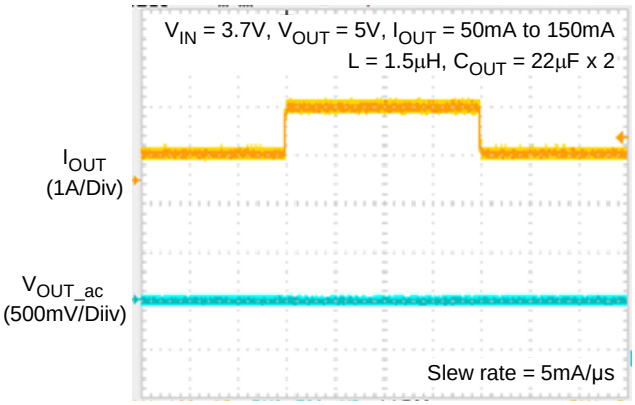
Load Transient Response



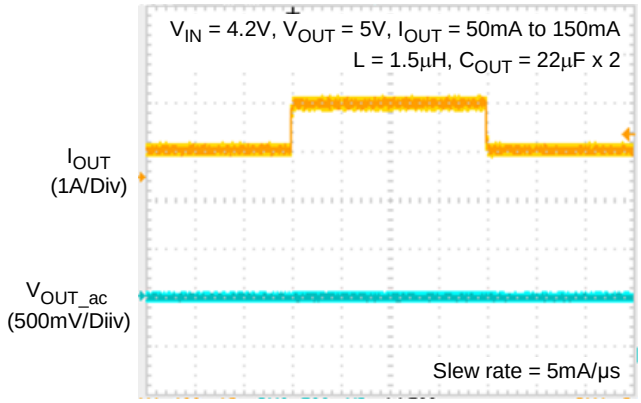
Load Transient Response



Load Transient Response

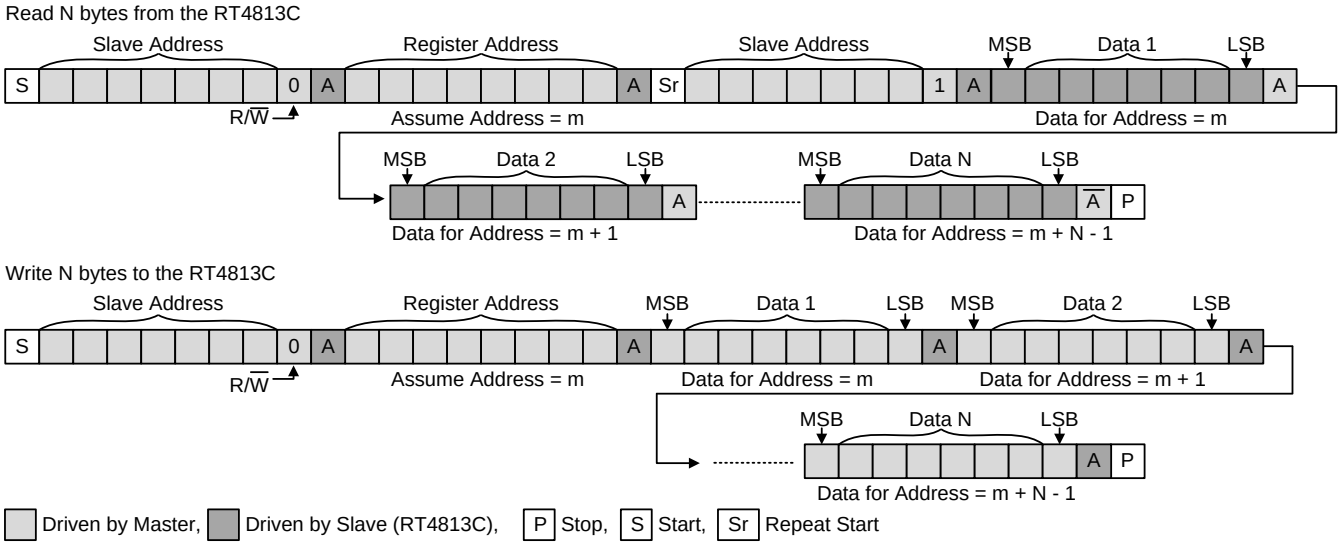


Load Transient Response

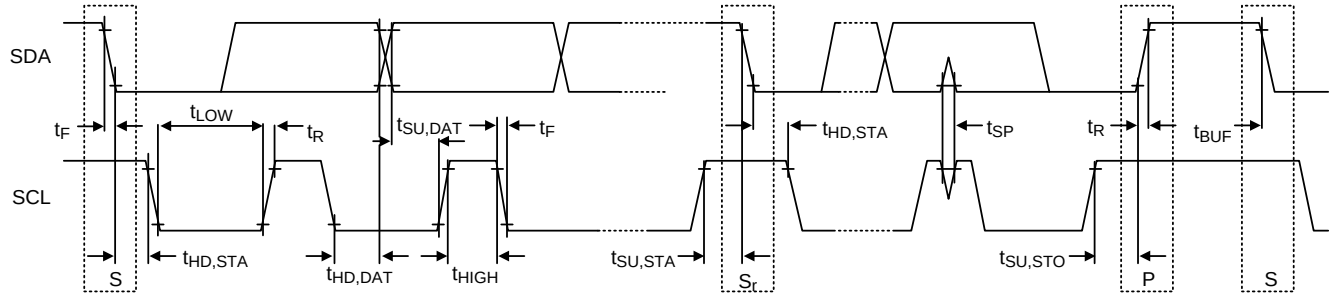


I²C Interface

The RT4813C I²C slave address = 0111001 (7 bits). I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :



I²C Waveform Information



I²C Register

Function	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
Config	0X01	Meaning	Reversed	ILIM_OFF	IPCHG		DRV_SEL<2:0>			SSFM
		Default	0	0	0	1	1	1	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ILIM_OFF			Boost valley current limit setting 0 : Boost current limit enable (default) 1 : Boost current limit disable							
IPCHG			Pre-charge current setting. 00 : 0.5A 01 : 1A (default) 10 : 1.5A 11 : 2A							
DRV_SEL<2:0>			LG driver driving capability 000 : Slowest : : 111 : Fastest (default)							
SSFM			Spread spectrum setting. 0 : Spread spectrum disable (default) 1 : Spread spectrum enable							

Function	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
Charger Control 3	0X03	Meaning	ILIM_SS<7:4>				ILIM_AVG<3:0>			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ILIM_SS<7:4>			Soft-start period boost current limit setting. The default current and soft-start min boost current limit setting is 3000mA.							
			Code	Current	Code	Current	Code	Current	Code	Current
			1001	3000mA (default)	1011	4000mA	1101	5000mA	1111	6000mA
			1010	3500mA	1100	4500mA	1110	5500mA		
ILIM_AVG<3:0>			Average Output Current limit setting. The default current is 3100mA.							
			Code	Current	Code	Current	Code	Current	Code	Current
			0000	3030mA (Default)	0100	2350mA	1000	1670mA	1100	990mA
			0001	2860mA	0101	2180mA	1001	1500mA	1101	820mA
			0010	2690mA	0110	2010mA	1010	1330mA	1110	650mA
			0011	2520mA	0111	1840mA	1011	1160mA	1111	480mA

Function	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
OPTION	0X04	Meaning	Reversed	Reversed	Reversed	Reversed	FSW		EN _IAVGCL	EN _Discharge
		Default	0	0	0	0	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
FSW			Boost frequency setting. 00 : 2MHz 01 : Do not allowed 10 : 1MHz 11 : 500kHz (default)							
EN_IAVGCL			Enable average output current limit 0 : Disable 1 : Enable (default)							
EN_Discharge			Enable discharge 0 : Disable 1 : Enable (default)							

Application Information

Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating with soft-start. Once the EN pin is set at low, the device will be shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

Soft-Start State

After the successful completion of the LIN state (V_{OUT} ≥ V_{IN} – 300mV), the regulator begins switching with boost valley-current limited value 3000mA.

During Soft-Start state, V_{OUT} is ramped up by Boost internal loop. If V_{OUT} fails to reach target value during the Soft-Start period for more than 2ms, a fault condition is declared.

Output Voltage Setting

The output voltage is adjustable by an external resistive divider. The resistive divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500mV. Output voltage can be calculated by equation as below :

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

Power Save Mode

PSM is the way to improve efficiency at light load.

When the output voltage is lower than a set threshold voltage, the converter will operate in PSM.

It raises the output voltage with several pulses until the loop exits PSM.

Under-Voltage Lockout

The under-voltage lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the power switches under undefined conditions and prevents the battery from deep discharge. VIN voltage must be greater than 1.65V to enable the converter. During operation, if VIN voltage drops below 1.55V, the converter is disabled until the supply exceeds the UVLO rising threshold. The RT4813C automatically restarts if the input voltage recovers to the input voltage UVLO high level.

Thermal Shutdown

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the threshold with a hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over temperature threshold.

Inductor Selection

The recommended nominal inductance value is 1.5μH

It is recommended to use inductor with dc saturation current ≥ 6000mA

Table 1. List of Inductors

Manufacturer	Series	Dimensions (in mm)	Saturation Current (mA)
TDK	SPM6530T	7.1 x 6.5 x 3.0	11500
Taiyo Yuden	NRS5040T	5.15 x 5.15 x 4.2	6400

Input Capacitor Selection

At least two capacitor and capacitance is 22μF with rating voltage is 16V for DC bias input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit for SW. And at least a 1μF ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

Output Capacitor Selection

At least 22μF x 2 capacitors is recommended to improve V_{OUT} ripple.

Output voltage ripple is inversely proportional to C_{OUT}.

Output capacitor is selected according to output ripple which is calculated as :

$$V_{RIPPLE(P-P)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}}$$

and

$$t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

therefore :

$$C_{OUT} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{V_{RIPPLE(P-P)}}$$

and

$$t_{SW} = \frac{1}{f_{SW}}$$

The maximum V_{RIPPLE} occurs at minimum input voltage and maximum output load.

Output Discharge Function

With the EN pin set to low, the VOUT pin is internally connected to GND for 10ms by an internal discharge N-MOSFET switch. After the 10ms, IC will be true-shut down.

This feature prevents residual charge voltages on capacitor connected to VOUT pins, which may impact proper power up of the system.

Valley Current Limit

The RT4813C employs a valley-current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current limit threshold, the off-time is increased until the current is decreased to valley-current threshold. Next on-time begins after current is decreased to valley-current threshold. On-time is decided by (V_{OUT} – V_{IN}) / V_{OUT} ratio. The output voltage decreases when further loading current increase. The current limit function is implemented by the scheme, refer to Figure 2.

Average Output Current Limit

The RT4813C features the average output current limit to protect the output terminal. When the load current is over the limit, output current will be clamped.

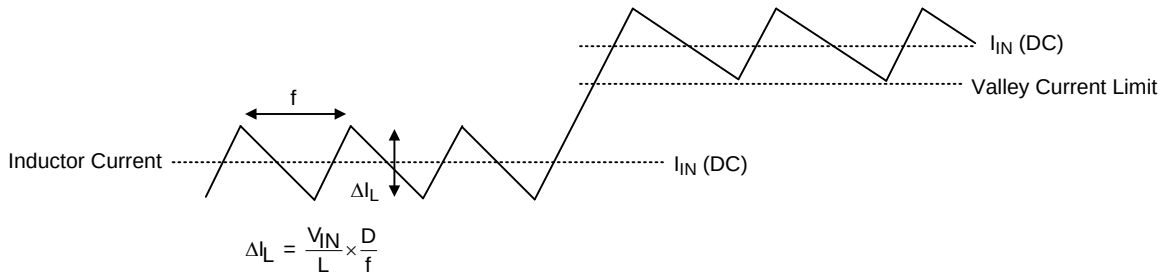


Figure 2. Inductor Currents In Current Limit Operation

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-9L 2x2 (FC) package, the thermal resistance, θ_{JA}, is 111.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (111.5°C/W) = 0.89W for a UQFN-9L 2x2 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

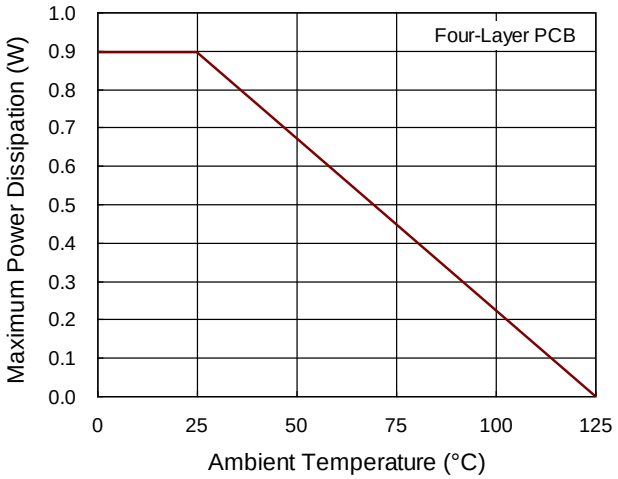


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Consideration

The PCB layout is an important step to maintain the high performance of the RT4813C.

Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the RT4813C through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4813C, the following PCB layout guidelines must be strictly followed.

- Input/Output capacitors must be placed as close as possible to the Input/Output pins.
- SW should be connected to Inductor by wide and short trace, keep sensitive components away from this trace.
- The feedback divider should be placed as close as possible to the FB pin.

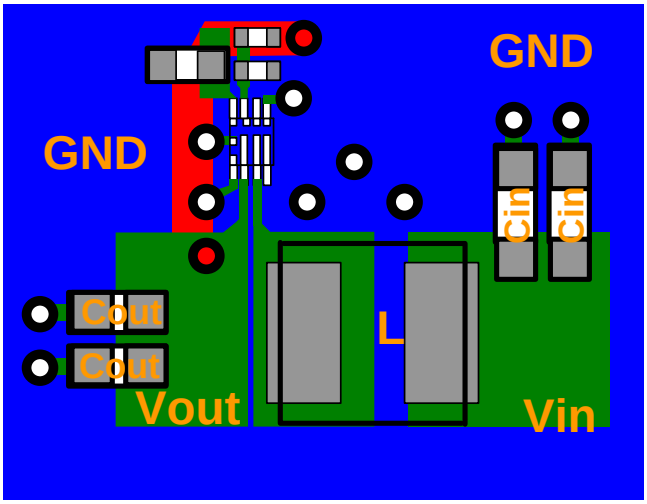
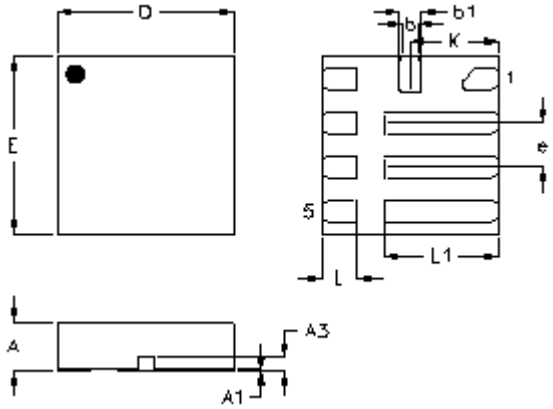


Figure 4. PCB Layout Guide

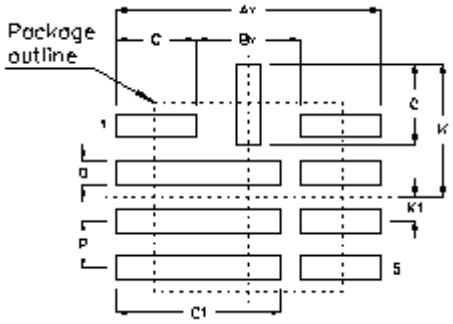
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008
b	0.130	0.230	0.005	0.009
b1	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
E	1.950	2.050	0.077	0.081
e	0.500		0.020	
K	1.000		0.039	
L	0.350	0.450	0.014	0.018
L1	1.250	1.350	0.049	0.053

U-Type 9L QFN 2x2 (FC) Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	Ax	Bx	C*6	C1*3	D*9	K	K1	
UQFN2*2-9(FC)	9	0.50	2.80	1.10	0.85	1.75	0.25	1.40	0.25	±0.05

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789