Triple Output AMOLED Bias

General Description

The RT4731 is a highly integrated Boost, two LDOs (one channel for AVDD and the other channel for VOP) and inverting charge pump to generate positive and negative output voltage. The negative output voltages can be adjusted from −0.6V to −2.4V with 100mV per step by SWIRE interface protocol. The part maintains the highest efficiency by utilizing a −0.33x/−0.5x mode fractional charge pump with automatic mode transition. With its input voltage range of 2.9V to 4.8V, the RT4731 is optimized for products powered by single-cell battery and the output current up to 30mA. The RT4731 is available in UBGA-21B 1.82x3.23 package to achieve optimized solution for PCB space.

Ordering Information

RT4731 □□

Package Type
QSU : UBGA-21B 1.82x3.23

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

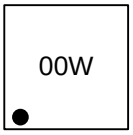
Features

- **2.9V to 4.8V Supply Voltage Range**
- **Single Wire Protocol**
- **Fixed 4.6V Positive Voltage Output**
- **Positive Output Voltage AVDD 2.8V**
- **Negative Voltage Output from –0.6V to –2.4V per 0.1V by SWIRE Pin**
- **Auto-Mode Transition of –0.33x/–0.5x Charge Pump**
- **Built-in Soft-Start**
- **30mA Maximum Output Current**
- **Programmable Output Fast Discharge Function**
- **High Impedance Output when IC Shutdown**
- **UVLO, OCP, SCP, OTP Protection**
- **Shutdown Current < 1μA**
- **Available in 21-Ball UBGA Package**

Applications

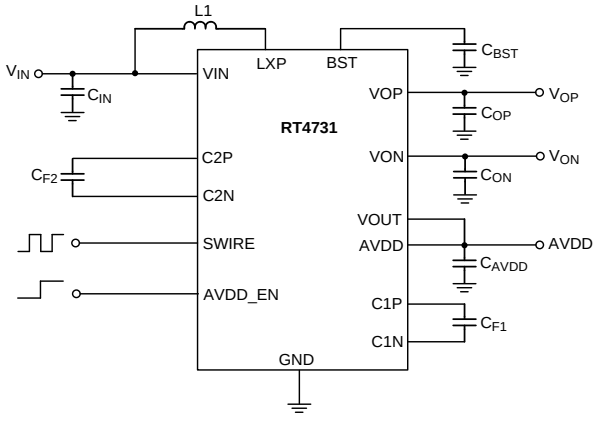
- AMOLED Bias in Portable Device

Marking Information



00 : Product Code
W : Date Code

Simplified Application Circuit



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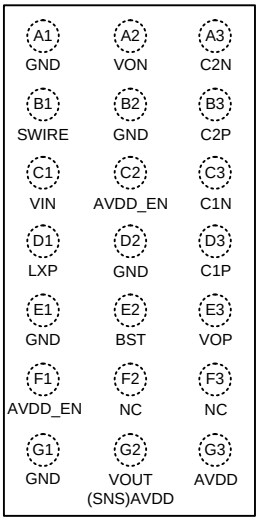
Pin Configuration

(TOP VIEW)



UBGA-21B 1.82x3.23

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, B2, D2, E1, G1	GND	Ground.
A2	VON	Negative terminal output.
A3	C2N	Flying capacitor 2 negative connection.
B1	SWIRE	Enable and VON voltage setting.
B3	C2P	Flying capacitor 2 positive connection.
C1	VIN	Power input.
C2, F1	AVDD_EN	Enable for AVDD with internal connected.
C3	C1N	Flying capacitor 1 negative connection.
D1	LXP	Switching node of boost converter.
D3	C1P	Flying capacitor 1 positive connection.
E2	BST	Output voltage of boost converter.
E3	VOP	Positive terminal output.
F2, F3	NC	No internal connection.
G2	VOUT (SNS)AVDD	Output voltage sense
G3	AVDD	AVDD LDO output.

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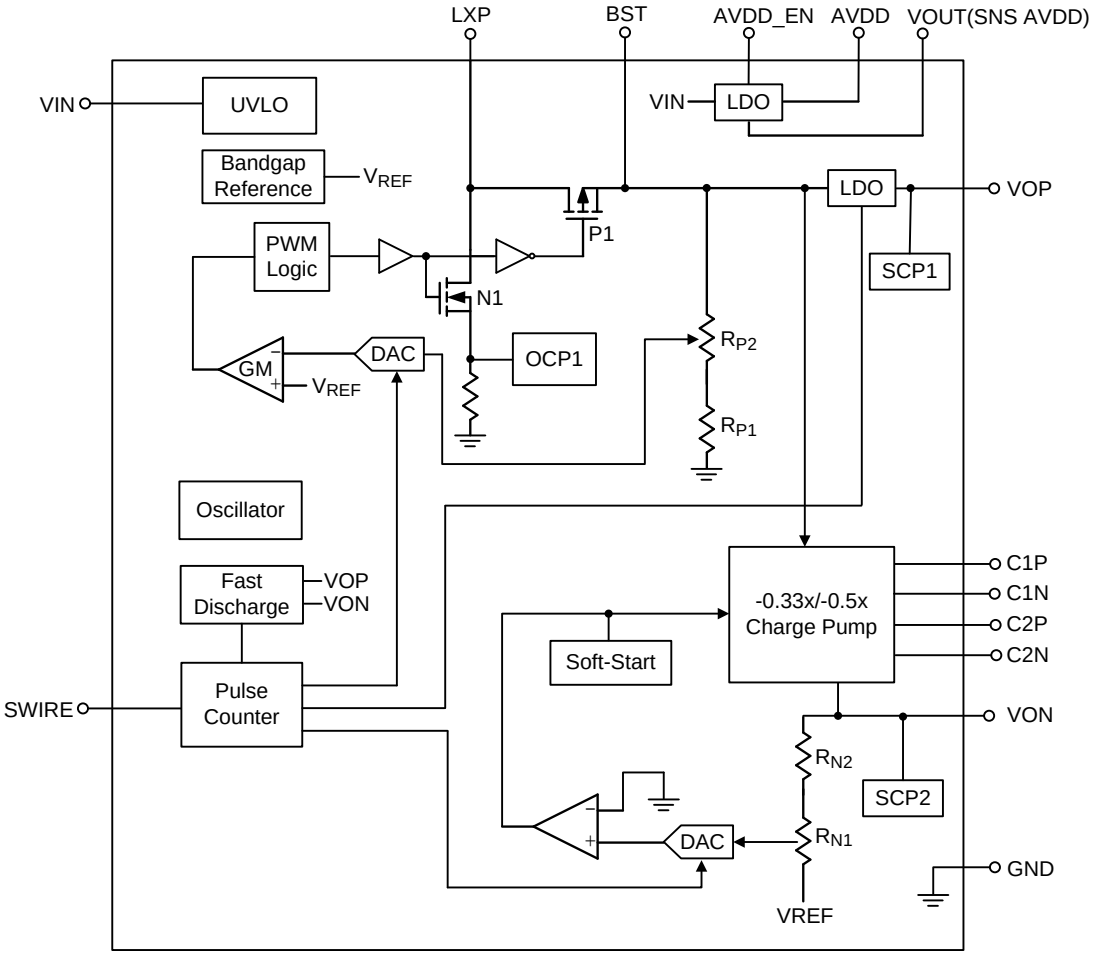
Functional Block Diagram



Operation

The RT4731 is a highly integrated Boost, two LDOs (one channel for AVDD and the other channel for VOP) and inverting charge pump to generate positive and negative output voltage. It can support input voltage range from 2.9V to 4.8V and the output current up to 30mA. The VOP positive output voltage is set at a typical value of 4.6V. The VON negative output voltage is set at a typical value of −2.4V and can be programmed through single wire protocol (SWIRE pin). The available voltage range is from −0.6V to −2.4V with 100mV per step. The AVDD positive output voltage is set at a typical value of 2.8V. The RT4731 provides Over- Temperature Protection (OTP) and Short Circuit Protection (SCP) mechanisms to prevent the device from damage with abnormal operations. When the SWIRE and AVDD_EN voltages are logic low, the IC will be shut down with low input supply current less than 1μA.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage VIN Pin ---------- –0.3V to 6V
- Output Voltage VOP Pin ---------- –0.3V to 6V
- Output Voltage AVDD Pin ---------- –0.3V to 6V
- Output Voltage VON Pin ---------- –6V to 0.3V
- VIN to VON ---------- –0.3V to 7.5V
- C2N to GND ---------- –6V to 0.3V
- Others Pin to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  UBGA-21B 1.82x3.23 ---------- 0.88W
- Package Thermal Resistance (Note 2)

  UBGA-21B 1.82x3.23, θ_{JA} ---------- 112.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage Range ---------- 2.9V to 4.8V
- Positive Output Voltage ---------- 4.6V
- Negative Output Voltage Range ---------- –2.4V to –0.6V
- AVDD Output Voltage ---------- 2.8V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.7V, V_{OP} = 4.6V, V_{ON} = –2.4V, AVDD = 2.8V, C_{IN} = 4.7µF, C_{BST} = 20µF, C_{OP} = 10µF, C_{AVDD} = 1µF, C_{ON} = 30µF, C_{F1} = 1µF, L1 = 2.2µH, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Input Voltage Range	V_{IN}		2.9	--	4.8	V
Under Voltage Lockout Threshold Voltage	V_{UVLO_H}	V_{IN} rising	--	2.2	2.5	V
	V_{UVLO_HYS}	V_{IN} hysteresis	--	100	--	mV
Over-temperature Protection	T_{OTP}	(Note 5)	--	140	--	°C
Over-temperature Protection Hysteresis	T_{OTP_HYST}	(Note 5)	--	15	--	°C
Shutdown Current	I_{SHDN}	SWIRE = 0V	--	--	1	µA

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VOP							
Positive Output Voltage Range		V_{OP}		--	4.6	--	V
Positive Output Voltage Accuracy		V_{OP_ACC}		–1	--	1	%
Positive Output Current Capability		I_{OP_MAX}		--	--	30	mA
		I_{OP_HBM}	VOP = 4.6V, VON ≤ |–2.2|V	--	--	55	
Positive Output Voltage Ripple		V_{OP_RIPPLE}	I_{OP} = 20mA (Note 5)	--	10	--	mV
Line Regulation		V_{OP_LINE}	V_{IN} = 2.9V to 4.8V, I_{OP} = 20mA (Note 5)	--	5	--	mV
Load Regulation		V_{OP_LOAD}	I_{OP} = 0mA to 30mA (Note 5)	--	5	--	mV
Fast Discharge Resistance		R_{DISP}		--	105	--	Ω
Short Circuit Protection		V_{SCP1}		--	< 80% VOP	--	V
AVDD							
Positive Output Voltage Range		AVDD	V_{IN} = 2.9V to 4.8V	--	2.8	--	V
Positive Output Voltage Accuracy		$AVDD\_ACC$	I_{AVDD}=1mA	–2	--	2.5	%
Positive Output Current Capability		I_{AVDD_MAX}		--	--	300	mA
AVDDEN Input Current		I_{AVDD_EN}	V_{AVDD_EN} = 3.3V	--	--	1	uA
Line Regulation		$AVDD\_LINE$	V_{IN} = 2.9V to 4.8V, I_{AVDD} = 1mA	--	0.13	0.35	%
Load Regulation		$AVDD\_LOAD$	I_{AVDD} = 1mA to 300mA	--	0.5	1	%
Output Current Limit		I_{AVDD_LIM}	V_{AVDD} = 90%V_{AVDD}	350	600	--	mA
Logic Input (AVDD_EN)							
AVDD Enable Input Voltage	Logic-High	V_{IH}		0.9	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	V
Charge Pump Output							
Negative Output Voltage Range		V_{ON}		–2.4	--	–0.6	V
Negative Output Voltage Setting Range		V_{ON_SET}	Per step	--	100	--	mV
Negative Output Voltage Accuracy		V_{ON_ACC}		–1	--	1	%
Negative Output Current Capability		I_{ON_MAX}	(Note 5)	--	--	30	mA
		I_{ON_HBM}	VOP = 4.6V, VON ≤ |–2.2|V (Note 5)	--	--	55	
Negative Charge Pump Switching Frequency		f_{OSC_N}		0.8	1	1.2	MHz
Negative Output Voltage Ripple		V_{ON_RIPPLE}	I_{ON} = 20mA (Note 5)	--	20	--	mV

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	V_{ON_LINE}	V_{IN} = 2.9V to 4.8V, I_{ON} = 20mA (Note 5)	--	10	--	mV
Load Regulation	V_{ON_LOAD}	I_{ON} = 0mA to 30mA (Note 5)	--	30	--	mV
Fast Discharge Resistance	R_{DISN}		--	60	--	Ω
Short Circuit Protection	V_{SCP2}		--	> 80% V_{ON}	--	V
Logic Input (SWIRE)						
SWIRE Turn-off Detection Time	t_{off_dly}		350	--	--	μs
SWIRE Signal Stop Indicate Time	t_{stop}		350	--	--	μs
Twait after Data	t_{wait_int}		10	--	--	ms
Rising Input High Threshold Voltage Level	V_{IH}		1.2	--	V_{IN}	V
Falling Input Low Threshold Voltage Level	V_{IL}		0	--	0.4	V
SWIRE Pull Low Resistor	R_{SWIRE}		--	300	--	kΩ
Wake up Delay	t_{wkp}		--	--	1	μs
SWIRE Rising Time	t_R		--	--	200	ns
SWIRE Falling Time	t_F		--	--	200	ns
Clocked SWIRE High	t_{ON}		2	10	40	μs
Clocked SWIRE Low	t_{OFF}		2	10	40	μs
SWIRE to VOP On Time	t_{VOP_ON}		--	1.6	--	ms
Input Clocked SWIRE Frequency	f_{SWIRE}		25	--	250	kHz

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Spec. is guaranteed by design.

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Typical Application Circuit

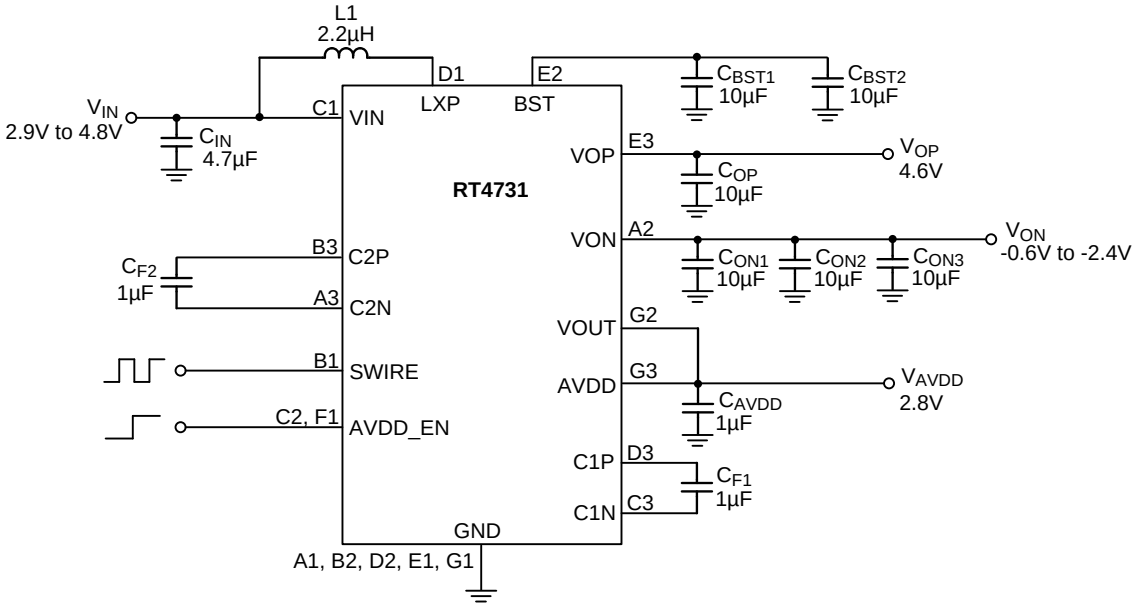
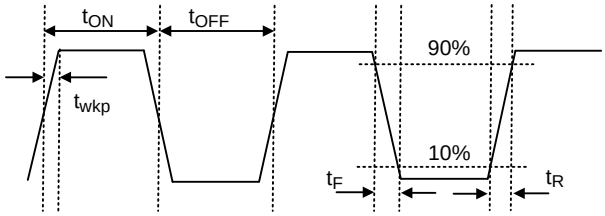


Table 1. Component List of Evaluation Board

Reference	Qty.	Part Number	Description	Package	Supplier
C_{IN}	1	GRM188R61C475KAAJ	4.7µF/16V/X5R	0603	Murata
C_{BST1}, C_{BST2}, C_{OP}, C_{ON1}, C_{ON2}, C_{ON3}	6	GRM188R61A106KE69	10µF/10V/X5R	0603	Murata
C_{AVDD}	1	GRM155R61C105KE01	1µF/16V/X5R	0402	Murata
C_{F1}, C_{F2}	2	GRM155R61C105KE01	1µF/16V/X5R	0402	Murata
L1	1	1269AS-H-2R2M=P2	2.2µH	2.5mmx2.0mmx1.0mm	Murata
		GLCLK2R201A	2.2µH	2.5mm x 2.0mm x 1.0mm	ALPS
		ZTFL-201610TB-2R2M	2.2µH	2.0mm x 1.6mm x 1.0mm	ZenithTek

Time Diagram

SWIRE Interface



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Power Sequence

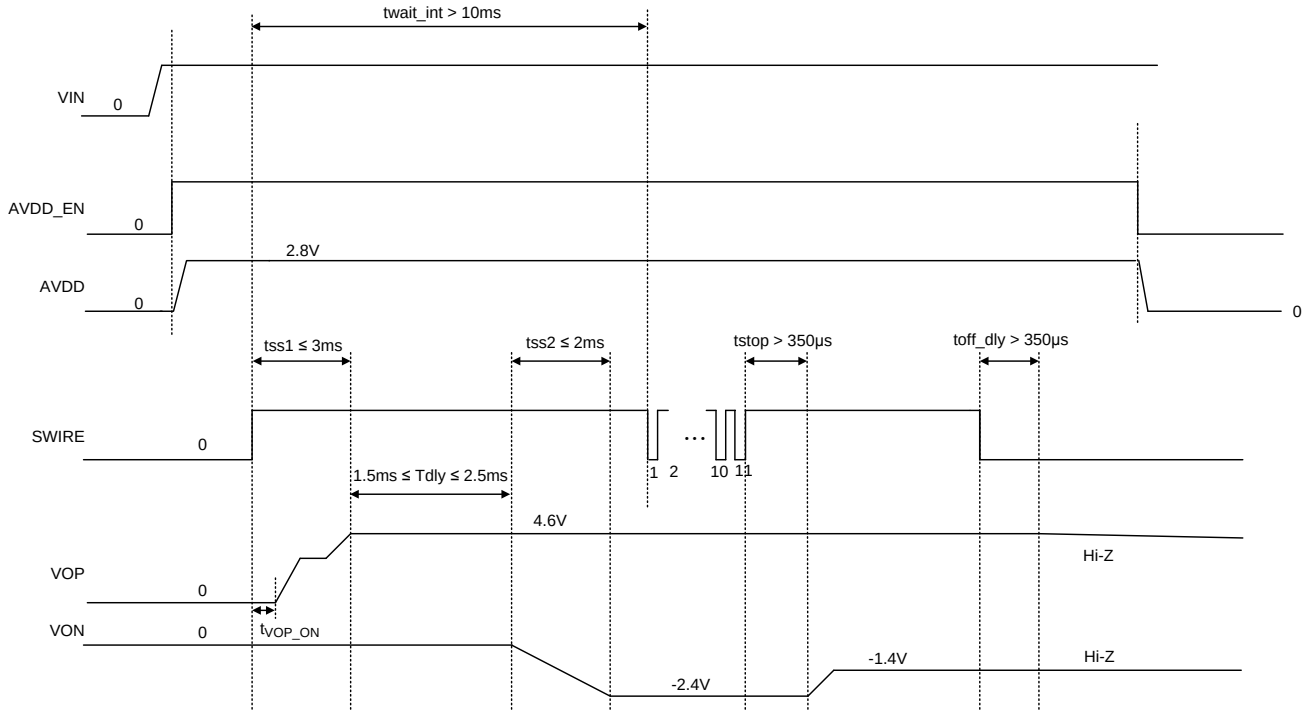

Table 2. VON Output Voltage with SWIRE Pulse

Pulse	VON(V)
0	–2.4 (default)
1	–2.4
2	–2.3
3	–2.2
4	–2.1
5	–2.0
6	–1.9
7	–1.8
8	–1.7
9	–1.6
10	–1.5
11	–1.4
12	–1.3
13	–1.2
14	–1.1
15	–1.0
16	–0.9
17	–0.8
18	–0.7
19	–0.6
20	0

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Table 3. VOP/VON Shutdown Discharge Selection with SWIRE Pulse

Pulse	Discharge
21	Enable

Once pulse 21 received on SWIRE pin, the RT4731 will enable the discharge function to discharge the VOP/VON outputs for 20ms and then enter high impedance state when fault or power-off condition. The discharge function is default disabled and outputs keep high impedance state when fault or power-off condition .

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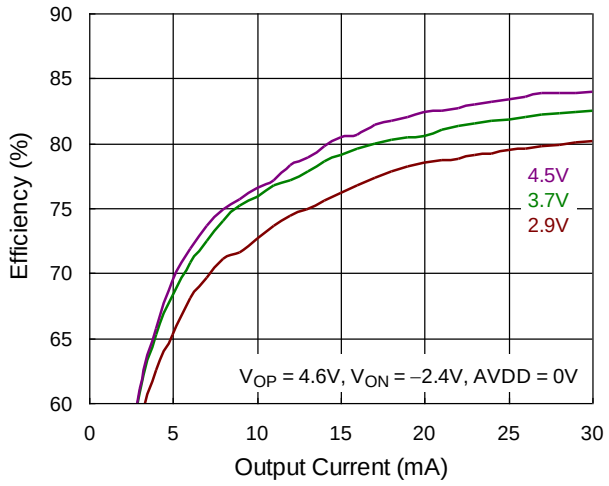
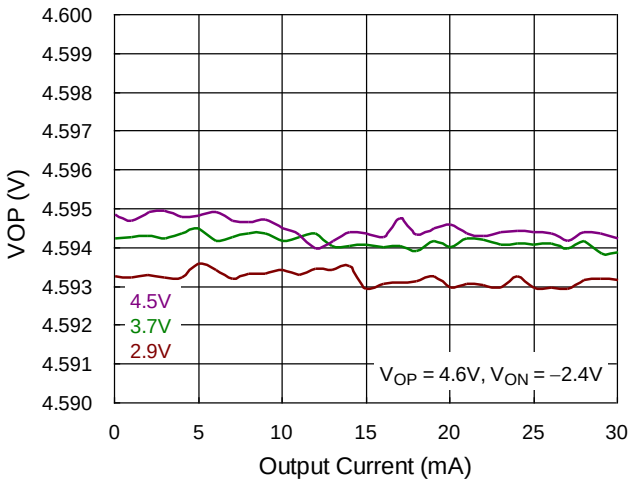
Typical Operating Characteristics

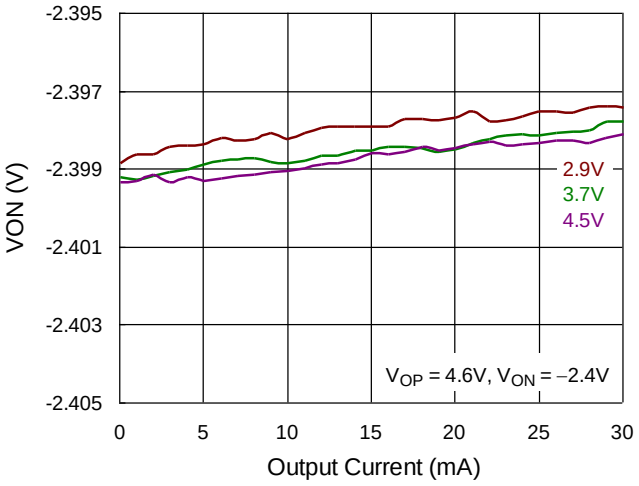
VOP, VON Efficiency vs. Output Current



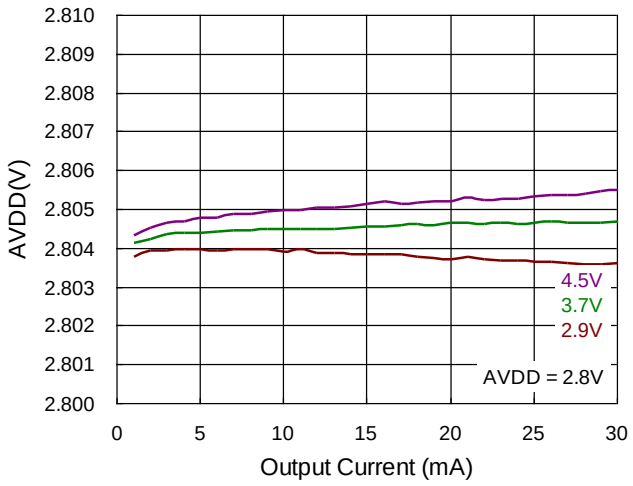
VOP vs. Output Current



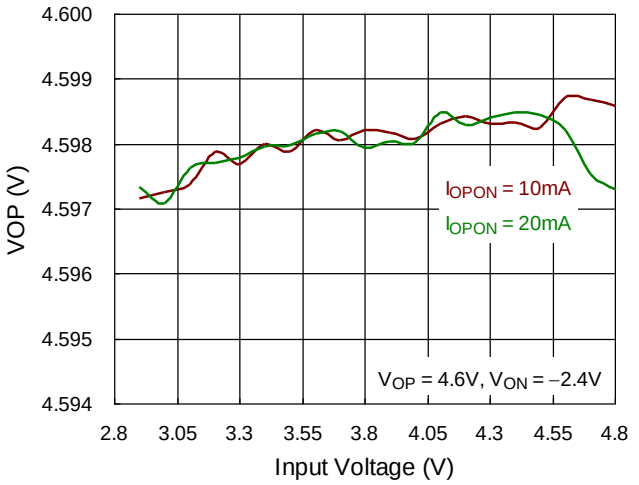
VON vs. Output Current



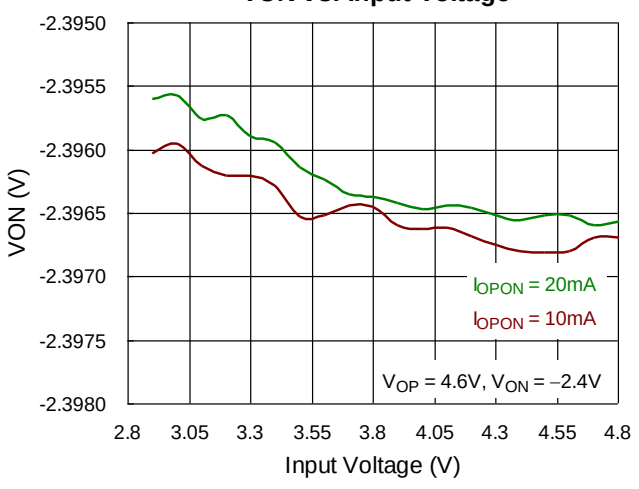
AVDD vs. Output Current



VOP vs. Input Voltage



VON vs. Input Voltage



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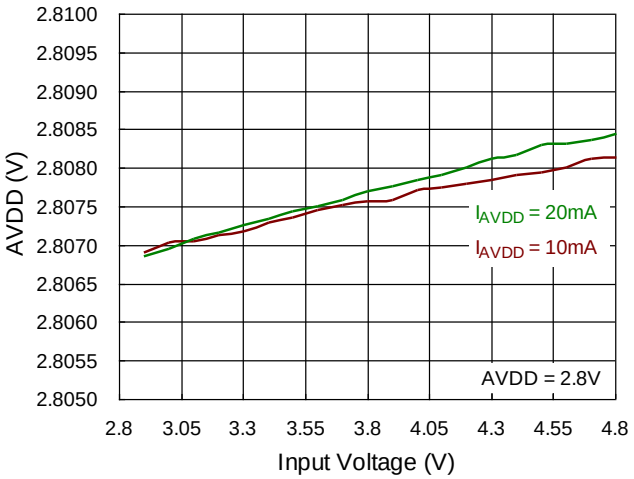
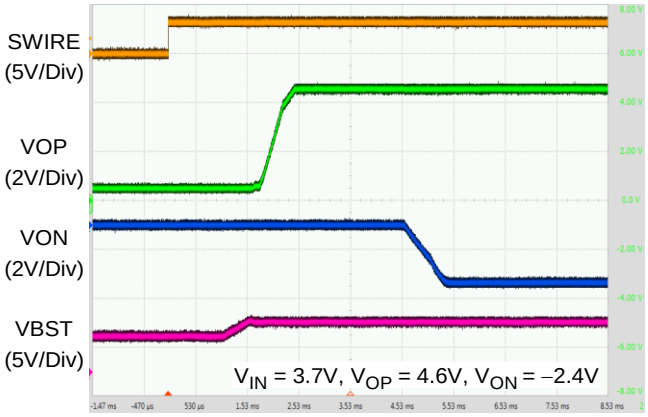
AVDD vs. Input Voltage

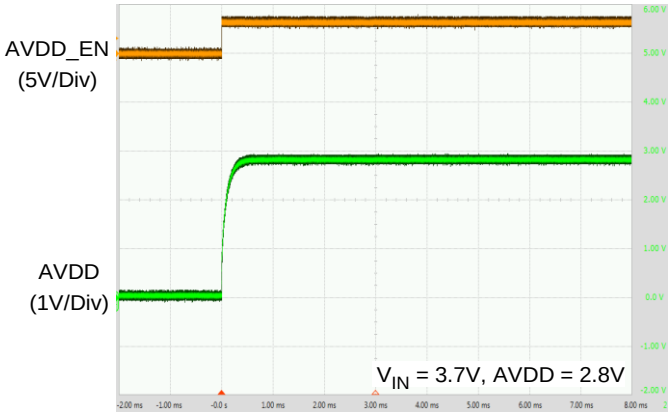


Power On (VOP, VON)



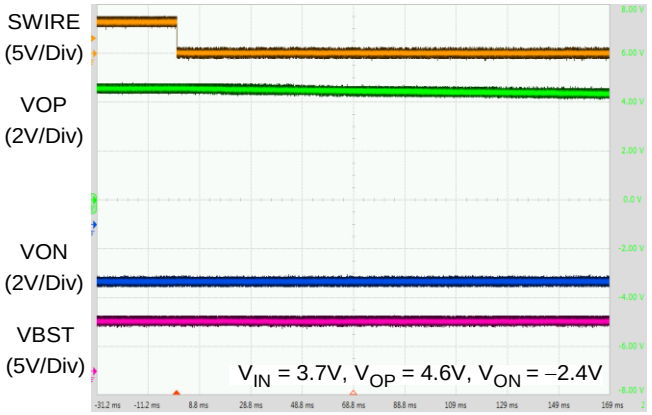
Time (1ms/Div)

Power On (AVDD)



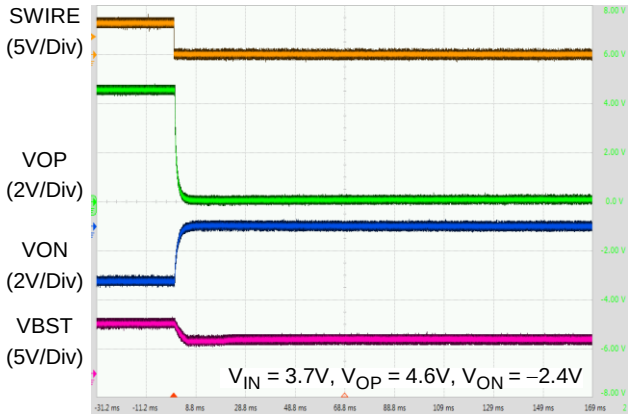
Time (1ms/Div)

Power Off without Discharge (VOP, VON)



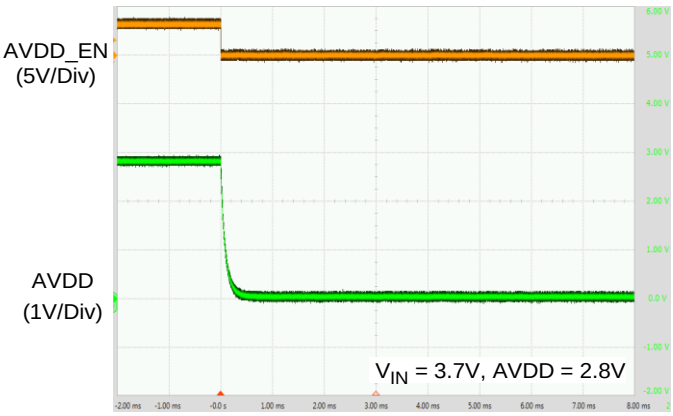
Time (20ms/Div)

Power Off with Discharge (VOP, VON)



Time (20ms/Div)

Power Off (AVDD)



Time (1ms/Div)

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Application Information

The RT4731 is a highly integrated Boost, LDO and inverting charge pump to generate positive and negative output voltages for AMLOED bias. It can support input voltage range from 2.9V to 4.8V and the output current up to 30mA. The V_{OP} positive output voltage is generated from the LDO supplied from a synchronous Boost converter, and V_{OP} is set at a typical value of 4.6V. The Boost converter output also drives an inverting charge pump controller to generate V_{ON} negative output voltage which is set at a typical value of −2.4V. The negative output voltage can be programmed through the dedicated pin which implements single wire protocol and the available voltage range is from −0.6V to −2.4V with 100mV per step. The AVDD positive voltage is generated from a LDO supplied from VIN. It is set at a typical value of 2.8V.

Input Capacitor Selection

Input ceramic capacitor with 4.7μF capacitance is suggested for applications. For better voltage filtering, select ceramic capacitors with low ESR, X5R and X7R types are suitable because of their wider voltage and temperature ranges.

Boost Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$\Delta I_L = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the V_{OP} Boost converter, $I_{IN(MAX)}$ is the maximum input current, and ΔI_L is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$I_{PEAK} = 1.2 \times I_{IN(MAX)}$

Note that the saturated current of the inductor must be greater than I_{PEAK}.

The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Output Capacitor Selection

The output ripple voltage is an important index for estimating IC performance. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in Figure 1, ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of Q, the ΔV_{OUT1} value can be calculated as the following equation :

$$Q = I_{OUT} \times D \times \frac{1}{f_{SOC}} = C_{OUT} \times \Delta V_{OUT1}$$

$$\Delta V_{OUT1} = \frac{I_{OUT} \times D}{f_{SOC} \times C_{OUT}}$$

where f_{OSC} is the switching frequency and D is the duty cycle.

Finally, taking ESR into consideration, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT1} = \Delta V_{ESR} + \frac{I_{OUT} \times D}{f_{OSC} \times C_{OUT}}$$

where $\Delta V_{ESR} = I_{Crms} \times R_{CESR}$

The output capacitor, C_{OUT}, should be selected accordingly.

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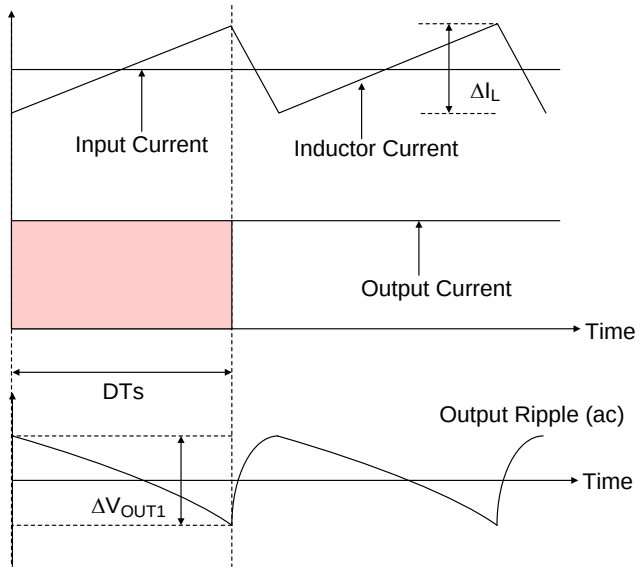

Figure 1. Output Ripple Voltage Without Contribution of ESR

Under Voltage Lockout

To prevent abnormal operation of the IC in low voltage condition, an under voltage lockout is included which shuts down VOP, VON operation when input voltage is lower than the specified threshold voltage.

Soft-Start

The RT4731 employs an internal soft-start feature to avoid high inrush current during start-up. The soft-start function is achieved by clamping the output voltage of the internal error amplifier with another voltage source that is increased slowly from zero to near VIN during the soft-start period.

Negative Output Voltage Setting

The Negative output voltage can be programmed by a MCU through the dedicated pin according to Table 2 "VON Output Voltage with SWIRE Pulse".

Shutdown Delay and Discharge

When the SWIRE signal is logic low for more than 350μs. The output VOP/VON can be actively discharged to GND with discharge function enabled referring to Table 3 "VOP/VON Shutdown Discharge Selection with SWIRE Pulse". The AVDD voltage can be shut down if AVDD_EN is logic low. In shutdown mode, the input supply current for the IC is less than 1μA.

Over Current Protection

The RT4731 includes a cycle-by-cycle current limit function which monitors the inductor current during each ON period. The power switch will be forced off to avoid large current damage once the current is over the limit level. The AVDD LDO contains an independent current limiter which limits the output current to 0.6A (typ.). The current limiting level is reduced to around 0.3A named fold-back current limit when the output voltage is further decreased.

Short Circuit Protection

The RT4731 has an advanced output short-circuit protection mechanism which prevents the IC from damage by unexpected applications. When VOP/VON becomes shorted to ground, and the output voltage is under the limit level with 1ms (typ.) duration, the bias function enters shutdown mode and can only re-start normal operation after triggering the SWIRE pin.

Over Temperature Protection

The RT4731 equips an over temperature protection circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down VOP/VON operation when temperature exceeds 140°C (typ.). The AVDD operation will be shut down when temperature exceeds 140°C (typ.), and the output current exceeds 80mA. Once the ambient temperature cools down by approximately 15°C, IC will automatically resume normal operation. To maintain continuous operation, the maximum junction temperature should be prevented from rising above 125°C.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A

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is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UBGA-21B 1.82x3.23 package, the thermal resistance, θ_{JA}, is 112.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (112.2°C/W) = 0.88W for a UBGA-21B 1.82x3.23 package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

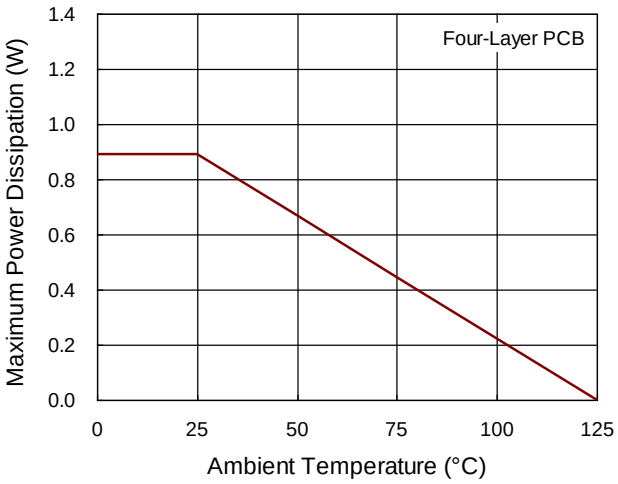

Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

For the best performance of the RT4731, the following PCB layout guidelines should be strictly followed.

- For good regulation, place the power components as close to the IC as possible. The traces should be wide and short especially for the high current output loop.
- The input and output bypass capacitor should be placed as close to the IC as possible and connected to the ground plane of the PCB.
- The flying capacitor should be placed as close to the C1P/C1N/C2P/C2N pin as possible to avoid noise injection.
- Minimize the size of the LXP node and keep the traces wide and short. Care should be taken to avoid running traces that carry and noise-sensitive signals near LXP or high-current traces.
- Separate power ground (PGND) and analog ground (GND). Connect the GND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes.

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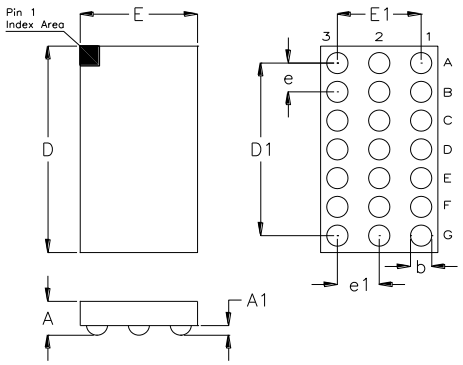
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.430	0.630	0.017	0.025
A1	0.100	0.200	0.004	0.008
b	0.190	0.290	0.007	0.011
D	3.180	3.280	0.125	0.129
D1	2.700		0.106	
E	1.770	1.870	0.070	0.074
E1	1.300		0.051	
e	0.450		0.018	
e1	0.650		0.026	

21B UBGA 1.82x3.23 Package

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