High Efficiency Inverting PWM Converter with Surge Stopper

General Description

The RT2910A is a PWM inverting converter integrates HV (High Voltage) Switch Driver. The HV switch driver protects loads from high voltage transients. It regulates the output during an over-voltage event, by controlling the Gate of an external N-MOSFET. The output is limited to a safe value thereby allowing the loads to continue functioning. The RT2910A also monitors the voltage drop between the VHV and SNS pins to protect against over-current faults. An internal amplifier limits the current sense voltage to 50mV. If the fault condition persists, the MOSFET is turned off. After a certain cooling off period, the gate is allowed to go up and turn on the MOSFET again. Moreover, the HV switch driver also can support back to back FETs application to prevent reverse leakage current from output.

The high-efficiency PWM inverting converter allows designers to implement compact, low noise, negative output DC-DC converters. This device operates from +4V to +7V input voltage and generates −500mV to −12.5V output. To minimize switching noise, it features a current-mode, constant frequency PWM control scheme. The operating frequency can be set from 300kHz to 800kHz through a resistor.

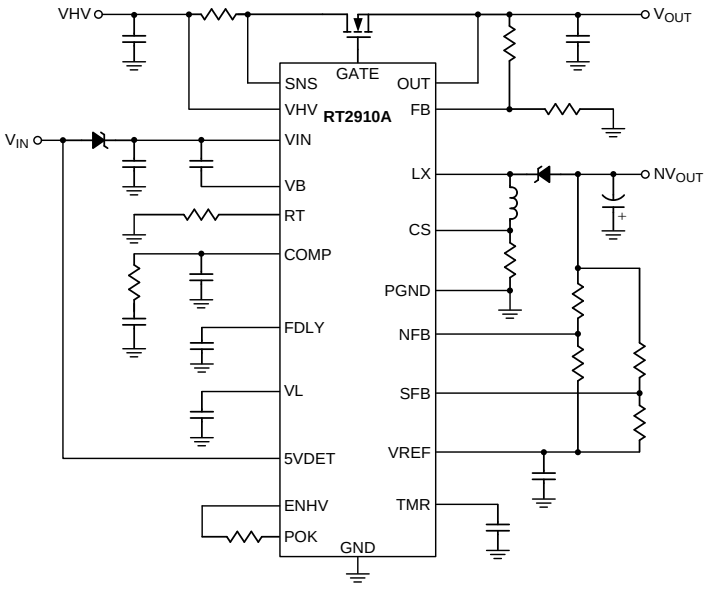
Features

- **HV Switch Driver**
  - **Adjustable Output Clamp Voltage**
  - **Over-Current Protection**
  - **Wide Operation Range : 5V to 60V**
  - **Reverse Input Protection to −60V**
  - **Adjustable Fault Timer**
  - **Support N-MOSFET**
- **Inverting PWM Converter**
  - **−12.5V to −0.5V Output**
  - **Integrate High-Side P-MOSFET**
  - **300kHz to 800kHz Switching Frequency**
  - **Current-Mode PWM Control**
  - **Internal Soft-Start**
  - **Power Ok Indicator**

Applications

- Ga-N MOSFET Bias
- Positive to Negative Conversion
- Industrial and Telecom Power Supplies
- Distributed Power System

Simplified Application Circuit



Ordering Information

RT2910A □□

- Package Type
  QW : WQFN-24L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

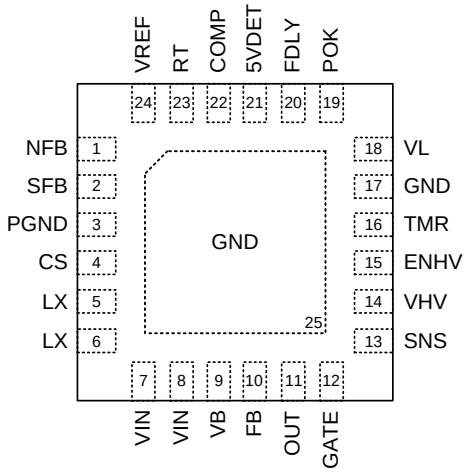
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT2910AGQW : Product Number
YMDNN : Date Code

Pin Configuration

(TOP VIEW)

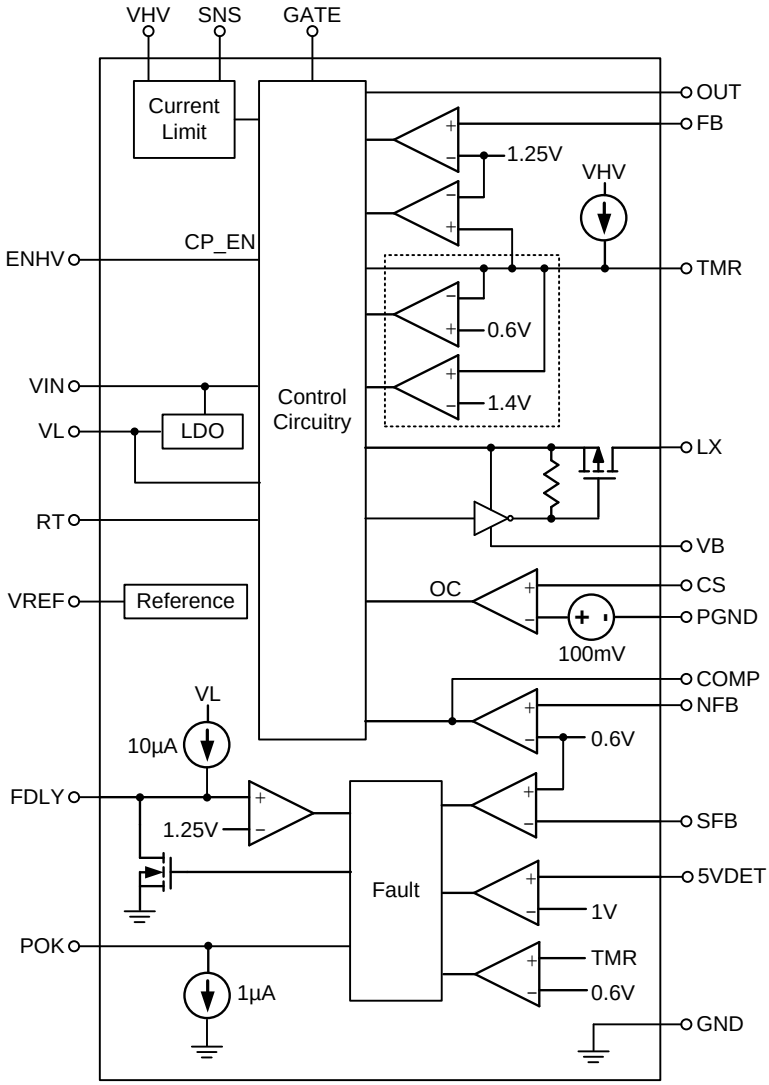


WQFN 5x5 24L

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	NFB	Feedback voltage input. The feedback for inverting output threshold is 0.6V for PWM inverting converter.
2	SFB	Secondary feedback voltage input. For adjusting POK threshold of Inverting. NV_{OUT} for PWM inverting converter.
3	PGND	Negative rail for driver and negative current sense input. Connected to GND.
4	CS	Positive current sense input for PWM inverting converter.
5, 6	LX	Switch node for PWM inverting converter.
7, 8	VIN	Power supply input for inverting PWM controller for PWM inverting converter.
9	VB	Voltage level keeper. Connect a 0.1μF ceramic capacitor to VIN.
10	FB	Voltage regulation feedback input for HV switch driver.
11	OUT	Output voltage sense input for HV switch driver.
12	GATE	N-MOSFET gate drive output for HV switch driver.
13	SNS	HVIN current sense input for HV switch driver.
14	VHV	Positive supply voltage input for HV switch driver.
15	ENHV	Enable control input for HV switch driver.
16	TMR	Fault timer setting for HV switch driver. Connect a 22nF at least ceramic capacitor to GND. There is a 3ms sense blanking time after POK pull high.
17, 25 (Exposed Pad)	GND	Ground. The exposed PAD must be soldered to a large PCB and connected to GND for maximum power dissipation.
18	VL	Low dropout regulator output for PWM inverting converter. Connect a ceramic capacitor from VL to GND. The capacitor value range from 0.47μF to 1μF.
19	POK	Logic output. Active high when SFB voltage is lower than its threshold and FDLY is higher than 1.25V. This pin can be used as HV swap controller enable control for PWM inverting converter.
20	FDLY	Delay set input for PWM inverting converter. There is an internal 10μA from VL after V_{TMR} higher than 0.6V threshold. POK is low during FDLY charge time. Connect a ceramic capacitor to GND for setting Fault delay time.
21	5VDET	VIN detection set input. For PWM Inverting Converter.
22	COMP	Compensation node for error amplifier for PWM inverting converter.
23	RT	Oscillator frequency setting for PWM inverting converter. Connect a resistor to GND for adjusting switching frequency from 300kHz to 800kHz.
24	VREF	1.25V reference output. Bypass only with a 0.1μF ceramic capacitor from VREF to GND for PWM inverting converter.

Functional Block Diagram



Operation

HV Power-Switch

The HV power switch embedded an over-voltage protection regulator that drives an external N-MOSFET only as the pass transistor. It can operate within a wide supply voltage range from 5V to 60V. The internal charge pump turns on the N-MOSFET to supply current to the loads with very little power loss. This improves the efficiency and increases the available supply voltage level to the load circuitry. Normally, the pass transistor is fully on, powering the loads with very little voltage drop. When the supply voltage surges too high, the Voltage Amplifier (VA) controls the Gate of the N-MOSFET and regulates the voltage at the OUT pin to a level that is set by the external resistive divider from the OUT pin to ground and the internal 1.25V reference. If the over-voltage/current is detected, a current source starts charging up the capacitor connected at the TMR pin to ground .The pass transistor stays on until the TMR pin reaches 1.45V, at which point the GATE pin pulls low turning off the N-MOSFET.

The potential at the TMR pin starts decreasing as soon as the over-voltage condition disappears. As the voltage at the TMR pin reaches 0.5V, the GATE pin begins to rise and turn on the MOSFET again.

The RT2910A senses an over-current condition by monitoring the voltage across a sense resistor placed between the VHV and SNS pins. An active current limit circuit controls the GATE pin to limit the sense voltage

to 50mV. A current is generated to start charging up the TMR pin when over current condition is detected. The MOSFET is turned off when it reaches 1.45V.

PWM Inverting Converter

PWM inverting converter can act a current mode non-synchronous Buck-Boost converter to generated negative output voltage, embedded an internal P-MOSFET. The UVLO (under-voltage lockout) function ensures PWM converter operates correctly with minimum VIN voltage. The VB regulator provides (V_{IN} – 5V) voltage for circuit powered directly by VIN. Connect a resistor from the RT pin to GND to set PWM switching frequency between 300kHz to 800kHz. Current limit comparator compares the CS pin voltage with 100mV reference voltage. Connect resistor between inductor and PGND to set peak inductor current limit threshold.

5VDET pin is VIN detection. After soft-start beginning, if 5VDET pin above 1V and SFB pin less 0.6V POK will pull high.

If HV-Switch Over-current/Over-voltage is triggered, the TMR pin will be charge. When V_{TMR} above 0.6V. POK will pull low immediately to turn off GATE.

At the same time, a 10μA current source is charging the FDLY capacitor. When the FDLY pin is a above 1.25V, POK will pull high to turn on GATE again.

The PWM converter also provides Over-Temperature Protection (OTP).

Absolute Maximum Ratings (Note 1)

- VHV, SNS to GND ---------- –60V to 85V
- ENHV to GND ---------- –0.3V to 45V
- ENHV Input Current ---------- 1mA
- OUT to GND ---------- –0.3V to 65V
- GATE to GND ---------- –0.3V to (OUT+AMR(GATE to OUT))
- GATE to OUT ---------- Note 5
- FB, TMR to GND ---------- –0.3V to 10V
- SFB, CS, VB, POK, FDLY, COMP, RT, VREF, NFB, VL to GND ---------- –0.3V to 6V
- VIN, 5VDET to GND ---------- –0.3V to 8V
- LX to VIN ---------- –20V to 0.3V
- TMR, FB, OUT, GATE (Note 6) ---------- –10mA
- Power Dissipation, PD @ TA = 25°C

  WQFN-24L 5x5 ---------- 3.57W
- Package Thermal Resistance (Note 2)

  WQFN-24L 5x5, θ_{JA} ---------- 28°C/W

  WQFN-24L 5x5, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  CDM (Discharge Device Model) ---------- 1kV

  HBM (Human Body Model) ---------- 2kV

  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- HV Supply Input Voltage at VHV ---------- 5V to 60V
- HV Output Voltage at OUT ---------- 4.5V to 60V
- Supply Input Voltage at VIN ---------- 4V to 7V
- Inverting Output Voltage, NV_{OUT} ---------- –12.5V to –0.5V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = V_{ENHV} = 5V, R_{RT} = 300kΩ, C_{REF} = 0.1μF, V_{HV} = 12V, T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Hot Swap Regulator with Over-Voltage Protection						
VHV Supply Current	I_{VHV}	V_{ENHV} = 0V	--	7	25	μA
		V_{ENHV} = 5V (V_{GATE} – V_{OUT})	--	2.3	5	mA
GATE Output High Voltage (Note 5)	ΔV_{GATE}	8V < V_{HV} < 80V (V_{GATE} – V_{OUT})	10	12	16	V
GATE Pull-Up Current	I_{GATE_UP}	V_{GATE} = 12V	15	40	60	μA
		V_{GATE} = V_{HV} = 48V	30	70	120	
GATE Pull-Down Current	I_{GATE_DN}	Over voltage, V_{FB} = 1.4V, V_{GATE} = 12V	45	80	150	mA
		Over current, V_{HV} – V_{SNS} = 120mV, V_{GATE} = 12V	1	3	4	
		Shutdown mode, V_{ENHV} = 0V, V_{GATE} = 12V	45	80	150	
Output						
FB Voltage	V_{FB}	V_{GATE} = 12V, V_{OUT} = 12V	1.18	1.25	1.32	V
FB Input Current	I_{FB}	V_{FB} = 1.25V	--	0.3	1	μA
Over Current Threshold	ΔV_{SNS}	V_{HV} – V_{SNS}, V_{HV} = 12V	40	50	58	mV
		V_{HV} = 48V	38	48	56	
SNS Input Current	I_{SNS}	V_{SNS} = V_{HV} = 12V to 48V	--	120	--	μA
OUT Pin Input Current	I_{OUT}	V_{SNS} = V_{HV} = 12V	--	200	500	μA
		V_{OUT} = V_{HV} = 12V, V_{ENHV} = 0V	--	0.5	2	mA
ENHV Input Voltage	V_{ENHV_H}	V_{HV} = 12V to 48V	3	--	--	V
	V_{ENHV_L}	V_{HV} = 12V to 48V	--	--	0.5	
ENHV Input Current	I_{ENHV}	V_{ENHV} = 3V	--	0.4	--	μA
TMR Current	I_{TMR_SO}	Sourcing, V_{TMR} = 1V, V_{FB} = 1.5V or ΔV_{SNS} = 60mV	20	25	30	μA
	I_{TMR_SI}	Sinking, V_{TMR} = 1V, V_{FB} = 1V or ΔV_{SNS} = 0V	2.5	3.5	5	μA
Inverting PWM Converter						
VIN Supply Voltage Range	V_{IN}		4	--	7	V
VIN Supply Current	I_{VIN}	V_{NFB} = 0.6V, V_{IN} > V_{UVLO}, V_{COMP} = 0V	--	0.75	1.5	mA
UVLO Threshold	V_{UVLO}	V_{IN} rising	--	3.6	3.9	V
		V_{IN} falling	3.2	3.5	--	
NFB Threshold	V_{NFB}	No load	0.585	0.6	0.615	V
NFB Input Current	I_{NFB}	V_{NFB} = 0.6V	--	0.1	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SFB Threshold	V_{SFB}	SFB rising	0.585	0.6	0.615	V
Current Limit Threshold	V_{CS}		90	100	110	mV
Inverting Output Voltage Range	NV_{OUT}		−12.5	--	−0.5	V
TMR Fault Detection						
TMR Threshold	V_{TMR_FT}	POK pull low, FDLY source 10μA CURRENT	--	0.6	--	V
TMR Sense Blank Time	V_{TMR_BLK}	TMR blank sensing after POK High	--	3	--	ms
FDLY						
FDLY Threshold	V_{FDLY}	Rising edge	--	1.25	--	V
FDLY Output Current	I_{FDLY}		--	10	--	μA
Reference & LDO						
VREF Output Voltage	V_{REF}	I_{REF} = 50μA	1.225	1.25	1.275	V
VL Output Voltage	V_{VL}	V_{IN} = 5V, I_{VL} = 0A	3.85	4.25	4.65	V
VL Load Regulation	V_{VL_Load}	V_{IN} = 5V, 0 < I_{VL} < 2mA	--	−20	−60	mV
Oscillator						
Oscillator Frequency	f_{SW}	R_{RT} = 300kΩ	400	500	600	kHz
Maximum Duty	D_{MAX}	300kHz to 800kHz	--	85	--	%
5VDET						
5VDET Threshold	V_{5VDET}	Falling edge, hys = 50mV	0.92	1	1.08	V
$R_{DS(ON)}$ & Thermal Shutdown						
Internal P-MOSFET On-Resistance	$R_{DS(ON)}$	V_{IN} = 5V, I_{LX} = 10mA	--	80	120	mΩ
Thermal Shutdown Temperature	T_{SD}		--	150	--	°C

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

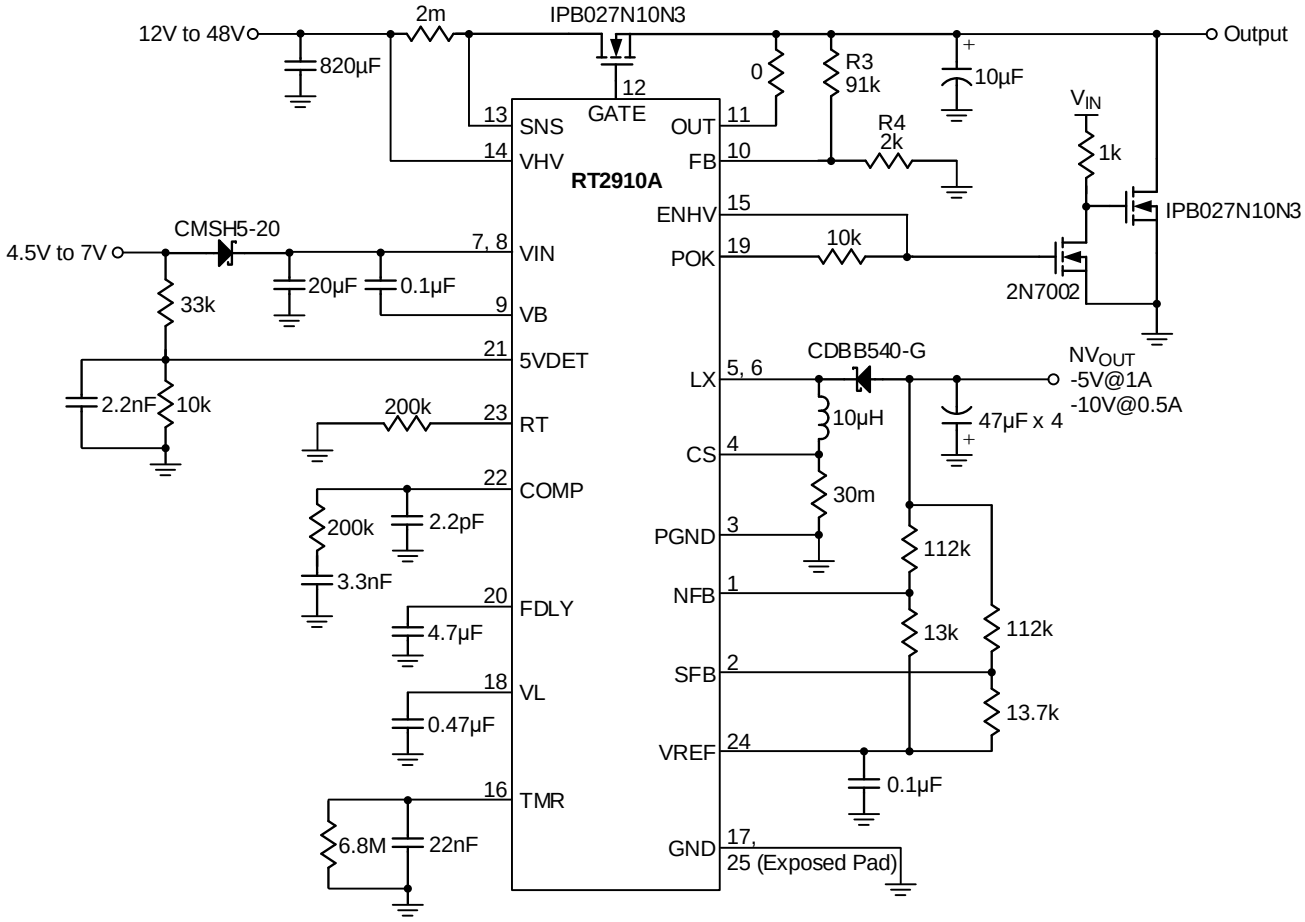
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. GATE to OUT voltage is internally generated and clamped. External driving at GATE pin is forbidden because it may damage the device.

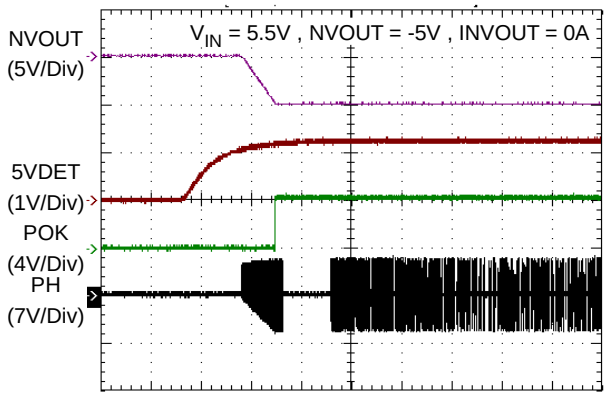
Note 6. All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Typical Application Circuit

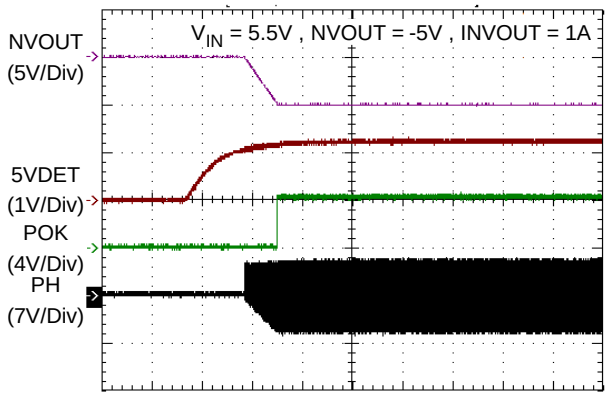


Typical Operating Characteristics

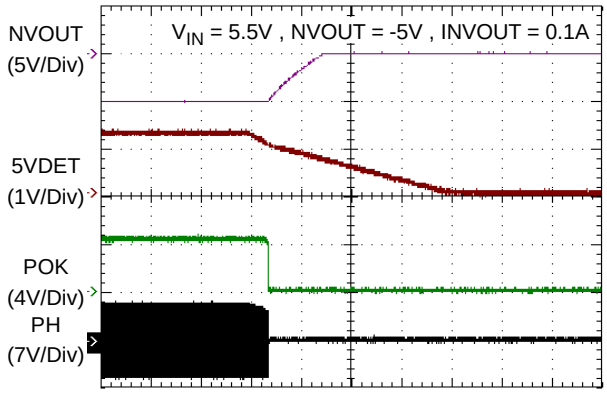
Inverting Power On from V_{IN}



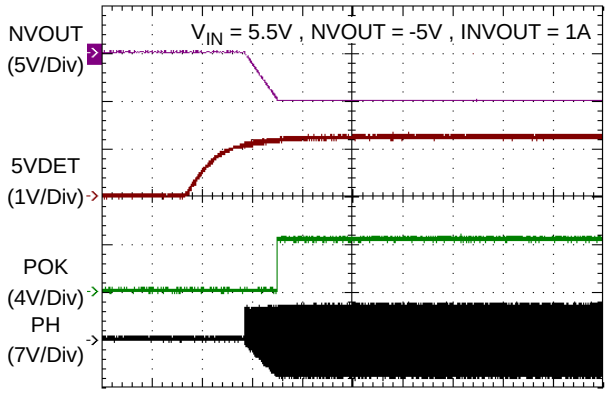
Inverting Power On from V_{IN}



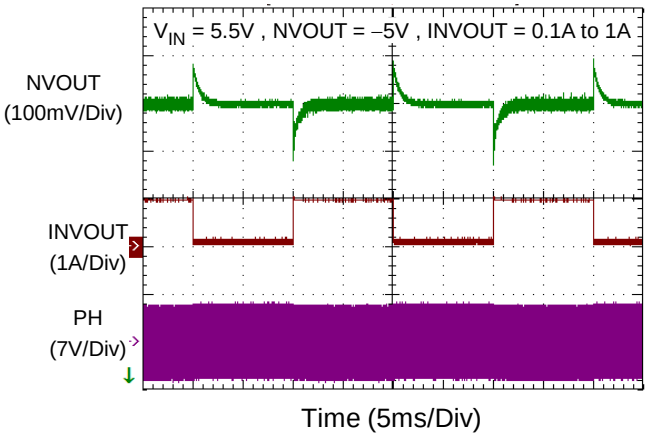
Inverting Power Off from V_{IN}



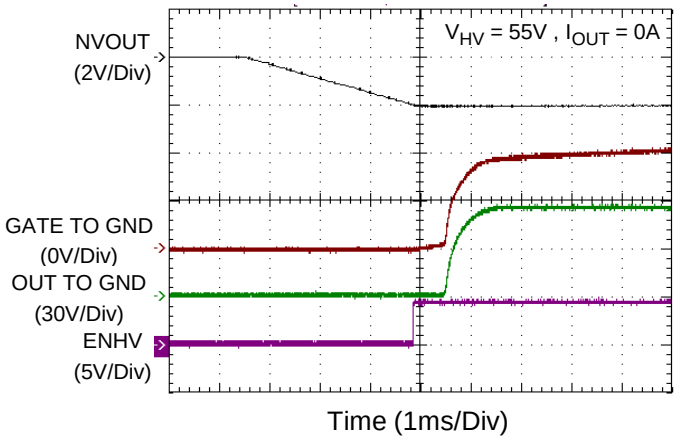
Inverting Power Off from V_{IN}



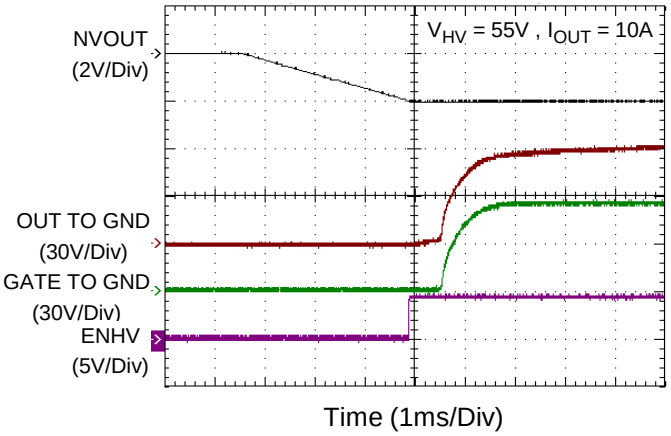
Inverting Load Transient



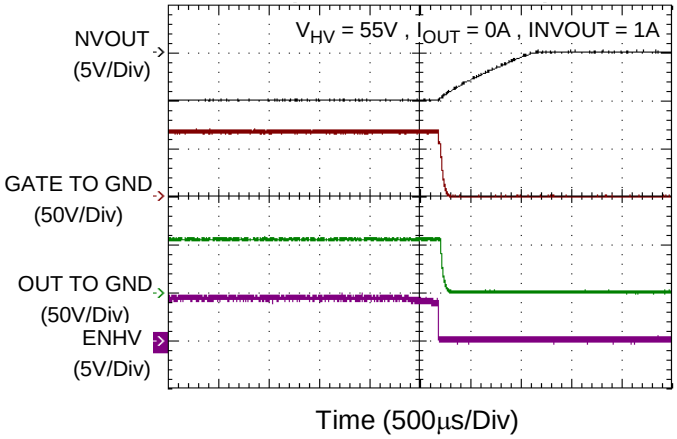
HV Switch Turn On from ENHV



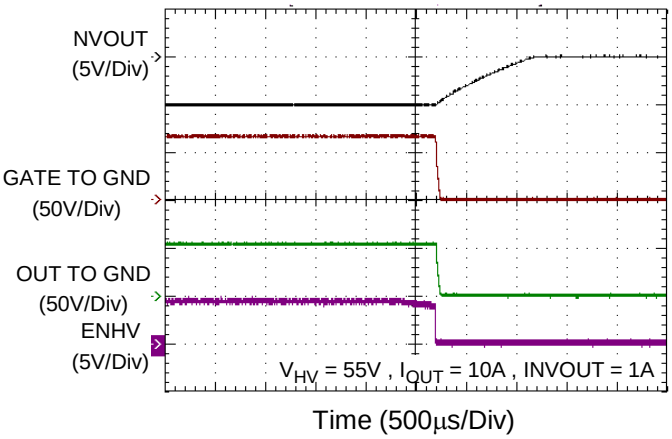
HV Switch Turn On from ENHV



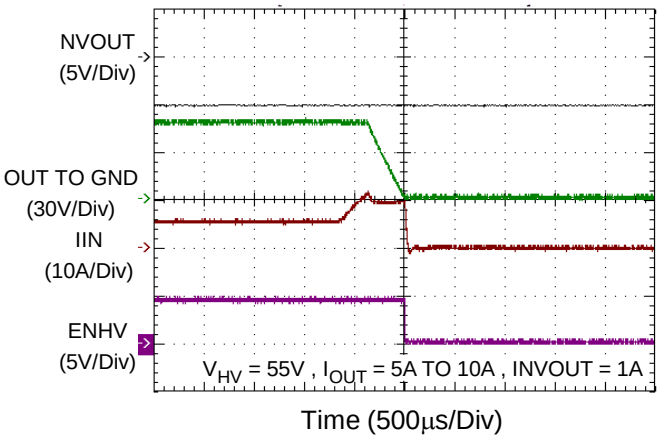
HV Switch Turn Off from ENHV



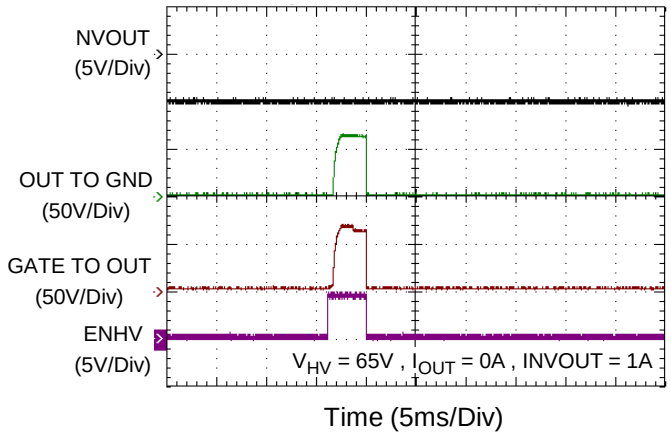
HV Switch Turn Off from ENHV



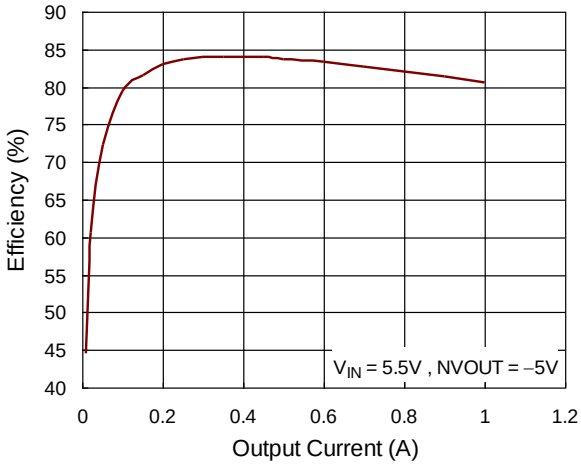
HV Switch OCP



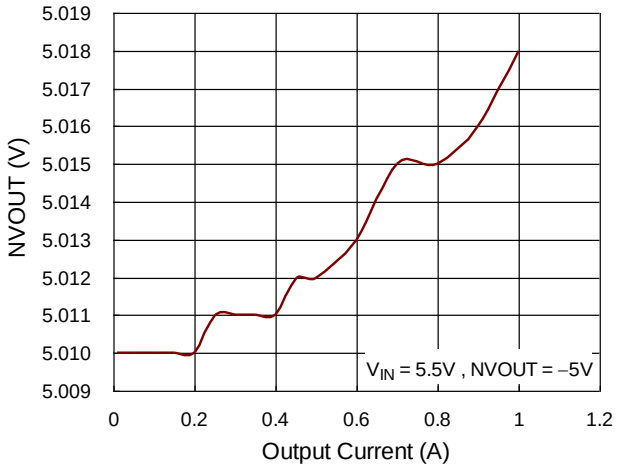
HV Switch OVP



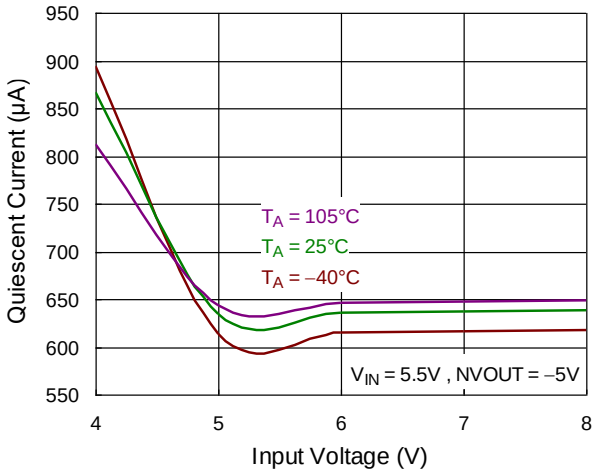
Efficiency vs. Output Current



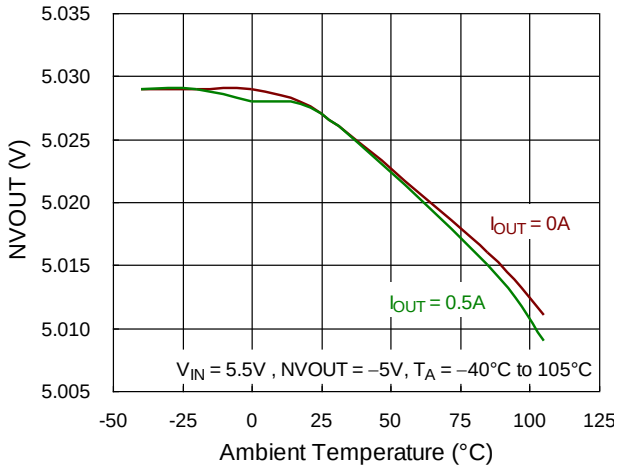
NVOUT vs. Output Voltage



Quiescent Current vs. Ambient Temperature



NVOUT VS. Ambient Temperature



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RT2910A is a PWM inverting converter integrates HV power switch driver. Features of the inverting converters include programmable constant switching frequency, current mode topology with slope compensation in case of sub-harmonic at over 50% duty cycle operation , internal linear regulator , and internal 0.6V NFB reference with soft-start control allows output voltage to be precisely regulated at adjustable output voltage .Protection features include adjustable current limit and over-temperature protection.

The HV power switch is suited for hot swap applications as an over-voltage protection regulator with programmable current limit threshold equals 50mV that drives an external N-MOSFET as the pass transistor. It features a TMR function for over-voltage protection and over-current protection to avoid N-Channel MOSFET damaged.

It operates from a wide supply voltage range of 5V to 60V. The internal charge pump circuit is included to turn on the N-Channel MOSFET to supply current to the loads with very little power loss.

HV Power Switch Driver

Over-Voltage Protection

The RT2910A is equipped with over-voltage protection (OVP) function. When the voltage at FB pin exceeds a threshold of approximate 1.25V, the MOSFET is turned off. The MOSFET can be turned on again once the voltage at FB pin drops below 1.25V

During this period, the N-MOSFET is still on, and continues to supply current to the load. This allows uninterrupted operation during short over-voltage transient events. When the voltage regulation loop is engaged for longer than the time-out period, set by the timer capacitor connected from the TMR pin to ground, the GATE pin is pulled low to turn off the MOSFET. This prevents the N-MOSFET from being damaged during a long period of over-voltage. The OVP voltage can be set by the following equation:

V_{OUT_OVP} = 1.25 x (1 + R3 / R4)

Where, R3 and R4 are the voltage divider from VOUT to GND with the divider center node connected to FB pin.

Over-Current Protection

The RT2910A features an adjustable current limit that protects against short circuits or excessive load current. During an over-current event, the GATE pin is regulated to limit the current sense voltage between the VHV and SNS pins to 50mV. The current limit is set by the following equation:

I_{LIM} = 50mV/R_{SNS}

An over-current fault occurs when the current limit circuitry has been engaged for longer than the time-out delay set by the TMR pin timer capacitor. The GATE pin is then immediately pulled low to GND turning off the MOSFET.

Fault Timer

The RT2910A includes an adjustable fault timer pin. Connecting a capacitor from the TMR pin to ground sets the delay timer period before the MOSFET is turned off. The same capacitor also sets the cool off period before the MOSFET is allowed to turn back on after the fault condition has disappeared. The TMR pin should be tied to ground if this feature is not used.

Once a fault condition, either over-voltage or over-current event, is detected, a current source charges up the TMR capacitor. The timer charge up current is fixed around 25μA. When the voltage at the TMR pin, reaches the 0.6V threshold,

1. POK pin is pulled low.
2. The ENHV pin is pulled low.
3. The V_{GATE_OUT} is pulled low.
4. C_{FDLY} start to charge , when V_{TMR} drop to 0.2V.
5. POK pin is pulled high again.

The fault sequence is as Figure 1.

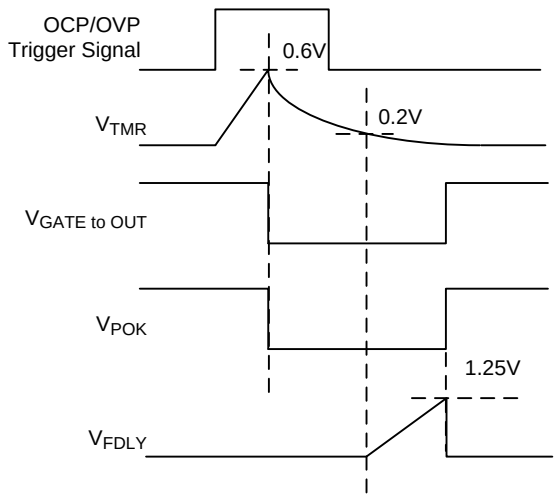


Figure 1. OCP/OVP Fault Sequence

If the fault condition persist, fault sequence as Figure 2. C_{FDLY} is charge to 1.25V POK (ENHV) , GATE pull high. HV switch is operation, but fault condition is still exist, C_{TMR} is charge to 1.45V within 3ms TMR blank time. POK (ENHV) , GATE pull low again. C_{TMR} is discharge by 3.5uA until 3ms time out. Because POK (ENHV) pull low, so V_{TMR} is discharged to 0.2V, C_{FDLY} start charge again.

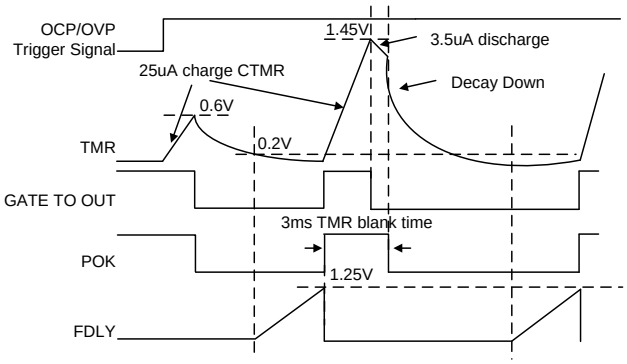


Figure 2. OCP/OVP Fault Condition Persist Sequence

MOSEFT Selection

The N-Channel MOSFET load switch is the critical component for the protection circuit. Choosing an appropriate device is not difficult but there are many important requirements. The most important are :

- on-resistance ($R_{DS(ON)}$)
- maximum current rating
- maximum drain-source voltage
- maximum gate-source voltage
- power dissipation and safe operating area (SOA)
- gate threshold (for lower VIN applications)

For most of the time the MOSFET will be fully on. In that state, the voltage loss and power dissipation are a simple matter of $R_{DS(ON)}$ and current. Choose a device that doesn't drop more voltage than is acceptable considering the minimum value the intended input voltage and the voltage requirements of the load, and one that can handle the required continuous current.

Avoid logic-level MOSFETs with their low VGS maximum ratings, or add a GATE-VOUT clamp to avoid damaging. The RT2910A GATE drive voltage may be as high as 14V so standard-threshold MOSFETs with 20V VGS ratings are recommended.

When the MOSFET is turned off (whether in shutdown or in OVP or OCP) the full input voltage appears across the MOSFET. Choose a MOSFET with a maximum drain-source voltage exceeding your maximum input surge voltage.

During an over-voltage (OV) event the MOSFET will linear regulate the output voltage delivered to the load. According to the timing determined by the capacitor connected at the TMR pin, the circuit will turn the load on and off periodically until the over-voltage ends. While linear-regulating, the MOSFET will dissipate power and heat up. Since TMR charges at twice the rate that it discharges, the MOSFET will linear regulate with a duty cycle of about 12% during a long continuous OV event. If the OV event is shorter than the TMR charge timing then examine the MOS ET's safe operating area (SOA) graph, using (V_{HV} – V_{OUT}) for MOSFET drain to source voltage and $I_{LOAD(VOUT)}$ for the drain current, to determine if the over-voltage event will cause MOSFET damage. It may be helpful to adjust C_{TMR} to meet the MOS ET's SOA limits.

If the OV event lasts more than one TMR cycle then the MOSFET will turn on and off, dissipating power each time it is on and linear regulating and cooling down when it is off. In this case, use one of the longer-timed areas of the SOA graph but adjust the drain current value by the 12% duty cycle of the MOSFET on periods determine if the MOSFET will work. For thermal management, the MOSFET dissipation during long over-voltage events is :

$PD_{MOSFET(OV)}$ = DC x (V_{HV} – V_{OUT}) x $I_{LOAD(VOUT)}$

where DC is the duty cycle of linear regulation, typically about 12%.

During an over-current (OC) event the MOSFET will regulate the output current delivered to the load and the output voltage will collapse to whatever voltage is needed to sustain the OC threshold current. According to the timing determined by the capacitor connected at the TMR pin, the circuit will turn the load on and off periodically until the over-current event ends. While regulating the load current, the MOSFET will dissipate power and heat up. Unlike an OV event, the output voltage and the MOSFET's drain-source voltage may not be easily predicted. If the output is shorted the voltage may collapse nearly to zero, placing the entire input voltage across the MOSFET. Further, this type of event is likely to continue for long periods. If the output voltage during the OC event is not easily determined, use zero for V_{OUT}.

For the rare OC event that is short compared to the TMR timing, examine the MOSFET's safe operating area (SOA) graph, using (V_{HV} – V_{OUT}) for MOSFET drain to source voltage and your $I_{OC\_THRESHOLD}$ for drain current, to determine if the over-current event will cause MOSFET damage.

If the OC event lasts more than one TMR cycle then the MOSFET will turn on and off, dissipating power each time it is on and cooling down when it is off. In this case, use one of the longer timed areas of the SOA graph (perhaps the DC area) but adjust the $I_{OC\_THRESHOLD}$ value by the 12% duty cycle of the MOSFET on periods to determine if the MOSFET will work. For thermal management, the MOSFET dissipation during long over-current events is :

$PD_{MOSFET(OC)}$ = DC x (V_{HV} – V_{OUT}) x $I_{OC\_THRESHOLD}$ where DC is the duty cycle of current regulation, typically about 12%.

Parallel MOSFETs

Select a single MOSFET for most applications. If the $R_{DS(ON)}$ target is very low and difficult to achieve at the necessary voltage rating, multiple devices may be used in parallel. Parallel devices can decrease the voltage drop in normal operation and reduce dissipation. However, SOA requirements must generally be met by a single device.

In OV and OC conditions, GATE will decrease until the programmed output voltage or current is maintained. In that state, the MOSFET with the lowest threshold will carry more current than other parallel MOSFETs with higher thresholds, perhaps dramatically more. It's generally best to assume that one device will be subjected to the entire SOA stress.

Application Design Example

Using the typical applications circuit as a design example with the following specifications: Automotive Application

V_{HV} = 48V to 55V DC with transients up to 80V.

Output Voltage : V_{OUT} <60V

Current Limit (I_{LIM}) : 10A

Over-voltage Duration : 5ms

Output Over-voltage Protection Setting :

Set the OVP threshold at 58V, choose R4 as 2k and calculate R3 according to the following equation:

V_{OUT_OVP} = 1.25 x (1 + R3 / R4)

Select R3 as a standard 1% value of 91k and calculate the resulting threshold as :

V_{OUT_OVP} = 1.25 x (1 + 91K / 2K) = 58.125V

Calculate the sense resistor, R_{SNS}, according to the following formula :

R_{SNS} = (V_{SNS} / I_{LIM}) = (50m / 10A) = 5mΩ

Calculate the power dissipation of RSNS to avoid overheating the sense resistor :

$PD_{(RSNS)}$ = 1.2 x $(I_{LIM})^2$ x R_{SNS} = 1.2 x $(10)^2$ x 5m = 0.6W

Select a 1W sense resistor consider a parallel combination of lower-wattage resistors.

Over-voltage/Over-current Timer Setting :

Calculate the value of fault timing capacitor (C_{TMR}) using the typical TMR pull-up current and TMR latch threshold with the following formula :

C_{TMR} = (t_{LATCH} x I_{TMR_UP}) / V_{TMR} = (5ms x 25μA) / 1.45 = 0.086μF

Select the standard value of 0.1μF and calculate the resulting fault timing :

T_{Latch} = (C_{TMR} x V_{TMR}) / I_{TMR_UP} = (0.1μ x 1.45) / 25μ = 5.8ms.

During an over-voltage or over-current event, GATE will

regulate the output voltage or current while CTMR charges. When the voltage on the timing capacitor (V_{TMR}) reaches the fault threshold (V_{TMR_F}, 1.45V typical) GATE will turn off the external MOSFET soon.

In the event of a long fault, GATE will turn on and off repeatedly. The on and off timings (t_{GATE_ON} and t_{GATE_OFF}) are controlled by the TMR charge and discharge currents (I_{TMR_UP} and I_{TMR_DN}) and the voltage difference between the TMR latch and unlatch thresholds (V_{TMR_L} - V_{TMR_UL}) :

$t_{GATE\_ON} = [C_{TMR} \times (V_{TMR\_L} - V_{TMR\_UL}) / I_{TMR\_UP}]$

$t_{GATE\_ON} = [0.1\mu F \times (1.45V - 0.4V) / 25\mu A] = 4.2ms$

$t_{GATE\_OFF} = [C_{TMR} \times (V_{TMR\_L} - V_{TMR\_UL}) / I_{TMR\_DN}]$

$t_{GATE\_OFF} = [0.1\mu F \times (1.45V - 0.4V) / 3.5\mu A] = 30ms$

Choose the MOSFET

Select the MOSFET VDS rating, allowing for your maximum input voltage and transients. Then select an operating $R_{DS(ON)}$ to meet any voltage drop specifications and your on-state dissipation allowance. Finally, its package must be able to handle that dissipation and control its operating temperature.

Most manufacturers list a maximum $R_{DS(ON)}$ at 25°C and provide a typical characteristics curve from which values at other temperatures can be estimated. You can also use the below equation to estimate maximum $R_{DS(ON)}$ from the 25°C specification :

$R_{DS(ON)\_MAX} = T_{J(MAX)} - 25°C) \times 0.5\% / 1°C$

Given the 48V minimum input and the 10A output current, the $R_{DS(ON)}$ must be very low to avoid dropping a large percentage of the input voltage. To limit the drop to 1% of 48V (48mV) requires an 4.8mΩ maximum. The package needs to dissipate about $(10A)^2 \times 4.8m\Omega$ = 0.48W into a hot automotive ambient temperature.

Something like the IR Rectifier IRFS4310PbF, with its V_{D-S} at 100V rating, 5.6mΩ $R_{DS(ON)}$ (typ.) can be to parallel in order to reduce thermal on MOSFET. D^2PAK package should be more than adequate.

PWM Inverting Converter

Internal Soft-start

The RT2910A feature a “digital soft-start” that is preset and requires no external capacitor. Upon startup, the NFB threshold decrements from the reference voltage 0.6V in 128 steps, and each step is 18 clock cycle. So soft-start time can be calculated as below

$T_{SS} = (128 \times 18) / F_S$

Where F_S is PWM switching frequency.

Soft-start is implemented:

1. When exiting under-voltage lockout.
2. When V_{5VDET} is above 1V.
3. When exiting OTP.

Once POK is high, soft-stare is canceled and NFB reference pulled to 0.6V immediately.

Internal Regulator

The RT2910A incorporates an internal low-dropout regulator (LDO). This LDO has a 4.25V output and provides PWM converter internal circuit power request. The internal LDO has under-voltage lockout circuit which monitors the voltage of VL. The under-voltage lockout threshold is typical 3.6V. For best performance, it is recommended to connect VL to VIN when the input supply is less than 4.5V and connect a 0.47μF capacitor to GND to compensate loop and decoupling.

UVLO (Under-Voltage Lockout)

The RT2910A have an internal under-voltage lockout circuit that monitors the voltage of VIN. If VIN falls below the UVLO threshold (Typ. 3.5V) the control logic turns off the internal P-MOSFET. The other internal circuits are still powered and operating. When VIN higher than UVLO falling threshold plus 100mV, the RT2910A resumes operation from a start-up condition (soft-start).

Oscillator Frequency

The RT2910A is a current mode constant switching frequency converter and it provides the RT pin for switching frequency setting. User can set switching frequency by resistor (R_{TON}) connected from the RT pin to GND. The switching frequency calculation is shown as below :

$F_S = 1 / [(R // R_{TON}) \times C + 0.2294\mu s]$

Where R is inverting resistor: R = 325kΩ

C = 11.4pF

Power On/Off Sequence :

The RT2910A use a POK indicator to enable HV-Switch gate driver.

Connects POK pin and ENHV pin. POK pulls high to enable HV-Switch gate driver to turn on external N-MOSFET.

POK go high must satisfy the below conditions :

1. V_{IN} is above POR threshold.
2. V_{TMR} is lower than 0.6V (HV Switch protection is not triggered).
3. V_{SFB} pin is lower than 0.6V.
4. V_{5VDET} pin is above 1V.
5. Not in OTP status.

In order to avoid inrush current on inductor, we suggest POK rising when NV_{OUT} = –4.75V (95% of NV_{OUT} = –5V)

The power on sequence must be NV_{OUT} rising to 4.75V then POK pull high to enable HV-Switch driver to turn on N-MOSFET, the power off sequence must be HV-Switch output voltage falling to 10% level, then NV_{OUT} start to falling.

The detail power on/off sequence is as Figure 3.

The power on/off sequence bases on typical application circuit.

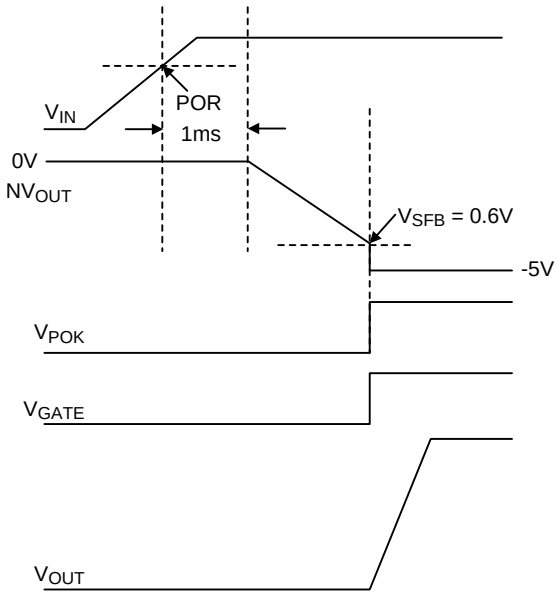


Figure 3. (a) Power On Sequence

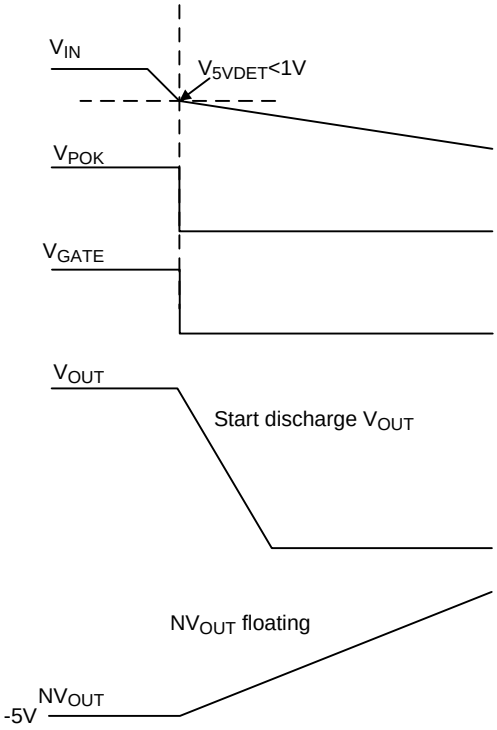


Figure 3. (b) Power Off Sequence

Connect a resistor divider at SFB between NV_{OUT} and V_{REF} to adjust POK falling edge threshold. The threshold voltage is set according to the following equation :

$NV_{OUT} = V_{REF} – (V_{REF} – V_{SFB}) \times [(R_{SFB1} + R_{SFB2}) / R_{SFB2}]$

Where V_{REF} is a reference voltage, V_{SFB} is scaled output voltage.

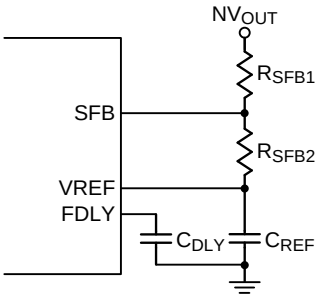


Figure 4. POK Threshold Voltage and Fault Delay Time Setting

Set Fault delay time by connecting FDLY pin with a capacitor (C_{DLY}) to GND. It utilizes the internal 10μA current source to charge C_{DLY} to 1.25V when V_{TMR} is over 0.6V threshold voltage. This calculation formula is as below :

$C_{DLY} \times V_{REF} = I_C \times T_{DLY}$

$T_{DLY} = (C_{DLY} \times V_{REF}) / I_C$

Where V_{REF} is 1.25V, I_C is internal current source (Typ. 10μA) and C_{DLY} is external component.

The RT2910A has a FDLY pin discharge monitor circuit to ensure the FDLY pin charging starts when the FDLY pin voltage is low enough (Typ. 0.2V). The function avoids POK low short pulse and provides enough Fault delay time. The detail sequence of FDLY pin is as Figure 5.

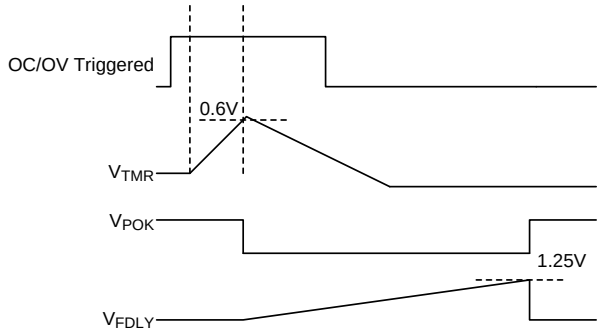


Figure 5. Fault Sequence when OC/OV

Current Limit

The RT2910A provides a cycle-by-cycle current limit control. The current limit circuit implement a peak current sensing mechanism. If the inductor current is over the current limit threshold, the PWM controller turns off the internal P-MOSFET to stop charging the inductor. The RT2910A sensing the inductor current by an external sensing resistor. We suggest that the OCP trigger point is set at 1.1 to 1.5 times of load current, where, we select 1.25 times.

The current limit calculation formula as below :

$I_{L\_OC} = [(I_{OUT} \times 1.25) / (1 - D)]$

$R_{SENSE} = V_{CS\_REF} / I_{L\_OC}$

Where V_{CS_REF} is current limit threshold.

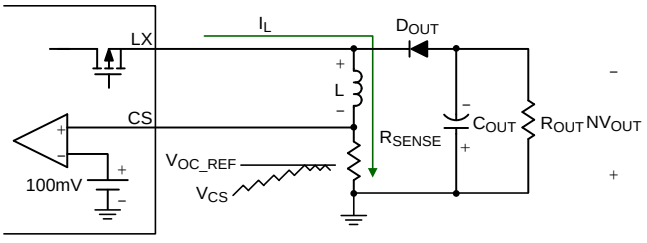


Figure 6.Over-Current Setting

Output Voltage Setting

Connect a resistor divider at the NFB pin and VREF pin to adjust the output voltage. The output voltage is set according to the following equation :

$NV_{OUT} = V_{REF} - (V_{REF} - V_{NFB}) \times [(R_{NFB1} + R_{NFB2}) / R_{NFB2}]$

Where V_{REF} is a reference voltage 1.25V, V_{NFB} is scaled output voltage.

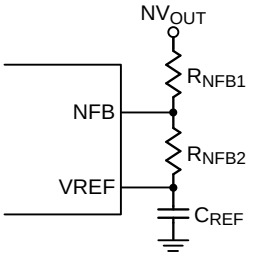


Figure 7. Setting Output Voltage with a Voltage Divider

Input Capacitor selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 20μF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The next step is to select a proper capacitor for RMS current rating. One good design uses more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to from a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$\Delta V = [I_{IN} \times (1 - D)] / (C_{IN} \times F_S) = (I_O \times D) / (C_{IN} \times F_S)$

$C_{IN} = (I_O \times D) / (\Delta V \times F_S)$

Output Capacitor Selection

The purpose of the output capacitor is to reduce the output ripple. We can use the following equation to calculation C_{OUT}.

$C_{OUT} > (I_{OUT} \times D_{MAX}) / \Delta V_{OUT} \times F_S$

When load transient condition occurs, the output

capacitor supplies the load current before the controller can respond.

Therefore, the ESR will dominate the output voltage SAG during load transient. The output voltage under-shoot (V_{SAG}) can be calculated by the following equation :

$V_{SAG} = \Delta I_{LOAD} * ESR$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient.

Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Inductor selection

There are different ways to calculate the required inductance. A good way to do this is to design the inductor current ripple current ΔI_L between 20%~30% of the average inductor current I_L. This will make the regulator designed into a good load transient response with an acceptable output ripple voltage.

Therefore, we suggest peak-to peak inductor current ripple ΔI_L is designed as :

$\Delta I_L = 0.2$ to $0.3 \times I_L$

So required inductance :

$L = (V_{IN} \times D) / (F_S \times \Delta I_L)$

Where $D = V_{OUT} / (V_{IN} + V_{OUT})$

Thermal Protection

The device implements an internal thermal shutdown function when the junction temperature exceeds 150°C. The thermal shutdown forces the device to stop loop regulation and pull low POK. Once OTP release, the RT2910A will soft-start again.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-24L 5x5 package, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (28°C/W) = 3.57W for a WQFN-24L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

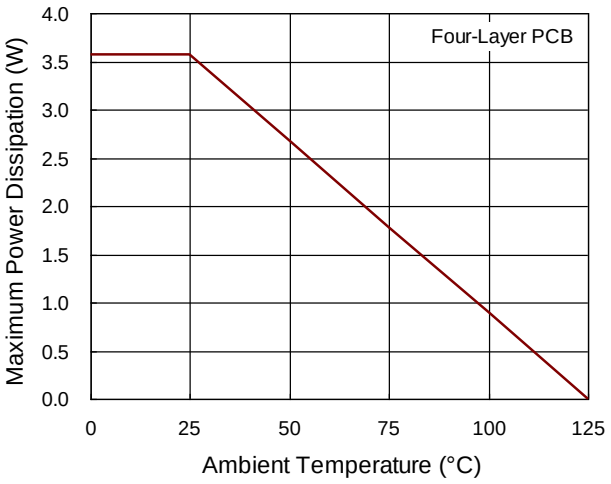
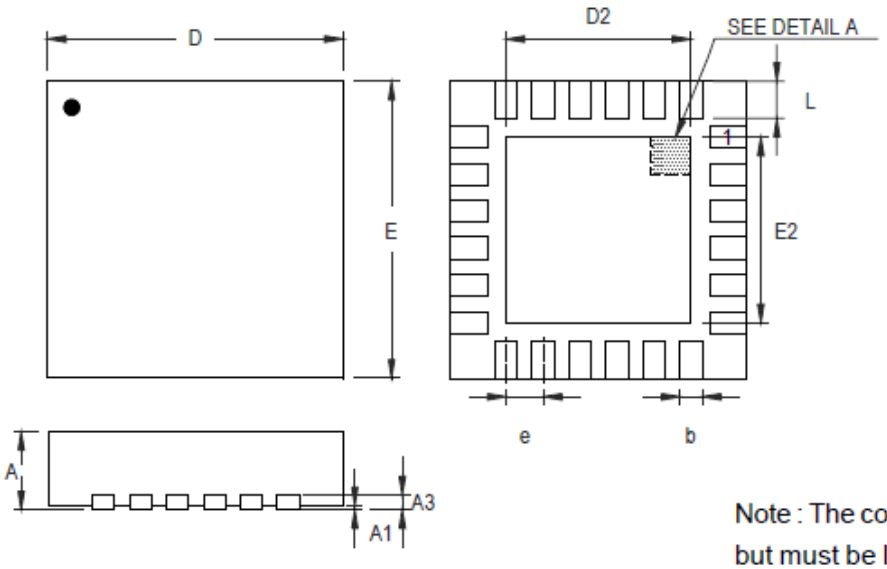
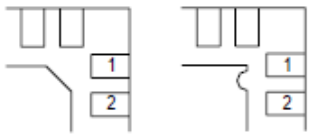


Figure 8. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.350	0.010	0.014
D	4.950	5.050	0.195	0.199
D2	3.100	3.400	0.122	0.134
E	4.950	5.050	0.195	0.199
E2	3.100	3.400	0.122	0.134
e	0.650		0.026	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 5x5 Package

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Datasheet Revision History

Version	Date	Description	Item
01	2023/5/30	Modify	Typical Application Circuit on P9 Application Information on P13