23V/8A Ideal Diode Protection Switch

1 General Description

The RT1985 provides an ideal diode reverse current blocking function with low forward voltage and an enable input for disconnection. The 3.4V to 23V input operating range and 8A continuous current rating make the RT1985 well suited for multi-port USB-C sink current applications. In addition, this part includes a 28V Absolute Maximum Rating (AMR), a 20A peak current rating (up to 10ms), undervoltage-lockout, overvoltage protection, and over-temperature protection.

An adjustable soft-start circuit sets the output voltage slew rate and manages inrush current into high capacitance loads. Short-circuit protection is provided during this period, while the integrated MOSFET provides a low forward voltage drop and high Safe Operating Area (SOA).

The RT1985 is available in a VDFN-12TL 3x3 package and can operate over –40°C to 125°C junction temperature.

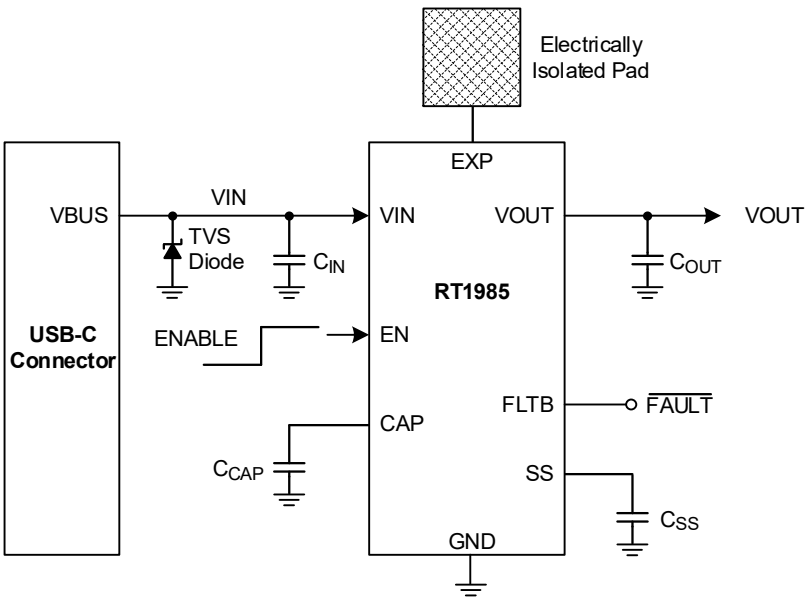
2 Features

- **8A Continuous/20A Peak Current Capability**
- **Input Supply Voltage: 3.4V to 23V**
- **20mΩ (typical) R_{ON}**
- **Analog Ideal Diode Gate Control**
  - **Blocks Reverse Current**
  - **Avoids Switch Chatter**
  - **Enables Fast Power Swap**
- **Programmable Soft-Start**
- **Overvoltage Protection**
- **Over-Temperature Protection**
- **Start-Up Short-Circuit Protection**
- **Compliance with IEC 61000-4-2 and IEC 61000-4-5 Standards**

3 Applications

- USB-C/Thunderbolt Sink Power Delivery
- Docking Stations
- Power ORing Applications

4 Simplified Application Circuit



5 Ordering Information

RT1985 □-□

Packing
A: Pin 1 Orientation
(Quadrant 2, Follow EIA-481)

Package Type(1)
N: VDFN-12TL 3x3 (V-Type)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

YG=: Product Code
YMDAN: Date Code

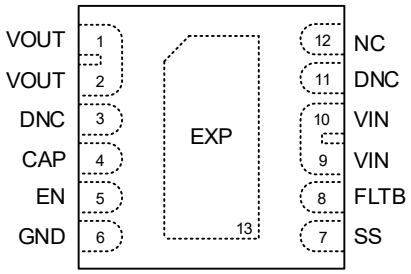
Ideal Diode Protection Switch Selection Table

Part Number	Input Supply Voltage	Continuous Current Capability	OVP Threshold	Package
RT1985	3.4V to 23V	8A	Fixed	VDFN-12TL 3x3
RT1986	3.4V to 23V	5.5A	Fixed	VDFN-12TL 3x3
RT1987	3.4V to 32V	8A	Programmable	VDFN-12T1L 3x3
RT1988	3.4V to 53V	8A	Programmable	VDFN-20TL 5.2x4

Table of Contents

7 Pin Configuration

(TOP VIEW)

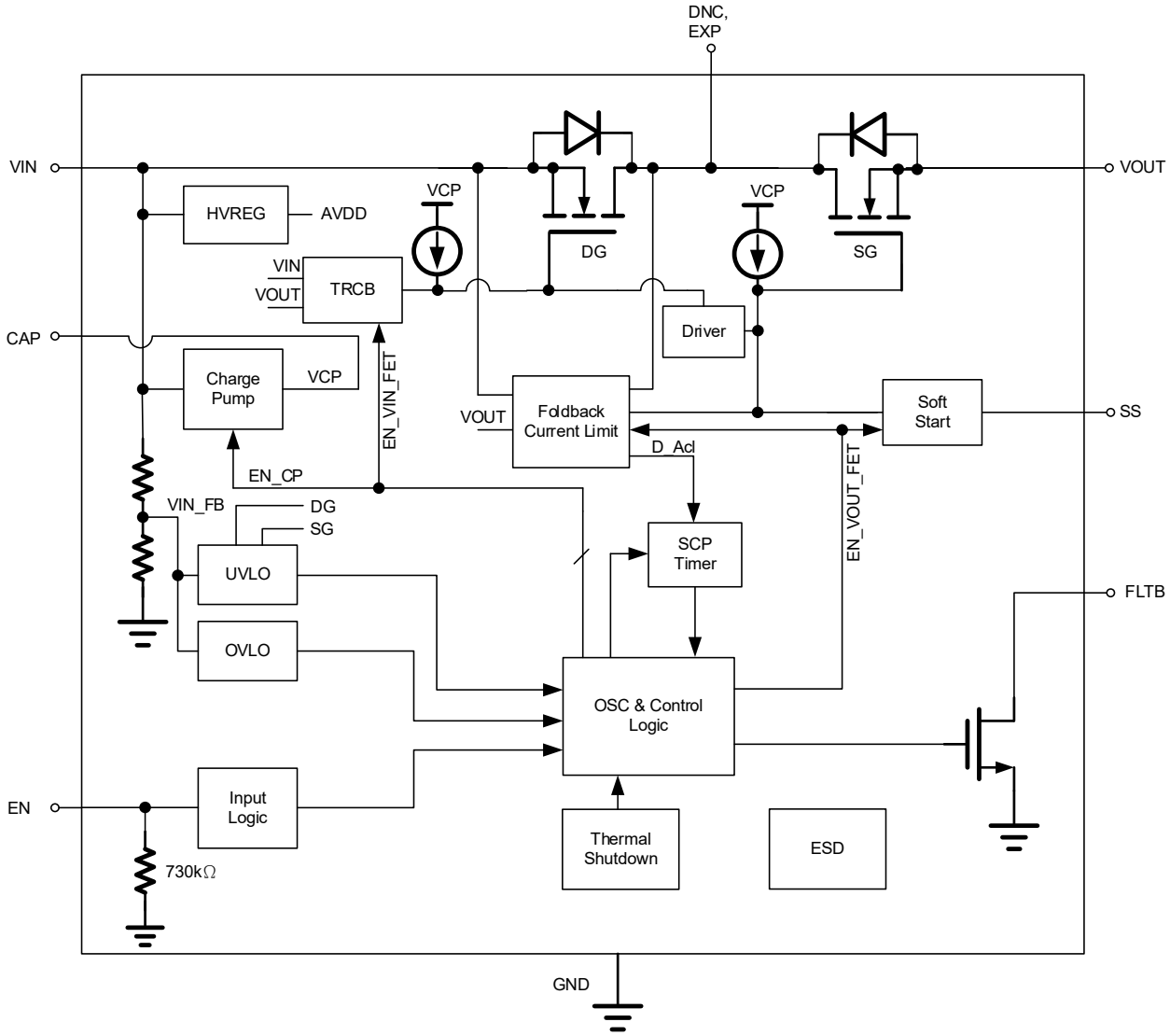


VDFN-12TL 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	VOUT	Output voltage. Connect to the load.
3	DNC	Do Not Connect. Internally connected to the Exposed Pad (EXP).
4	CAP	Connect a 1nF capacitor to GND.
5	EN	Enable active high. Pull high to enable the ideal diode function. Pull low to disconnect VIN from VOUT.
6	GND	Ground.
7	SS	Soft-start input. Connect a capacitor, C_{SS}, from SS to GND to set the soft-start time.
8	FLTB	Open-drain fault indicator. Connect a pull-up resistor to a low-voltage supply. This pin pulls low if a fault condition is detected.
9, 10	VIN	Input voltage. Connect to a power input and bypass with a 10μF capacitor to GND.
11	DNC	Do Not Connect. Internally connected to VIN.
12	NC	No Connect.
13 (Exposed Pad)	EXP	Exposed pad. The exposed pad is electrically connected to the common-drain node of the internal power MOSFET and must be electrically isolated. For improved thermal performance, this pad should be soldered to a large electrically isolated pad and tied to as much copper (electrically isolated) as possible using many vias.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN, VOUT, DNC to GND ---------- –0.3V to +28V
- EN, SS, FLTB to GND ---------- –0.3V to +6V
- CAP to GND ---------- –0.3V to +36V
- CAP to VIN ---------- -0.3V to +12V
- IEC 61000-4-5 at VIN no CAP ---------- 35V
- Power Dissipation, P_D @ T_A = 25°C

  VDFN-12TL 3x3 ---------- 1.85W
- Package Thermal Resistance (Note 3)

  VDFN-12TL 3x3, θ_{JA} ---------- 53.98°C/W

  VDFN-12TL 3x3, θ_{JC} ---------- 5.25°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

11 ESD Ratings

(Note 4)

- HBM (Human Body Model) All Pins ---------- ±4kV
- IEC 61000-4-2 at VIN and VOUT ---------- ±8kV

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VIN ---------- 3.4V to 23V
- EN, FLTB ---------- 0V to 5.5V
- CAP to VIN ---------- 0V to 5.5V
- SS ---------- 0V to 3V
- IVIN, IVOUT ---------- 0A to 8A
- Peak IVIN, IVOUT for 10ms at 2% Duty Cycle ---------- 20A
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

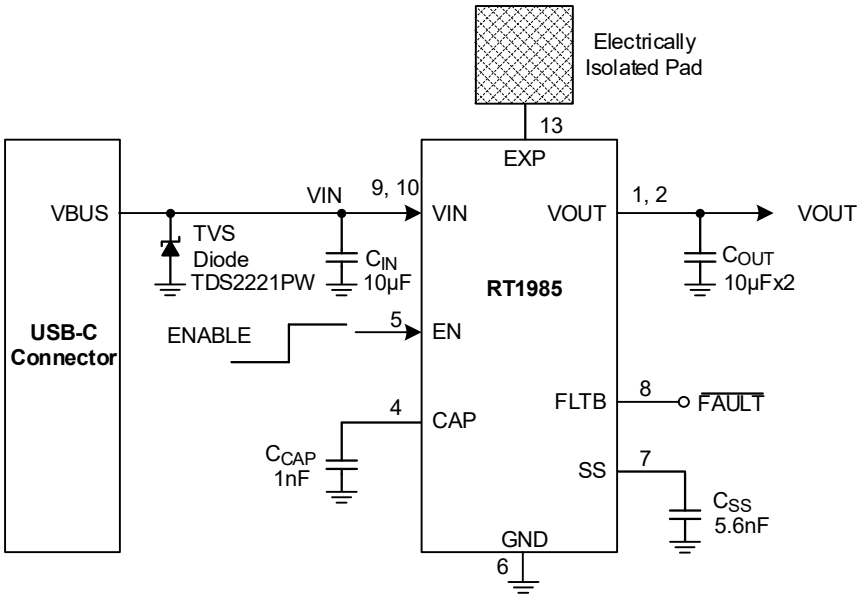
13 Electrical Characteristics

T_A = T_J = 25°C, V_{IN} = 20V, V_{EN} = 5V, C_{IN} = 10µF, C_{OUT} = 10µF, C_{SS} = 5.6nF, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
Input Voltage Range	V_{IN}		3.4	--	23	V
Input Undervoltage-Lockout	V_{IN_UVLO}	VIN rising	3.0	--	3.35	V
UVLO Hysteresis	V_{UVLO_HYS}		--	250	--	mV
Input Quiescent Current	I_Q	I_{OUT} = 0A	--	500	750	µA
Input Shutdown Current	I_{SHDN}	EN = 0V	--	32	70	µA
Output Leakage Current	I_{OUT_LK}	V_{OUT} = 20V, V_{IN} = 0V, EN = 0V	--	32	48	µA
Switch On Resistance	R_{ON_20V}	V_{IN} = 20V, I_{OUT} = 1A (Note 6)	--	20	--	mΩ
	R_{ON_5V}	V_{IN} = 5V, I_{OUT} = 1A (Note 6)	--	21	--	mΩ
Enable Input Rising Threshold	V_{EN_R}	EN rising	--	--	1.4	V
Enable Input Falling Threshold	V_{EN_F}	EN falling	0.6	--	--	V
Enable Input Pull-down Resistance	R_{EN_PD}	EN rising	475	730	985	kΩ
FLTB Pull-down Voltage	V_{FLTB_PD}	I_{FLTB} = –3mA	--	--	0.3	V
Input Overvoltage Protection						
Overvoltage Protection Threshold	V_{OVP_R}	VIN rising	23.1	24	25	V
Overvoltage Protection Blanking Time	t_{BLK_OVP}	Latch off. No restart.	--	512	--	µs
Ideal Diode (Reverse Current Blocking)						
Ideal Diode Forward Regulation Voltage	V_{FWD}	VIN – VOUT	--	35	--	mV
Fast Reverse Current Threshold	V_{FRC}	VIN – VOUT fast turn off	--	–50	--	mV
Fast Reverse Current Delay Time	t_{FRC}		--	0.5	--	µs
Dynamic Timing Characteristics						
Turn-On Delay Time	t_{D_ON}	From EN rising edge to VOUT reaching 10% of VIN	--	8	--	ms
Turn-On Rise Time	t_{ON}	VOUT from 10% to 90%	--	1.9	--	ms
Short-Circuit Protection Restart Time	t_{SCP_RST}	During soft-start	--	64	--	ms
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}	Temperature rising. System latches off.	--	140	--	°C
Start-Up Short-Circuit Protection						
Short-Circuit Protection Current Limit	I_{SCP}	VIN – VOUT ≥ 18V, during soft-start	--	3	--	A
		VIN – VOUT = 10V, during soft-start	--	10	--	
		VIN – VOUT ≤ 4V, during soft-start	13	--	--	

Note 6. R_{ON} is tested at 1A in test mode to bypass ideal diode regulation.

14 Typical Application Circuit



15 Timing Diagram

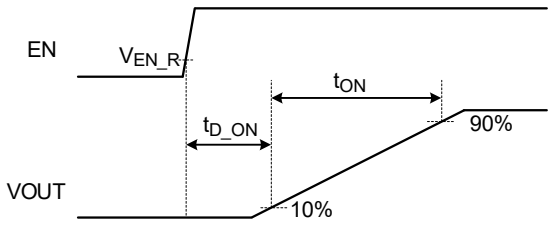


Figure 1. Turn-On Delay Time and Turn-On Rise Time

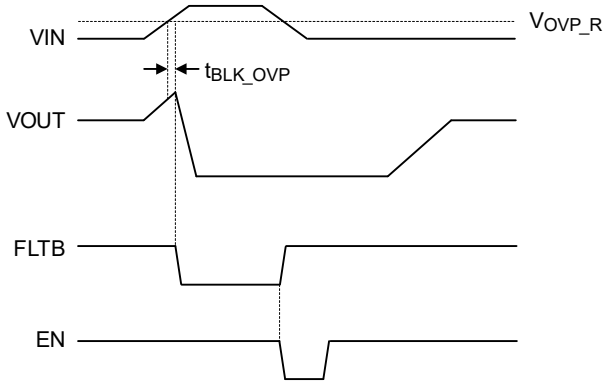
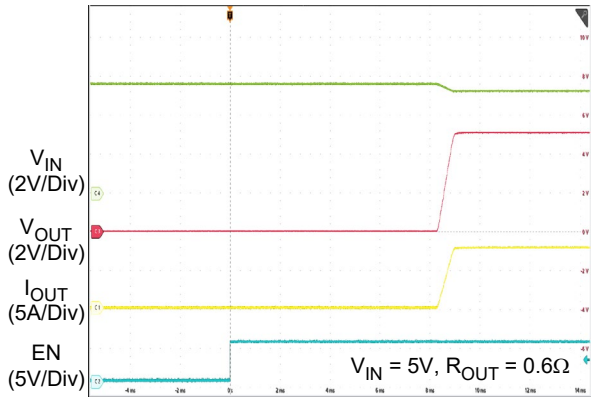


Figure 2. Overvoltage Protection

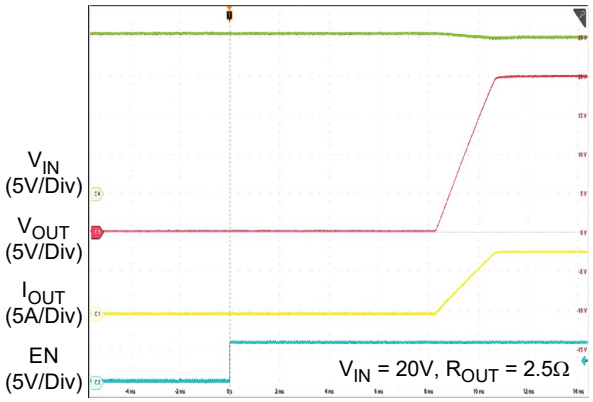
16 Typical Operating Characteristics

Turn-On Delay Time



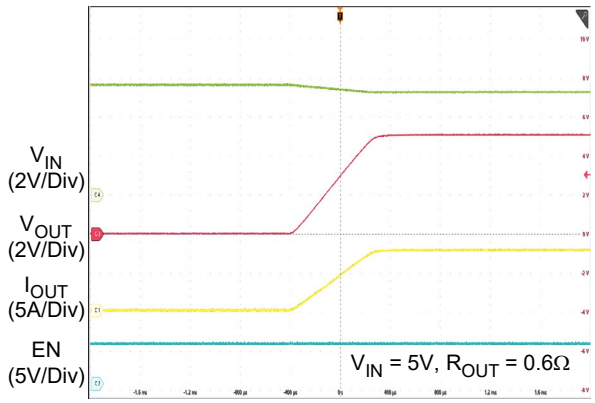
Time (2ms/Div)

Turn-On Delay Time



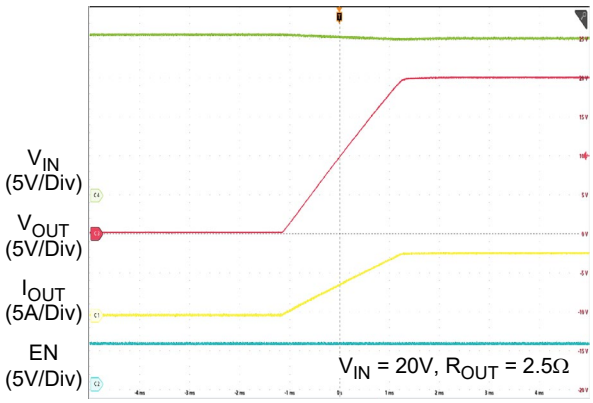
Time (2ms/Div)

Turn-On Rise Time



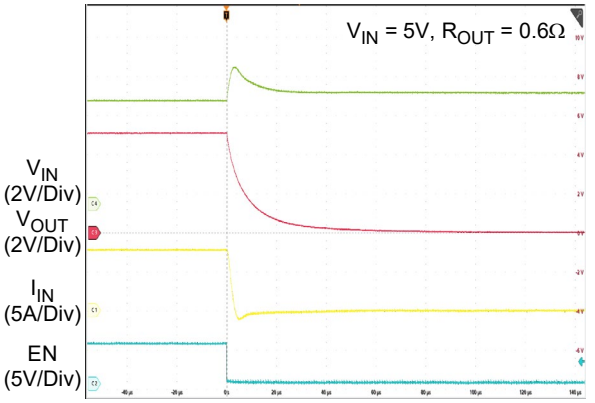
Time (400µs/Div)

Turn-On Rise Time



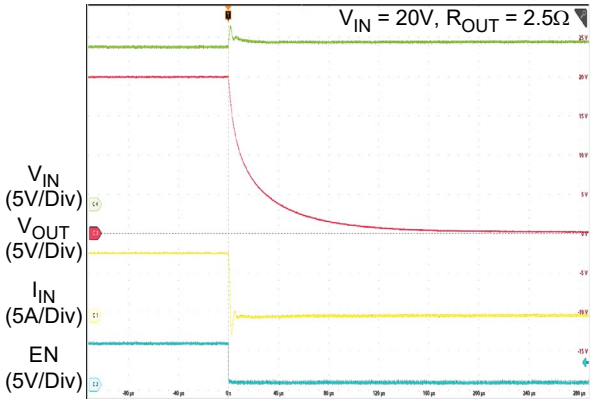
Time (1ms/Div)

Power Off



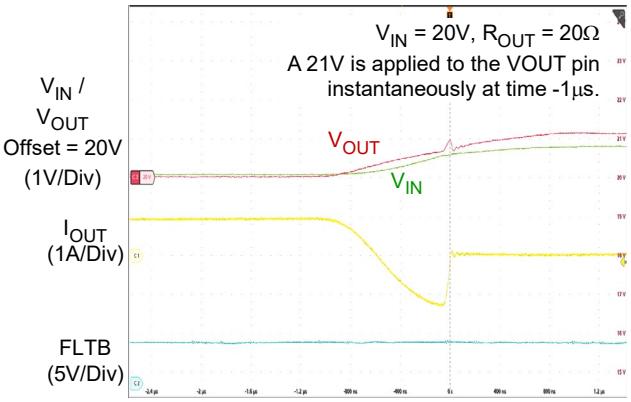
Time (20µs/Div)

Power Off

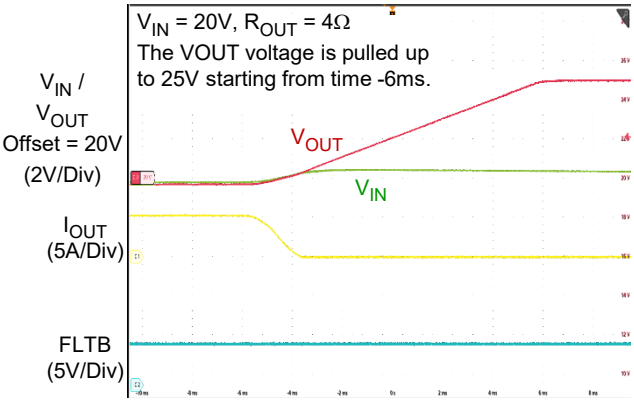


Time (40µs/Div)

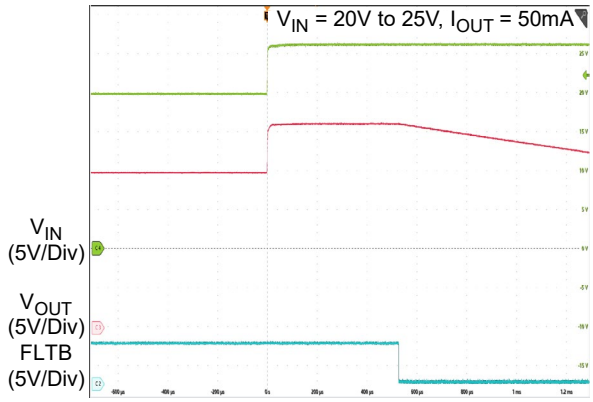
Fast Reverse Current Blocking



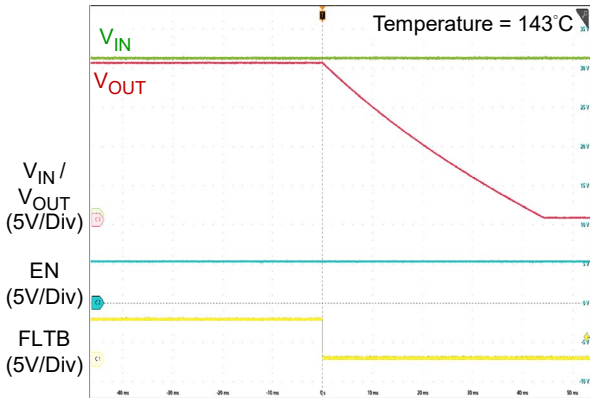
Ideal Diode True Reverse Current Blocking



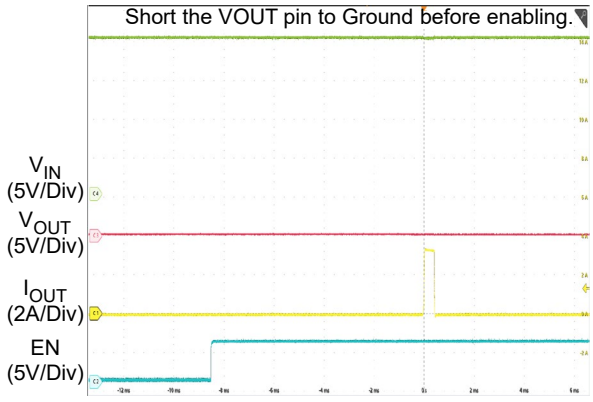
Overvoltage Protection



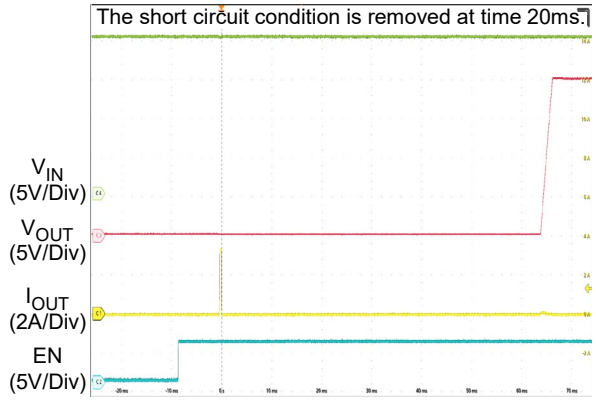
Over Temperature Protection



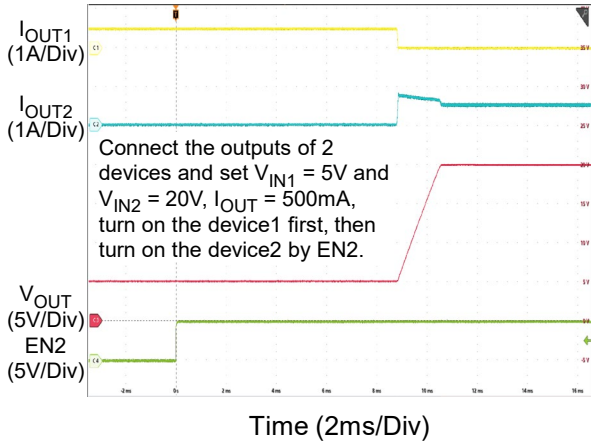
Start-Up Short-Circuit Protection



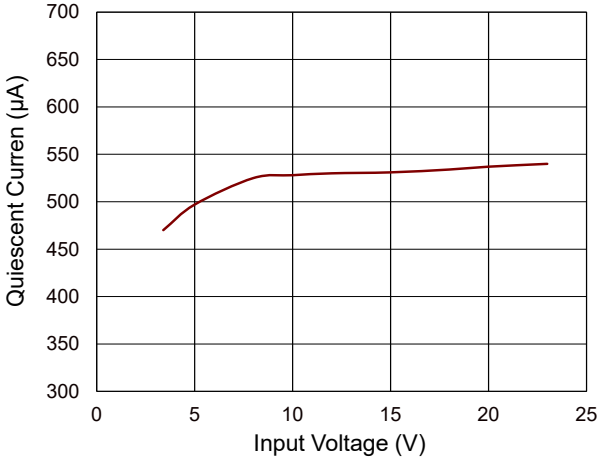
Start-Up Short-Circuit Protection Restart Time



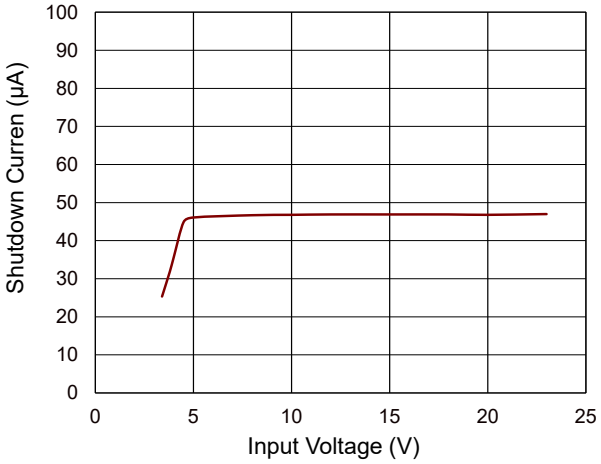
Dual Port with Same Output



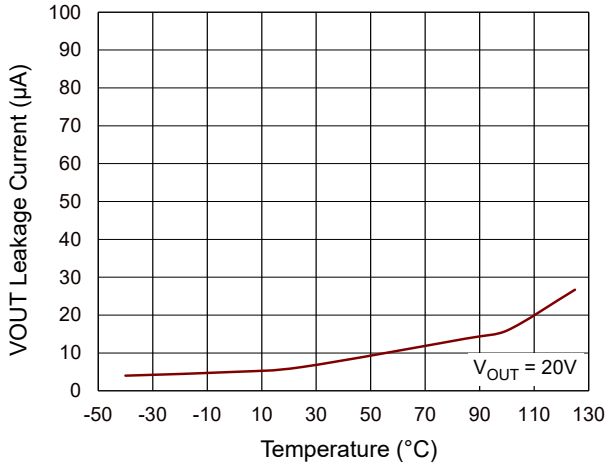
Quiescent Current vs. Input Voltage



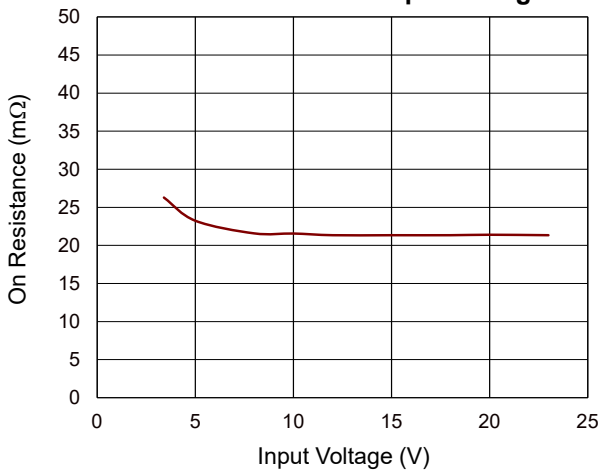
Shutdown Current vs. Input Voltage



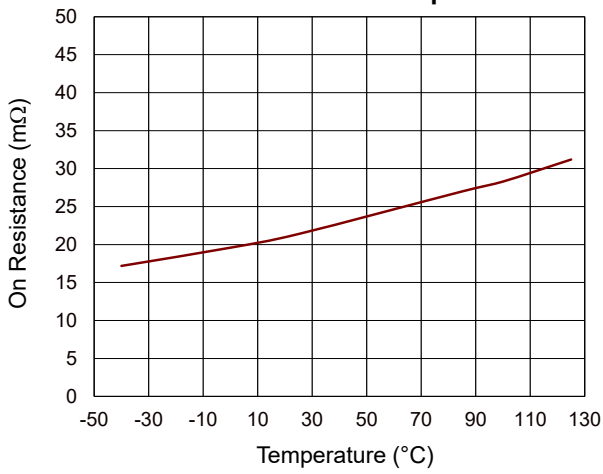
VOUT Leakage Current vs. Temperature



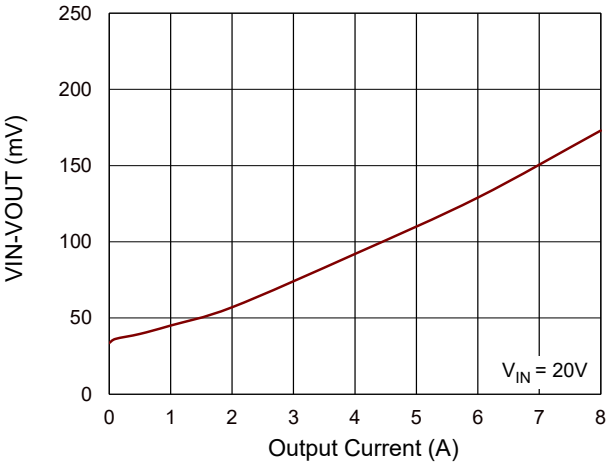
On Resistance vs. Input Voltage



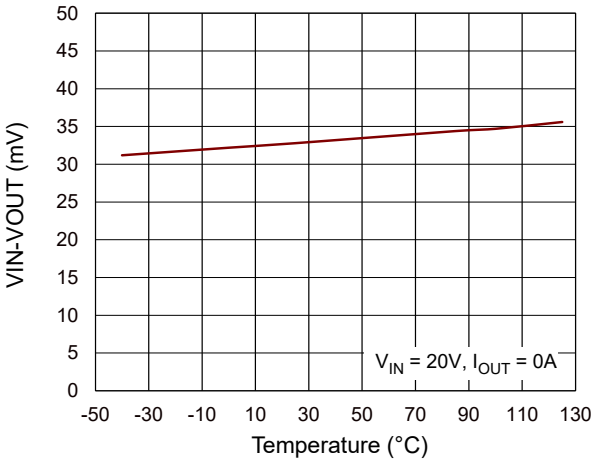
On Resistance vs. Temperature



Ideal Diode Regulation Voltage vs. Output Current



Ideal Diode Regulation Voltage vs. Temperature



17 Operation

The RT1985 is a high-side protection device, which is particularly well suited for USB-C sink applications. Its ideal diode functionality and back-to-back integrated 20mΩ MOSFETs provide reverse current blocking and diode-OR power source sharing while programmable soft-start, overvoltage, over-temperature, and short-circuit protection features protect the system from faults. The 3.4 to 23V operating range aligns with USB-C voltage levels as well as other common power supplies. Unlike single MOSFET devices, the RT1985 completely isolates VIN and VOUT when disabled using the EN input.

17.1 Enable (EN and UVLO)

The active high EN pin provides on/off control for the power path while the input undervoltage-lockout (UVLO) circuit monitors the input voltage (VIN). When VIN > V_{IN_UVLO} (typically 3.175V), driving EN above V_{EN_R} (1.4V max) turns on the power path. The timing diagram is shown in Figure 1. Assuming no other faults – such as OVP or OTP – VOUT will start to ramp after t_{D_ON} (typically 8ms). VOUT ramps up to VIN with a 10% to 90% rise time of approximately t_{ON}, as set by C_{SS}. See the Soft-Start Slew Rate Control section for more information.

Driving EN below V_{EN_F} (0.6Vmin) disables the power path and puts the RT1985 in a low quiescent current state, drawing just I_{SHDN} (typically 32μA). A low input voltage (VIN < V_{IN_UVLO} – V_{UVLO_HYS}, typically 2.925V) also disables the power path.

17.2 Power Delivery and Soft-Start

When an input voltage is first applied to the RT1985, the voltage at VOUT ramps up linearly with a slope determined by the SS pin capacitance. During this time, which is typically a few milliseconds, the RT1985 has high internal MOSFET stress with a power dissipation equal to (VIN – VOUT) x IOUT, where IOUT is the sum of the system load current and the current required to charge the output capacitance. The internal power dissipation is calculated as follows:

$$\text{Power} = (\text{VIN} - \text{VOUT}) \times \text{IOUT} = (\text{VIN} - \text{VOUT}) \times \left(\text{ISYS} + \frac{\text{dVOUT}}{\text{dt}} \times C_{OUT} \right)$$

Where ISYS is the system load current and C_{OUT} is the output capacitance. The internal MOSFET ability to survive this high-power scenario depends on the FET safe operating area (SOA) as well as the thermal performance of the package – with a soft-start time of just a few milliseconds, the thermal performance of the PCB does not play a significant role. Refer to the Application Information section for example calculations and SOA curves to help determine an appropriate soft-start time for a given application.

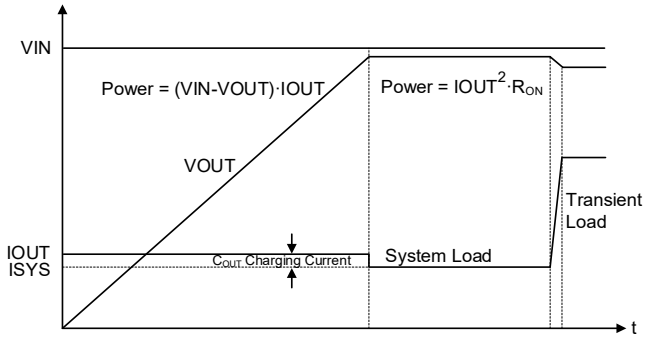


Figure 3. Soft-Start Power Dissipation

When the soft-start ramp is complete, the internal power device switches completely on (provided ISYS x R_{ON} > V_{FWD}) and acts like a resistor with resistance R_{ON}. Because of the low differential voltage between VIN and VOUT, the power dissipation during this mode is considerably lower than during soft-start. Careful PCB layout consideration of thermal performance, combined with the low on-resistance of the internal power device, will ensure maximum system efficiency and minimal heat generation.

17.3 Soft-Start Slew Rate Control

When the RT1985 is first enabled, the soft-start function limits the rate of rise on the internal gate of the power device to control the VOUT ramp and limit inrush current. An external capacitor, C_{SS}, on the SS pin programs the 10% to 90% ramp time, t_{ON}, as follows:

$$t_{ON} = \frac{VIN}{24} x \left(\frac{C_{SS}}{0.0023} - 100 \right)$$

With C_{SS} in nF and t_{ON} in μs. To calculate C_{SS}:

$$C_{SS} = \frac{t_{ON}}{18.1 x VIN} + 0.23$$

17.4 Fault Protection

The RT1985 provides protection against reverse current (TRCB), overvoltage (OVP), overtemperature (OTP), and short-circuit (OCP) faults. When the device is first enabled, if any of the following conditions exist, the internal power MOSFET will not turn on:

1. VIN – VOUT < V_{FRC} (typically -50mV)
2. VIN > V_{OVP_R} (typically 24V)
3. T_{DIE} > T_{OTP} (typically 140°C)

Note that a TRCB condition prevents the power device from turning on but does not result in a fault indication. The RT1985 continuously monitors these conditions to determine when to allow the power path to be enabled. See Table 1 for more information.

Table 1. Fault Response to Protection Features

Protection	Fault Response	FLTB Status
Reverse Current (TRCB)	Auto-restart without soft-start at fault removal	High Impedance
Overvoltage Protection (OVP)	Auto-restart with soft-start at fault removal	Low
Over-Temperature Protection (OTP)	Auto-restart with soft-start at fault removal	Low
Start-Up Short-Circuit Protection (SCP)	Auto-restart after t_{SCP_RST} (typically 64 ms)	High Impedance

17.5 Start-Up Short-Circuit Protection (SCP)

During the soft-start ramp (t_{ON}), the RT1985 monitors for short-circuit faults. If the output current, IOUT, exceeds I_{SCP} during the soft-start ramp, the internal MOSFET will turn off. To maximize the power handling capability of the internal MOSFET within SOA, I_{SCP} varies with VIN – VOUT. When the output voltage begins to start up, the initial value of the current limit is 3A. As the output voltage rises above 2V, the current limit starts to increase, with its value inversely proportional to VIN – VOUT, as shown in Figure 4. A fixed timer is set to disable the power path if the inrush current is continuously clamped by the short-circuit current limit for 380μs. The timer resets if the

inrush current drops below the current limit. In the case of an output short-circuit, the RT1985 will disable the power path by turning off the internal MOSFET when the 380μs timer elapses. After t_{SCP_RST} (typically 64ms), the auto-retry mode will enable the power path and try to start up again. Both the SCP current limit and shutdown functions are disabled after t_{ON} (when the soft-start completes and the internal MOSFET is fully enhanced). Large output capacitors may require a longer soft-start time.

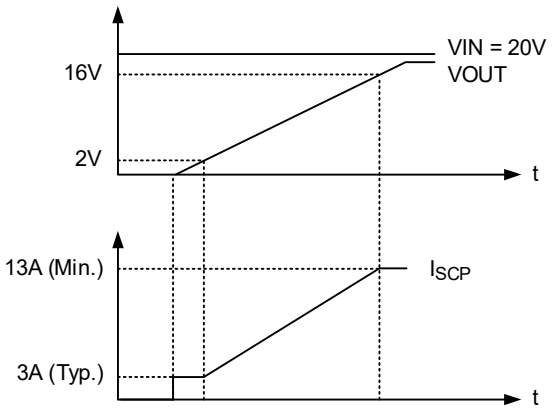


Figure 4. Short-Circuit Protection

17.6 Ideal Diode True Reverse Current Blocking (TRCB)

When the power path is enabled, the ideal diode control circuitry attempts to regulate $V_{IN} - V_{OUT} = V_{FWD}$ (typically 35 mV). Provided that $I_{OUT} \times R_{ON} < V_{FWD}$, the drive circuitry adjusts the internal gate drive to maintain this differential voltage. If the load current increases such that $I_{OUT} \times R_{ON} > V_{FWD}$, then the internal MOSFET is fully enhanced, and the V_{IN} to V_{OUT} voltage is determined by the load current and R_{ON}. If V_{IN} decreases (or V_{OUT} increases) such that $V_{IN} - V_{OUT}$ falls to less than V_{FWD}, the ideal diode gate drive will force the internal MOSFET off. The ideal diode control circuitry is designed to accommodate relatively slow changes in load conditions. In the case of a fast transient, the RT1985 includes a fast reverse current comparator that trips within t_{FRC} (typically about 0.5μs) if $V_{IN} - V_{OUT}$ falls below V_{FRC} (typically – 50mV).

17.7 Overvoltage Protection (OVP)

The OVP circuit monitors the input voltage (V_{IN}) for an overvoltage event to protect downstream loads. When the RT1985 detects an overvoltage event, the resulting behavior depends on the current state of the power path. If the power path is on, the internal power device will be switched off after the OVP blanking time (t_{BLK_OVP} – typically 512μs). If the power path is off, OVP will prevent the internal power device from being turned on. In both cases, the FLTB pin is pulled low, indicating a fault condition. The RT1985 can be re-enabled by toggling the EN pin or cycling the input power supply.

17.8 Over-Temperature Protection (OTP)

If the RT1985 die temperature reaches 140°C, the power path is disabled. Toggle the EN pin or cycle the input power to re-enable the part.

18 Application Information

(Note 7)

18.1 Input Capacitor Selection

A quality input capacitor provides a low impedance at high frequency to reduce input voltage transients, supply fast load transients, and reduce high-frequency noise. A 10μF ceramic input capacitor is recommended and should be placed as close to the VIN and GND pins as possible.

18.2 Output Capacitor Selection

While the RT1985 does not require a specific amount of output capacitance, the user should choose enough low ESR output capacitance to minimize high-frequency output voltage transients due to dynamic loads.

18.3 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VDFN-12TL 3x3 package, the thermal resistance, θ_{JA}, is 53.98°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (53.98°C/W) = 1.85W for a VDFN-12TL 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

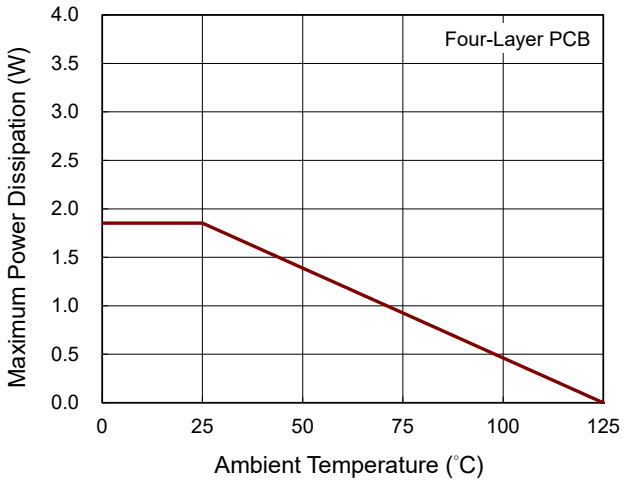
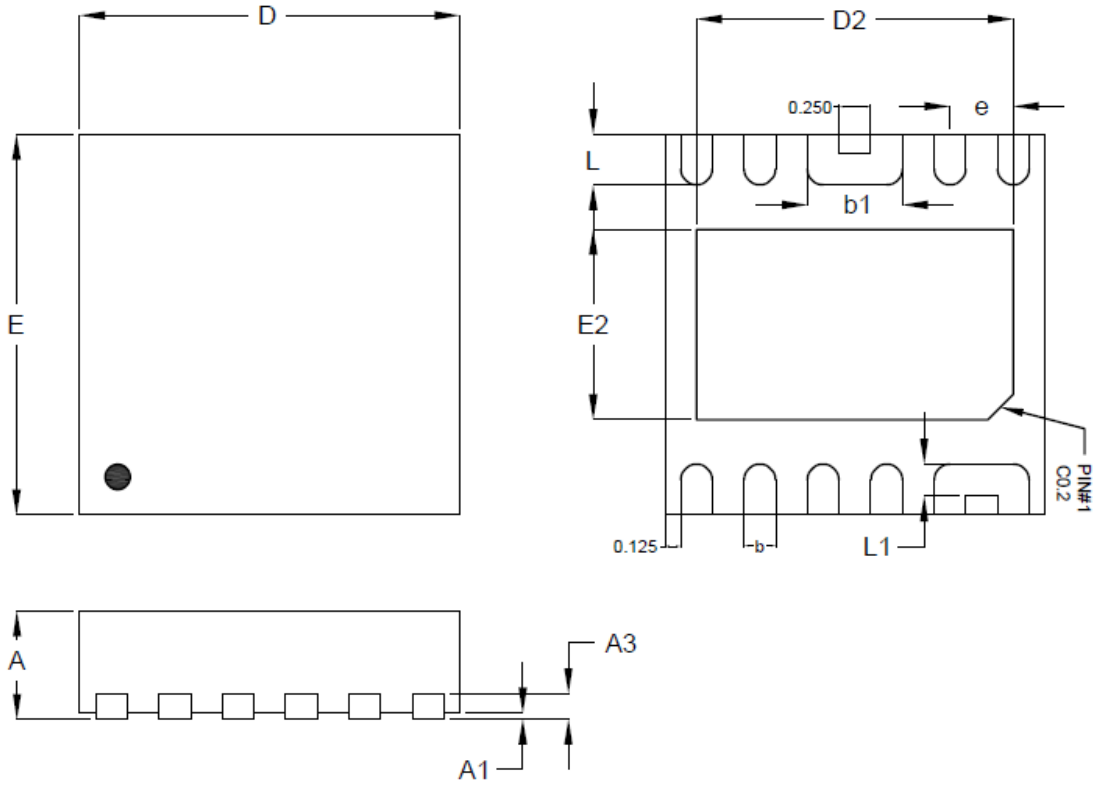


Figure 5. Derating Curve of Maximum Power Dissipation

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

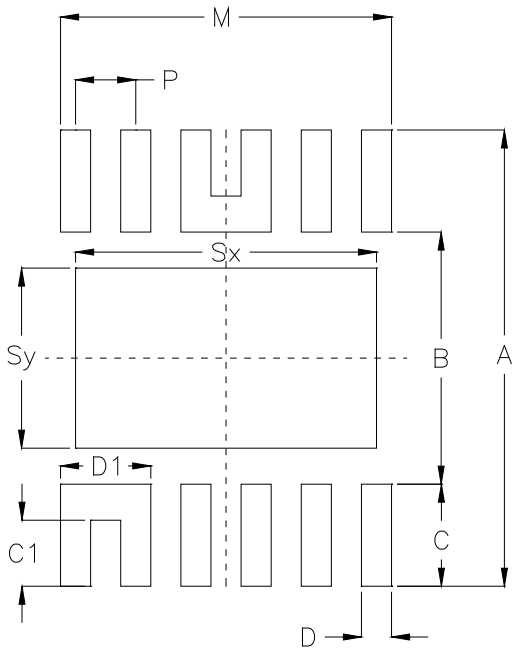
19 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
b1	0.700	0.800	0.028	0.031
D	2.950	3.050	0.116	0.120
D2	2.450	2.550	0.096	0.100
E	2.950	3.050	0.116	0.120
E2	1.450	1.550	0.057	0.061
e	0.500		0.020	
L	0.350	0.450	0.014	0.018
L1	0.200	0.300	0.008	0.012

V-Type 12TL DFN 3x3 Package

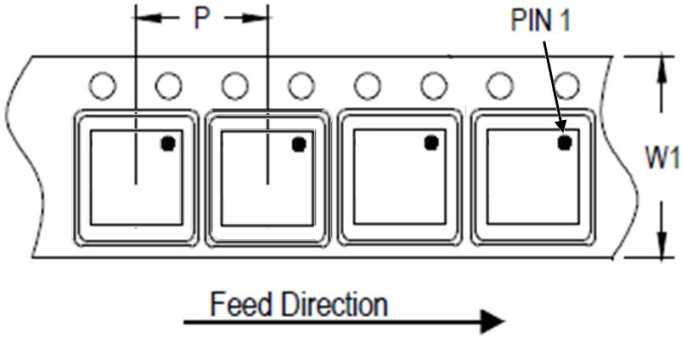
20 Footprint Information

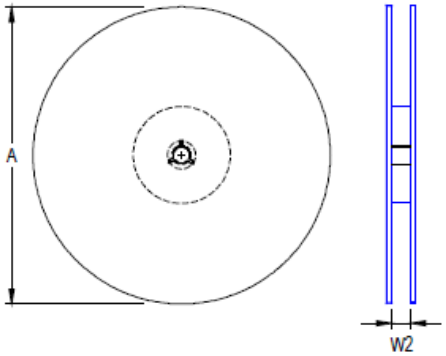


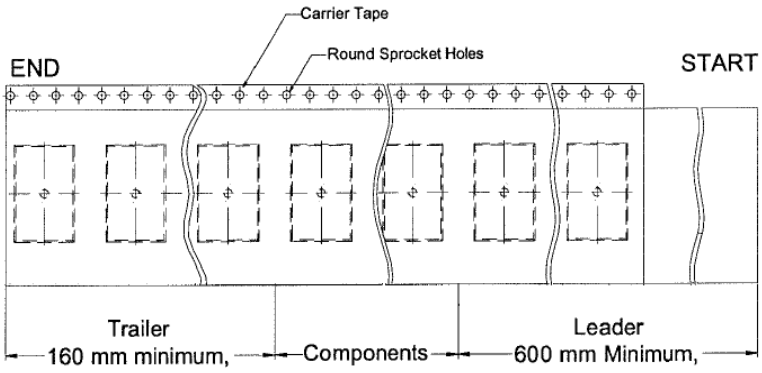
Package	Number of Pins	Footprint Dimension (mm)										Tolerance
		P	A	B	C	C1	D	D1	Sx	Sy	M	
V/W/U/XDFN3x3-12T	12	0.500	3.800	2.100	0.850	0.550	0.250	0.750	2.500	1.500	2.750	±0.05

21 Packing Information

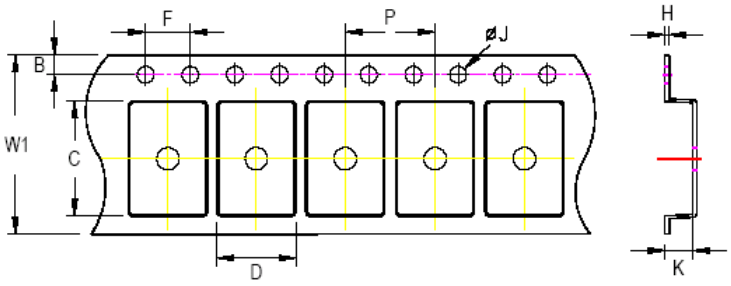
21.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	330	13	2,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
QFN and DFN 3x3	13”	2,500	Box G	1	2,500	Carton A	6	15,000

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

22 Datasheet Revision History

Version	Date	Description	Item
00	2024/9/20	Final	