Type-C CC and SBU Short to VBUS Over-Voltage and IEC ESD Protection Switch

General Description

The RT1738C is an USB Type-C interface over-voltage protection IC.

The RT1738C protects CC/SBU pins which are adjacent to VBUS from high voltage up to 28V since USB Power Delivery (PD) allows VBUS can be sourced from 3.3V to 21V.

The RT1738C is integrated with the protection ESDs which can meet IEC61000-4-2 to withstand contact discharge ±8kV on CON_CC1/CON_CC2 and ±6kV on CON_SBU1/ CON_SBU2. Besides, the ultra-fast OVP response time can protect the application IC on system side from the risks of high voltage damage.

Ordering Information

RT1738C□

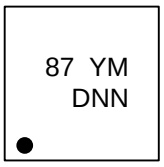
Package Type
WSC : WL-CSP-16B 1.62x1.62 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



87 : Product Code
YMDNN : Date Code

Features

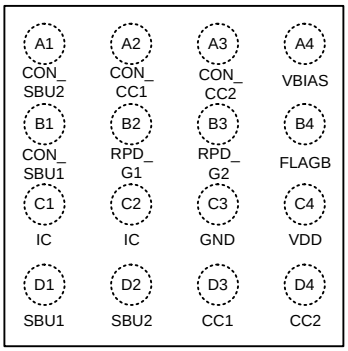
- **4-Channels of short to VBUS Over-Voltage Protection (CON_CC1, CON_CC2, CON_SBU1, CON_SBU2)**
- **IEC61000-4-2 Contact Discharge Protection**
  - **CON_CC1/CON_CC2 : ±8kV**
  - **CON_SBU1/CON_SBU2 : ±6kV**
- **High Absolute Maximum Ratings = 28V of CON_CC1, CON_CC2, CON_SBU1 and CON_SBU2**
- **60ns Ultra-Fast OVP Response Time of SBU**
- **80ns Ultra-Fast OVP Response Time of CC**
- **255mΩ Ultra-Low R_{ON} of CC Switch Typical**
- **3.6Ω Low R_{ON} of SBU Switch Typical**
- **40μA Low Quiescent Current in Standby**
- **High Bandwidth of 1GHz for SBU Switch**
- **Dead Battery Support**
- **WL-CSP-16B 1.62x1.62 (BSC) Package**

Applications

- PC/Notebook
- Smart Phone/Tablet
- TV/Monitor
- USB-C Dongle/Docking/Hubs

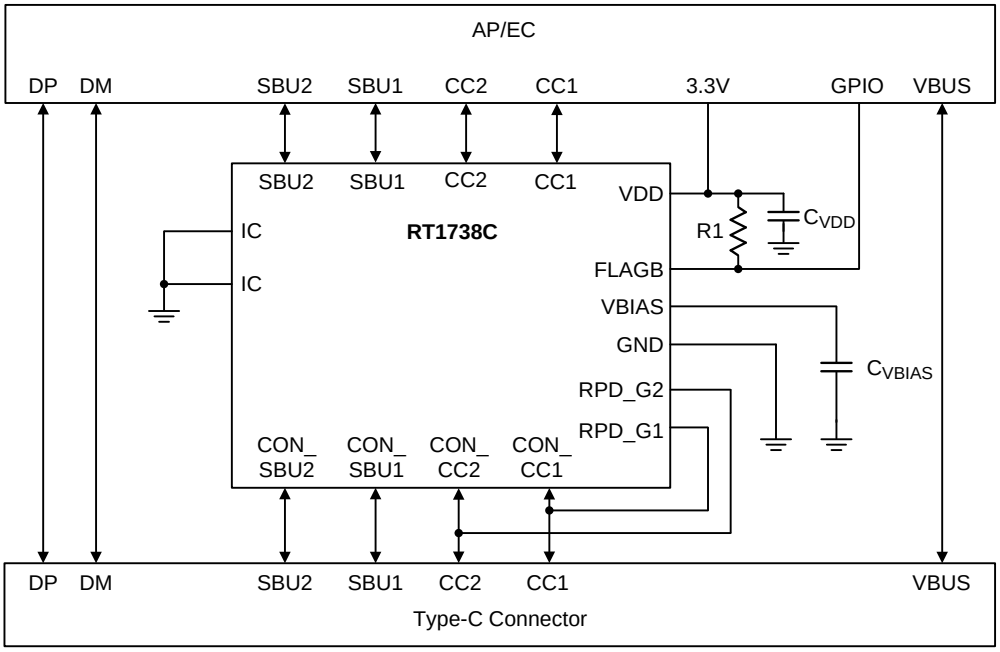
Pin Configuration

(TOP VIEW)



WL-CSP-16B 1.62x1.62 (BSC)

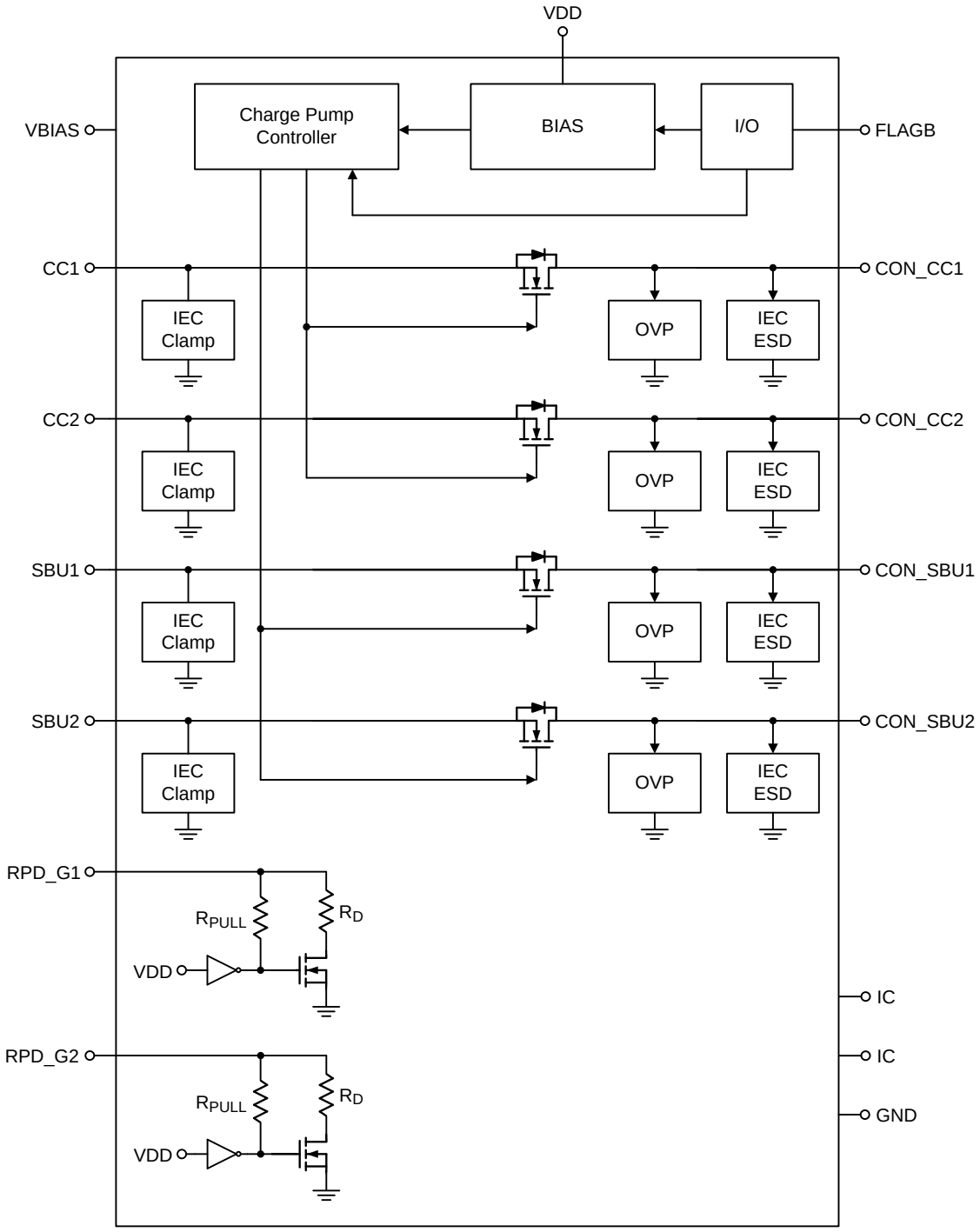
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	CON_SBU2	Type-C connector side SBU2 switch. Connect SBU2 pin of the USB Type-C connector.
A2	CON_CC1	Type-C connector side CC1 switch. Connect CC1 pin of the USB Type-C connector.
A3	CON_CC2	Type-C connector side CC2 switch. Connect CC2 pin of the USB Type-C connector.
A4	VBIAS	VBIAS pin connect capacitor for ESD protection. Put a 0.1μF capacitor on this pin to ground.
B1	CON_SBU1	Type-C connector side SBU1 switch. Connect SBU1 pin of the USB Type-C connector.
B2	RPD_G1	If dead battery resistors are required, short pin to CON_CC1. If dead battery resistors are not required, short pin to GND.
B3	RPD_G2	If dead battery resistors are required, short pin to CON_CC2. If dead battery resistors are not required, short pin to GND.
B4	FLAGB	Open-drain output cautioning fault condition.
C1, C2	IC	Internal connection. They must be connected to GND.
C3	GND	Ground.
C4	VDD	2.5V to 5.5V power supply. Bypass VDD to GND with a 1μF capacitor.
D1	SBU1	System side of the SBU1 switch. Connect to SBU pin of the SBU MUX.
D2	SBU2	System side of the SBU2 switch. Connect to SBU pin of the SBU MUX.
D3	CC1	System side of the CC1 switch. Connect to CC pin of the CC/PD controller.
D4	CC2	System side of the CC2 switch. Connect to CC pin of the CC/PD controller.

Functional Block Diagram



Absolute Maximum Ratings (Note1)

- CON_CC1/CON_CC2/CON_SBU1/CON_SBU2 ---------- –0.3V to 28V
- VBIAS/RPD_G1/RPD_G2 ---------- –0.3V to 28V
- CC1/CC2/SBU1/SBU2/VDD/FLAGB ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 1V
- Output Current (CON_CC1/CON_CC2/CC1/CC2) ---------- –1.25A to 1.25A
- Output Current (CON_SBU1/CON_SBU2/SBU1/SBU2) ---------- –100mA to 100mA
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-16B 1.62x1.62 (BSC) ---------- 2.69W
- Package Thermal Resistance (Note 2)

  WL-CSP-16B 1.62x1.62 (BSC), θ_{JA} ---------- 37.1°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- ±2kV

  CDM ---------- ±500V

  CON_CC1/CON_CC2 (IEC 61000-4-2 Contact Discharge) ---------- ±8kV

  CON_CC1/CON_CC2 (IEC 61000-4-2 Air Discharge) ---------- ±15kV

  CON_SBU1/CON_SBU2 (IEC 61000-4-2 Contact Discharge) ---------- ±6kV

  CON_SBU1/CON_SBU2 (IEC 61000-4-2 Air Discharge) ---------- ±15kV

  CON_CC1/CON_CC2 (Connect to RPD_G1/G2) (IEC 61000-4-5 Surge) ---------- ±35V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 2.5V to 5.5V
- CON_CC1/CON_CC2/CC1/CC2/RPD_G1/RPD_G2/FLAGB ---------- 0V to 5.5V
- CON_SBU1/CON_SBU2/SBU1/SBU2 ---------- 0V to 4.25V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
V_{DD} Under-Voltage Lockout	V_{VDD_UVLO}	V_{DD} = 1.5V, and the rises V_{DD} until CC and SBU switches turn on.	2	2.2	2.45	V
V_{DD} Under-Voltage Lockout Hysteresis	$V_{VDD\_UVLO\_HYS}$	V_{DD} = 3V, and the lower V_{DD} until CC and SBU switches turn off measure the difference between rising and falling.	95	165	260	mV
Quiescent Supply Current	Iq	V_{DD} = 3.3V (Typical)	--	40	70	μA
Leakage Current for CC Pins when Device is Powered	I_{CC_LEAK}	V_{DD} = 3.3V, V_{CON_CCx} = 5V; CCx floating	--	--	5	μA
Leakage Current for SBU Pins when Device is Powered	I_{SBU_LEAK}	V_{DD} = 3.3V, V_{CON_SBUx} = 3.6V; SBUx floating	--	--	2	μA
Leakage Current for CON_CC Pins when Device is in OVP	$I_{CON\_CC\_LEAK\_OVP}$	V_{DD} = 3.3V, V_{CON_CCx} = 24V; V_{CCx} = 0V, measure the current of CON_CCx	–1	350	800	μA
Leakage Current for CON_SBU Pins when Device is in OVP	$I_{CON\_SBU\_LEAK\_OVP}$	V_{DD} = 3.3V, V_{CON_SBUx} = 24V; V_{SBUx} = 0V, measure the current of CON_SBUx	–1	350	800	μA
Leakage Current for CC Pins when Device is in OVP	$I_{CC\_LEAK\_OVP}$	V_{DD} = 3.3V, V_{CON_CCx} = 24V; V_{CCx} = 0V, measure the current into CCx	–1	--	30	μA
Leakage Current for SBU Pins when Device is in OVP	$I_{SBU\_LEAK\_OVP}$	V_{DD} = 3.3V, V_{CON_SBUx} = 24V; V_{SBUx} = 0V, measure the current into SBUx	–1	--	1	μA
CC Switch Characteristics						
Switch Turn On Resistance	R_{ON_CC}	V_{DD} = 3.3V, V_{CCx} = 5V	--	255	390	mΩ
Switch Turn On Resistance Flatness	$R_{ON\_CC\_FLAT}$	Sweep CCx voltage between 0V and 3.6V	--	--	5	mΩ
Threshold Voltage of the Pull-Down Switch in Series with Rd during Dead Battery	V_{TH_DB}	External 80μA	0.3	--	1.2	V
		External 180μA	0.5	--	1.2	
		External 330μA	0.9	--	2.13	
OVP Threshold on CC Pins	V_{OVPCC}	V_{DD} = 3.3V, CON_CCx rises from 5.5V until FLAGB goes from H to L	5.7	5.9	6.1	V
Hysteresis on CC OVP	V_{OVPCC_HYS}	V_{DD} = 3.3V, CON_CCx falls from 6.1V until FLAGB goes from L to H	--	75	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On Bandwidth Single Ended (–3dB)	BW_{CC}	Single ended, 50Ω terminal, V_{CCx} = 0.1V to 1.2V	--	400	--	MHz
Clamp Voltage on System Side	V_{CLAMP}	Hot plug voltage CON_CCx from 0V to 24V, 40V/μs; load 30Ω in series to GND on CCx	--	8	--	V
SBU Switch Characteristics						
Switch Turn on Resistance	R_{ON_SBU}	V_{DD} = 3.3V, V_{SBUx} = 3.6V	--	3.6	6.5	Ω
Switch Turn on Resistance Flatness	$R_{ON\_SBU\_FLAT}$	Sweep SBUx voltage between 0V and 3.6V	--	30	150	mΩ
OVP Threshold on SBU Pins	V_{OVPSBU}	V_{DD} = 3.3V, CON_SBUx rises from 4.5V until FLAGB goes from H to L	4.35	4.5	4.7	V
Hysteresis on SBU OVP	V_{OVPSBU_HYS}	V_{DDf} = 3.3V, CON_SBUx falls from 4.8V until FLAGB goes from L to H	--	60	--	mV
On Bandwidth Single Ended (–3dB)	BW_{SBU}	Single ended, 50Ω terminal, V_{SBUx} = 0.1V to 1.2V	--	1	--	GHz
Crosstalk	Xtalk	Swing 1VPP at 1MHz, measure the SBU1 to CON_SBU2 or SBU2 to CON_SBU1 with 50Ω terminal	--	–75	--	dB
Clamp Voltage on System Side	V_{CLAMP}	Hot plug voltage CON_SBUx from 0V to 24V, 40V/μs; load 100nF cap and 40Ω in series to GND on SBUx	--	8	--	V
Over-Temperature Protection						
Over-Temperature Protection Shutdown Threshold Rising	T_{SD}	V_{DD} = 3.3V	--	150	--	°C
Over-Temperature Protection Shutdown Threshold Hysteresis	T_{SD_HYS}	V_{DD} = 3.3V	--	20	--	°C
FLAGB Characteristics						
Low-Level Output Voltage	V_{OL}	I_{OL} = 5mA	--	--	0.4	V
VIH High-Level Leakage Current	I_{OH}	V_{FLAGB} = 5.5V	--	--	1	μA
Switch Dynamic Characteristics						
Turn-On Time, Time form Rising V_{DD} UVLO to CC Switches Turn on	t_{ON_CC}	V_{DD} power-up from UVLO until CCx switches fully turn on	--	1.5	--	ms
Turn-On Time, Time from Rising V_{DD} UVLO to SBU Switches Turn On	t_{ON_SBU}	V_{DD} power-up from UVLO until SBUx switches fully turn on	--	1.3	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Time from Crossing Rising V_{DD} UVLO until CC and SBU Switches Turn On and the Dead Battery Resistors Turn Off	t_{ON_DB}	V_{DD} power-up from UVLO until the dead battery resistors turn off	--	5	--	ms
Minimum Slew Rate Allowed to Ensure CC and SBU Switches Turn Off during a Power Off	dV_{DD_OFF}/dt	1μF cap to GND on VDD	–0.5	--	--	V/μs
OVP Response Time on the CC Switches. Time from OVP Predicated until Switches Turn Off	$t_{OVP\_RESPONSE\_CC}$	Time from OVP trip voltage predicated to switches to turn OFF	--	80	--	ns
OVP Response Time on the SBU Switches. Time from OVP Predicated until Switches Turn Off	$t_{OVP\_RESPONSE\_SBU}$	Time from OVP trip voltage predicated to switches to turn OFF	--	60	--	ns
OVP Recovery Time on the CCx	$t_{OVP\_RECOVERY\_CC}$	CON_CCx OVP remove until CCx switches fully turn back on	--	0.87	--	ms
OVP Recovery Time on the SBUx	$t_{OVP\_RECOVERY\_SBU}$	CON_SBUx OVP remove until SBUx switches fully turn back on	--	0.75	--	ms
OVP Recovery Time on the CON_CCx's Dead Battery Resistors	$t_{OVP\_RECOVERY\_CC\_DB}$	CON_CCx OVP remove until the dead battery resistors turn back off	--	5	--	ms
Time from OVP Asserted to FLAGB Assertion	$t_{OVP\_FLAGB\_ASSERTION}$	Switches OVP asserted until FLAGB pull down	10	20	40	μs
Time from Switches Turn On after an OVP to FLAGB De-Assertion	$t_{OVP\_FLAGB\_DEASSERTION}$	Switches OVP de-asserted until FLAGB pull high	--	5	--	ms
Time from OTP to FLAGB Assertion	$t_{OTP\_FLAGB\_ASSERTION}$	Switches OTP de-asserted until FLAGB pull down	10	20	40	μs

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

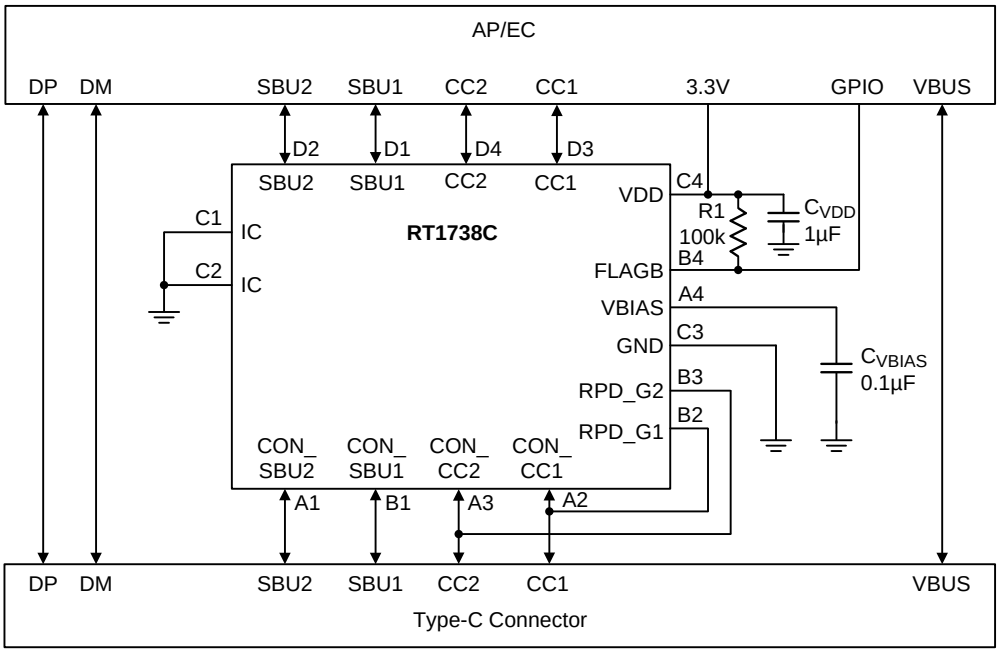
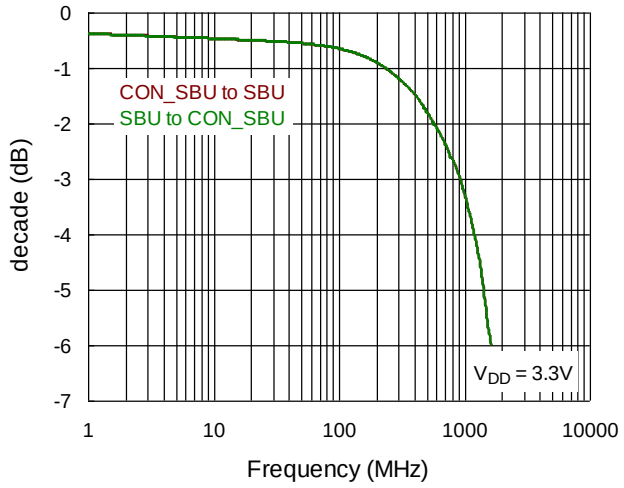


Table 1. Recommended Components Information

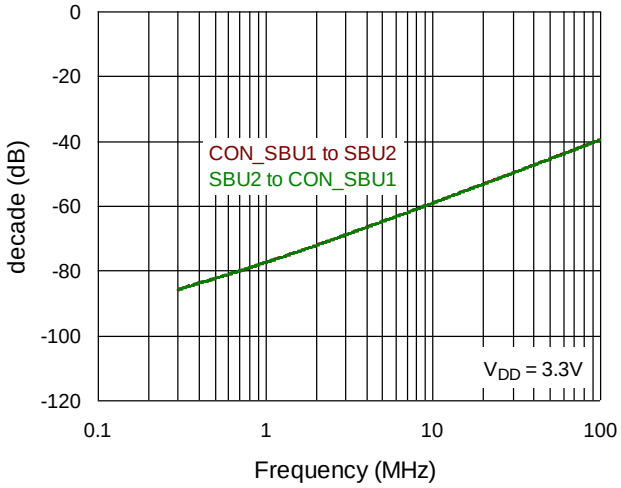
Reference	Q'ty	Part Number	Description	Package	Manufacturer
C_{VDD}	1	GRM155R61E105KA12	1µF/X5R/25V	0402	Murata
C_{VBIAS}	1	0402B104K500CT	0.1µF/50V/X7R	0402	WALSIN
R1	1	RTT021003FTH	100k	0402	RALEC

Typical Operating Characteristics

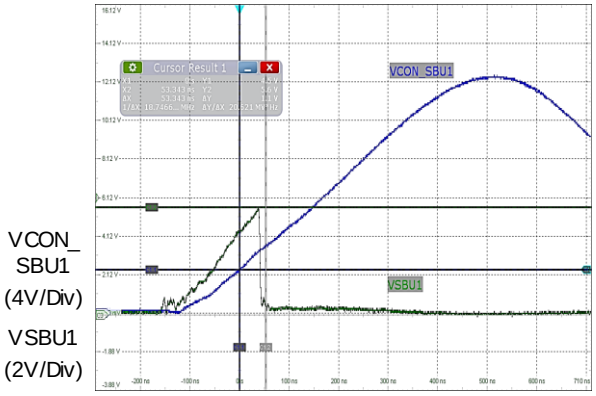
SBU Switch Bandwidth



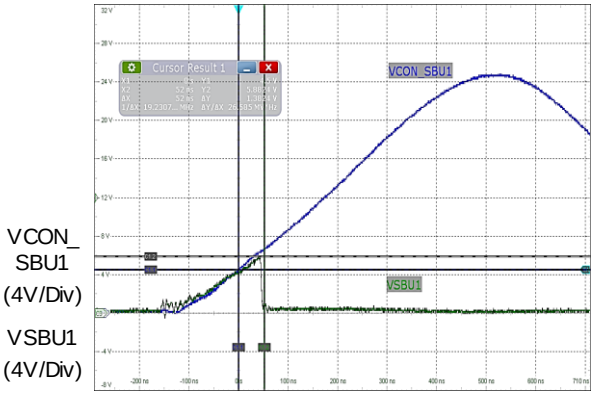
SBU Switch Crossalk



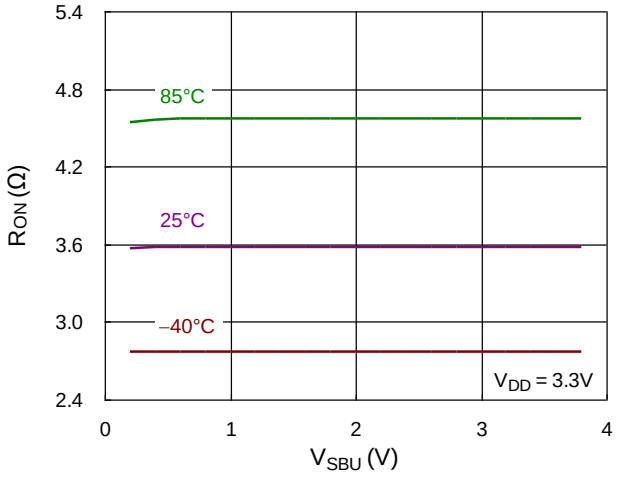
SBU Clamp Voltage on System Side



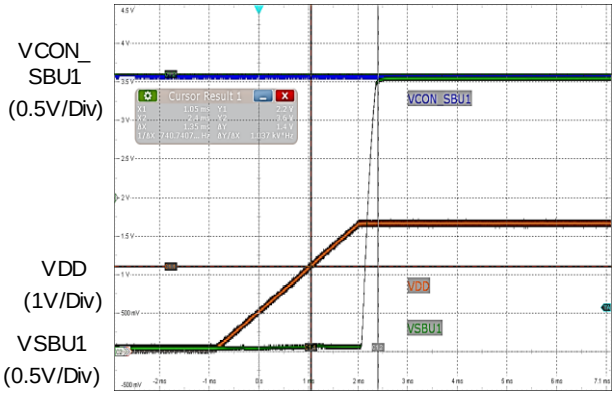
SBU OVP Response Time



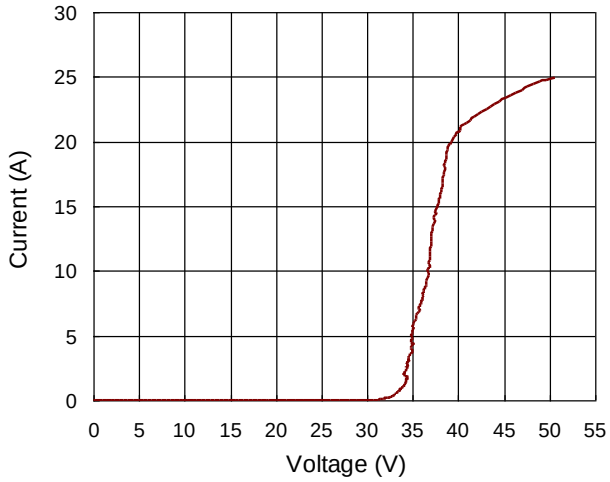
SBU Switch R_{ON} Flatness



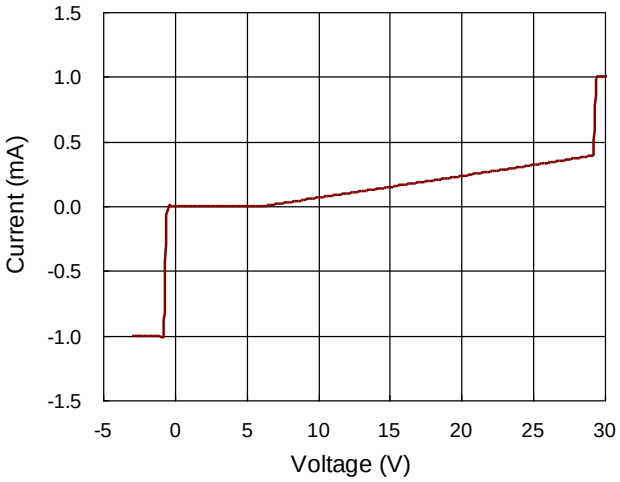
SBU Switch Turn on Timing



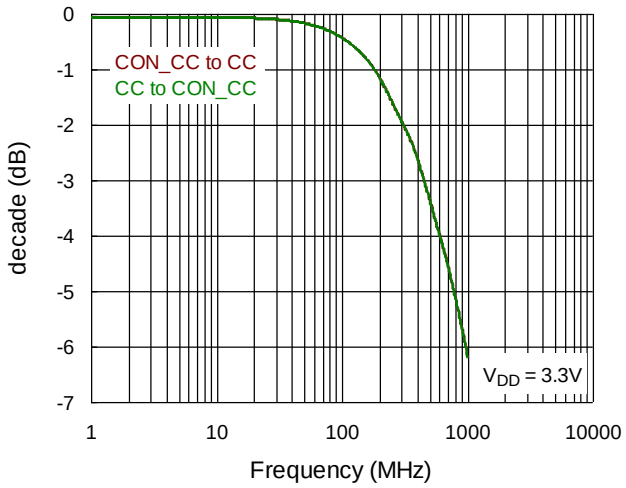
CON_SBU TLP Curve Unpowered



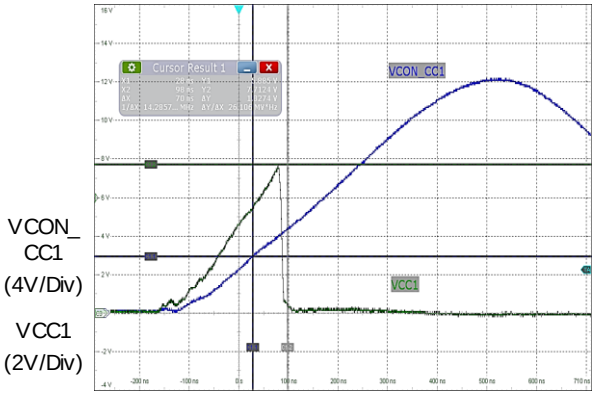
CON_SBU IV Curve



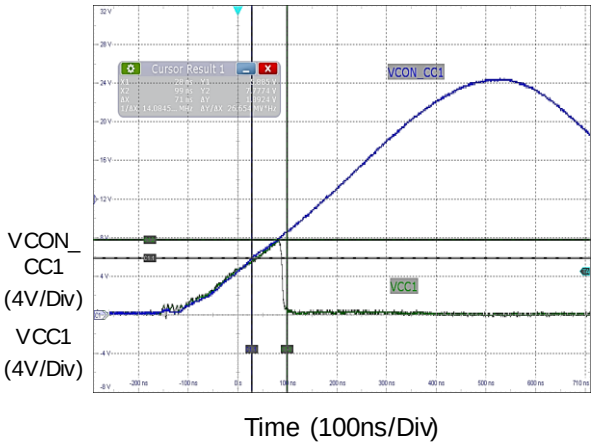
CC Switch Bandwidth



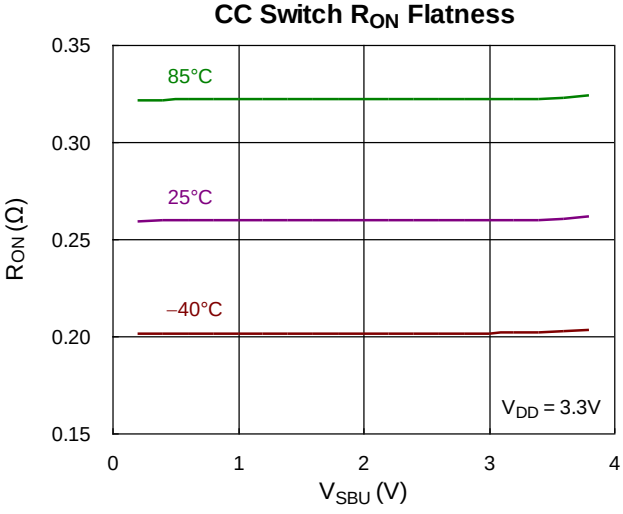
CC Clamp Voltage on System Side



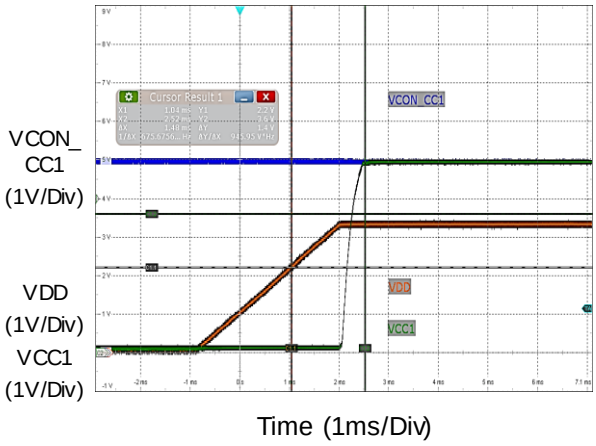
CC OVP Response Time



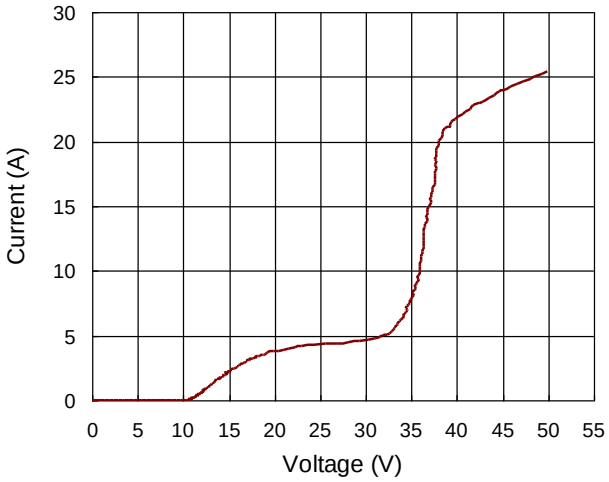
CC Switch R_{ON} Flatness



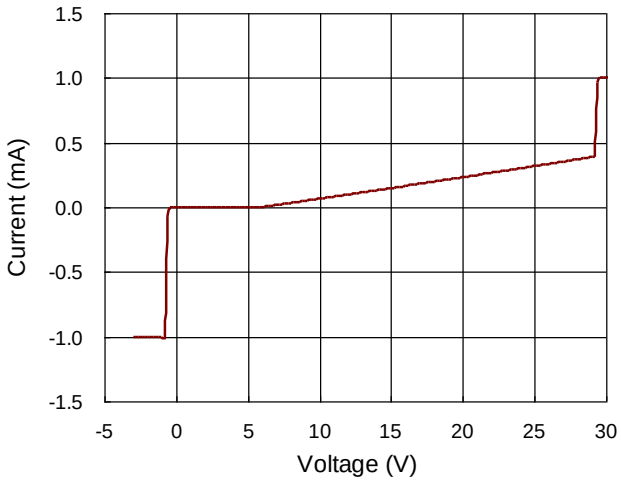
CC Switch Turn on Timing



CON_CC TLP Curve Unpowered



CON_CC IV Curve



Application Information

4-Channels of IEC 61000-4-2 ESD Protection (CON_CC1, CON_CC2, CON_SBU1, CON_SBU2)

The RT1738C provides 4-Channels of IEC 61000-4-2 system level ESD protection for the CC1, CC2, SBU1, SBU2 pins. That USB Type-C interface is needed to achieve ESD protection of IEC system level can avoid the ESD events from the connector inducing from end users.

Input Over-Voltage Protection

There are 4-channels of Short to VBUS over-voltage protection for the CC1, CC2, SBU1 and SBU2 pins respectively in the USB Type-C receptacle via internal OVP circuit in the RT1738C. When the input voltage exceeds the OVP level, the RT1738C will ultra-fast turn off internal switches around 60/80ns to prevent the high input voltage from damaging the end system. When the CC/SBU input voltage returns to normal operation voltage range with hysteresis 75/60mV, the channels will be turned on again normally.

There are individual OVP circuits in CC1/2 and SBU1/2 by themselves to control their own switches. If any one of channel voltage exceed OVP threshold, the channel switch is turned off, and the other switches are all turned off.

Over-Temperature Protection (OTP)

The RT1738C monitors its internal temperature to prevent thermal failures. The chip turns off the switches when the junction temperature reaches 150°C. The IC will resume after the junction temperature is 20°C below the threshold.

Dead Battery

The RT1738C supports dead battery function. Connecting RPD_G1 pin to CON_CC1 pin and RPD_G2 pin to CON_CC2 pin can make RT1738C achieve dead battery function. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default VBUS.

If dead battery function is not required in application, connect the RPD_G1 and RPD_G2 pins to ground.

FLAGB Pin Operation

The FLAGB operation is used for fault indicator. When OVP or OTP event occurs, FLAGB pin will be pulled low until fault event is asserted. Time from OVP or OTP to FLAGB pull down is around 20μs, then time from OVP asserted to FLAGB assertion is around 5ms.

How to Connect Unused Pins

If the RPD_Gx pins and the IC pin C1, C2 are unused in a design, they must be connected to GND.

Device Functional Modes

The RT1738C all functional modes.

MODE		VDD	RPD_Gx	TJ	FLAGB	CC Switches	SBU Switches
Normal Operating Conditions	Powered Off No Dead Battery Support	< UVLO	Grounded		High-Z	OFF	OFF
	Powered Off Dead Battery Support	< UVLO	Shorted to CON_CCx		High-Z	OFF	OFF
	Powered On	> UVLO	Forced OFF	< OT	High-Z	ON	ON
Fault Conditions	Thermal shutdown	> UVLO	Forced ON	> OT	Low	OFF	OFF
	CC Over-Voltage Condition	> UVLO	Forced ON	< OT	Low	OFF	OFF
	SBU Over-Voltage Condition	> UVLO	Forced ON	< OT	Low	OFF	OFF

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-16B 1.62x1.62 (BSC) package, the thermal resistance, θ_{JA}, is 37.1°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (37.1°C/W) = 2.69W for a WL-CSP-16B 1.62x1.62 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

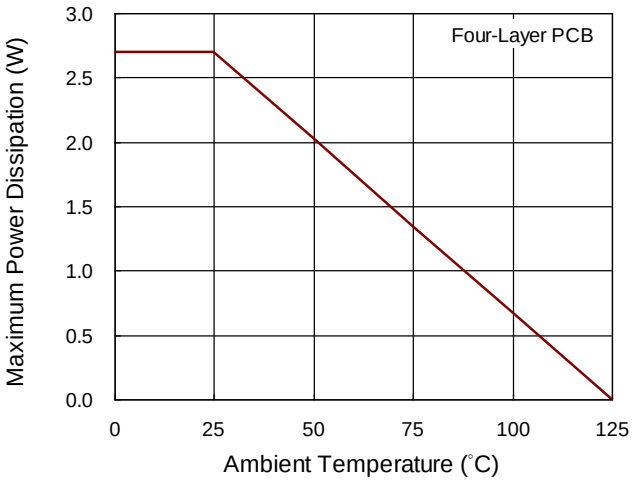


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

Appropriate routing and placement is significant to maintain the signal integrity the SBU, CC signals. The following guidelines apply to the RT1738C : Place the bypass capacitors close to the VDD pin, and ESD protection capacitor close to the VBIAS pin. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during such as short to VBUS and ESD event. The SBU trace need to be routed straight and sharp bends must be minimized.

Standard ESD suggestion apply to the CON_CC1, CON _CC2, CON _SBU1 and CON _SBU2 pins as well :

The optimum placement for the device is as close to the connector as possible. The PCB designer must be keeping out unprotected traces away from the protected traces which are between the RT1738C and the connector.

Route the protected path as straight as possible. Reduce any sharp corners on the protected traces between the connector by using rounded corners with the largest radii as possible.

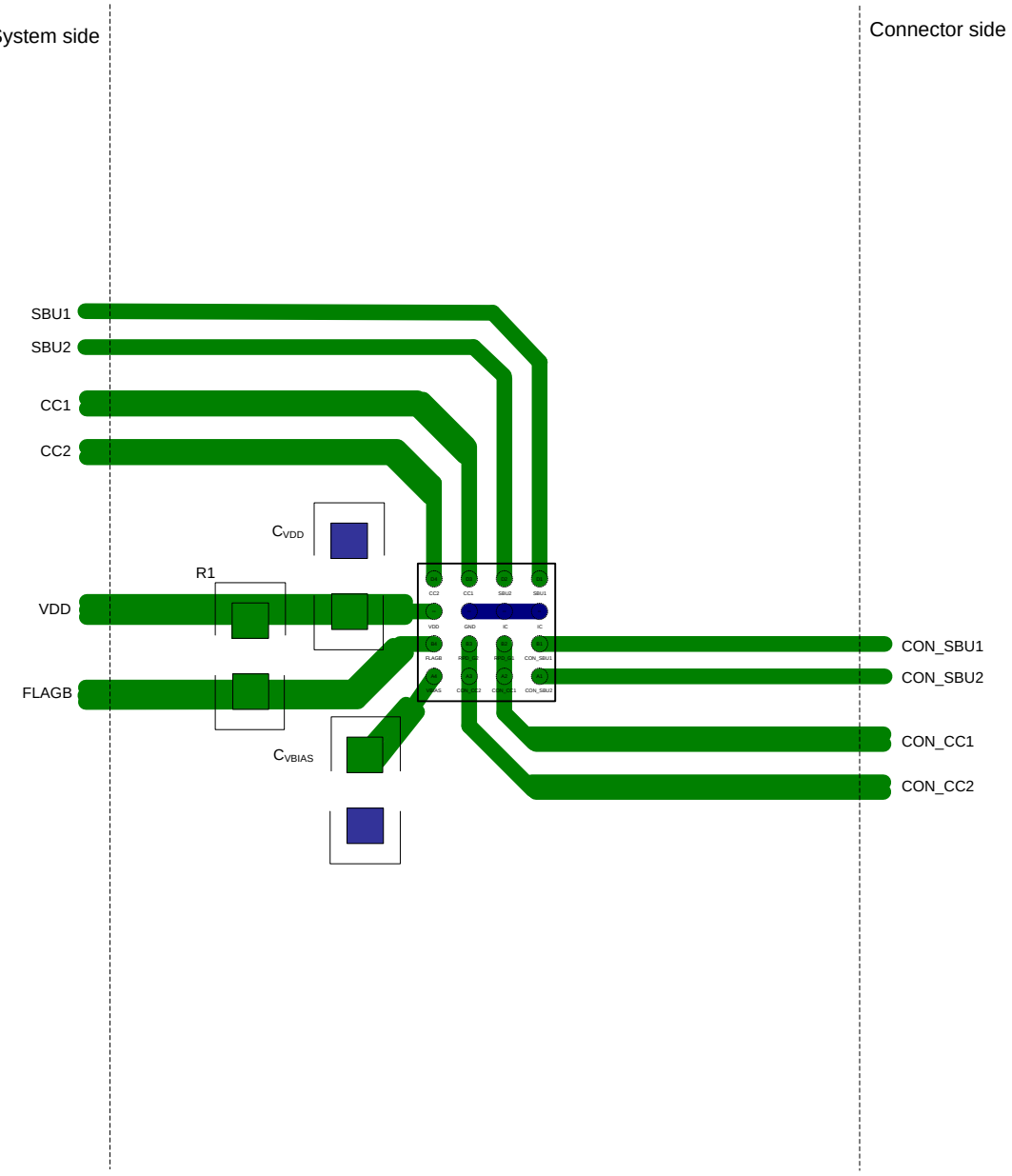
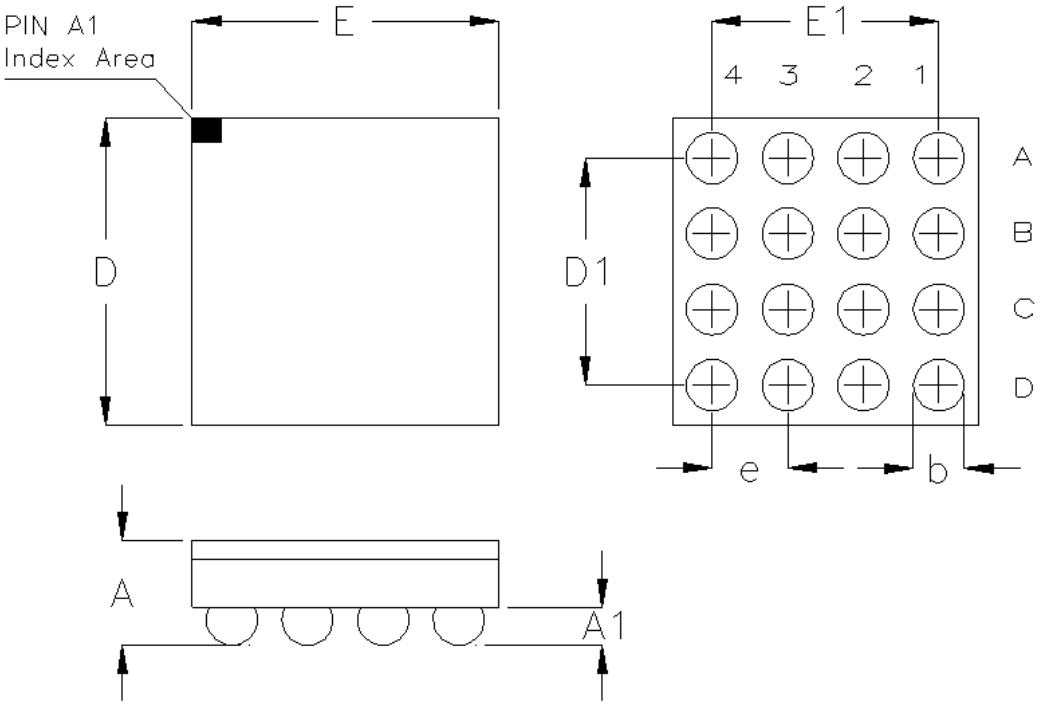


Figure 2. RT1738C Layout Guide

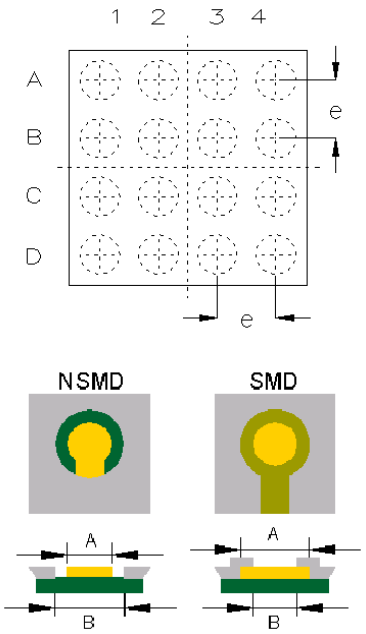
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.580	1.660	0.062	0.065
D1	1.200		0.047	
E	1.580	1.660	0.062	0.065
E1	1.200		0.047	
e	0.400		0.016	

WL-CSP-16B 1.62x1.62 (BSC) Package

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.62x1.62-16(BSC)	16	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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