Type-C CC and SBU Short to VBUS Over-Voltage and IEC ESD Protection Switch

General Description

The RT1738 is an USB Type-C interface over-voltage protection IC.

The RT1738 protects the high voltage shorted to VBUS to adjacent pins of CC/SBU up to 28V due to USB Power Delivery (PD) allowing VBUS from 3.3 to 21V sourcing.

The RT1738 is integrated the protection ESDs of IEC61000-4-2 with contact discharge ±8kV on CON_CC1/CON_CC2, D1/D2 and ±6kV on CON_SBU1/CON_SBU2. The surge immunity level of CON_CC1 /CON_CC2 is up to ±35V. Besides, the ultra-fast OVP response time of 60ns can protect the system side of application IC from damage.

The RT1738 is available in a 3×3mm WQFN package.

Ordering Information

RT1738□□□

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  QW : WQFN-20L 3x3 (W-Type)
  W : RDL Wafer
  WB : RDL Die
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- ▸ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▸ Suitable for use in SnPb or Pb-free soldering processes.

Features

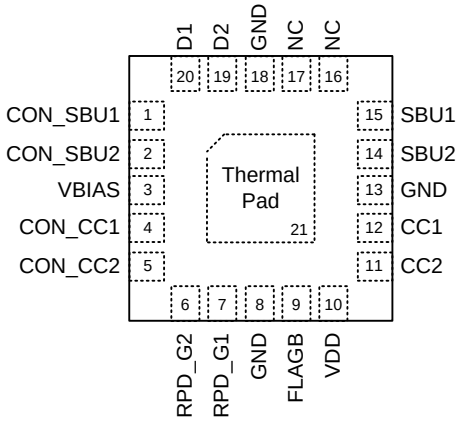
- **4-Channels of short to VBUS Over-Voltage Protection (CON_CC1, CON_CC2, CON_SBU1, CON_SBU2)**
- **IEC61000-4-2 Contact Discharge Protection**
  - ▸ **CON_CC1/CON_CC2 : ±8kV**
  - ▸ **D1/D2 : ±8kV**
  - ▸ **CON_SBU1/CON_SBU2 : ±6kV**
- **High Absolute Maximum Ratings = 28V of CON_CC1, CON_CC2, CON_SBU1 and CON_SBU2**
- **60ns Ultra-Fast OVP Response Time of CC/SBU**
- **255mΩ Ultra-Low R_{ON} of CC Switch Typical**
- **3.6Ω Low R_{ON} of SBU Switch Typical**
- **40μA Low Quiescent Current in Standby**
- **High Bandwidth of 1.1GHz for SBU Switch**
- **Dead Battery Support**
- **20-Pin 3x3mm WQFN Package**

Applications

- PC/Notebook
- Smart Phone/Tablet
- TV/Monitor
- USB-C Dongle/Docking/Hubs

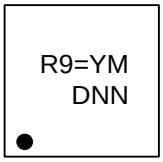
Pin Configuration

(TOP VIEW)



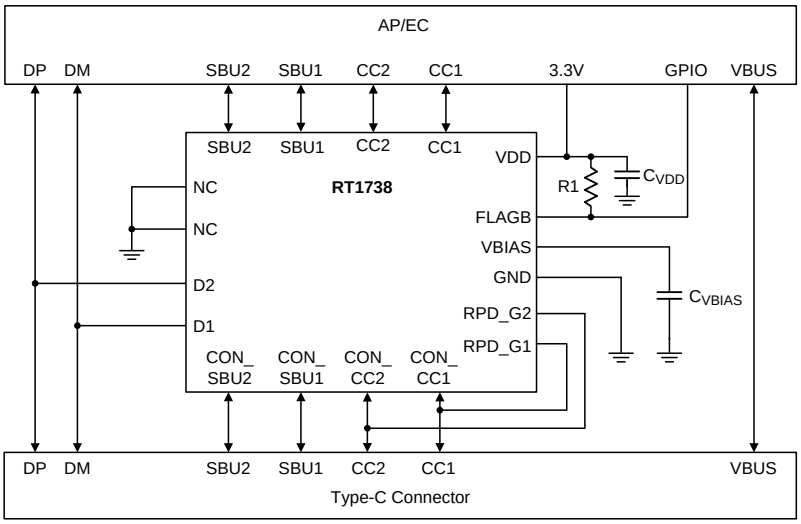
WQFN-20L 3x3

Marking Information



R9= : Product Code
YMDNN : Date Code

Simplified Application Circuit

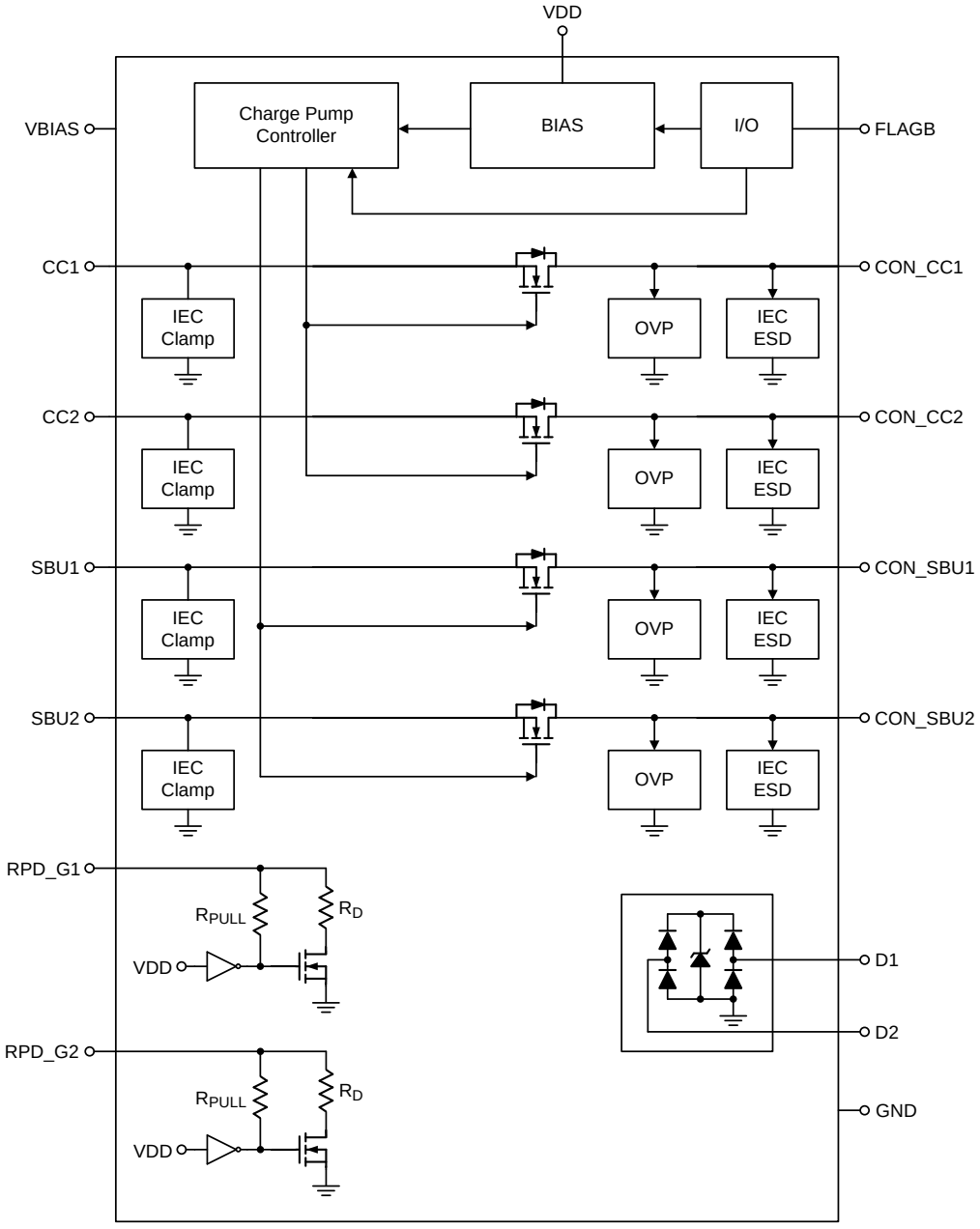


Functional Pin Description

Pin No.	Pin Name	Pin Function
1	CON_SBU1	Type-C connector side SBU1 switch. Connect SBU1 pin of the USB Type-C connector.
2	CON_SBU2	Type-C connector side SBU2 switch. Connect SBU2 pin of the USB Type-C connector.
3	VBIAS	VBIAS pin connect capacitor for ESD protection. Put a 0.1μF capacitor on this pin to ground.
4	CON_CC1	Type-C connector side CC1 switch. Connect CC1 pin of the USB Type-C connector.
5	CON_CC2	Type-C connector side CC2 switch. Connect CC2 pin of the USB Type-C connector.
6	RPD_G2	If dead battery resistors are required, short pin to CON_CC2. If dead battery resistors are not required, short pin to GND.
7	RPD_G1	If dead battery resistors are required, short pin to CON_CC1. If dead battery resistors are not required, short pin to GND.
8, 13, 18	GND	Ground.
9	FLAGB	Open-drain output cautioning fault condition.
10	VDD	2.5V to 5.5V power supply. Bypass VDD to GND with a 1μF capacitor.
11	CC2	System side of the CC2 switch. Connect to CC pin of the CC/PD controller.
12	CC1	System side of the CC1 switch. Connect to CC pin of the CC/PD controller.

Pin No.	Pin Name	Pin Function
14	SBU2	System side of the SBU2 switch. Connect to SBU pin of the SBU MUX.
15	SBU1	System side of the SBU1 switch. Connect to SBU pin of the SBU MUX.
16, 17	NC	No internal connection. Connect to ground.
19	D2	USB2.0 IEC ESD protection. Connect to the USB2.0 pins of the USB Type-C connector.
20	D1	USB2.0 IEC ESD protection. Connect to the USB2.0 pins of the USB Type-C connector.
--	Thermal Pad	Used as a heatsink. Thermal pad connect to PCB ground plane.

Functional Block Diagram



Absolute Maximum Ratings (Note1)

- CON_CC1/CON_CC2/CON_SBU1/CON_SBU2 ---------- –0.3V to 28V
- VBIAS/RPD_G1/RPD_G2 ---------- –0.3V to 28V
- CC1/CC2/SBU1/SBU2/VDD/FLAGB/D1/D2 ---------- –0.3V to 6V
- Output Current (CON_CC1/CON_CC2/CC1/CC2) ---------- –1.25A to 1.25A
- Output Current (CON_SBU1/CON_SBU2/SBU1/SBU2) ---------- –100mA to 100mA
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-20L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)

  WQFN-20L 3x3, θ_{JA} ---------- 30°C/W

  WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- ±2kV

  CDM ---------- ±500V

  CON_CC1/CON_CC2/D1/D2 (IEC 61000-4-2 Contact Discharge) ---------- ±8kV

  CON_CC1/CON_CC2/D1/D2 (IEC 61000-4-2 Air Discharge) ---------- ±15kV

  CON_SBU1/CON_SBU2 (IEC 61000-4-2 Contact Discharge) ---------- ±6kV

  CON_SBU1/CON_SBU2 (IEC 61000-4-2 Air Discharge) ---------- ±15kV

  CON_CC1/CON_CC2 (IEC 61000-4-5 Surge) ---------- ±35V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 2.5V to 5.5V
- CON_CC1/CON_CC2/CC1/CC2/RPD_G1/RPD_G2/D1/D2/FLAGB ---------- 0V to 5.5V
- CON_SBU1/CON_SBU2/SBU1/SBU2 ---------- 0V to 4.25V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
V_{DD} Under-Voltage Lockout	V_{VDD_UVLO}	V_{DD} = 1.5V, and the rises V_{DD} until CC and SBU switches turn on.	2	2.2	2.45	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{DD} Under-Voltage Lockout Hysteresis	$V_{VDD\_UVLO\_HYS}$	V_{DD} = 3V, and the lower V_{DD} until CC and SBU switches turn off measure the difference between rising and falling.	95	165	260	mV
Quiescent Supply Current	Iq	V_{DD} = 3.3V (Typical)	--	40	70	μA
Leakage Current for CC Pins when Device is Powered	I_{CC_LEAK}	V_{DD} = 3.3V, V_{CON_CCx} = 5V; CCx floating	--	--	3	μA
Leakage Current for SBU Pins when Device is Powered	I_{SBU_LEAK}	V_{DD} = 3.3V, V_{CON_SBUx} = 3.6V; SBUx floating	--	--	1	μA
Leakage Current for CON_CC Pins when Device is in OVP	$I_{CON\_CC\_LEAK\_OVP}$	V_{DD} = 3.3V, V_{CON_CCx} = 24V; V_{CCx} = 0V, measure the current of CON_CCx	–1	66	150	μA
Leakage Current for CON_SBU Pins when Device is in OVP	$I_{CON\_SBU\_LEAK\_OVP}$	V_{DD} = 3.3V, V_{CON_SBUx} = 24V; V_{SBUx} = 0V, measure the current of CON_SBUx	–1	66	250	μA
Leakage Current for CC Pins when Device is in OVP	$I_{CC\_LEAK\_OVP}$	V_{DD} = 3.3V, V_{CON_CCx} = 24V; V_{CCx} = 0V, measure the current into CCx	–1	--	30	μA
Leakage Current for SBU Pins when Device is in OVP	$I_{SBU\_LEAK\_OVP}$	V_{DD} = 3.3V, V_{CON_SBUx} = 24V; V_{SBUx} = 0V, measure the current into SBUx	–1	--	1	μA
Leakage Current for Dx Pins	I_{Dx_LEAK}	V_{DD} = 3.3V, V_{Dx} = 3.6V measure the current into Dx	–1	--	1	μA
CC Switch Characteristics						
Switch Turn On Resistance	R_{ON_CC}	V_{DD} = 3.3V, V_{CCx} = 5V	--	255	390	mΩ
Switch Turn On Resistance Flatness	$R_{ON\_CC\_FLAT}$	Sweep CCx voltage between 0V and 3.6V	--	--	5	mΩ
Equivalent on Capacitance	C_{ON_CC}	Capacitance between CCx/CON_CCx and Ground when powered on. V_{DD} = 3.3V, V_{CCx} = 0V to 1V, f = 1MHz	--	11.25	--	pF
Threshold Voltage of the Pull-Down Switch in Series with Rd during Dead Battery	V_{TH_DB}	External 80μA	0.3	--	1.2	V
		External 180μA	0.5	--	1.2	
		External 330μA	0.9	--	2.13	
OVP Threshold on CC Pins	V_{OVPCC}	V_{DD} = 3.3V, CON_CCx rises from 5.5V until FLAGB goes from H to L	5.7	5.9	6.1	V
Hysteresis on CC OVP	V_{OVPCC_HYS}	V_{DD} = 3.3V, CON_CCx falls from 6.1V until FLAGB goes from L to H	--	75	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On Bandwidth Single Ended (–3dB)	BW_{CC}	Single ended, 50Ω terminal, V_{CCx} = 0.1V to 1.2V	--	400	--	MHz
Clamp Voltage on System Side	V_{CLAMP}	Hot plug voltage CON_CCx = 24V, 40V/μs; load 30Ω in series to GND on CCx	--	--	7	V
SBU Switch Characteristics						
Switch Turn on Resistance	R_{ON_SBU}	V_{DD} = 3.3V, V_{SBUx} = 3.6V	--	3.6	6.5	Ω
Switch Turn on Resistance Flatness	$R_{ON\_SBU\_FLAT}$	Sweep SBUx voltage between 0V and 3.6V	--	30	150	mΩ
Equivalent on Capacitance	C_{ON_SBU}	Capacitance between SBUx/CON_SBUx and Ground when powered on. V_{DD} = 3.3V, V_{SBUx} = 0V to 1.2V, f = 1MHz	--	6.4	--	pF
OVP Threshold on SBU Pins	V_{OVPSBU}	V_{DD} = 3.3V, CON_SBUx rises from 4.5V until FLAGB goes from H to L	4.35	4.5	4.7	V
Hysteresis on SBU OVP	V_{OVPSBU_HYS}	V_{DD} = 3.3V, CON_SBUx falls from 4.8V until FLAGB goes from L to H	--	60	--	mV
On Bandwidth Single Ended (–3dB)	BW_{SBU}	Single ended, 50Ω terminal, V_{SBUx} = 0.1V to 1.2V	--	1.1	--	GHz
Crosstalk	Xtalk	Swing 1VPP at 1MHz, measure the SBU1 to CON_SBU2 or SBU2 to CON_SBU1 with 50Ω terminal	--	–80	--	dB
Clamp Voltage on System Side	V_{CLAMP}	Hot plug voltage CON_SBUx = 24V, 40V/μs; load 100nF cap and 40Ω in series to GND on SBUx	--	--	7	V
Over-Temperature Protection						
Over-Temperature Protection Shutdown Threshold Rising	T_{SD}	V_{DD} = 3.3V	--	150	--	°C
Over-Temperature Protection Shutdown Threshold Hysteresis	T_{SD_HYS}	V_{DD} = 3.3V	--	20	--	°C
FLAGB Characteristics						
Low-Level Output Voltage	V_{OL}	I_{OL} = 5mA	--	--	0.4	V
VIH High-Level Leakage Current	I_{OH}	V_{FLAGB} = 5.5V	--	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dx ESD Protection						
Reverse Stand-Off Voltage from Dx to GND	V_{RWM_POS}	Dx to GND. IDx ≤ 1μA	--	--	5.5	V
Reverse Stand-Off Voltage from GND to Dx	V_{RWM_NEG}	GND to Dx	--	--	0	V
Break-Down Voltage from Dx to GND	V_{BR_POS}	Dx to GND. IBR = 1mA	7	--	--	V
Break-Down Voltage from GND to Dx	V_{BR_NEG}	GND to Dx. IBR = 8mA	0.6	--	--	V
Dx to GND or GND to Dx	C_{IO}	f= 1MHz, VIO = 2.5V	--	D1 = 3 D2 = 3	--	pF
Differential Capacitance between Two Dx Pins	ΔC_{IO}	f = 1MHz, VIO = 2.5V	--	0.02	--	pF
Dynamic On-Resistance Dx IEC Clamps	R_{DYN}	Dx to GND or GND to Dx	--	0.45	--	Ω
Switch Dynamic Characteristics						
Turn-On Time, Time form Rising V_{DD} UVLO to CC Switches Turn on	t_{ON_CC}	V_{DD} power-up from UVLO until CCx switches fully turn on	--	1.5	--	ms
Turn-On Time, Time from Rising V_{DD} UVLO to SBU Switches Turn On	t_{ON_SBU}	V_{DD} power-up from UVLO until SBUx switches fully turn on	--	1.3	--	ms
Time from Crossing Rising V_{DD} UVLO until CC and SBU Switches Turn On and the Dead Battery Resistors Turn Off	t_{ON_DB}	V_{DD} power-up from UVLO until the dead battery resistors turn off	--	5	--	ms
Minimum Slew Rate Allowed to Ensure CC and SBU Switches Turn Off during a Power Off	dV_{DD_OFF}/dt		–0.5	--	--	V/μs
OVP Response Time on the CC Switches. Time from OVP Predicated until Switches Turn Off	$t_{OVP\_RESPONSE\_CC}$	Time from OVP trip voltage predicated to switches to turn OFF	--	60	--	ns
OVP Response Time on the SBU Switches. Time from OVP Predicated until Switches Turn Off	$t_{OVP\_RESPONSE\_SBU}$	Time from OVP trip voltage predicated to switches to turn OFF	--	60	--	ns
OVP Recovery Time on the CCx	$t_{OVP\_RECOVERY\_CC}$	CON_CCx OVP remove until CCx switches fully turn back on	--	0.87	--	ms
OVP Recovery Time on the SBUx	$t_{OVP\_RECOVERY\_SBU}$	CON_SBUx OVP remove until SBUx switches fully turn back on	--	0.75	--	ms
OVP Recovery Time on the CON_CCx's Dead Battery Resistors	$t_{OVP\_RECOVERY\_CC\_DB}$	CON_CCx OVP remove until the dead battery resistors turn back off	--	5	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Time from OVP Asserted to FLAGB Assertion	$t_{OVP\_FLAGB\_ASSERTION}$	Switches OVP asserted until FLAGB pull down	10	20	40	μs
Time from Switches Turn On after an OVP to FLAGB De-Assertion	$t_{OVP\_FLAGB\_DEASSERTION}$	Switches OVP de-asserted until FLAGB pull high	--	5	--	ms
Time from OTP to FLABG Assertion	$t_{OTP\_FLAGB\_ASSERTION}$	Switches OTP de-asserted until FLAGB pull down	10	20	40	μs

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

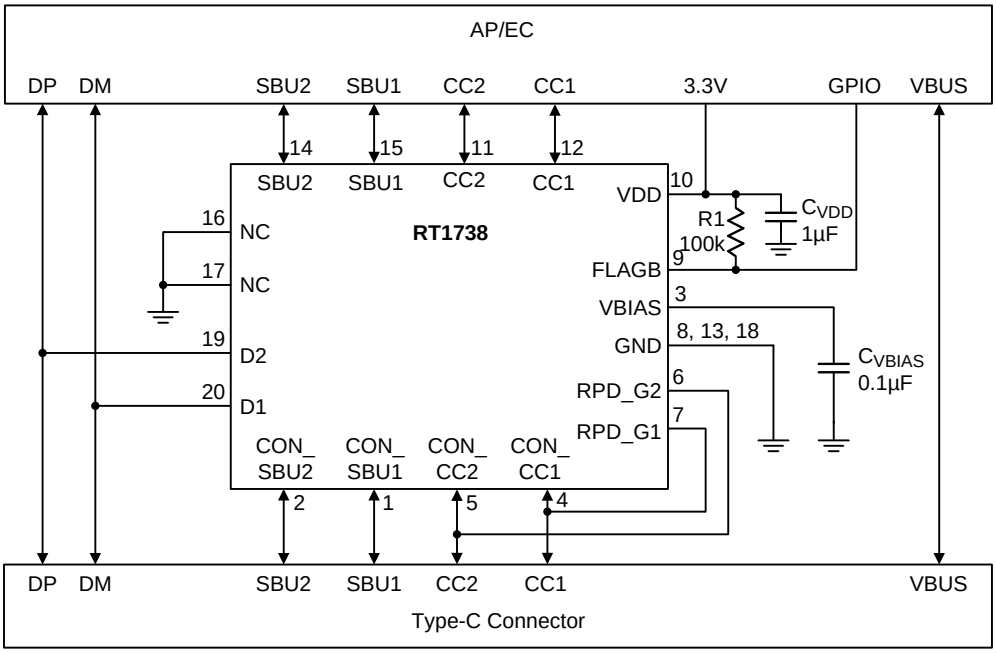
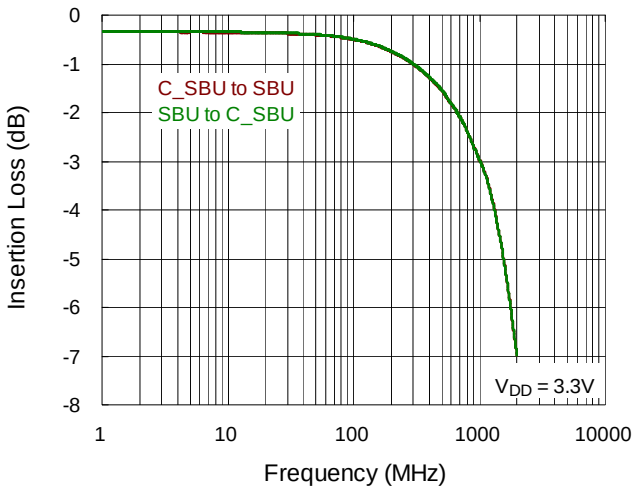


Table 1. Recommended Components Information

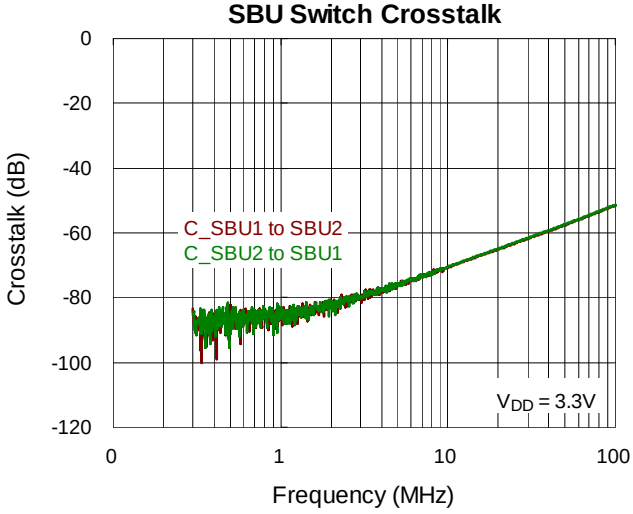
Reference	Q'ty	Part Number	Description	Package	Manufacturer
C_{VDD}	1	TMK107BJ105KA-T	1µF/X5R/25V	0603	TAIYO YUDEN
C_{VBIAS}	1	0402B104K500CT	0.1µF/50V/X7R	0402	WALSIN
R1	1	RTT021003FTH	100k	0402	RALEC

Typical Operating Characteristics

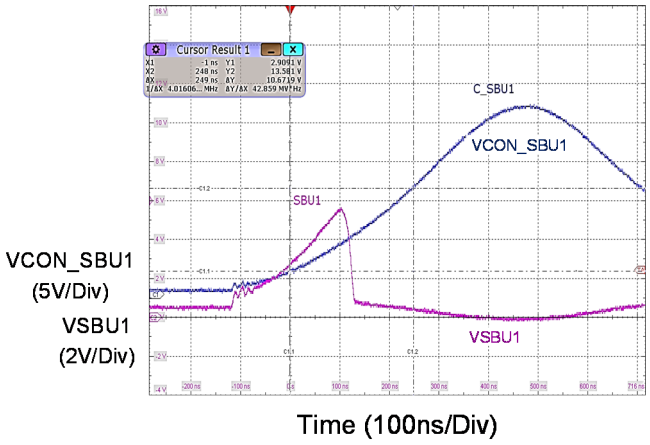
SBU Switch Bandwidth



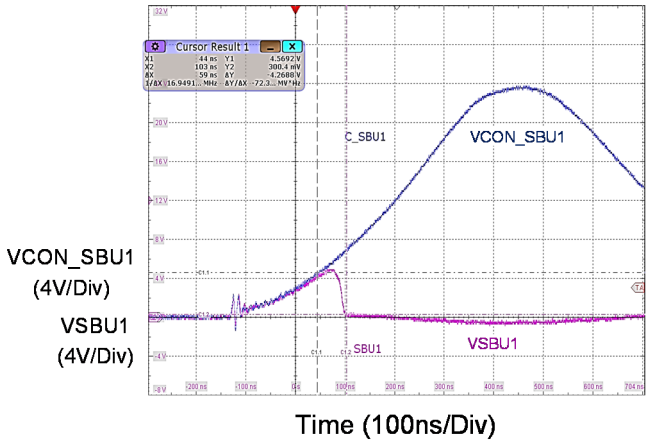
SBU Switch Crosstalk



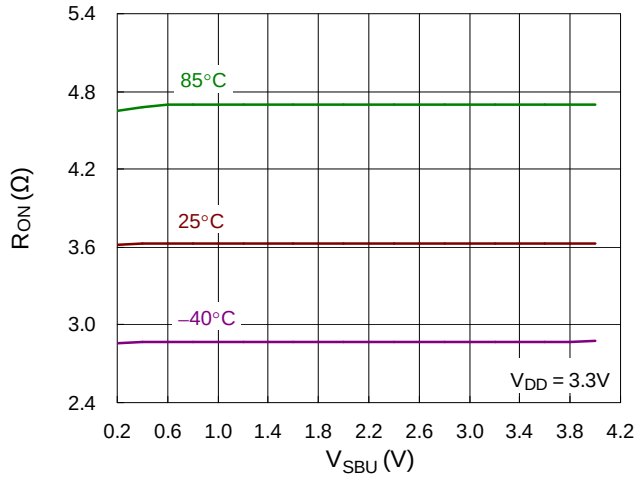
SBU Clamp Voltage on System Side



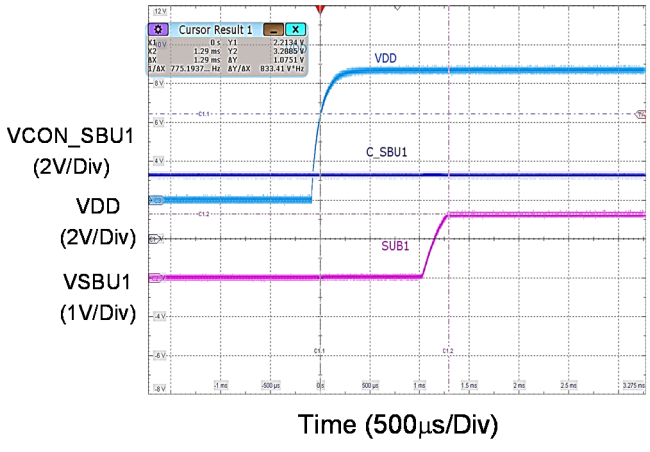
SBU OVP Response Time



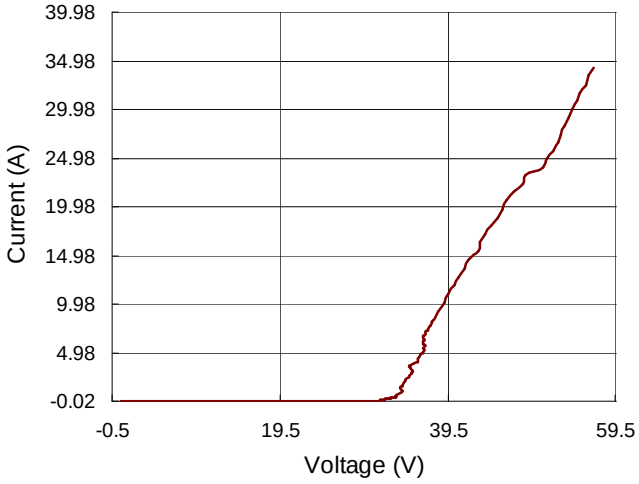
SBU Switch R_{ON} Flatness



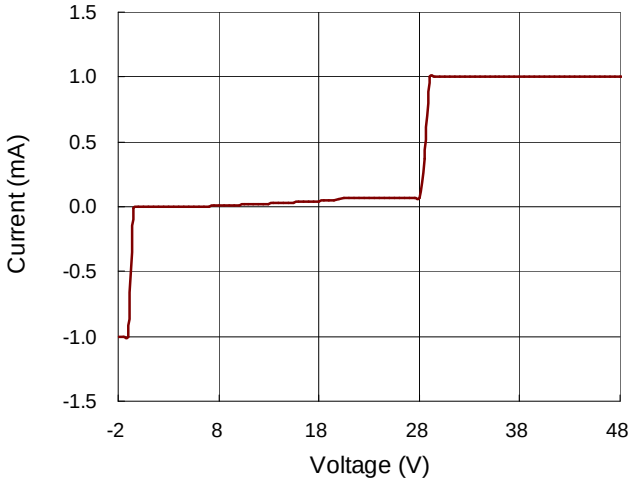
SBU switch Turn on Timing



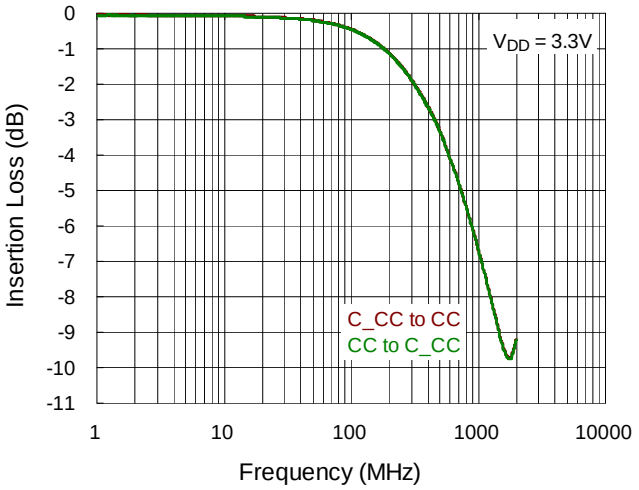
CON_SBU TLP Curve Unpowered



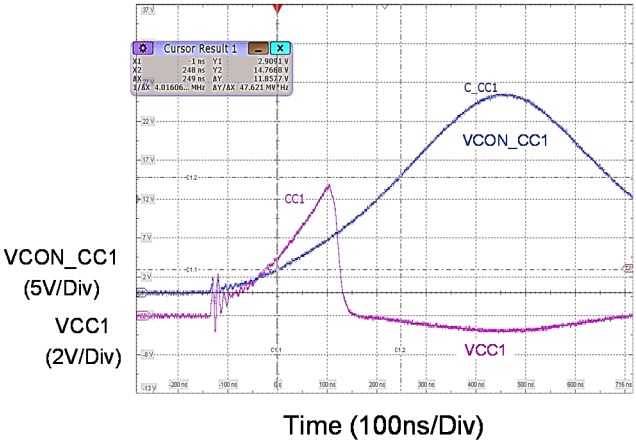
CON_SBU IV Curve



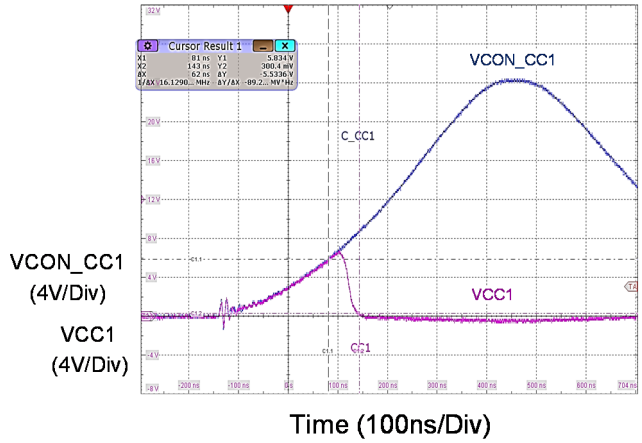
CC Switch Bandwidth



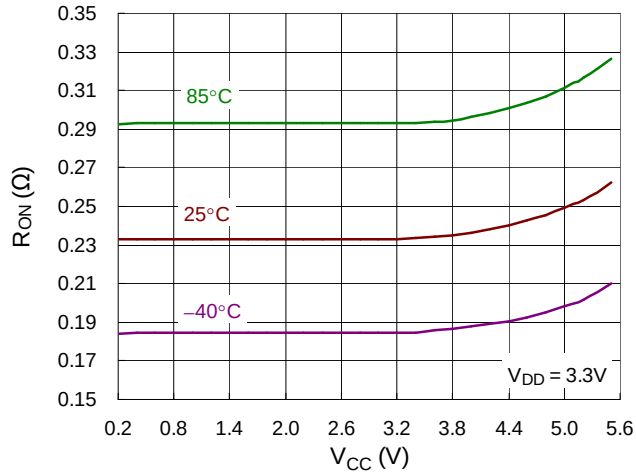
CC Clamp Voltage on System Side



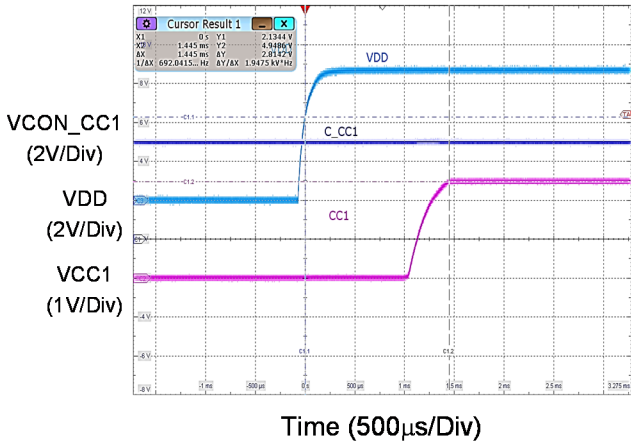
CC OVP Response Time



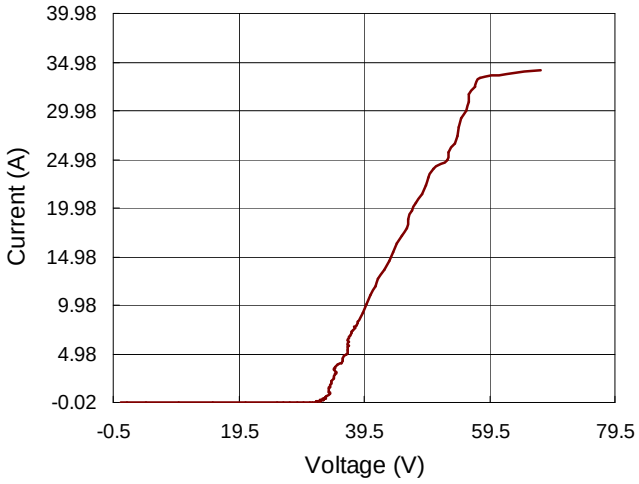
CC Switch R_{ON} Flatness



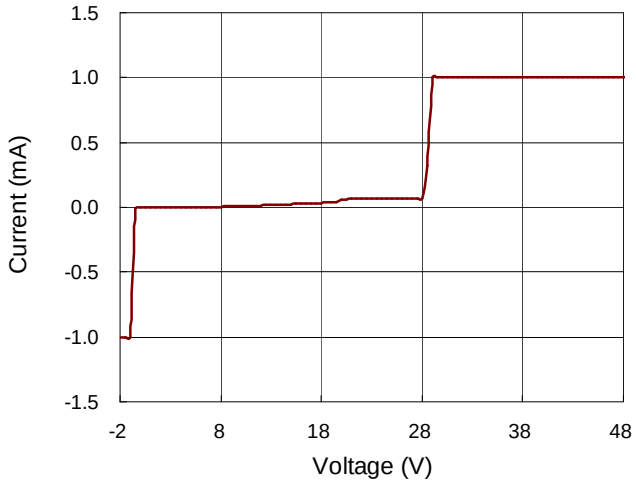
CC switch Turn on Timing



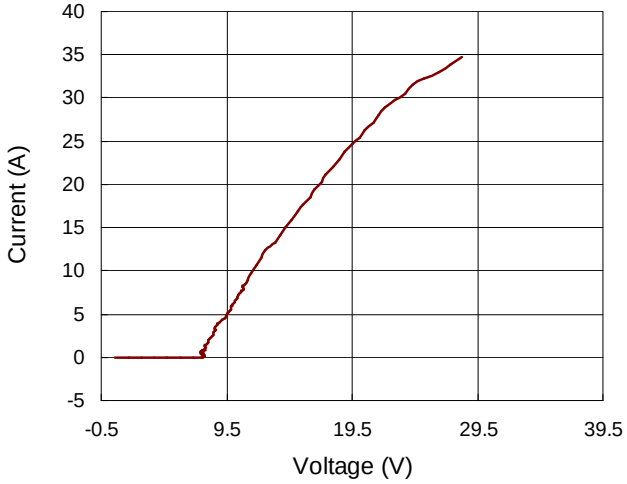
CON_CC TLP Curve Unpowered



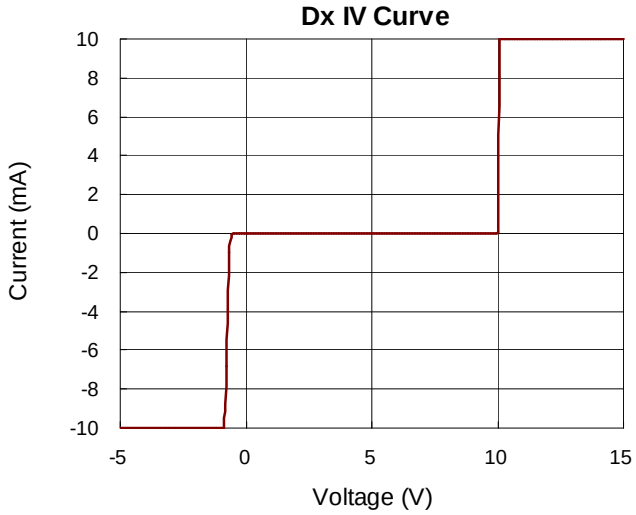
CON_CC IV Curve



Dx TLP Curve



Dx IV Curve



Application Information

6-Channels of IEC 61000-4-2 ESD Protection (CON_CC1, CON_CC2, CON_SBU1, CON_SBU2, D1 and D2)

The RT1738 provide 6-Channels of IEC 61000-4-2 system level ESD protection for the CC1, CC2, SBU1, SBU2, D1 and D2 pins. As USB Type-C interface need IEC system level ESD protection in order to provide plenty protection for the ESD events that the connector can be exposed to end users.

Input Over-Voltage Protection

The RT1738 have 4-channels of Short to VBUS overvoltage protection for the CC1, CC2, SBU1 and SBU2 pins of the USB Type-C receptacle via internal OVP level. When the input voltage exceeds the OVP level, the RT1738 will ultra-fast turn off internal switches around 60ns to prevent the high input voltage from damaging the end system. When the CC/SBU input voltage returns to normal operation voltage range with hysteresis 75/60mV, the will turn on the switches to turn on channel.

All switches for CC1/2 and SBU1/2 are each own OVP comparator and controlled by its comparator independently. If any one of channel voltage exceed OVP threshold, the channel switch is turned off, and the others switches are also turned off.

Over-Temperature Protection (OTP)

The RT1738 monitors its internal temperature to prevent thermal failures. The chip turns off the switches when the junction temperature reaches 150°C. The IC will resume after the junction temperature is cooled down 20°C.

Dead Battery

The RT1738 supports dead battery function. If system side haven't enough power to provide the RT1738 work, short the RPD_G1 pin to the CON_CC1 pin, and short the RPD_G2 pin to the CON_CC2 pin. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default VBUS.

If dead battery function is not required in application, connect the RPD_G1 and RPD_G2 pins to ground.

FLAGB Pin Operation

The FLAGB operation for fault reporting. When OVP or OTP event occurred, FLAGB pin will pull low until fault event assert. Time from OVP or OTP to FLAGB pull down is around 20μs, then time from OVP asserted to FLAGB assertion is around 5ms.

How to Connect Unused Pins

If the RPD_Gx pins, the Dx pins and the NC pin 16, 17 are unused in a design, they must be connected to GND.

Device Functional Modes

The RT1738 all functional modes.

MODE		VDD	RPD_Gx	TJ	FLAGB	CC Switches	SBU Switches
Normal Operating Conditions	Powered Off No Dead Battery Support	< UVLO	Grounded		High-Z	OFF	OFF
	Powered Off Dead Battery Support	< UVLO	Shorted to CON_CCx		High-Z	OFF	OFF
	Powered On	> UVLO	Forced OFF	< OT	High-Z	ON	ON
Fault Conditions	Thermal shutdown	> UVLO	Forced OFF	> OT	Low	OFF	OFF
	CC Over-Voltage Condition	> UVLO	Forced OFF	< OT	Low	OFF	OFF
	SBU Over-Voltage Condition	> UVLO	Forced OFF	< OT	Low	OFF	OFF

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (30°C/W) = 3.33W for a WQFN-20L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

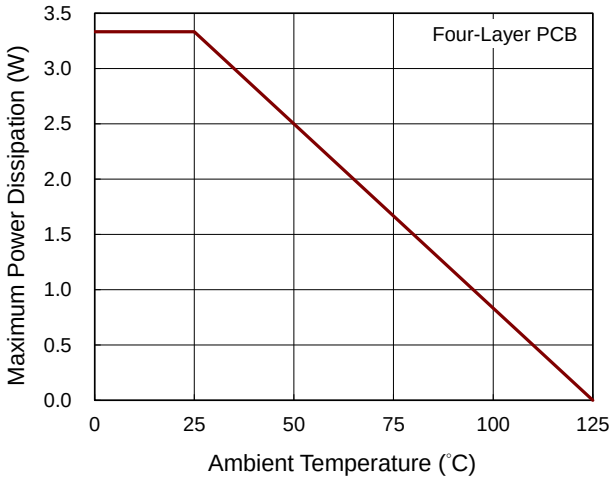


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

Appropriate routing and placement is significant to maintain the signal integrity the USB2.0, SBU, CC signals. The following guidelines apply to the RT1738 : Place the bypass capacitors close to the VDD pin, and ESD protection capacitor close to the VBIAS pin. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during such as short to VBUS and ESD event. The USB2.0 and SBU trace need to be routed straight and sharp bends must be minimized.

Standard ESD suggestion apply to the CON_CC1, CON _CC2, CON _SBU1, CON _SBU2, D1, and D2 pins as well :

The optimum placement for the device is as close to the connector as possible. The PCB designer must be keeping out unprotected traces away from the protected traces which are between the RT1738 and the connector.

Route the protected path as straight as possible. Reduce any sharp corners on the protected traces between the connector by using rounded corners with the largest radii possible. Suggest to reduce Dx pin via up to another layer and to continue that trace on that same layer.

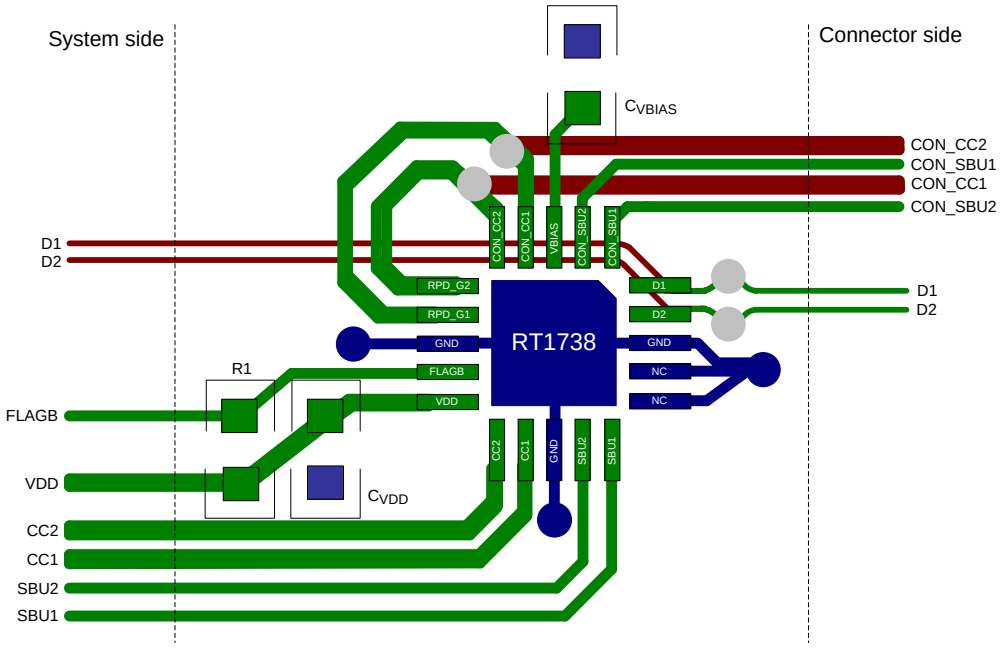
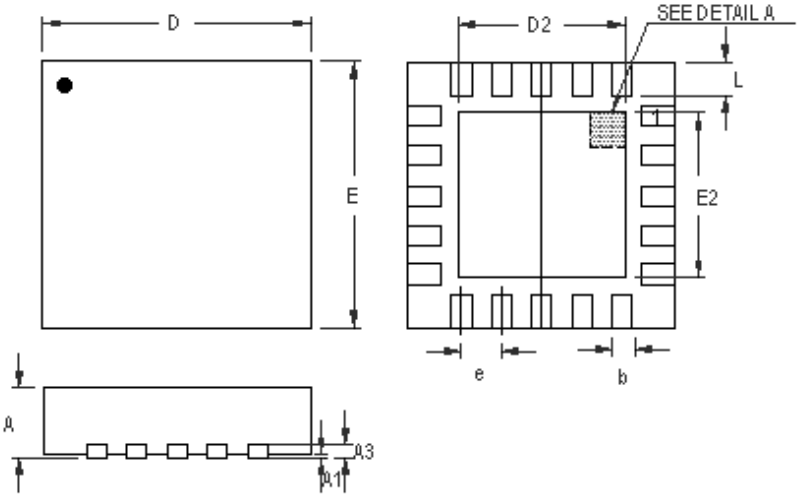
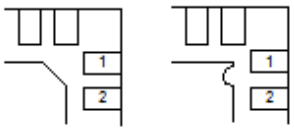


Figure 2. RT1738 Layout Guide

Outline Dimension





DETAIL A

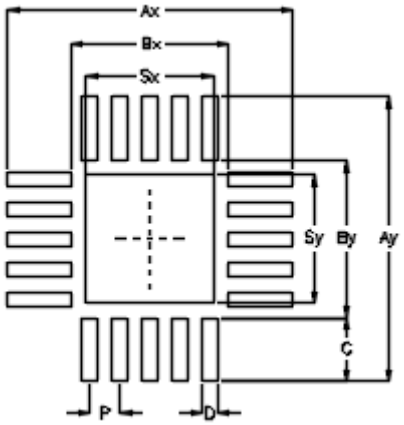
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-20	20	0.40	3.80	3.80	2.10	2.10	0.85	0.20	1.70	1.70	±0.05

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